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TCS3472

Color Light-to-Digital Converter with IR Filter

General Description

The TCS3472 device provides a digital return of red, green, blue (RGB), and clear light sensing values. An IR blocking filter, integrated on-chip and localized to the color sensing photodiodes, minimizes the IR spectral component of the incoming light and allows color measurements to be made accurately. The high sensitivity, wide dynamic range, and IR blocking filter make the TCS3472 an ideal color sensor solution for use under varying lighting conditions and through attenuating materials.

The TCS3472 color sensor has a wide range of applications including RGB LED backlight control, solid-state lighting, health/fitness products, industrial process controls and medical diagnostic equipment. In addition, the IR blocking filter enables the TCS3472 to perform ambient light sensing (ALS). Ambient light sensing is widely used in display-based products such as cell phones, notebooks, and TVs to sense the lighting environment and enable automatic display brightness for optimal viewing and power savings. The TCS3472, itself, can enter a lower-power wait state between light sensing measurements to further reduce the average power consumption.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3472, Color Light-to-Digital Converter with IR Filter are listed below:

Figure 1:
Added Value of Using TCS3472

Benefits	Features
• Enables accurate color and light sensing measurements under varying lighting conditions by minimizing IR and UV spectral component effects	• Red, Green, Blue (RGB), and Clear Light • Sensing with IR blocking filter • Programmable analog gain and integration time • 3,800,000:1 dynamic range • Very high sensitivity - ideally suited for operation behind dark glass
• Programmable interrupt pin enables level-style interrupts when pre-set values are exceeded, thus reducing companion micro-processor overhead	• Maskable interrupt • Programmable upper and lower thresholds with persistence filter

Benefits	Features
• Enabling a low-power wait-state between RGBC measurements to reduce average power consumption	• Power management • Low power - 2.5µA sleep state • 65µA wait state with programmable wait state time from 2.4ms to > 7 seconds
• Digital interfaces are less susceptible to noise	• I^2C fast mode compatible interface • Data rates up to 400 kbit/s • Input voltage levels compatible with V_{DD} or 1.8 V_{BUS}
• Backward compatibility enables interchangeability and re-usability in systems	• Register set and pin compatible with the TCS3x71 series
• Reduces PCB space requirements while simplifying designs	• Small 2mm x 2.4mm dual flat no-lead • FN package

Applications

The applications of TCS3472 include:

- RGB LED backlight control
- Light color temperature measurement
- Ambient light sensing for display backlight control
- Fluid and gas analysis
- Product color verification and sorting

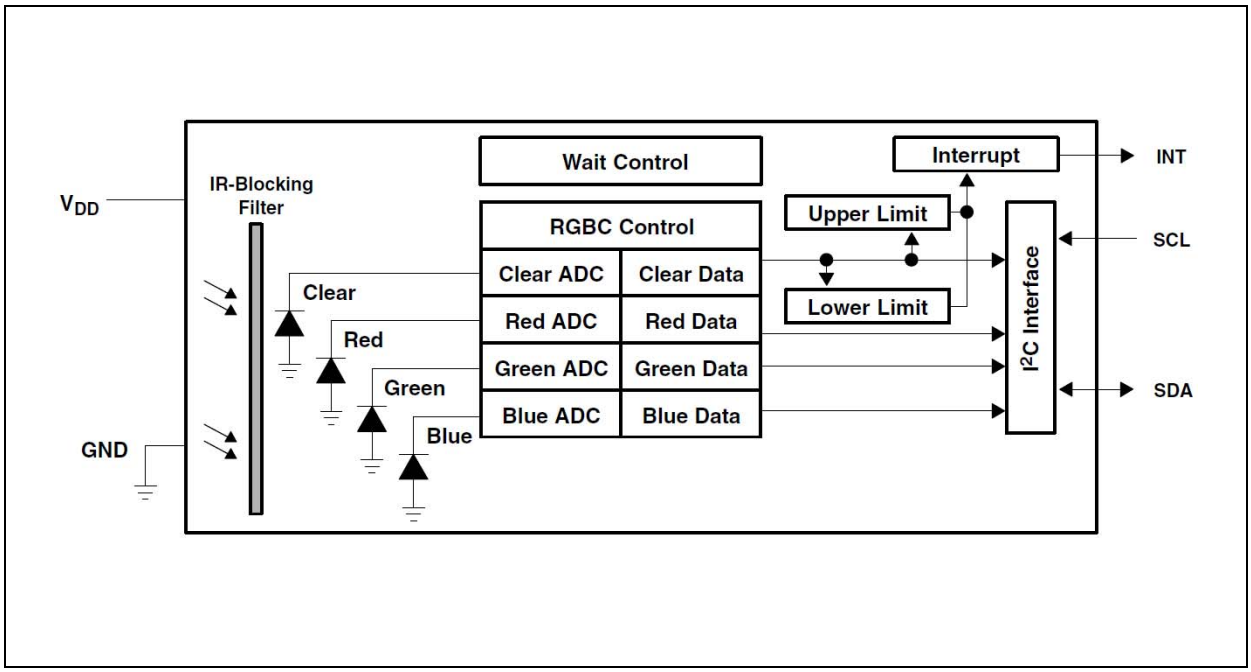
End Products and Market Segments

- TVs, mobile handsets, tablets, computers, and monitors
- Consumer and commercial printing
- Medical and health fitness
- Solid state lighting (SSL) and digital signage
- Industrial automation

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Block Diagram



Detailed Description

The TCS3472 light-to-digital converter contains a 3 × 4 photodiode array, four analog-to-digital converters (ADC) that integrate the photodiode current, data registers, a state machine, and an I^2C interface. The 3 × 4 photodiode array is composed of red-filtered, green-filtered, blue-filtered, and clear (unfiltered) photodiodes. In addition, the photodiodes are coated with an IR-blocking filter. The four integrating ADCs simultaneously convert the amplified photodiode currents to a 16-bit digital value. Upon completion of a conversion cycle, the results are transferred to the data registers, which are double-buffered to ensure the integrity of the data. All of the internal timing, as well as the low-power wait state, is controlled by the state machine.

Communication of the TCS3472 data is accomplished over a fast, up to 400 kHz, two-wire I^2C serial bus. The industry standard I^2C bus facilitates easy, direct connection to microcontrollers and embedded processors.

In addition to the I^2C bus, the TCS3472 provides a separate interrupt signal output. When interrupts are enabled, and user-defined thresholds are exceeded, the active-low interrupt is asserted and remains asserted until it is cleared by the controller. This interrupt feature simplifies and improves the efficiency of the system software by eliminating the need to poll the TCS3472. The user can define the upper and lower interrupt thresholds and apply an interrupt persistence filter. The interrupt persistence filter allows the user to define the number of consecutive out-of-threshold events necessary before generating an interrupt. The interrupt output is open-drain, so it can be wire-ORed with other devices.

Pin Assignment

The TCS3472 pin assignment is described below.

Figure 3:
Pin Diagram

Package FN Dual Flat No-Lead (Top View): Package drawing is not to scale.

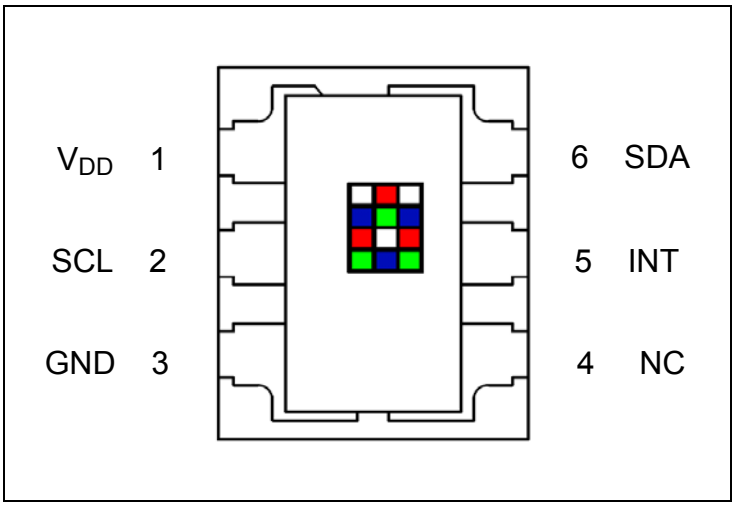


Figure 4:
Pin Description

Pin Number	Pin Name	Pin Type	Description
1	V_{DD}		Supply voltage
2	SCL	Input	I^2C serial clock input terminal – clock signal for I^2C serial data
3	GND		Power supply ground. All voltages are referenced to GND
4	NC	Output	No connect - do not connect
5	INT	Output	Interrupt - open drain (active low).
6	SDA	Input/Output	I^2C serial data I/O terminal - serial data I/O for I^2C.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings over Operating Free-Air Temperature Range (unless otherwise noted)

Parameter	Min	Max	Units	Comments
Supply voltage, V_{DD}		3.8	V	All voltages are with respect to GND
Input terminal voltage	- 0.5	3.8	V	
Output terminal voltage	- 0.5	3.8	V	
Output terminal current	- 1	20	mA	
Storage temperature range, T_{strg}	- 40	85	ºC	
ESD tolerance, human body model	±2000		V	

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	TCS34725 (I^2C $V_{BUS} = V_{DD}$)	2.7	3	3.6	V
		TCS34727 (I^2C V_{BUS} = 1.8 V)	2.7	3	3.3	
T_A	Operating free - air temperature		-30		70	°C

Figure 7:
Operating Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD}	Supply current	Active		235	330	µA
		Wait state		65		
		Sleep state - no I^2C activity		2.5	10	
V_{OL}	INT SDA output low voltage	3 mA sink current	0		0.4	V
		6 mA sink current	0		0.6	
I_{LEAK}	Leakage current, SDA, SCL, INT pins		-5		5	µA
	Leakage current, LDR pin		-5		5	
V_{IH}	SCL SDA input high voltage	TCS34725	0.7 V_{DD}			V
		TCS34727	1.25			
V_{IL}	SCL SDA input low voltage	TCS34725			0.3 V_{DD}	V
		TCS34727			0.54	

Figure 8:
Optical Characteristics, V_{DD}=3 V, T_A= 25°C, AGAIN = 16, ATIME = 0xF6 (unless otherwise noted)(1)

Parameter	Test Conditions	Red Channel		Green Channel		Blue Channel		Clear Channel			Unit
		Min	Max	Min	Max	Min	Max	Min	Typ	Max	
R_e Irradiance responsivity	λ_D = 465 nm(2)	0%	15%	10%	42%	65%	88%	11.0	13.8	16.6	counts /µW /cm^2
	λ_D = 525 nm(3)	4%	25%	60%	85%	10%	45%	13.2	16.6	20.0	
	λ_D = 615 nm(4)	80%	110%	0%	14%	5%	24%	15.6	19.5	23.4	

Notes:

1. The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
2. The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 465 nm, spectral halfwidth $\Delta\lambda$½ = 22 nm.
3. The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength λ_D = 525 nm, spectral halfwidth $\Delta\lambda$½ = 35 nm.
4. The 615 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength λ_D = 615 nm, spectral halfwidth $\Delta\lambda$½ = 15 nm.

Figure 9:
RGBC Characteristics, V_{DD} = 3 V, T_A = 25°C, AGAIN = 16, AEN = 1 (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Dark ADC count value	Ee = 0, AGAIN = 60×, ATIME = 0xD6 (100 ms)	0	1	5	counts
ADC integration time step size	ATIME = 0xFF	2.27	2.4	2.56	ms
ADC number of integration steps (1)		1		256	steps
ADC counts per step (1)		0		1024	counts
ADC count value (1)	ATIME = 0xC0 (153.6 ms)	0		65535	counts
Gain scaling, relative to 1X gain setting	4X	3.8	4	4.2	X
	16X	15	16	16.8	
	60X	58	60	63	

Note(s):

1. Parameter ensured by design and is not tested.

Figure 10:
Wait Characteristics, V_{DD} = 3 V, T_A = 25°C, WEN = 1 (unless otherwise noted)

Parameter	Conditions	Channel	Min	Typ	Max	Units
Wait step size	WTIME = 0xFF		2.27	2.4	2.56	ms
Wait number of integration steps (1)			1		256	steps

Note(s):

1. Parameter ensured by design and is not tested.

Timing Characteristics

The timing characteristics of TCS3472 are given below.

Figure 11:
AC Electrical Characteristics, V_{DD} = 3 V, T_A = 25°C (unless otherwise noted)

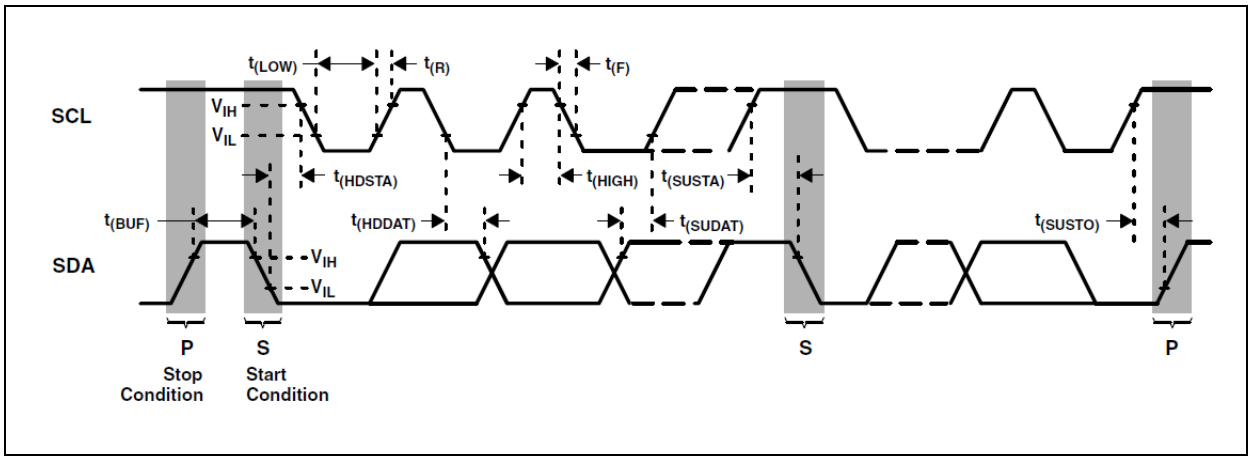
Parameter	Description	Min	Typ	Max	Units
$f_{(SCL)}$	Clock frequency (I^2C only)	0		400	kHz
$t_{(BUF)}$	Bus free time between start and stop condition	1.3			µs
$t_{(HDSTA)}$	Hold time after (repeated) start condition. After this period, the first clock is generated.	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(HDDAT)}$	Data hold time	0		0.9	µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
t_F	Clock/data fall time			300	ns
t_R	Clock/data rise time			300	ns
C_i	Input pin capacitance			10	pF

Note(s):

1. Specified by design and characterization; not production tested.

Timing Diagram

Figure 12:
Parameter Measurement Information



Typical Operating Characteristics

Figure 13:
Photodiode Spectral Responsivity RGBC

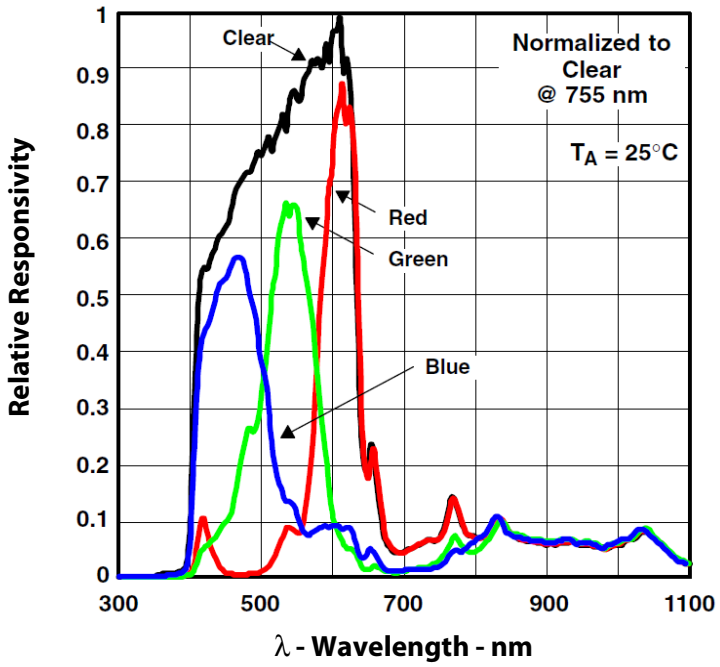


Figure 14:
Normalized Responsivity vs. Angular Displacement

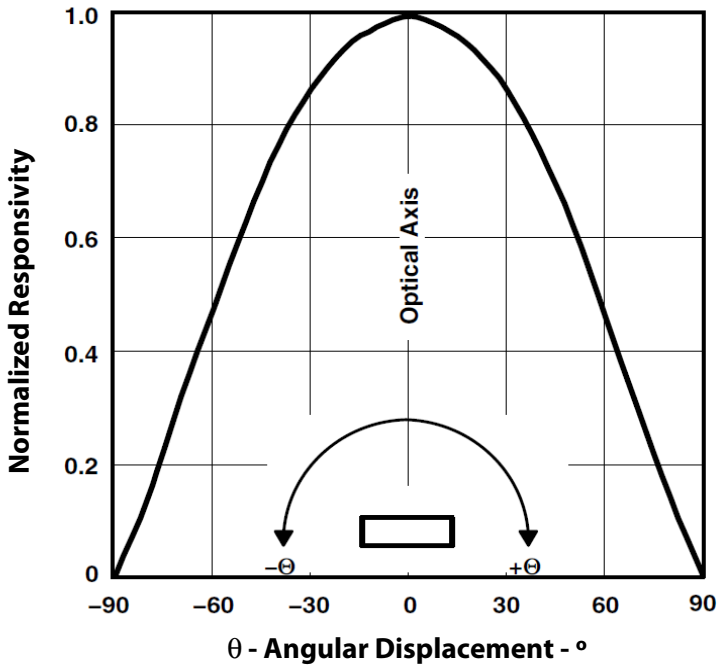


Figure 15:
Normalized I_{DD} vs. V_{DD} and Temperature

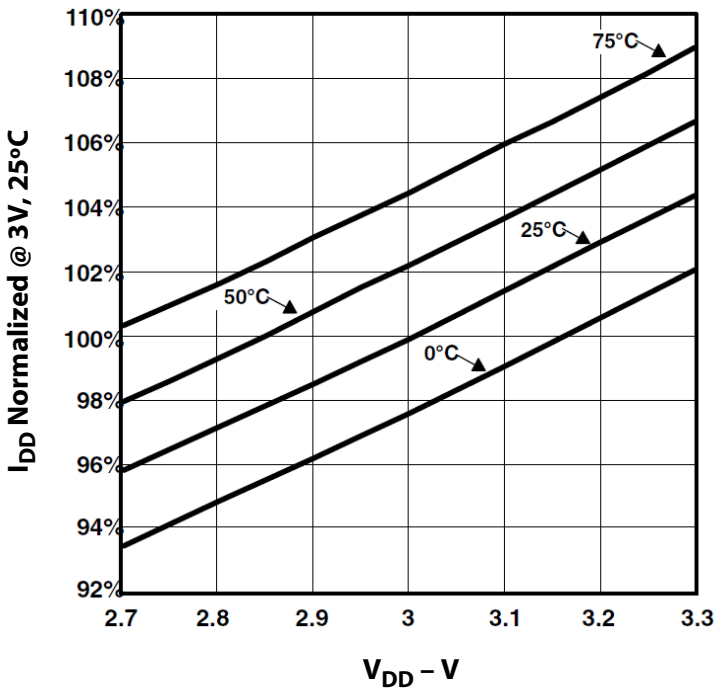
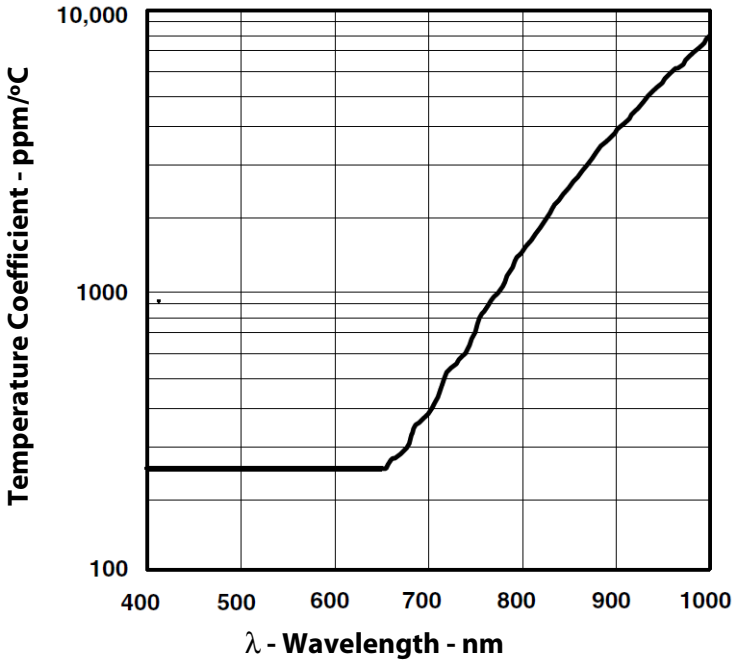


Figure 16:
Responsivity Temperature Coefficient



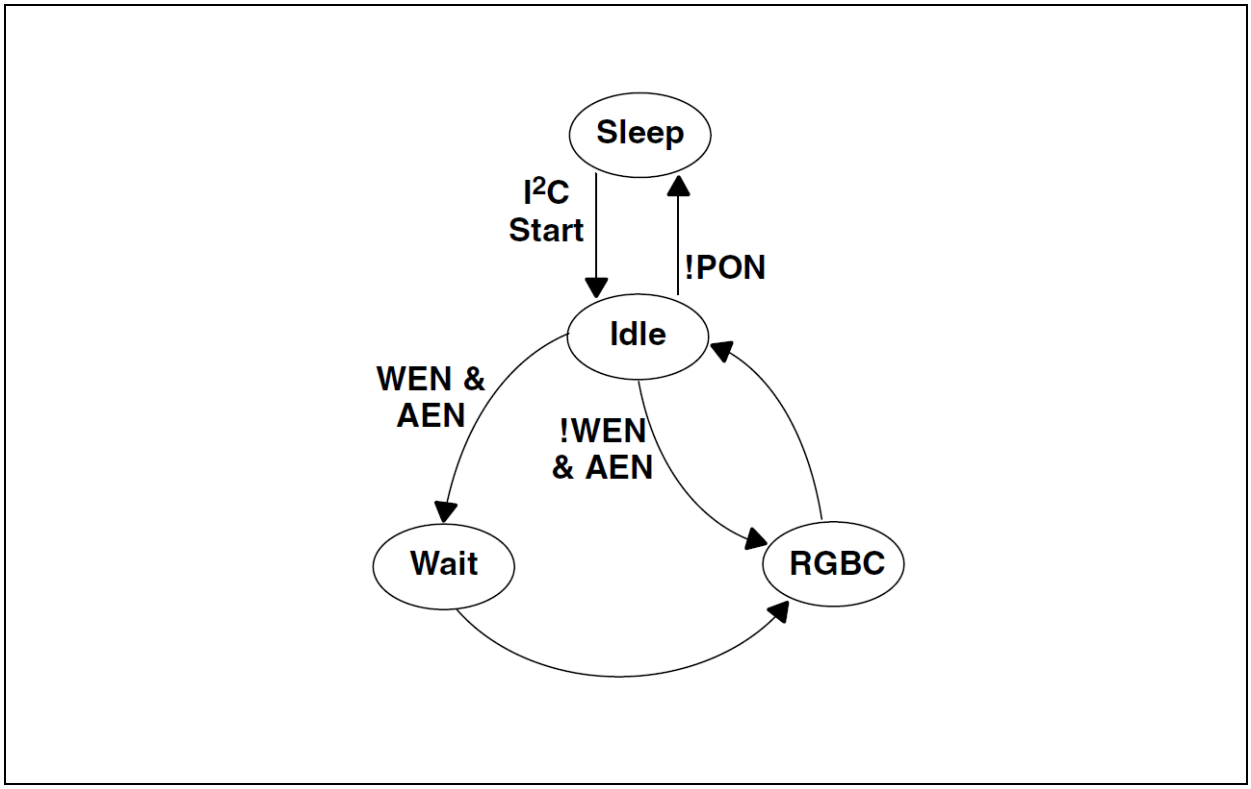
Principles of Operation

System States

An internal state machine provides system control of the RGBC and power management features of the device. At power up, an internal power-on-reset initializes the device and puts it in a low-power Sleep state.

When a start condition is detected on the I²C bus, the device transitions to the Idle state where it checks the Enable Register (0x00) PON bit. If PON is disabled, the device will return to the Sleep state to save power. Otherwise, the device will remain in the Idle state until the RGBC function is enabled (AEN). Once enabled, the device will execute the Wait and RGBC states in sequence as indicated in Figure 16. Upon completion and return to Idle, the device will automatically begin a new Wait-RGBC cycle as long as PON and AEN remain enabled.

Figure 17:
Simplified State Diagram

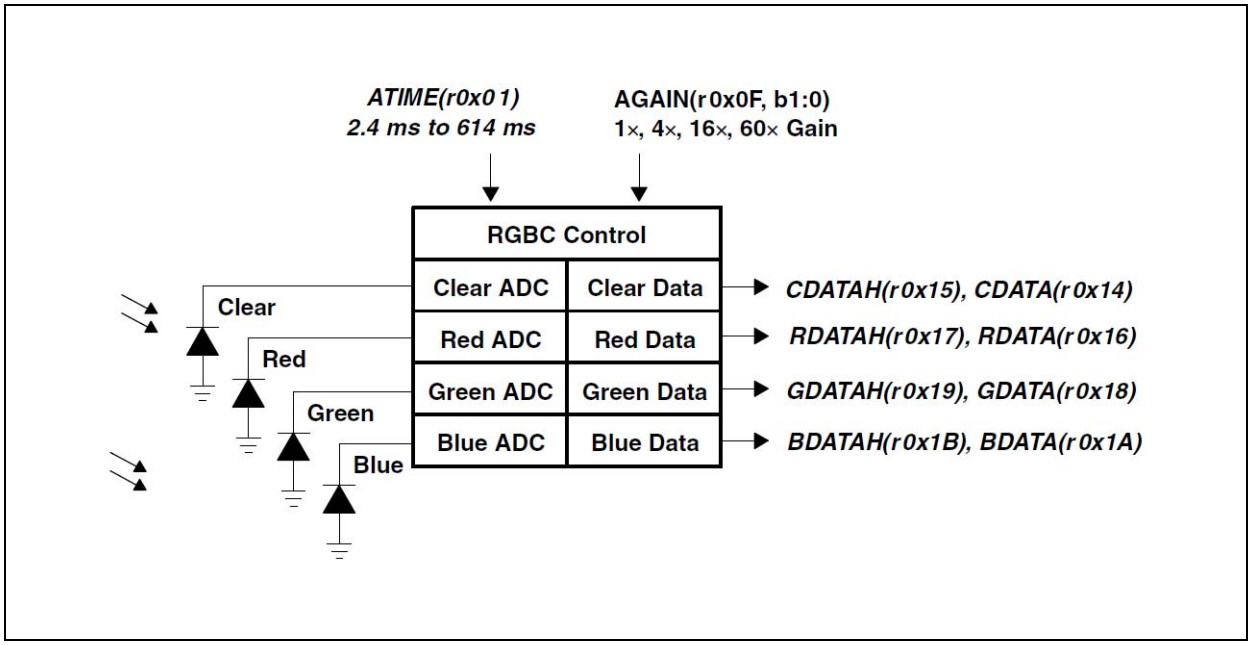


RGBC Operation

The RGBC engine contains RGBC gain control (AGAIN) and four integrating analog-to-digital converters (ADC) for the RGBC photodiodes. The RGBC integration time (ATIME) impacts both the resolution and the sensitivity of the RGBC reading. Integration of all four channels occurs simultaneously and upon completion of the conversion cycle, the results are transferred to the color data registers. This data is also referred to as channel *count*.

The transfers are double-buffered to ensure that invalid data is not read during the transfer. After the transfer, the device automatically moves to the next state in accordance with the configured state machine.

Figure 18:
RGBC Operation



Note(s):

1. In this document, the nomenclature uses the bit field name in italics followed by the register address and bit number to allow the user to easily identify the register and bit that controls the function. For example, the power on (PON) is in register 0x00, bit 0. This is represented as *PON (r0x00:b0)*.

The registers for programming the integration and wait times are a 2's compliment values. The actual time can be calculated as follows:

ATIME = 256 − Integration Time / 2.4 ms

Inversely, the time can be calculated from the register value as follows:

Integration Time = 2.4 ms × (256 − ATIME)

For example, if a 100-ms integration time is needed, the device needs to be programmed to:

256 − (100 / 2.4) = 256 − 42 = 214 = 0xD6

Conversely, the programmed value of 0xC0 would correspond to:

(256 − 0xC0) × 2.4 = 64 × 2.4 = 154 ms.

Interrupts

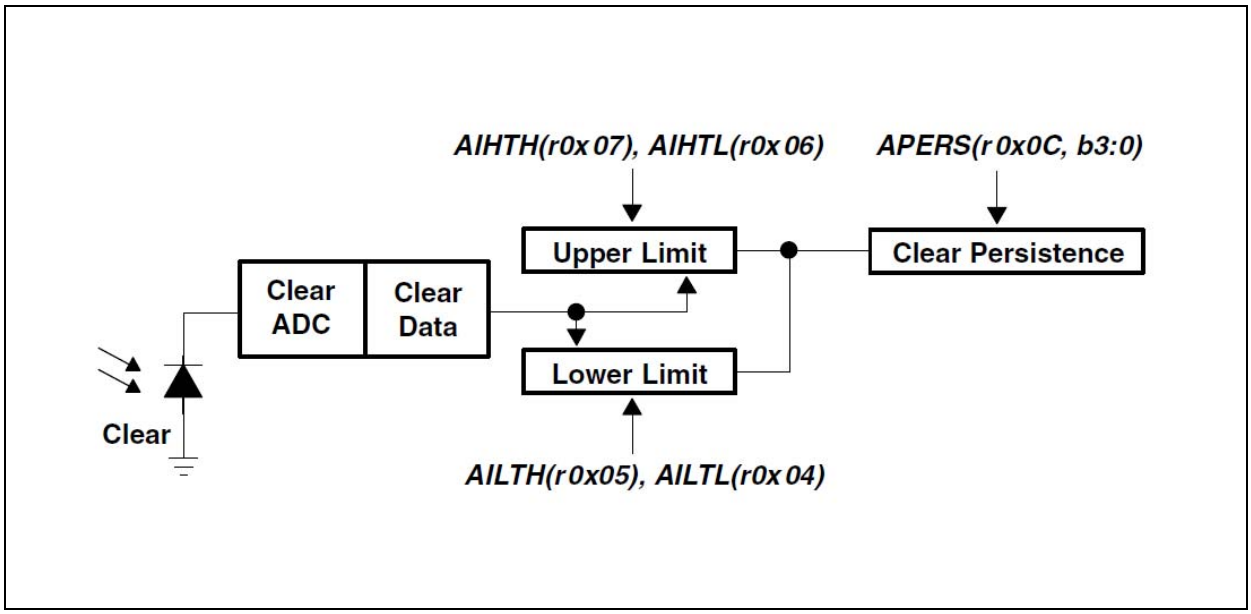
The interrupt feature simplifies and improves system efficiency by eliminating the need to poll the sensor for light intensity values outside of a user-defined range. While the interrupt function is always enabled and its status is available in the status register (0x13), the output of the interrupt state can be enabled using the RGBC interrupt enable (AIEN) field in the enable register (0x00).

Two 16-bit interrupt threshold registers allow the user to set limits below and above a desired light level. An interrupt can be generated when the Clear data (CDATA) is less than the Clear interrupt low threshold (AILTx) or is greater than the Clear interrupt high threshold (AIHTx).

It is important to note that the thresholds are evaluated in sequence, first the low threshold, then the high threshold. As a result, if the low threshold is set above the high threshold, the high threshold is ignored and only the low threshold is evaluated.

To further control when an interrupt occurs, the device provides a persistence filter. The persistence filter allows the user to specify the number of consecutive out-of-range Clear occurrences before an interrupt is generated. The persistence filter register (0x0C) allows the user to set the Clear persistence filter (APERS) value. See the persistence filter register for details on the persistence filter value. Once the persistence filter generates an interrupt, it will continue until a special function interrupt clear command is received (see command register).

Figure 19:
Programmable Interrupt



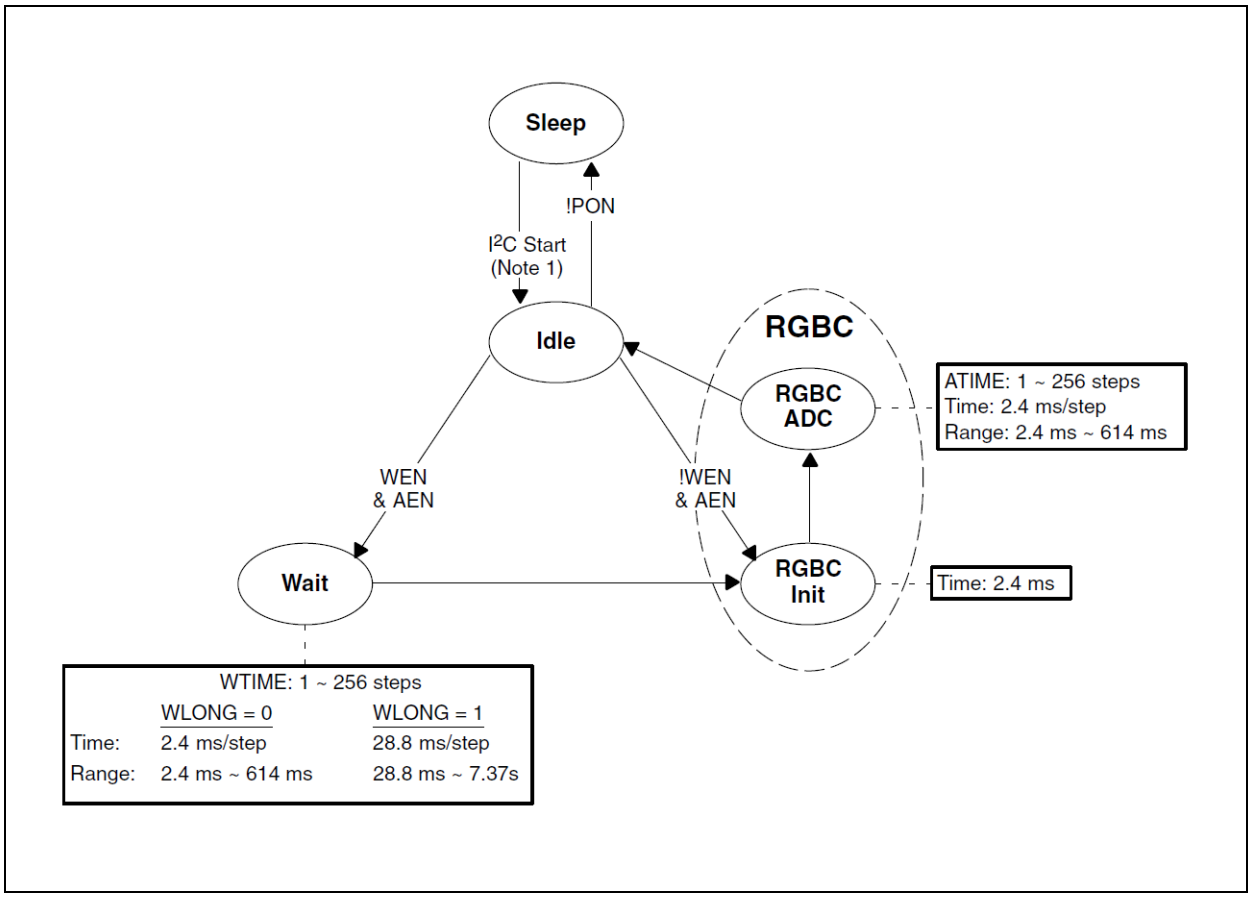
System Timing

The system state machine shown in Figure 17 provides an overview of the states and state transitions that provide system control of the device. This section highlights the programmable features, which affect the state machine cycle time, and provides details to determine system level timing.

When the power management feature is enabled (WEN), the state machine will transition to the Wait state. The wait time is determined by WLONG, which extends normal operation by 12× when asserted, and WTIME. The formula to determine the wait time is given in the box associated with the Wait state in Figure 20.

When the RGBC feature is enabled (AEN), the state machine will transition through the RGBC Init and RGBC ADC states. The RGBC Init state takes 2.4 ms, while the RGBC ADC time is dependent on the integration time (ATIME). The formula to determine RGBC ADC time is given in the associated box in Figure 20. If an interrupt is generated as a result of the RGBC cycle, it will be asserted at the end of the RGBC ADC.

Figure 20:
Detailed State Diagram



Notes:

1. There is a 2.4 ms warm-up delay if PON is enabled. If PON is not enabled, the device will return to the Sleep state as shown.
2. PON, WEN, and AEN are fields in the Enable register (0x00).

Power Management

Power consumption can be managed with the Wait state, because the Wait state typically consumes only 65 µA of I_{DD} current. An example of the power management feature is given below. With the assumptions provided in the example, average I_{DD} is estimated to be 152 µA.

Figure 21:
Power Management

System State Machine State	Programmable Parameter	Programmed Value	Duration	Typical Current
Wait	WTIME	0xEE	43.2 ms	0.065 mA
	WLONG	0		
RGBC Init			2.40 ms	0.235 mA
RGBC ADC	ATIME	0xEE	43.2 ms	0.235 mA

Average I_{DD} Current = ((43.2 × 0.065) + (43.2 × 0.235) + (2.40 × 0.235)) / 89 ≈ 152 µA

Keeping with the same programmed values as the example, Figure 22 shows how the average I_{DD} current is affected by the Wait state time, which is determined by WEN, WTIME, and WLONG. Note that the worst-case current occurs when the Wait state is not enabled.

Figure 22:
Average I_{DD} Current

WEN	WTIME	WLONG	WAIT State	Average I_{DD} Current
0	n/a	n/a	0 ms	291 µA
1	0xFF	0	2.40 ms	280 µA
1	0XEE	0	43.2 ms	152 µA
1	0x00	0	614 ms	82 µA
1	0x00	1	7.37 s	67 µA

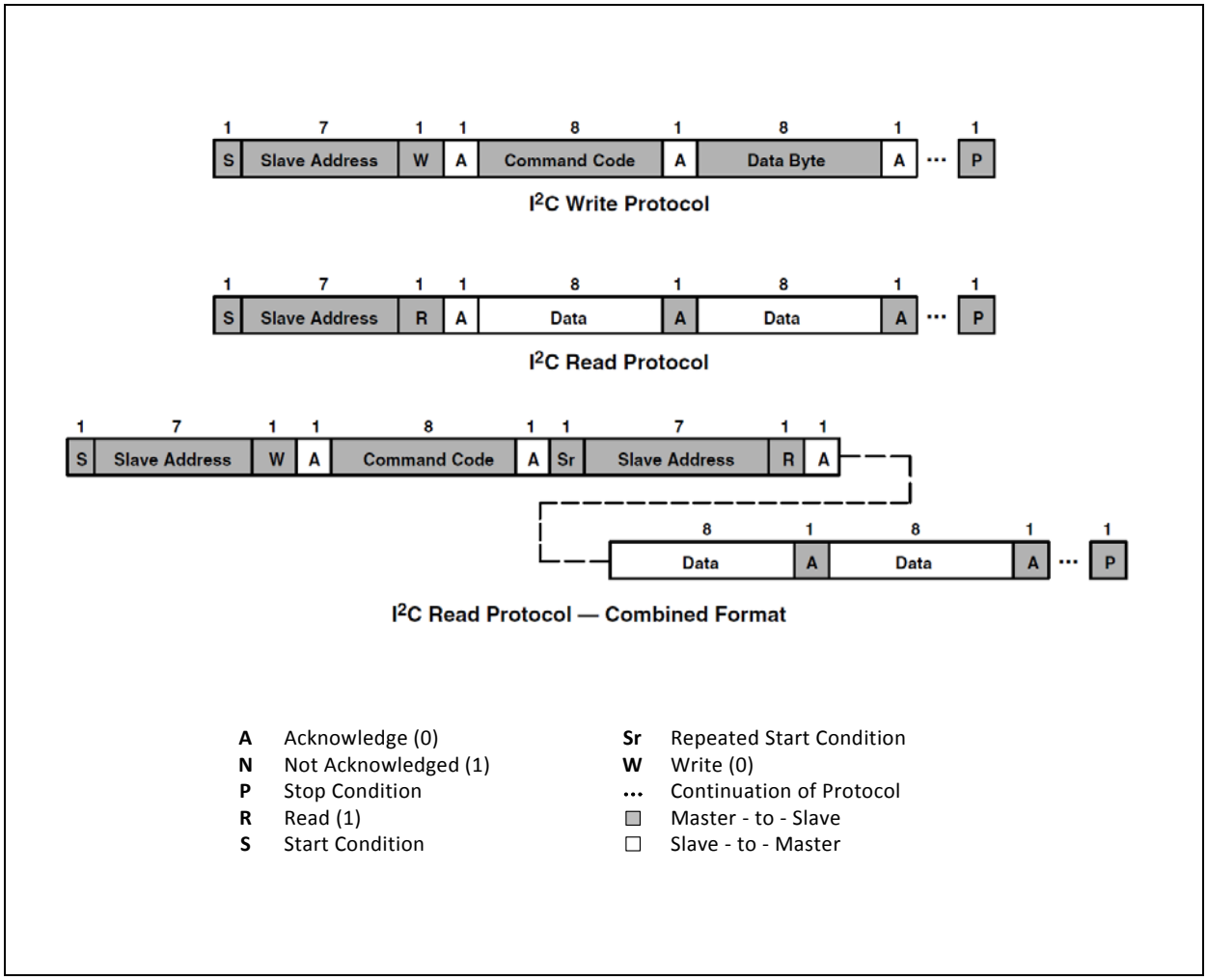
I²C Protocol

Interface and control are accomplished through an I²C serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C addressing protocol.

The I²C standard provides for three types of bus transaction: read, write, and a combined protocol (Figure 23). During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at www.i2c-bus.org/references/.

Figure 23:
I²C Protocols



Register Description

The TCS3472 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions. The register set is summarized in Figure 24.

Figure 24:
Register Set

Address	Register Name	R/W	Register Function	Reset Value
––	COMMAND	W	Specifies register address	0x00
0x00	ENABLE	R/W	Enables states and interrupts	0x00
0x01	ATIME	R/W	RGBC time	0xFF
0x03	WTIME	R/W	Wait time	0xFF
0x04	AILTL	R/W	Clear interrupt low threshold low byte	0x00
0x05	AILTH	R/W	Clear interrupt low threshold high byte	0x00
0x06	AIHTL	R/W	Clear interrupt high threshold low byte	0x00
0x07	AIHTH	R/W	Clear interrupt high threshold high byte	0x00
0x0C	PERS	R/W	Interrupt persistence filter	0x00
0x0D	CONFIG	R/W	Configuration	0x00
0x0F	CONTROL	R/W	Control	0x00
0x12	ID	R	Device ID	ID
0x13	STATUS	R	Device status	0x00
0x14	CDATAL	R	Clear data low byte	0x00
0x15	CDATAH	R	Clear data high byte	0x00
0x16	RDATAL	R	Red data low byte	0x00
0x17	RDATAH	R	Red data high byte	0x00
0x18	GDATAL	R	Green data low byte	0x00
0x19	GDATAH	R	Green data high byte	0x00
0x1A	BDATAL	R	Blue data low byte	0x00
0x1B	BDATAH	R	Blue data high byte	0x00

The mechanics of accessing a specific register depends on the specific protocol used. See the section on I^2C protocols on the previous pages. In general, the COMMAND register is written first to specify the specific control-status-data register for subsequent read/write operations.

Command Register

The command register specifies the address of the target register for future write and read operations.

Figure 25:
Command Register

7	6	5	4	3	2	1	0
CMD	TYPE		ADDR/SF				

Fields	Bits	Description	
CMD	7	Select Command Register. Must write as 1 when addressing COMMAND register.	
TYPE	6:5	Selects type of transaction to follow in subsequent data transfers:	
		FIELD VALUE	**TRANSACTION TYPE**
		00	Repeated byte protocol transaction
		01	Auto-increment protocol transaction
		10	Reserved — Do not use
		11	Special function — See description below
		Byte protocol will repeatedly read the same register with each data access. Block protocol will provide auto-increment function to read successive bytes.	
ADDR/SF	4:0	Address field/special function field. Depending on the transaction type, see above, this field either specifies a special function command or selects the specific control-status-data register for subsequent read and write transactions. The field values listed below only apply to special function commands:	
		FIELD VALUE	**READ VALUE**
		00110	Clear channel interrupt clear
		Other	Reserved — Do not write
		The Clear channel interrupt clear special function clears any pending interrupt and is self-clearing.	

Enable Register (0x00)

The ENABLE register is used primarily to power the TCS3472 device ON and OFF, and enable functions and interrupts as shown below.

Figure 26:
Enable Register

7	6	5	4	3	2	1	0
Reserved			AIEN	WEN	Reserved	AEN	PON

Fields	Bits	Description
Reserved	7:5	Reserved. Write as 0.
AIEN	4	RGBC interrupt enable. When asserted, permits RGBC interrupts to be generated.
WEN	3	Wait enable. This bit activates the wait feature. Writing a 1 activates the wait timer. Writing a 0 disables the wait timer.
Reserved	2	Reserved. Write as 0.
AEN	1	RGBC enable. This bit actives the two-channel ADC. Writing a 1 activates the RGBC. Writing a 0 disables the RGBC.
PON[1], [2]	0	Power ON. This bit activates the internal oscillator to permit the timers and ADC channels to operate. Writing a 1 activates the oscillator. Writing a 0 disables the oscillator.

Notes:

1. See Power Management section for more information.
2. A minimum interval of 2.4 ms must pass after PON is asserted before an RGBC can be initiated.

RGBC Timing Register (0x01)

The RGBC timing register controls the internal integration time of the RGBC clear and IR channel ADCs in 2.4-ms increments. Max RGBC Count = (256 – ATIME) × 1024 up to a maximum of 65535.

Figure 27:
RGBC Timing Register

Fields	Bits	Description			
		VALUE	**INTEG_CYCLES**	**TIME**	**MAX COUNT**
ATIME	7:0	0xFF	1	2.4 ms	1024
		0xF6	10	24 ms	10240
		0xD5	42	101 ms	43008
		0xC0	64	154 ms	65535
		0x00	256	700 ms	65535

Wait Time Register (0x03)

Wait time is set 2.4 ms increments unless the WLONG bit is asserted, in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number.

Figure 28:
Wait Time Register

Fields	Bits	Description			
		REGISTER VALUE	**WAIT TIME**	**TIME (WLONG= 0)**	**TIME (WLONG= 1)**
WTIME	7:0	0xFF	1	2.4 ms	0.029 sec
		0xAB	85	204 ms	2.45 sec
		0x00	256	614 ms	7.4 sec

RGBC Interrupt Threshold Registers (0x04 – 0x07)

The RGBC interrupt threshold registers provides the values to be used as the high and low trigger points for the comparison function for interrupt generation. If the value generated by the clear channel crosses below the lower threshold specified, or above the higher threshold, an interrupt is asserted on the interrupt pin.

Figure 29:
RGBC Interrupt Threshold Registers

Register	Address	Bits	Description
AILTL	0x04	7:0	RGBC clear channel low threshold lower byte
AILTH	0x05	7:0	RGBC clear channel low threshold upper byte
AIHTL	0x06	7:0	RGBC clear channel high threshold lower byte
AIHTH	0x07	7:0	RGBC clear channel high threshold upper byte

Persistence Register (0x0C)

The persistence register controls the filtering interrupt capabilities of the device. Configurable filtering is provided to allow interrupts to be generated after each integration cycle or if the integration has produced a result that is outside of the values specified by the threshold register for some specified amount of time.

Figure 30:
Persistence Register

7	6	5	4	3	2	1	0
Reserved				APERS			

Field	Bits	Description
PPERS	7:4	Reserved

Field	Bits	Description		
APERS	3:0	Interrupt persistence. Controls rate of interrupt to the host processor.		
		FIELD VALUE	**MEANING**	**INTERRUPT PERSISTENCE FUNCTION**
		0000	Every	Every RGBC cycle generates an interrupt
		0001	1	1 clear channel value outside of threshold range
		0010	2	2 clear channel consecutive values out of range
		0011	3	3 clear channel consecutive values out of range
		0100	5	5 clear channel consecutive values out of range
		0101	10	10 clear channel consecutive values out of range
		0110	15	15 clear channel consecutive values out of range
		0111	20	20 clear channel consecutive values out of range
		1000	25	25 clear channel consecutive values out of range
		1001	30	30 clear channel consecutive values out of range
		1010	35	35 clear channel consecutive values out of range
		1011	40	40 clear channel consecutive values out of range
		1100	45	45 clear channel consecutive values out of range
		1101	50	50 clear channel consecutive values out of range
		1110	55	55 clear channel consecutive values out of range
		1111	60	60 clear channel consecutive values out of range

Configuration Register (0x0D)

The configuration register sets the wait long time.

Figure 31:
Configuration Register

7	6	5	4	3	2	1	0
Reserved						WLONG	Reserved

Fields	Bits	Description
Reserved	7:2	Reserved. Write as 0.
WLONG	1	Wait Long. When asserted, the wait cycles are increased by a factor 12× from that programmed in the WTIME register.
Reserved	0	Reserved. Write as 0.