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TDA1566

I²C-bus controlled dual channel 46 W/2 Ω, single channel 92 W/1 Ω amplifier with load diagnostic features

Rev. 02 — 20 August 2007 Product data sheet

1. General description

The TDA1566 is a car audio power amplifier with a complementary output stage realized in BCDMOS. The TDA1566 has two Bridge Tied Load (BTL) output stages and comes in a HSOP24 or DBS27P package.

The TDA1566 can be controlled with or without I²C-bus. With I²C-bus control gain settings per channel and diagnostic trigger levels can be selected. Failure conditions as well as load identification can be read with I²C-bus. The load identification detects whether the outputs of a BTL channel are connected with a DC or AC load and discriminates between a speaker load, a line driver load and an open (unconnected) load.

The TDA1566 can be configured in a single BTL mode and drive a 1 Ω load. For the single BTL mode it is necessary to connect on the Printed-Circuit Board (PCB) the outputs of both BTL channels in parallel.

2. Features

- Operates in I²C-bus mode and non-I²C-bus mode
- TH version: four I²C-bus addresses controlled by two pins; J version: two I²C-bus addresses controlled by one pin
- Two 4 Ω or 2 Ω capable BTL channels or one 1 Ω capable BTL channel
- Low offset
- Pop free off/standby/mute/operating mode transitions
- Speaker fault detection
- Selectable gain (26 dB and 16 dB)
- In I²C-bus mode:
  - DC load detection: open, short and speaker or line driver present
  - AC load (tweeter) detection
  - Programmable trigger levels for DC and AC load detection
  - Per channel programmable gain (26 dB and 16 dB, selectable per channel)
  - Selectable diagnostic levels for clip detection and thermal pre-warning
  - Selectable information on the DIAG pin for clip information of each channel separately and independent enabling of thermal-, offset- or load fault
- Independent short-circuit protection per channel
- Loss of ground and open V_P safe
- All outputs short-circuit proof to V_P, GND and across the load
- All pins short-circuit proof to ground
- Temperature controlled gain reduction at high junction temperatures

- Fault condition diagnosis per channel: short to ground, short to supply, shorted lead and speaker fault (wrongly connected)
- Low battery voltage detection
- TH version: pin compatible with the TDA8566TH1

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDA1566TH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3
TDA1566J	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)	SOT827-1

4. Block diagram

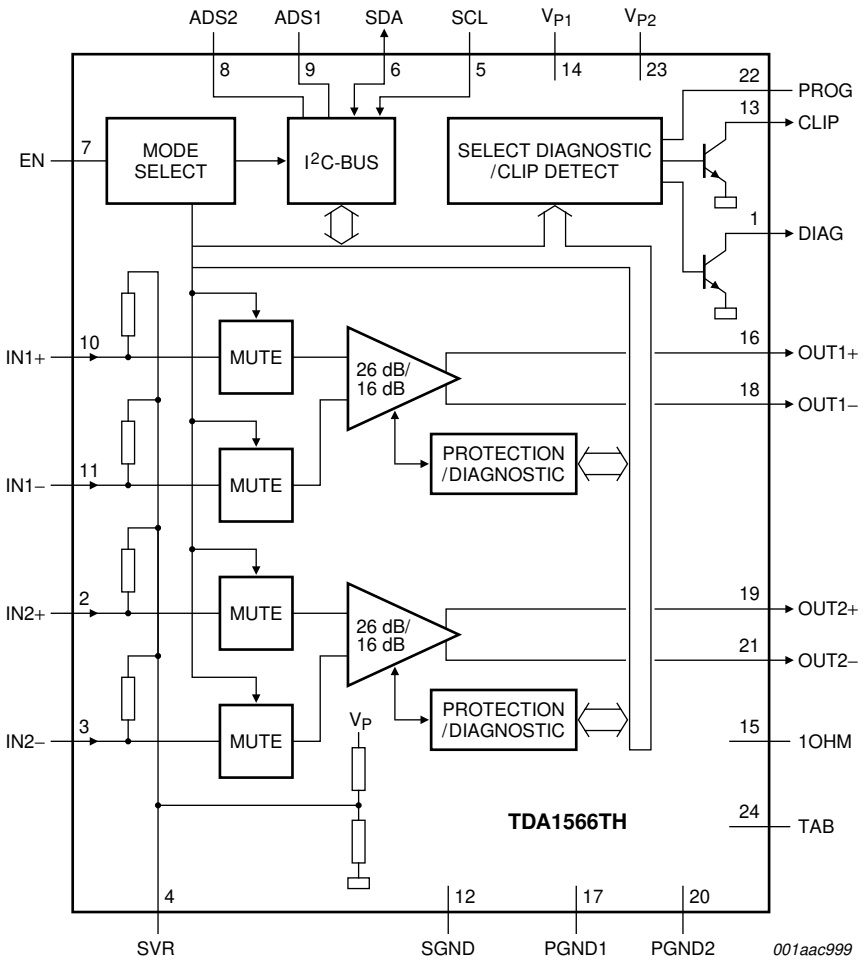

Fig 1. Block diagram (TDA1566TH)

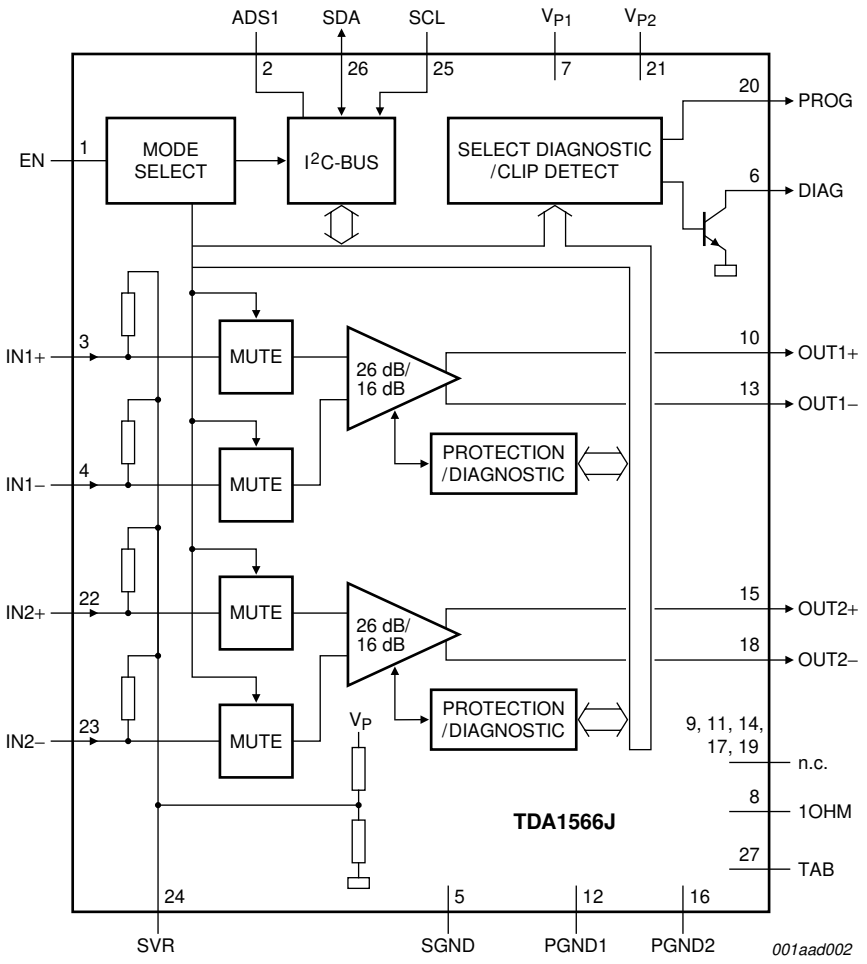

Fig 2. Block diagram (TDA1566J)

5. Pinning information

5.1 Pinning

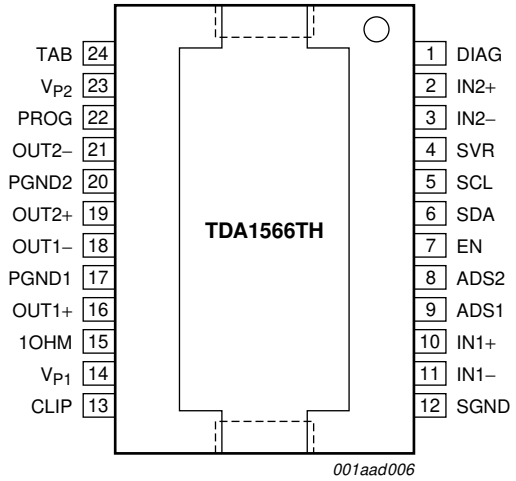

Fig 3. Pin configuration for TDA1566TH (top view)

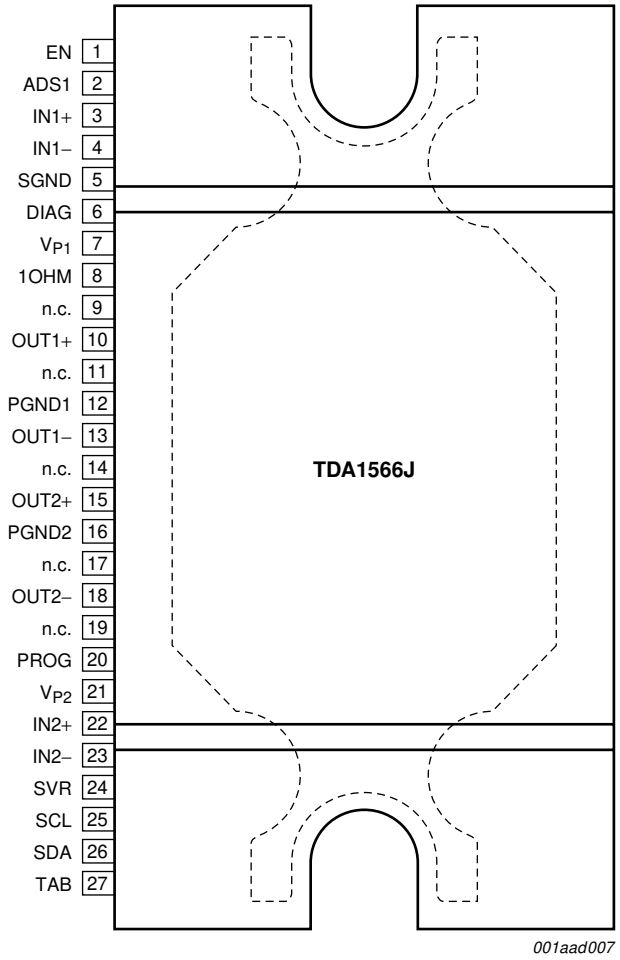

Fig 4. Pin configuration for non mounting base TDA1566J (front)

5.2 Pin description

Table 2. Pin description TDA1566TH

Symbol	Pin	Description
DIAG	1	diagnostic output
IN2+	2	positive input channel 2
IN2−	3	negative input channel 2
SVR	4	supply voltage ripple decoupling
SCL	5	I²C-bus clock input
SDA	6	I²C-bus data input/output
EN	7	enable input
ADS2	8	I²C-bus address select bit 2
ADS1	9	I²C-bus address select bit 1
IN1+	10	positive input channel 1
IN1−	11	negative input channel 1
SGND	12	signal ground

Table 2. Pin description TDA1566TH *...continued*

Symbol	Pin	Description
CLIP	13	clip detect and temperature pre-warning output
V_{P1}	14	supply voltage channel 1
1OHM	15	1 Ω select pin
OUT1+	16	positive output channel 1
PGND1	17	power ground channel 1
OUT1−	18	negative output channel 1
OUT2+	19	positive output channel 2
PGND2	20	power ground channel 2
OUT2−	21	negative output channel 2
PROG	22	program input/output
V_{P2}	23	supply voltage channel 2
TAB	24	connect to PGND

Table 3. Pin description TDA1566J

Symbol	Pin	Description
EN	1	enable input
ADS1	2	I²C-bus address select bit 1
IN1+	3	positive input channel 1
IN1−	4	negative input channel 1
SGND	5	signal ground
DIAG	6	diagnostic output
V_{P1}	7	supply voltage channel 1
1OHM	8	1 Ω select pin
n.c.	9	not connected
OUT1+	10	positive output channel 1
n.c.	11	not connected
PGND1	12	power ground channel 1
OUT1−	13	negative output channel 1
n.c.	14	not connected
OUT2+	15	positive output channel 2
PGND2	16	power ground channel 2
n.c.	17	not connected
OUT2−	18	negative output channel 2
n.c.	19	not connected
PROG	20	program input/output
V_{P2}	21	supply voltage channel 2
IN2+	22	positive input channel 2
IN2−	23	negative input channel 2
SVR	24	supply voltage ripple decoupling

Table 3. Pin description TDA1566J *...continued*

Symbol	Pin	Description
SCL	25	I²C-bus clock input
SDA	26	I²C-bus data input/output
TAB	27	connect to PGND

6. Functional description

6.1 General

Naming conventions used in this document:

- Reference to bits in instruction bytes: IBx[Dy] refers to bit Dy of instruction byte x
- Reference to bits in data bytes: DBx[Dy] refers to bit Dy of data byte x

6.1.1 Mode selection

The ADS1 pin selects the I²C-bus or non-I²C-bus mode operation as listed in Table 4. See Section 6.1.6 and Section 6.4.3 for the ADS1 pin functionality.

Table 4. Mode selection with the ADS1 pin

Pin	Non-I²C-bus mode	I²C-bus mode
ADS1	GND	open or via 33 kΩ to GND

Table 5 lists the control for the I²C-bus mode operation. In I²C-bus mode the EN pin operates at CMOS compatible LOW and HIGH logic levels. With the EN pin LOW the TDA1566 is switched off and the quiescent current is at its lowest value. With the enable pin HIGH the operation mode of the TDA1566 is selected with IB1[D0] and IB1[D1]. The I²C-bus instruction and data bytes are described in Section 6.4.2 and Section 6.4.3.

Table 5. I²C-bus mode operation

EN pin	IB1[D0]	IB2[D0]	Operation mode
HIGH (> 2.6 V)	1	0	operating
	1	1	mute
	0	don't care	standby
LOW (< 1.0 V)	don't care	don't care	off

In non-I²C-bus mode the TDA1566 has 3 operation modes: off/mute/operation. The operation mode is selected with the EN pin. Figure 5 displays the required voltage levels at the EN pin in I²C-bus and non-I²C-bus mode. For the voltage levels see Section 9 "Characteristics".

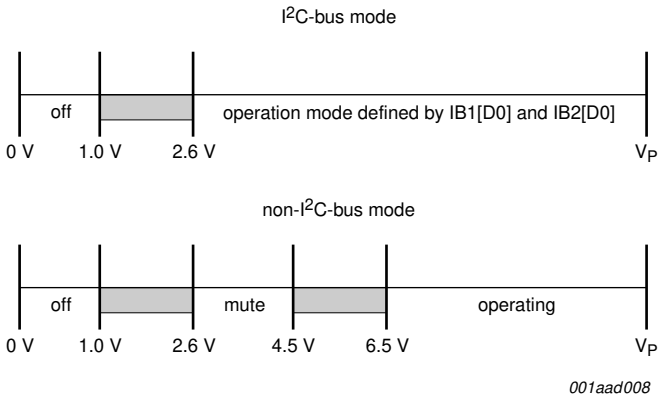

Fig 5. Enable pin mode switching in I²C-bus and non-I²C-bus mode

6.1.2 Gain selection

The TDA1566 features a 16 dB and a 26 dB gain setting. The 16 dB setting is referred to as line driver mode, the 26 dB setting is referred to as amplifier mode. Table 6 shows how the gain is selected.

Table 6. Gain select in I²C-bus and non-I²C-bus mode

Gain select	16 dB	26 dB
I²C-bus	IB3[D6] = 1	IB3[D6] = 0[1]
	IB3[D5] = 1	IB3[D5] = 0[2]
Non-I²C-bus	PROG connected with 1.5 kΩ to GND	PROG open[3]

[1] Channel 1.

[2] Channel 2.

[3] Both channels.

6.1.2.1 I²C-bus mode

The gain is selected with IB3[D6] for channel 1 and IB3[D5] for channel 2. If the gain select is performed when the amplifier is muted, the gain select will be pop free. See Section 6.4.2 for the definition of the instruction bytes.

If DC load detection is used, IB1[D1] = 1, auto gain select is activated. Detection of an open load (see Section 6.2.1) will result in a line driver mode setting. If the load detection data is invalid, IB3[D5] and IB3[D6] will define the gain setting.

6.1.2.2 Non-I²C-bus mode

The gain for channel 1 and channel 2 is selected with the PROG pin. Leaving the pin unconnected selects 26 dB gain and connecting a resistor of 1500 Ω between the PROG pin and GND selects 16 dB gain.

When the amplifier is used in line driver mode loads of 2 Ω and 4 Ω can be driven. With a load larger than 25 Ω a Zobel network of 33 nF in series with 22 Ω should be connected between the amplifier output terminals. The Zobel network should be placed close to the output pins. To prevent instability in 1 Ω mode the amplifier must not be used in line driver mode with a load larger than 25 Ω.

6.1.3 Balanced and unbalanced input sources

The TDA1566 accepts balanced as well as unbalanced input signals. Table 7 and Table 8 show the required hard or software setting and Figure 6 shows the input source connection. Note that the unbalanced input source should be connected to the positive BTL channel input. Note that the J version accepts in non-I²C-bus mode only a balanced input source.

Table 7. Balanced and unbalanced input source setting TDA1566TH

Source	Balanced input source	Unbalanced input source
I²C-bus mode	IB3[D1] = 0	IB3[D1] = 1
Non-I²C-bus mode	ADS2 pin connected to GND	ADS2 pin unconnected

Table 8. Balanced and unbalanced input source setting TDA1566J

Source	Balanced input source	Unbalanced input source
I²C-bus mode	IB3[D1] = 0	IB3[D1] = 1
Non-I²C-bus mode	default	not selectable

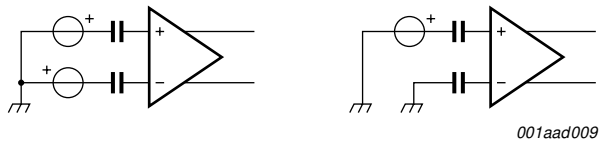

Fig 6. Balanced (left) and unbalanced (right) input source

6.1.4 Single channel 1 Ω operation

The input and output pins for single channel 1 Ω operation are listed in Table 9. The 1 Ω operation requires that on the PCB the output pins are shorted as indicated in Table 9. In the 1 Ω operation the input signal is taken from channel 1.

To prevent instability in 1 Ω operation the amplifier must not be used in line driver mode with a load larger than 25 Ω.

Table 9. Pinning for the single channel 1 Ω mode; TDA1566TH and TDA1566J

Symbol	Pin (TDA1566TH)	Pin (TDA1566J)	Description single channel operation	Description dual channel operation
IN2+	2	22	disabled: connect IN2+ with 470 nF to SGND	positive input channel 2
IN2−	3	23	disabled: connect IN2+ with 470 nF to SGND	negative input channel 2
IN1+	10	3	positive input channel 1	positive input channel 1
IN1−	11	4	negative input channel 1	negative input channel 1
1OHM	15	8	1 Ω select pin connected to V_P	1 Ω select pin connected to GND
OUT1+	16	10	positive output channel 1	positive output channel 1
OUT1−	18	13	negative output channel 1	negative output channel 1
OUT2+	19	15	shorted on board to OUT1−	positive output channel 2
OUT2−	21	18	shorted on board to OUT1+	negative output channel 2

6.1.5 Mute speed setting

In I²C-bus mode the amplifier can be muted slow (20 ms) or fast (0.1 ms). The mute speed is selected with IB2[D2].

See Section 6.4.2 for the definition of the instruction bytes. Table 10 lists the operation mode transitions where slow and fast mute are applied. The operation modes are described in Section 6.1.1, Table 5.

Table 10. Mute speed setting

Mode transition	I²C-bus mode	Non-I²C-bus mode
Mute to operating	slow mute	slow mute
Operating to mute	IB2[D2] = 0: slow mute	slow mute
	IB2[D2] = 1: fast mute	
Operating to standby	slow mute	n.a.
Operating to off	fast mute	fast mute

6.1.6 Pins with double functions

Table 11. Pins with double functions

Pin	I²C-bus mode	Non-I²C-bus mode
PROG	load detection reference current programming, see Section 6.2.1 and 6.2.2	gain select, see Section 6.1.2
ADS1	I²C-bus address select bit 1, see Section 6.4.1	non-I²C-bus mode select, see Section 6.1.1
ADS2[1]	I²C-bus address select bit 2, see Section 6.4.1	balanced/unbalanced input, see Section 3
EN	chip enable, see Section 6.1.1	mode select, see Section 6.1.1

[1] TH version only.

6.2 Load identification (I²C-bus mode only)

6.2.1 DC load detection

The default setting IB1[D1] = 0 disables DC load detection. When the DC load detection is enabled with IB1[D1] = 1, an offset is slowly applied at the output of the amplifiers at the beginning of the start-up cycle. The DC load is measured and compared with R_{trip1} and R_{trip2} to distinguish between an amplifier load, line driver load or open load. R_{trip1} and R_{trip2} are set with resistor R_{PROG} (1 %) connected between the PROG pin and GND.

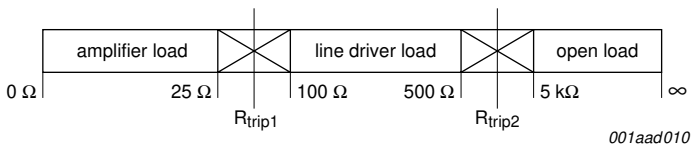

Fig 7. DC load detection limits (R_{PROG} = 1500 Ω/1 %)

The relation between R_{PROG}, R_{trip1} and R_{trip2} is approximated by (valid for R_{PROG} should be between 1.2 kΩ and 4 kΩ):

$R_{trip1} = 0.1 \times (R_{PROG} - 720)\ \Omega$

$R_{trip2} = 1.05 \times (R_{PROG} - 450)\ \Omega$

R_{trip1} and R_{trip2} levels presented refer to the advised value of 1500 Ω. Note that a shorted load will be interpreted as an amplifier load.

The result of the DC load detection is stored in DB1[D4] and DB1[D5] for channel 1 and in DB2[D4] and DB2[D5] for channel 2, see Table 12.

Table 12. Interpretation of DC load detection bits

Open load bits DB1[D4] and DB2[D4]	Amplifier load bits DB1[D5] and DB2[D5]	DC load valid bit DB3[D3]	Description
0	0	1	amplifier load
0	1	1	line driver load
1	don't care	1	open load
Don't care	don't care	0	invalid DC load detection result

Note that the DC load bits are only valid if DB3[D3] = 1. The DC load detection valid bit is reset, DB3[D3] = 0, when the DC load detection is started with a not completely discharged SVR capacitor (V_{SVR} > 0.3 V) or when the DC load detection is interrupted by an engine start (V_P < 7.5 V typical, see Section 9).

6.2.2 AC load detection

The AC load detection is used to detect if AC coupled speakers like tweeters are connected correctly during assembly. The detection starts when IB1[D2] changes from LOW to HIGH. A sine wave of a certain frequency (e.g. 19 kHz) needs to be applied to the inputs of the amplifier. The output voltage over the load impedance will cause an output current in the amplifier. Output currents larger than $1.15 \times I_{ref}$ will set the AC load detection bit and no AC load is detected when the output current is less than $0.85 \times I_{ref}$, see Figure 8. The reference current I_{ref} is set with an external resistor R_{PROG} (1 %) connected between the PROG pin and GND. The relation between R_{PROG} and I_{ref} is given by:

$I_{ref} = 390 / R_{PROG}$ [A] (valid for R_{PROG} between 1.2 kΩ and 4 kΩ).

To set the AC load detection bit the peak output current must pass the $1.15 \times I_{ref}$ threshold three times. The three 'threshold cross' counter is used to prevent false AC load detection caused by switching the input signal on or off. To reset the slope counter, IB1[D2] needs to be reset. With R_{PROG} = 1500 Ω the current thresholds are set to 200 mA and 320 mA.

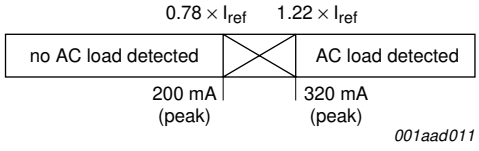

Fig 8. AC load detection limits

The levels presented refer to the advised value of 1500 Ω.

For instance at an output voltage of 4 V peak the total impedance must be less than 10 Ω to detect the AC coupled load or more than 13.4 Ω to guarantee no connected AC load is detected. Values between 10 Ω and 13.4 Ω cannot be recognized. The result of the AC load detection is shown in DB1[D7] for channel 1 and DB2[D7] for channel 2.

When IB1[D2] = 1 the AC load detection is enabled. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection. The default setting of IB1[D2] = 0 disables AC load detection.

Note: in the 1 Ω mode I_{ref} is doubled, so $I_{ref} = 2 \times 390 / R_{PROG}$ [A].

6.3 Diagnostic

6.3.1 Diagnostic table

The available diagnostic information is shown in Table 13 and Table 14. Refer to Table 17 and Table 18 for the bitmap of the instruction and data bytes.

DIAG and CLIP have an open-drain output, are active LOW and must have an external pull-up resistor to an external voltage.

DIAG shows fixed information and via the I²C-bus selectable information. This information will be seen on DIAG and CLIP as a logical OR. The temperature pre-warning diagnostic and clip information is available on the CLIP.

In case of a failure, DIAG will remain LOW and the microprocessor can read out the failure information via the I²C-bus. The I²C-bus bits are set on a failure and will be reset with the I²C-bus read command. Even when the failure is removed the microprocessor will know what was wrong by reading the I²C-bus. The consequence of this procedure is that during the I²C-bus read old information is read. Most actual information will be gathered with 2 read commands after each other.

DIAG will give actual diagnostic information (when selected). When a failure is removed, DIAG will be released instantly, independently of the I²C-bus latches.

Table 13. Available diagnostic data TH version

Diagnostic	I²C-bus mode		Non-I²C-bus mode	
	DIAG	CLIP	DIAG	CLIP
POR	yes	no	no	no
Low V_P or load dump detection	yes	no	yes	no
Clip detection	selectable	yes	no	yes
Temperature pre-warning	selectable	yes	no	yes
Short	selectable	no	yes	no
Speaker protection	selectable	no	yes	no
Offset detection	selectable	no	yes	no
Maximum temperature protection	yes	no	yes	no
Load detection	no	no	no	no

Note that in the J version no CLIP pin is available.

Table 14. Available diagnostic data J version

Diagnostic	I²C-bus mode	Non-I²C-bus mode
	DIAG	DIAG
POR	yes	no
Low V_P or load dump detection	yes	yes
Clip detection	selectable	yes
Temperature pre-warning	selectable	yes
Short	selectable	yes
Speaker protection	selectable	yes
Offset detection	selectable	no
Maximum temperature protection	yes	yes
Load detection	no	no

Following diagnostic information is only available via I²C-bus:

- DC and AC load detection results, see Section 6.2
- DB3[D4] is set when the DC settling of the amplifier has almost completed and the SVR voltage has risen to a value of V_P / 2 or above, see Section 6.5.1

6.3.2 Diagnostic level settings

Table 15. Clip and temperature pre-warning level setting

Setting	I²C-bus mode	Non-I²C-bus mode
Clip detection level	IB2[D7] = 0 selects 3 %	3 %
	IB2[D7] = 1 selects 7 %	
Temperature pre-warning level	IB3[D4] = 0 selects 145 °C	145 °C
	IB3[D4] = 1 selects 122 °C	

6.3.3 Temperature pre-warning

If in I²C-bus mode the average junction temperature reaches a by I²C-bus selectable level, the pre-warning will be activated resulting in a LOW CLIP pin.

In non-I²C mode the thermal pre-warning is set on 145 °C.

In the TH version the thermal pre-warning is available on the CLIP pin in I²C-bus mode and non-I²C mode.

In the J version the thermal pre-warning is available on the DIAG pin in non-I²C-bus mode. In I²C-bus mode the presence of the thermal pre-warning on the DIAG is selected with IB1[D4], see Section 6.3.1 and Section 6.4.2.

If the temperature increases above the pre-warning level, the temperature controlled gain reduction will be activated for both channels resulting in a lower output power. If this does not reduce the average junction temperature, both channels will be switched off at the absolute maximum temperature T_{off}, typical 175 °C.

6.3.4 Speaker protection

To prevent damage of the speaker when one side of the speaker is connected to ground, see Figure 9, a 'missing current protection' is implemented.

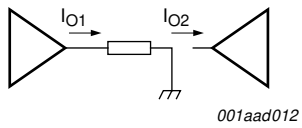

Fig 9. Speaker protection condition

When in one BTL channel the absolute value of the current through the output terminals differ, so $|I_{O1}| \neq |I_{O2}|$, a fault condition is assumed, and the BTL channel will be switched off. The 'speaker protection active' diagnosis options for I²C-bus and non-I²C-bus mode are listed in Table 13.

6.3.5 Offset detection

The offset detection can be performed with no input signal (for instance when the DSP is in mute after a start-up) or with input signal.

In I²C-bus mode the offset bits DB1[D2] and DB2[D2] are set by executing a read command. The offset bits will be reset when the BTL output voltage $V_o = |V_{OUT1+} - V_{OUT1-}|$ enters the offset threshold window of 1.5 V. The offset bits are read with a 2nd read command.

In non-I²C-bus mode (or in I²C-bus mode with offset diagnostic selected on DIAG) DIAG will be pulled LOW if the BTL output voltage is more than 1.5 V.

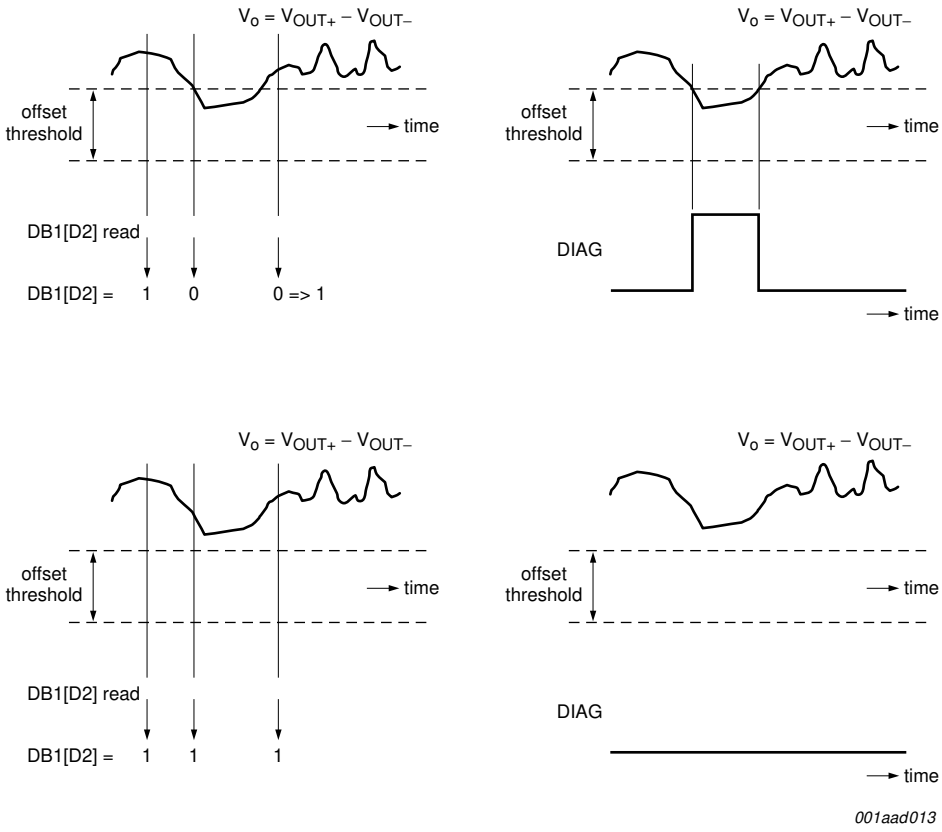

Fig 10. Offset detection in I²C-bus mode and in non-I²C-bus mode

6.4 I²C-bus operation

6.4.1 I²C-bus address with hardware address select

Table 16. I²C-bus address table TH version

ADS1	ADS2	A6	A5	A4	A3	A2	A1	A0	R/W[1]
open	open	1	1	0	1	0	0	0	1/0
	GND	1	1	0	1	0	0	1	1/0
33 kΩ to GND	open	1	1	0	1	0	1	0	1/0
	GND	1	1	0	1	0	1	1	1/0

[1] 0 = write to TDA1566TH; 1 = read from TDA1566TH.

Table 17. I²C-bus address table J version

ADS1	A6	A5	A4	A3	A2	A1	A0	R/W[1]
open	1	1	0	1	0	0	1	1/0
33 kΩ to GND	1	1	0	1	0	1	1	1/0

[1] 0 = write to TDA1566J; 1 = read from TDA1566J.

6.4.2 Instruction bytes

If R/W bit = 0, the TDA1566 expects 3 instruction bytes; IB1, IB2 and IB3. After a power-on reset, all instruction bits are set to zero. In 1 Ω mode the instruction bits of channel 1 are used. The instruction bits labelled 'reserved for test' should be set to zero.

Table 18. Instruction bytes

Bit	Instruction byte IB1		Instruction byte IB2		Instruction byte IB3	
D7	0	slow start enable	0	clip detect level on 3 %	reserved for test	
	1	slow start disable	1	clip detect level on 7 %		
D6	0	channel 1 no clip detect on DIAG	reserved for test		0	channel 1 26 dB gain
	1	channel 1 clip detect on DIAG			1	channel 1 16 dB gain
D5	0	channel 2 no clip detect on DIAG	reserved for test		0	channel 2 26 dB gain
	1	channel 2 clip detect on DIAG			1	channel 2 16 dB gain
D4	0	no temperature pre-warning on DIAG	0	speaker protection or short on DIAG	0	temperature pre-warning on 145 °C
	1	temperature pre-warning on DIAG	1	no speaker protection or short on DIAG	1	temperature pre-warning on 122 °C
D3	reserved for test		reserved for test		0	channel 1 enabled
					1	channel 1 disabled
D2	0	AC load detection disabled; detection slope counter reset	0	slow mute (20 ms)	0	channel 2 enabled
	1	AC load detection enabled	1	fast mute (0.1 ms)	1	channel 2 disabled
D1	0	DC load detection disabled	0	offset fault on DIAG	0	balanced input
	1	DC load detection enabled	1	no set fault on DIAG	1	unbalanced input
D0	0	TDA1566 in standby	0	channel 1 and channel 2 operating	reserved for test	
	1	TDA1566 in mute or operating (see IB2[D0])	1	channel 1 and channel 2 muted		

6.4.3 Data bytes

If R/W = 1, the TDA1566 will send 3 data bytes to the microprocessor: DB1, DB2, and DB3. All short diagnostic and offset detect bits are latched. All bits are reset after a read operation except DB1[D7], DB2[D7], DB1[D4], DB2[D4], DB1[D5] and DB2[D5]. DB1[D2] and DB2[D2] are set after a read operation, see Section 6.3.5. DB1[D7] and DB2[D7] are reset when IB1[D2] is LOW. In 1 Ω mode the diagnostic information will be shown in DB1. The content of the bits 'reserved for test' should be ignored.

Table 19. Data bytes

Bit	Data byte DB1 channel 1		Data byte DB2 channel 2		Data byte DB3 both channels	
D7	0	no AC load detected	0	no AC load detected	0	TDA1566 in mute or operating (IB1[D0] = 1)
	1	AC load detected	1	AC load detected	1	power-on reset has occurred or TDA1566 in standby (IB1[D0] = 0)
D6	0	no speaker fault	0	no speaker fault	0	below maximum temperature
	1	speaker fault	1	speaker fault	1	maximum temperature protection activated
D5	0	amplifier load (D4 = 0)	0	amplifier load (D4 = 0)	0	no temperature warning
		not valid (D4 = 1)		not valid (D4 = 1)		
	1	line driver load (D4 = 0)	1	line driver load (D4 = 0)	1	temperature pre-warning active
		open load (D4 = 1)		open load (D4 = 1)		
D4	0	amplifier load (D5 = 0)	0	amplifier load (D5 = 0)	0	SVR below V_P / 2
		line driver load (D5 = 1)		line driver load (D5 = 1)		
	1	not valid (D5 = 0)	1	not valid (D5 = 0)	1	SVR above V_P / 2
		open load (D5 = 1)		open load (D5 = 1)		
D3	0	no shorted load	0	no shorted load	0	invalid DC load data
	1	shorted load	1	shorted load	1	valid DC load data
D2	0	no output offset	0	no output offset	reserved for test	
	1	output offset detected	1	output offset detected		
D1	0	no short to V_P	0	no short to V_P	reserved for test	
	1	short to V_P	1	short to V_P		
D0	0	no short to ground	0	no short to ground	reserved for test	
	1	short to ground	1	short to ground		

6.5 Timing waveforms

6.5.1 Start-up and shutdown

To prevent switch-on or switch-off pop noise, the capacitor on the SVR pin C_{SVR} is used for smooth start-up and shutdown. During start-up and shutdown the output voltage tracks the SVR voltage. With IB1[D7] = 0 the time constant made with the SVR capacitor can be increased to reduce turn on transients at the load. Consequently the start-up time $t_{d(mute\_off)}$ increases with approximately 420 ms (V_P = 14.4 V, C_{SVR} = 22 µF, T_{amb} = 25 °C). Note that in non-I²C-bus mode the IB1[D7] = 0 setting will be used.

Increasing C_{SVR} results in a longer start-up and shutdown time. Note that a larger SVR capacitor value will also result in a longer DC load detection cycle.

For optimized pop performance it is recommended to keep the amplifier in mute until the SVR voltage has reached its final level.

When the amplifier is switched off by pulling the EN pin LOW the amplifier is muted (fast mute) and the capacitor on the SVR pin will be discharged. With an SVR capacitor of 22 μF the off current is reached 2 s after the EN pin is switched to zero.

Start-up and shutdown in I²C-bus mode is shown in Figure 11 and explained in Table 20.

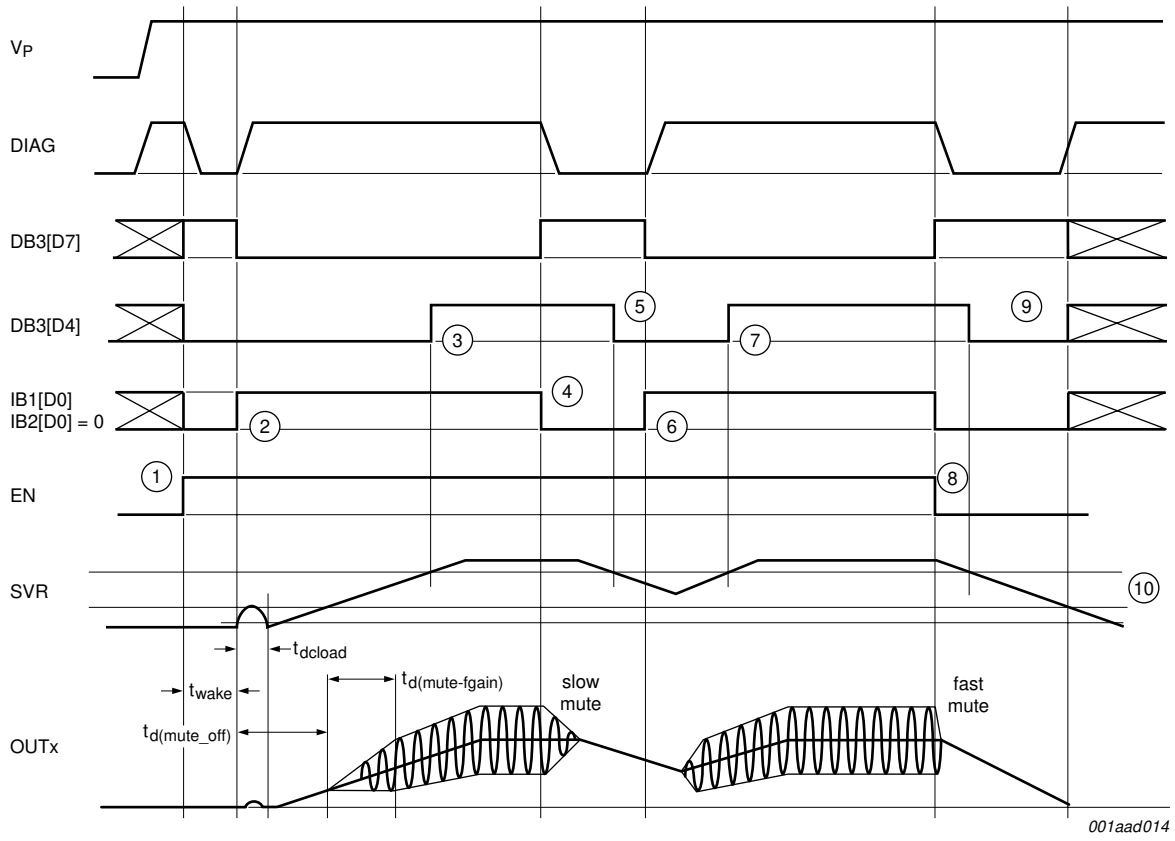

Fig 11. Start-up and shutdown timing in I²C-bus mode

Table 20. Start-up and shutdown timing in I²C-bus mode

Step	Action	Result
1	TDA1566 is enabled with EN	TDA1566 from off to standby
		DB3[D7] is set and DIAG is pulled LOW to indicate power-on reset
2	TDA1566 is switched from standby to operating with IB1[D0] = 1	DIAG is released
		DB3[D7] is reset
		SVR capacitor is charged, OUTx voltage tracks SVR voltage
		gradual increase of gain; when the SVR voltage increases above a threshold of 2 V + $2V_{BE}$ the amplifiers operate at full gain

Table 20. Start-up and shutdown timing in I²C-bus mode *...continued*

Step	Action	Result
3		SVR voltage has become larger than V_P / 2 resulting in setting DB3[D4]
4	TDA1566 is switched from operating to standby with IB1[D0] = 0	DIAG is pulled LOW
		SVR is discharged, OUTx voltage tracks SVR voltage
		amplifier is slow muted
5		SVR voltage has dropped below V_P / 2 resulting in resetting DB3[D4]
6	TDA1566 is switched from standby to operating with IB1[D0] = 1	see step 2
7		see step 3
8	TDA1566 is disabled with EN	DIAG is pulled LOW
		amplifier is fast muted
		SVR is discharged, OUTx voltage tracks SVR voltage
9		see step 5
10		OUTx is at ground potential, DIAG is released, TDA1566 is off

6.5.2 Engine start

The DC-output voltage of the amplifier follows the voltage on the SVR pin. On the SVR pin a capacitor is connected which is used for start-up and shutdown timing as well as for DC load detection. If the supply voltage drops during engine start below 8.6 V the SVR capacitor will be discharged and the fast mute is activated to prevent audible transients at the output.

If in I²C-bus mode the supply voltage drops below 5.5 V (see $V_{P(POR)}$) the content of the I²C-bus latches cannot be guaranteed and the power-on reset will be activated: DB3[D7] = 1. All latches will be reset, the amplifier is switched off and the DIAG pin will be pulled LOW to indicate that a power-on reset has occurred. The TDA1566 will not start-up but wait for a command to start-up.

7. Limiting values

Table 21. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage	operating; R_L = 4 Ω	-	18	V
		operating; R_L = 2 Ω or 1 Ω	-	16	V
		non operating	−1	+50	V
		load dump protection; during 50 ms; $t_r \geq 2.5$ ms	-	50	V
$V_{P(r)}$	reverse supply voltage	maximum 10 minutes	-	−2	V
I_{OSM}	non-repetitive peak output current		-	13	A

Table 21. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I_{ORM}	repetitive peak output current			-	8	A
I_{BGM}	peak back gate current	loss off GND or open V_P application failure; supply decoupling capacitor of maximum 3×2200 µF/16 V and a series resistance of 70 mΩ		-	50	A
V_{1OHM}	voltage on pin 1OHM	operating, non operating	[1]	0	24	V
V_{EN}	voltage on pin EN	operating, non operating	[1]	0	24	V
V_{IN1-}	voltage on pin IN1−	operating, non operating	[2]	0	13	V
V_{IN1+}	voltage on pin IN1+	operating, non operating	[2]	0	13	V
V_{IN2-}	voltage on pin IN2−	operating, non operating	[2]	0	13	V
V_{IN2+}	voltage on pin IN2+	operating, non operating	[2]	0	13	V
V_{DIAG}	voltage on pin DIAG	operating, non operating	[2]	0	13	V
V_{CLIP}	voltage on pin CLIP	operating, non operating	[2]	0	13	V
V_{PROG}	voltage on pin PROG	operating, non operating	[2]	0	13	V
V_{SVR}	voltage on pin SVR	operating, non operating	[2]	0	13	V
V_{SCL}	voltage on pin SCL	operating, non operating	[2]	0	6.5	V
V_{SDA}	voltage on pin SDA	operating, non operating	[2]	0	6.5	V
V_{ADS1}	voltage on pin ADS1	operating, non operating	[2]	0	6.5	V
V_{ADS2}	voltage on pin ADS2	operating, non operating	[2]	0	6.5	V
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			−55	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
$V_{(prot)}$	protection voltage	AC and DC short-circuit voltage of output pins and across the load		-	V_P	V
P_{tot}	total power dissipation	T_{case} = 70 °C		-	80	W

Table 21. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{esd}	electrostatic discharge voltage	HBM			
		C = 100 pF; R_s = 1500 Ω	-	2000	V
		MM			
		C = 200 pF; R_s = 10 Ω; L = 0.75 µH	-	200	V

[1] The voltage on this pin is clamped by an ESD protection. If this pin is connected to V_P a series resistance of 10 kΩ should be added.

[2] The voltage on this pin is clamped by an ESD protection.

8. Thermal characteristics

Table 22. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case			
	TDA1566TH		1.0	K/W
	TDA1566J		1.0	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			
	TDA1566TH	in free air	35	K/W
	TDA1566J	in free air	35	K/W

9. Characteristics

Table 23. Characteristics

Refer to test circuit (see Figure 22); V_P = 14.4 V; R_L = 4 Ω; −40 °C < T_{amb} < +85 °C and −40 °C < T_j < +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply voltage behavior							
$V_{P(oper)}$	operating supply voltage	R_L = 4 Ω		$V_{P(low)(mute)}$	14.4	18	V
		R_L = 2 Ω or 1 Ω	[1]	$V_{P(low)(mute)}$	14.4	16	V
I_q	quiescent current	no load		-	180	220	mA
I_{stb}	standby current	I²C-bus mode only		-	10	15	mA
I_{off}	off-state current	V_{EN} ≤ 0.4 V; T_j < 85 °C		-	2	10	µA
V_O	output voltage			6.7	7.2	7.6	V
$V_{P(low)(mute)}$	low supply voltage mute	falling supply voltage		6.5	7.2	7.7	V
		rising supply voltage		7.0	7.6	8.2	V
$V_{P(POR)}$	power-on reset supply voltage			4.1	5.0	5.8	V

Table 23. Characteristics *...continued*

Refer to test circuit (see Figure 22); V_P = 14.4 V; R_L = 4 Ω; −40 °C < T_{amb} < +85 °C and −40 °C < T_j < +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{O(offset)}$	output offset voltage	amplifier mode; on		−50	0	+50	mV
		line driver mode; on		−25	0	+25	mV
		amplifier and line driver mode; mute		−25	0	+25	mV
Mode select pin EN (see Figure 5)							
V_{EN}	voltage on pin EN	off condition; I²C-bus and non-I²C-bus mode		-	-	1.0	V
		standby mode; I²C-bus mode		2.6	-	V_P	V
		mute condition; non-I²C-bus mode		2.6	-	4.5	V
		operating condition; non-I²C-bus mode	[2]	6.5	-	V_P	V
I_{EN}	current on pin EN	V_{EN} = 8.5 V	[3]	-	10	70	µA
Start-up, shutdown and mute timing (see Figure 11)							
t_{wake}	wake-up time	time after wake-up via EN pin before first I²C-bus transmission is recognized		-	300	500	µs
$t_{d(mute\_off)}$	mute off delay time	I²C-bus mode with slow start enabled and non-I²C-bus mode; DC load detection disabled					
		C_{SVR} = 22 µF	[4]	-	380	-	ms
		C_{SVR} = 10 µF	[4]	-	170	-	ms
		I²C-bus mode only; DC load detection enabled; slow start enabled					
		C_{SVR} = 22 µF	[4]	-	510	-	ms
		C_{SVR} = 10 µF	[4]	-	250	-	ms
		I²C-bus mode only; DC load detection disabled; slow start disabled					
		C_{SVR} = 22 µF	[4]	-	230	-	ms
		C_{SVR} = 10 µF	[4]	-	110	-	ms
		I²C-bus mode only; DC load detection enabled; slow start disabled					
		C_{SVR} = 22 µF	[4]	-	370	-	ms
		C_{SVR} = 10 µF	[4]	-	180	-	ms
$t_{det(DCload)}$	DC load detection time	I²C-bus mode only; DC load detection enabled					
		C_{SVR} = 22 µF	[4]	-	160	-	ms
		C_{SVR} = 10 µF	[4]	-	70	-	ms
$t_{d(mute-fgain)}$	mute to full gain delay time	C_{SVR} = 22 µF	[5]	-	90	-	ms
		C_{SVR} = 10 µF	[5]	-	40	-	ms

Table 23. Characteristics *...continued*

Refer to test circuit (see Figure 22); V_P = 14.4 V; R_L = 4 Ω; −40 °C < T_{amb} < +85 °C and −40 °C < T_j < +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(mute-on)}$	mute to on delay time	I²C-bus mode: IB2[D0] = 1 to 0	-	20	40	ms
		non-I²C-bus mode: V_{EN} from 3.3 V to 8 V	-	20	40	ms
$t_{d(slow\_mute)}$	slow mute delay time	I²C-bus mode: IB2[D0] = 0 to 1; IB2[D2] = 0	-	20	40	ms
		non-I²C-bus mode: V_{EN} from 8 V to 3.3 V	-	20	40	ms
$t_{d(fast\_mute)}$	fast mute delay time	on to mute in I²C-bus mode; IB2[D2] = 1; IB2[D0] = 0 to 1	-	0.1	1	ms
		on to standby in I²C-bus mode; IB2[D0] = 0; IB1[D0] = 1 to 0	-	20	40	ms
		on to off in I²C-bus and non-I²C-bus mode: V_{EN} from 8 V to 0.5 V	-	0.1	1	ms
$t_{(on-SVR)}$	time from amplifier switch-on to SVR above V_P / 2	via I²C-bus (IB1[D0]) to DB3[D4] = 1 (SVR above V_P / 2); I²C-bus mode with slow start enabled; DC load detection disabled				
		C_{SVR} = 22 µF	-	1000	-	ms
		C_{SVR} = 10 µF	-	440	-	ms
		I²C-bus mode only; DC load detection enabled; slow start enabled.				
		C_{SVR} = 22 µF	-	1100	-	ms
		C_{SVR} = 10 µF	-	530	-	ms
		I²C-bus mode only; DC load detection disabled; slow start disabled				
		C_{SVR} = 22 µF	-	810	-	ms
		C_{SVR} = 10 µF	-	370	-	ms
		I²C-bus mode only; DC load detection enabled; slow start disabled				
		C_{SVR} = 22 µF	-	940	-	ms
		C_{SVR} = 10 µF	-	450	-	ms
I²C-bus interface and 1 Ω selection[6]						
$V_{IL(SCL)}$	LOW-level input voltage on pin SCL		-	-	1.5	V
$V_{IL(SDA)}$	LOW-level input voltage on pin SDA		-	-	1.5	V
$V_{IH(SCL)}$	HIGH-level input voltage on pin SCL		2.3	-	5.5	V

Table 23. Characteristics *...continued*

Refer to test circuit (see Figure 22); V_P = 14.4 V; R_L = 4 Ω; −40 °C < T_{amb} < +85 °C and −40 °C < T_j < +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{IH(SDA)}$	HIGH-level input voltage on pin SDA			2.3	-	5.5	V
$V_{OL(SDA)}$	LOW-level output voltage on pin SDA	I_{load} = 5 mA		-	-	0.4	V
f_{clk}	clock frequency			-	400	-	kHz
V_{1OHM}	voltage on pin 1OHM	mono channel mode	[7]	2.5	-	V_P	V
		dual channel mode		0	-	1.5	V
I_{1OHM}	current on pin 1OHM	V_{1OHM} = 1.5 V		-	130	200	µA
		V_{1OHM} = 5.5 V		-	-	5	µA
I_{SCL}	current on pin SCL	V_{SCL} = 1.5 V		-	-	5	µA
		V_{SCL} = 5.5 V		-	-	5	µA
I_{SDA}	current on pin SDA	V_{SDA} = 1.5 V		-	-	5	µA
		V_{SDA} = 5.5 V		-	-	5	µA
I_{ADS1}	current on pin ADS1	ADS1 pin connected to GND		-	300	400	µA
		ADS1 pin connected via 33 kΩ to GND		-	70	100	µA
I_{ADS2}	current on pin ADS2	ADS2 pin connected to GND		-	300	400	µA
		ADS2 pin connected via 33 kΩ to GND		-	70	100	µA
Diagnostic							
$V_{OL(DIAG)}$	LOW-level output voltage on pin DIAG	fault condition; I_{DIAG} = 1 mA		-	-	0.3	V
$V_{OL(CLIP)}$	LOW-level output voltage on pin CLIP	TH version only; clip or temperature pre-warning active; I_{CLIP} = 1 mA		-	-	0.3	V
$I_{LIH(CLIP)}$	HIGH-level input leakage current on pin CLIP	diagnostic, clip or temperature pre-warning not activated		-	-	2	µA
$I_{LIH(DIAG)}$	HIGH-level input leakage current on pin DIAG	diagnostic, clip or temperature pre-warning not activated		-	-	2	µA
$V_{th(offset)}$	threshold voltage for offset detection			1.0	1.5	2.0	V
THD_{CLIP7}	7 % clip detection level (THD)	I²C-bus mode: IB2[D7] = 1	[8]	-	7	-	%
THD_{CLIP3}	3 % clip detection level (THD)	I²C-bus mode: IB2[D7] = 0 and non-I²C-bus mode	[8]	-	3	-	%
$T_{j(AV)(warn1)}$	average junction temperature for pre-warning 1	I²C-bus mode: IB3[D4] = 0 and non-I²C-bus mode		-	145	-	°C
$T_{j(AV)(warn2)}$	average junction temperature for pre-warning 2	I²C-bus mode: IB3[D4] = 1		-	122	-	°C

Table 23. Characteristics *...continued*

Refer to test circuit (see Figure 22); V_P = 14.4 V; R_L = 4 Ω; −40 °C < T_{amb} < +85 °C and −40 °C < T_j < +150 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$T_{j(AV)(G(-0.5dB))}$	average junction temperature for 0.5 dB gain reduction	V_i = 0.05 V		-	155	-	°C
$\Delta T_{j(warn1\text{-}mute)}$	difference in junction temperature between pre-warning 1 and mute			-	10	-	°C
$\Delta T_{j(G(-0.5\text{-}40dB))}$	difference in junction temperature between 0.5 dB and 40 dB gain reduction			-	20	-	°C
$T_{j(AV)(off)}$	average junction temperature for off			-	175	185	°C
$Z_{th(load)}$	load detection threshold impedance	amplifier DC load detection; I²C-bus mode only: R_{PROG} = 1500 Ω/1 %		-	-	25	Ω
		line driver DC load detection; I²C-bus mode only: R_{PROG} = 1500 Ω/1 %		120	-	500	Ω
		open load DC load detection; I²C-bus mode only: R_{PROG} = 1500 Ω/1 %	[9]	5	-	-	kΩ
I_{oM}	peak output current	AC load bit is set; I²C-bus mode only: R_{PROG} = 1500 Ω/1 %; T_j > 0 °C		320	-	-	mA
		AC load bit is not set; I²C-bus mode only: R_{PROG} = 1500 Ω/1 %; T_j > 0 °C		-	-	200	mA