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TDA18271HD

Silicon Tuner IC

Rev. 04 — 19 May 2009 Product data sheet

1. General description

The TDA18271HD is a Silicon Tuner IC designed mainly for terrestrial analog and digital TV reception. The TDA18271HD integrates the overall tuning function, including selectivity.

The TDA18271HD is compatible with all analog and digital TV standards and delivers a low IF signal to a demodulator (for analog TV) and/or channel decoder (for digital TV).

This specification is based on software version 3.4.

2. Features

- Fully integrated RF tracking filters for unwanted signal suppression
- Fully integrated IF selectivity (no need for external SAW filters)
- Worldwide multistandard terrestrial (all analog and digital worldwide terrestrial standards supported)
- Integrated loop-through and slave tuner output for straightforward multi-Silicon Tuner application
- Fully integrated oscillators with no external components
- Alignment free
- Integrated wide-band gain control
- Single 3.3 V power supply
- Low power consumption
- Crystal oscillator output buffer (16 MHz) for single crystal applications
- I^2C-bus interface compatible with 3.3 V and 5 V microcontrollers
- Three Standby modes
- RoHS packaging

3. Applications

3.1 Target applications

- Hybrid (analog and digital TV) for PCTV, DVD-R and TV applications
- Application optimization is described in application notes *AN602*, *AN604* and *AN605*

3.2 Key benefits

- The TDA18271HD is a Silicon Tuner targeting digital and analog TV applications. The aim is to match the performance of conventional Can tuners while reducing the size of the tuner function. Additionally, the following benefits are provided:
  - Easy on-board integration
  - Easy dual tuner configuration
  - Drastic size reduction of the tuner function and power consumption

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$f_{RF(STO)}$	RF frequency on pin STO	slave tuner output		45	-	864	MHz
NF_{tun}	tuner noise figure	maximum gain		-	5.5	-	dB
φ_n	phase noise	1 kHz and 10 kHz		-	–89	-	dBc/Hz
P	power dissipation			-	780	-	mW
$V_{i(max)}$	maximum input voltage	1 dB gain compression, one analog TV signal at RF input (–5 dBm)		-	103	-	dBµV
α_{image}	image rejection			-	65	-	dB
S_{dig}	digital sensitivity	DVB-T (64 QAM $^2/_3$); BER = 2.10^{-4}	[1]	-	–82	-	dBm
S_a	analog sensitivity	50 dB video SNR weighted 22 dBµV (color loss)	[2]	-	58	-	dBµV

[1] Measured with TDA10048HN channel decoder.

[2] Measured with TDA8295 IF modulator.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA18271HD/C2	HLQFN64R	plastic thermal enhanced low profile quad flat package; no leads; 64 terminals; resin based; body 9 × 9 × 1.6 mm	SOT903-1

6. Block diagram

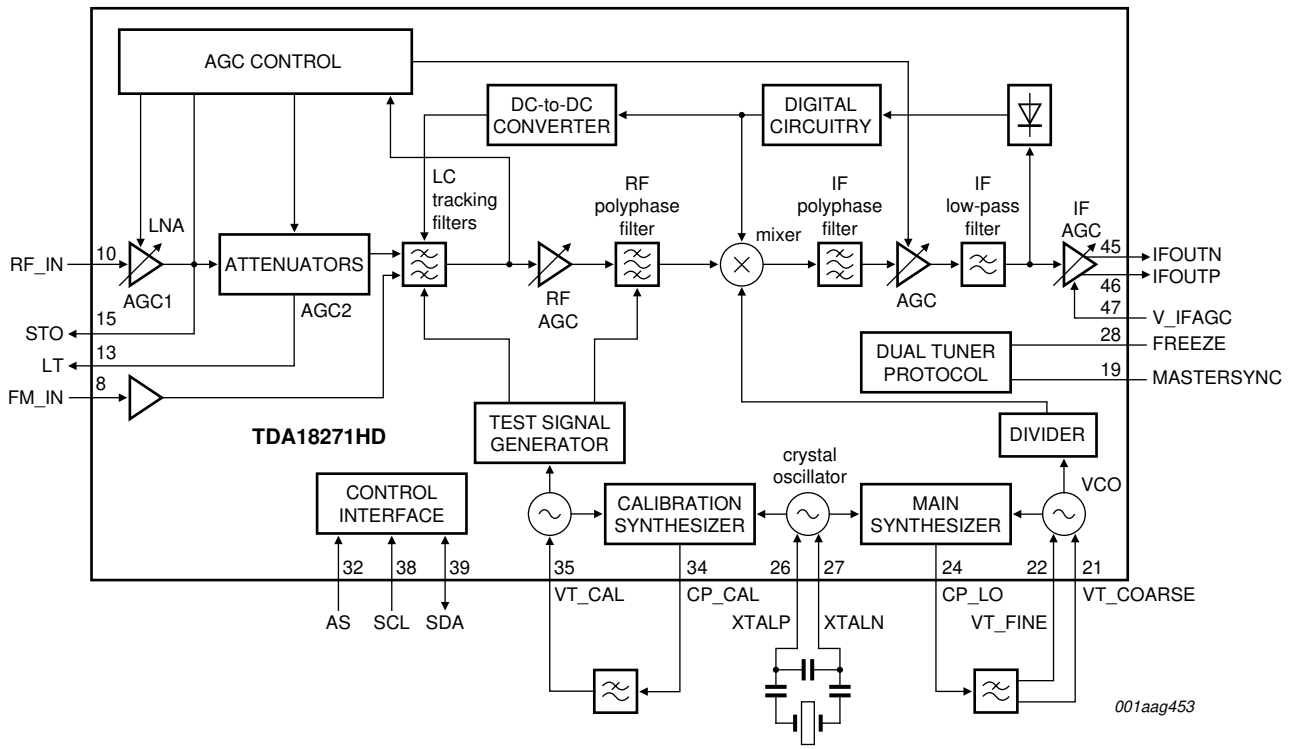


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

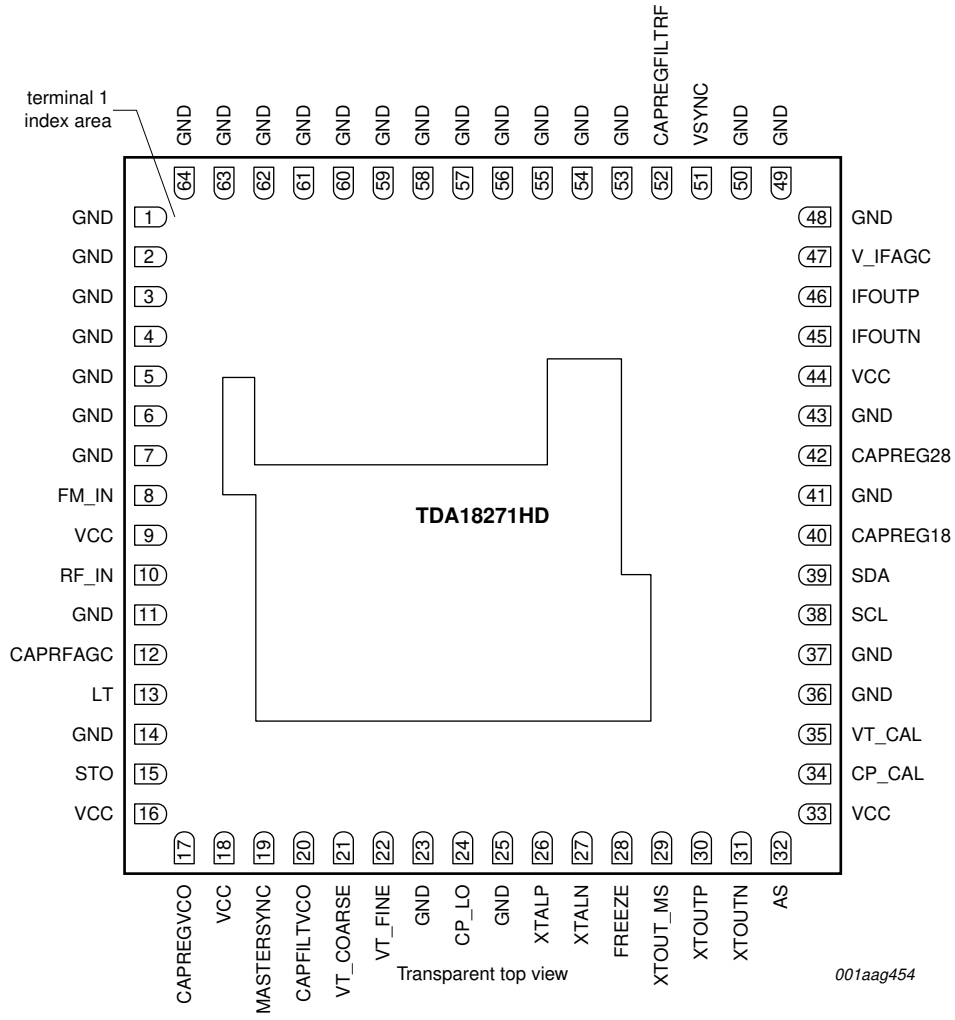


Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
GND	1 to 7	ground
FM_IN	8	unbalanced FM input
VCC	9	3.3 V supply voltage
RF_IN	10	unbalanced RF (TV) input
GND	11	ground
CAPRFAGC	12	RF AGC filtering
LT	13	loop-through output

Table 3. Pin description *...continued*

Symbol	Pin	Description
GND	14	ground
STO	15	slave tuner output
VCC	16	3.3 V supply voltage
CAPREGVCO	17	VCO supply decoupling
VCC	18	3.3 V supply voltage
MASTERSYNC	19	synchronization signal for dual tuner applications; leave open for single tuner applications
CAPFILTVCO	20	VCO reference decoupling
VT_COARSE	21	LO tuning voltage input
VT_FINE	22	LO tuning voltage input
GND	23	ground
CP_LO	24	charge pump of the local synthesizer
GND	25	ground
XTALP	26	crystal oscillator input
XTALN	27	crystal oscillator input
FREEZE	28	synchronization signal for multi tuner applications; leave open for single tuner applications
XTOUT_MS	29	XTOUT mode and master/slave selection
XTOUTP	30	crystal oscillator output buffer
XTOUTN	31	crystal oscillator output buffer
AS	32	I^2C-bus address selection input
VCC	33	3.3 V supply voltage
CP_CAL	34	charge pump of the calibration synthesizer
VT_CAL	35	tuning voltage of the calibration synthesizer
GND	36, 37	ground
SCL	38	I^2C-bus clock input
SDA	39	I^2C-bus data input/output
CAPREG18	40	internal regulator decoupling
GND	41	ground
CAPREG28	42	internal regulator decoupling
GND	43	ground
VCC	44	3.3 V supply voltage
IFOUTN	45	IF output
IFOUTP	46	IF output
V_IFAGC	47	IF gain control input
GND	48 to 50	ground
VSYNC	51	vertical synchronization input for analog applications; connect to ground for digital applications
CAPREGFILTRF	52	internal regulator decoupling
GND	53 to 64	ground
GND	exposed die	ground

8. Functional description

The RF input signal is driven to a low-noise amplifier. It is then band-pass filtered, amplified and fed to the image rejection mixer. The mixer downconverts the RF signal to a low IF depending on the channel bandwidth.

Standard IF filters are implemented for 1.5 MHz, 6 MHz, 7 MHz and 8 MHz channel bandwidths; see Table 43.

The Silicon Tuner can be used either as TV receiver or FM radio receiver.

The TDA18271HD requires a single 16 MHz crystal for clock generation. When bit XTOUT_ON = 1, a clock signal is available on pins XTOUTP and XTOUTN to drive a second tuner, a channel decoder or an IF demodulator (TDA8295) for analog TV reception and FM radio.

Remark: Most recent video decoders from NXP Semiconductors include a low IF demodulation function.

8.1 TV and FM reception

The Silicon Tuner can be used in two modes, selectable via the I^2C-bus:

- TV reception: the RF signal must be connected to pin RF_IN
- FM reception: the RF signal must be connected to pin FM_IN or RF_IN

The RF_IN input pin can also be used for FM reception at the cost of software modification. The FM_IN input pin can only receive signals in the FM frequency range.

8.2 Master and slave operation

The TDA18271HD allows easy dual-tuner configuration.

Each individual tuner has to be set either to Master mode or Slave mode by applying a specific DC voltage to the XTOUT_MS pin; see Table 4. This will decide whether the crystal oscillator part is used as negative impedance connected to the crystal part or as a current buffer.

Table 4. Master/slave selection

Voltage on pin XTOUT_MS	Tuner type	Crystal oscillator function
0 V to $0.1V_{CC}$	master	negative impedance presented to the crystal
$0.4V_{CC}$ to $0.6V_{CC}$	slave	current input buffer

In dual tuner applications:

- The first tuner is set to Master mode
- The second tuner has to be set to Slave mode

In single tuner applications:

- The tuner must be set to Master mode

8.3 Tuner outputs

The tuner provides a slave tuner output (pin STO) and a loop-through output (pin LT). These outputs are used to transmit the antenna signal to other tuners. Each output has its own characteristics (see Table 58 and Table 59).

8.3.1 Loop-through output

The gain between the antenna connector and the loop-through pin (pin LT) equals 0 dB. This pin can be connected to any consumer electronic equipment.

8.3.2 Slave tuner output

In dual tuner applications the slave tuner output (pin STO) must be connected to the RF input of the slave tuner TDA18271HD.

The gain between the antenna connector and the slave tuner output can change according to the input level. The slave tuner will automatically compensate for the gain change, using the MASTERSYNC and FREEZE signals.

8.4 Crystal input mode

The TDA18271HD requires a 16 MHz crystal reference. The chosen crystal must withstand at least 100 µW drive level and an additional shunt capacitor with a typical value of 5.6 pF as shown in Figure 1 is also needed. The quartz references for which the performances are guaranteed are:

- NDK NX5032
- Siward SX-5032
- TXC 9C series
- Chungho Elcom HC49S profile

Clock reference:

- In Master mode, the clock reference must be provided by a 16 MHz crystal connected between pins XTALP and XTALN of the master tuner
- In Slave mode, the clock reference must be provided by pins XTOUTP and XTOUTN of the tuner in Master mode to pins XTALP and XTALN of the tuner in Slave mode

8.5 Crystal output mode

Pins XTOUTP and XTOUTN deliver a symmetrical sine waveform to drive the channel decoder and/or IF demodulator. The load on these outputs should be made similar to ensure optimum performances. If only one crystal output is used, the unused output should be loaded by an equivalent capacitance.

9. Control interface

9.1 I²C-bus format, Write/Read mode

Remark: The I²C-bus read in the TDA18271HD must read the entire I²C-bus map, with required subaddress 00h. The number of bytes read is 16, or 39 in extended register mode; see Table 7. Reading write-only bits can return values that are different from the programmed values.

Table 5. I²C-bus format

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Address byte 1	-	-	1	1	0	0	0	MA[1:0]		R/W
Address byte 2	-	-	0	0	AD[5:0]					
ID byte	ID	00h	1	ID[6:0]						
Thermo byte	TM	01h	POR	LOCK	TM_RANGE	TM_ON	TM_D[3:0]			
Power level byte	PL	02h	POWER_LEVEL[7:0]							
Easy prog byte 1	EP1	03h	POWER_ LEVEL[8]	DIS_ POWER_ LEVEL	0	RF_CAL_OK	IR_CAL_OK	BP_FILTER[2:0]		
Easy prog byte 2	EP2	04h	RF_BAND[2:0]			GAIN_TAPER[4:0]				
Easy prog byte 3	EP3	05h	SM	SM_LT	SM_XT	AGCK_MODE[1:0]		STD[2:0]		
Easy prog byte 4	EP4	06h	FM_RFN	XTOUT_ON	1	IF_LEVEL[2:0]			CAL_MODE[1:0]	
Easy prog byte 5	EP5	07h	EXTENDED _REG	IR_GSTEP[2:0]			0	IR_MEAS[2:0]		
Cal post-divider byte	CPD	08h	CAL_POST_DIV[7:0]							
Cal divider byte 1	CD1	09h	0	CAL_DIV[22:16]						
Cal divider byte 2	CD2	0Ah	CAL_DIV[15:8]							
Cal divider byte 3	CD3	0Bh	CAL_DIV[7:0]							
Main post-divider byte	MPD	0Ch	IF_NOTCH	MAIN_POST_DIV[6:0]						
Main divider byte 1	MD1	0Dh	0	MAIN_DIV[22:16]						
Main divider byte 2	MD2	0Eh	MAIN_DIV[15:8]							
Main divider byte 3	MD3	0Fh	MAIN_DIV[7:0]							
Extended byte 1	EB1	10h	EB1[7:3]					CALVCO_ FORLON	AGC1_ ALWAYS_ MASTERN	AGC1_ FIRSTN
Extended byte 2	EB2	11h	EB2[7:0]							
Extended byte 3	EB3	12h	EB3[7:0]							
Extended byte 4	EB4	13h	EB4[7:6]		LO_FORCE SRCE	EB4[4:0]				
Extended byte 5	EB5	14h	EB5[7:0]							
Extended byte 6	EB6	15h	EB6[7:0]							

Table 5. I²C-bus format *…continued*

Name	Byte name	Sub address	Bit							
			7	6	5	4	3	2	1	0
Extended byte 7	EB7	16h	EB7[7:6]		CAL_ FORCE SRCE	EB7[4:0]				
Extended byte 8	EB8	17h	CID_ALARM	EB8[6:4]			EB8[3]	EB8[2:0]		
Extended byte 9	EB9	18h	EB9[7:0]							
Extended byte 10	EB10	19h	EB10[7:6]		CID_GAIN[5:0]					
Extended byte 11	EB11	1Ah	EB11[7:0]							
Extended byte 12	EB12	1Bh	EB12[7:6]		PD_AGC1_ DET	PD_AGC2_ DET	EB12[3:0]			
Extended byte 13	EB13	1Ch	EB13[7]	RFC_K[2:0]			RFC_M[1:0]		EB13[1:0]	
Extended byte 14	EB14	1Dh	RFC_CPROG[7:0]							
Extended byte 15	EB15	1Eh	EB15[7:4]				EB15[3:0]			
Extended byte 16	EB16	1Fh	EB16[7:0]							
Extended byte 17	EB17	20h	EB17[7:0]							
Extended byte 18	EB18	21h	AGC1_ LOOP_OFF	EB18[6:2]					AGC1_GAIN[1:0]	
Extended byte 19	EB19	22h	EB19[7:0]							
Extended byte 20	EB20	23h	EB20[7:6]		FORCE_ LOCK	EB20[4:0]				
Extended byte 21	EB21	24h	AGC2_ LOOP_OFF	EB21[6:2]					AGC2_GAIN[1:0]	
Extended byte 22	EB22	25h	EB22[7]	RF_TOP[2:0]			IF_TOP[3:0]			
Extended byte 23	EB23	26h	EB23[7:3]					FORCELP_ FC2_EN	LP_FC	EB23[0]

9.2 I²C-bus at Power-On Reset

Table 6. I²C-bus at Power-On Reset

Name	Byte	Subaddress	7[1]	6[1]	5[1]	4[1]	3[1]	2[1]	1[1]	0[1]
Address byte 1	-	-	1	1	0	0	0	MA[1]	MA[0]	X
Address byte 2	-	-	X	X	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]
ID byte	ID	00h	1	0	0	0	0	1	0	0
Thermo byte	TM	01h	1	0	0	0	X	X	X	X
Power level byte	PL	02h	X	X	X	X	X	X	X	X
Easy prog byte 1	EP1	03h	X	1	0	0	0	1	1	0
Easy prog byte 2	EP2	04h	1	1	0	1	1	1	1	1
Easy prog byte 3	EP3	05h	1	0	0	1	0	0	1	0
Easy prog byte 4	EP4	06h	0	1	1	0	0	0	0	0
Easy prog byte 5	EP5	07h	0	0	1	1	0	0	0	0
Cal post-divider byte	CPD	08h	0	0	0	0	0	0	0	0
Cal divider byte 1	CD1	09h	0	0	0	0	0	0	0	0
Cal divider byte 2	CD2	0Ah	0	0	0	0	0	0	0	0
Cal divider byte 3	CD3	0Bh	0	0	0	0	0	0	0	0
Main post-divider byte	MPD	0Ch	0	0	0	0	0	0	0	0
Main divider byte 1	MD1	0Dh	0	0	0	0	0	0	0	0
Main divider byte 2	MD2	0Eh	0	0	0	0	0	0	0	0
Main divider byte 3	MD3	0Fh	0	0	0	0	0	0	0	0
Extended byte 1	EB1	10h	1	1	1	1	1	1	1	1
Extended byte 2	EB2	11h	0	0	0	0	0	0	0	1
Extended byte 3	EB3	12h	1	0	0	0	0	1	0	0
Extended byte 4	EB4	13h	0	1	0	0	0	0	0	1
Extended byte 5	EB5	14h	0	0	0	0	0	0	0	1
Extended byte 6	EB6	15h	1	0	0	0	0	1	0	0
Extended byte 7	EB7	16h	0	1	0	0	1	0	0	0
Extended byte 8	EB8	17h	0	1	1	1	X	1	0	1
Extended byte 9	EB9	18h	0	0	0	0	0	0	0	0
Extended byte 10	EB10	19h	X	X	X	X	X	X	X	X
Extended byte 11	EB11	1Ah	1	0	0	0	0	1	1	0
Extended byte 12	EB12	1Bh	0	0	0	0	0	1	1	1
Extended byte 13	EB13	1Ch	1	1	0	0	0	0	1	0
Extended byte 14	EB14	1Dh	0	0	0	0	0	0	0	0
Extended byte 15	EB15	1Eh	1	0	0	0	X	X	X	X
Extended byte 16	EB16	1Fh	0	0	0	X	X	X	0	0
Extended byte 17	EB17	20h	0	0	0	X	X	X	X	X
Extended byte 18	EB18	21h	0	0	0	0	0	0	0	0
Extended byte 19	EB19	22h	0	0	0	X	X	X	0	0
Extended byte 20	EB20	23h	1	0	0	X	X	X	X	X

Table 6. I²C-bus at Power-On Reset *…continued*

Name	Byte	Subaddress	7[1]	6[1]	5[1]	4[1]	3[1]	2[1]	1[1]	0[1]
Extended byte 21	EB21	24h	0	0	1	1	0	0	1	1
Extended byte 22	EB22	25h	0	1	0	0	1	0	0	0
Extended byte 23	EB23	26h	1	0	1	1	0	0	0	0

[1] X indicates a bit not changed on reset.

9.3 Description of symbols used in I²C-bus format table

Table 7. I²C-bus register bits explanation

Address	Byte	Symbol	Description	Reference
		MA[1:0]	programmable address bits	Table 8
		AD[5:0]	programmable address bits of the first programming byte	Table 9
Data bytes				
00h	ID	ID[6:0]	chip identification number	Table 10
01h	TM	POR	Power-On Reset bit	Table 11
		LOCK	indicates that the main synthesizer is locked to the programmed frequency	
		TM_RANGE	range selection bit for the internal die sensor	
		TM_ON	enables die temperature measurement	
		TM_D[3:0]	data from die temperature measurement (read only)	
02h	PL	POWER_LEVEL[7:0]	Power level indicator value (read only)	Table 12
03h	EP1	POWER_LEVEL[8]		
		DIS_POWER_LEVEL	disables the power-on level function	Table 13
		RF_CAL_OK	indicates that the RF tracking filter calibration procedure has been successful	
		IR_CAL_OK	indicates that the complete image rejection calibration procedure has been successful	
		BP_FILTER[2:0]	RF band-pass filter selection	
04h	EP2	RF_BAND[2:0]	RF tracking filter band selection	Table 14
		GAIN_TAPER[4:0]	gain taper value	
05h	EP3	SM	Sleep mode, Standby modes	Table 15
		SM_LT		
		SM_XT		
		AGCK_MODE[1:0]	defines the standard	
		STD[2:0]	defines the standard	
06h	EP4	FM_RFN	selects which input is fed to RF filter	Table 18
		XTOUT_ON	provides the 16 MHz crystal reference on the XTOUTP and XTOUTN pins	
		IF_LEVEL[2:0]	IF output level selection	
		CAL_MODE[1:0]	calibration mode selection	
07h	EP5	EXTENDED_REG	enables the extended register addressing	Table 19
		IR_GSTEP[2:0]	gain step for image rejection calibration	
		IR_MEAS[2:0]	image rejection measurement frequency range	

Table 7. I²C-bus register bits explanation *...continued*

Address	Byte	Symbol	Description	Reference
08h	CPD	CAL_POST_DIV[7:0]	calibration synthesizer post-divider	Table 20
09h	CD1	CAL_DIV[22:16]	calibration synthesizer main divider bits	Table 21
0Ah	CD2	CAL_DIV[15:8]		
0Bh	CD3	CAL_DIV[7:0]		
0Ch	MPD	IF_NOTCH	adds a DC notch in IF for a better adjacent channels rejection; depends on standards	Table 22
		MAIN_POST_DIV[6:0]	LO synthesizer post-divider bits	
0Dh	MD1	MAIN_DIV[22:16]	LO synthesizer main divider bits	Table 23
0Eh	MD2	MAIN_DIV[15:8]		
0Fh	MD3	MAIN_DIV[7:0]		
Extended bytes				
10h	EB1	CALVCO_FORLON	determines which VCO is used during Normal mode operations	Table 24
		AGC1_ALWAYS_MASTERN	enables AGC1 normal operation whatever the tuner type (master or slave)	
		AGC1_FIRSTN	determines which AGC (1 or 2) will be detected when detectors 1 and 2 are up	
13h	EB4	LO_FORCESRCE	forces the main PLL charge pump to source current to the main PLL loop filter	
16h	EB7	CAL_FORCESRCE	forces the calibration PLL charge pump to source current to the calibration PLL loop filter	
17h	EB8	CID_ALARM	indicates that signal sensed by the power detector used during calibrations is out of range	
19h	EB10	CID_GAIN[5:0]	calibration power detector output	
1Bh	EB12	PD_AGC1_DET	power-down of AGC1 detector	
		PD_AGC2_DET	power-down of AGC2 detector	
1Ch	EB13	RFC_K[2:0]	parameter used during the RF tracking filter calibration	
		RFC_M[1:0]	parameter used during the RF tracking filter calibration	
1Dh	EB14	RFC_CPROG[7:0]	tuning word of the RF tracking filters	
21h	EB18	AGC1_LOOP_OFF	turns off the AGC1 loop	
		AGC1_GAIN[1:0]	AGC1 gain	
23h	EB20	FORCE_LOCK	forces the internal PLLs lock indicator to logic 1	
24h	EB21	AGC2_LOOP_OFF	turns off the AGC2 loop	
		AGC2_GAIN[1:0]	AGC2 gain	
25h	EB22	RF_TOP[2:0]	Take-Over Point (TOP) of the RF AGC, detection in RF	
		IF_TOP[3:0]	TOP of the RF AGC, detection in IF	
26h	EB23	FORCELP_FC2_EN	FM filter selection	
		LP_FC		

9.3.1 I²C-bus address selection

The programmable module address bits MA[1:0] allow up to four tuners to be addressed in one system. Bits MA1 and MA0 are programmed by a specific voltage (V_{AS}) applied to pin AS. The relationship between the status of bits MA[1:0] and the voltage applied to pin AS is shown in Table 8.

Table 8. Address byte 1 bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 3	-	R/W	1 1000*	must be set to 1 1000
2 to 1	MA[1:0]	R/W		programmable address bits
			00	V_{AS} = 0 V to 0.1 × V_{CC}
			01	V_{AS} = 0.2 × V_{CC} to 0.3 × V_{CC}
			10	V_{AS} = 0.4 × V_{CC} to 0.6 × V_{CC}
			11	V_{AS} = 0.9 × V_{CC} to V_{CC}
0	R/W	R/W	0	write mode
			1	read mode

Table 9. Address byte 2 bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 6	-	R/W	00	must be set to 00
5 to 0	AD[5:0]	R/W	-	programmable address bits of the first programming byte

9.3.2 Description of chip ID byte

Table 10. ID - identification byte (subaddress 00h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	-	R	1*	must be 1
6 to 0	ID[6:0]	R	000 0100*	TDA18271HD/C2 identification number

9.3.3 Description of temperature sensor byte

The temperature sensor is not available in Device-off mode, as it requires a 16 MHz clock to operate.

Table 11. TM - Thermo byte (subaddress 01h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	POR	R	1*	power supply falls below the power-on reset level and is reset after a read operation ending with a stop condition
			0	power supply is above the power-on reset level
6	LOCK	R	1	main synthesizer is locked to the programmed frequency
			0*	main synthesizer is not locked to the programmed frequency
5	TM_RANGE	R/W		temperature range selection for the internal die sensor (see Table 52)
			1	92 °C to 122 °C
			0*	60 °C to 90 °C
4	TM_ON	R/W	1	enables die temperature measurement (see Table 52)
			0*	disables die temperature measurement (see Table 52)
3 to 0	TM_D[3:0]	R	XXXX	data from die temperature measurement (see Table 52)

9.3.4 Description of power level byte (read mode)

There are 9 power level bits sent in power level bytes 2 and 3. They indicate the composite voltage gain of the LNA, the loaded attenuator voltage gains, and the level at the input of the RF AGC.

Table 12. PL - Power level (address 02h and 03h) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
03h	EP1	7	POWER_LEVEL[8]	R		AGC2 gain, attenuator voltage gain including load, the attenuator load is 50 Ω (allows the maximum gain of −6 dB)
02h	PL	7	POWER_LEVEL[7]			
					00	−15 dB
					01	−12 dB
					10	−9 dB
					11	−6 dB
		6 to 5	POWER_LEVEL[6:5]	R		AGC1 gain, LNA voltage gain, the LNA voltage gain assumes a 75 Ω source impedance and a low output impedance
					00	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
		4 to 0	POWER_LEVEL[4:0]	R		sensed level at the input of the RF AGC, detector slope is −1 dB/step
					0 0000	103 dBµV (RMS value)
					0 0001	102 dBµV (RMS value)
					...	...
					1 1110	73 dBµV (RMS value)
					1 1111	72 dBµV (RMS value)

9.3.5 Description of Easy prog byte 1

Table 13. EP1 - Easy prog byte 1 (subaddress 03h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	POWER_LEVEL[8]	R		see Table 12
6	DIS_POWER_LEVEL	R/W	1*	power level disabled
			0	power level enabled
5	-	R/W	0*	must be set to 0
4	RF_CAL_OK	R/W		RF tracking filter calibration procedure (see Section 9.4.9); updated each time the procedure is started
			1	successful
			0*	not successful

Table 13. EP1 - Easy prog byte 1 (subaddress 03h) bit description *...continued*

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
3	IR_CAL_OK	R/W		complete image rejection calibration procedure (see Section 9.4.4); can only be reset with POR
			1	successful
			0*	not successful
2 to 0	BP_FILTER[2:0]	R/W	110*	RF band-pass filter selection (see Table 44)

9.3.6 Description of Easy prog byte 2

Table 14. EP2 - Easy prog byte 2 (subaddress 04h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 5	RF_BAND[2:0]	R/W	110*	RF tracking filter band selection (see Table 45)
4 to 0	GAIN_TAPER[4:0]	R/W		gain taper value (see Table 49)
			1 1111*	minimum attenuation
			0 0000	maximum attenuation

9.3.7 Description of Easy prog byte 3

The TDA18271HD has three different Standby modes. Two Standby modes are dedicated to special application demands; the third Standby mode is called ‘device-off’. It represents the smallest achievable power consumption.

Table 15. EP3 - Easy prog byte 3 (subaddress 05h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 5	SM, SM_LT, SM_XT	R/W	100	Power modes Table 16
4 to 3	AGCK_MODE[1:0]	R/W	10010*	defines the standard
2 to 0	STD[2:0]	R/W		description of standards (see Table 43)

Table 16. Power modes

Bit			Circuit			Mode[1]
SM	SM_LT	SM_XT	Loop-through	Slave-tuner output	Crystal oscillator	
0	0	0	on	on	on	Normal mode
1	0	0	on	on	on	Standby mode with crystal oscillator, slave-tuner output and loop-through output on
1	1	0	off	off	on	Standby mode with only crystal oscillator and its output buffer on
1	1	1	off	off	off	Device-off mode

[1] In all modes, the I²C-bus interface remains active. All other bit settings are invalid.

Table 17. AGC modes

Standard	AGC_MODE[1:0] EP3[4:3][1]		Reference signal
FM radio	1	1	internal
Analog TV standards	0	1	VSYNC
Digital TV standards	1	1	internal

[1] Depending on the programmed AGC_MODE, AGC1 can be synchronous with either VSYNC or an internal 16 MHz signal; for analog reception, when no synchronization signal is available for VSYNC pin, the internal reference may be used.

9.3.8 Description of Easy prog byte 4

Table 18. EP4 - Easy prog byte 4 (subaddress 06h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	FM_RFN	R/W		selection which input is fed to RF filter
			1	FM input (RF LNA on; FM LNA on)
			0*	RF input (RF LNA on; FM LNA off)
6	XTOUT_ON	R/W	1*	16 MHz on pins XTOUT
			0	not 16 MHz on pins XTOUT
5	-	R/W	1*	must be set to logic 1
4 to 2	IF_LEVEL[2:0]	R/W		IF output level selection and attenuation with regard to 2 V (p-p)
			000*	2 V (p-p); 0 dB
			001	1.25 V (p-p); 4 dB
			010	1 V (p-p); 6 dB
			011	0.8 V (p-p); 8 dB
			100	not used
			101	not used
			110	0.6 V (p-p); 10.4 dB
			111	0.5 V (p-p); 12 dB
1 to 0	CAL_MODE[1:0]	R/W		calibration mode selection
			00*	no calibration (Normal mode)
			01	Power detection mode
			10	image rejection calibration (IRCAL) mode
			11	RF tracking filter calibration (RFCAL) mode

All calibrations require a precise set of sequential operations, therefore it is mandatory to follow the flowcharts described in Section 9.4.

The TDA18271HD has two calibration modes: one for the image rejection calibration and one for the RF tracking filter calibration.

The image rejection calibration optimizes tunable parameters inside the mixer using a set of internal measurements to ensure a 65 dB typical value of image rejection. The internal signal used during this phase is generated by the PLL calibration (CAL PLL).

The RF tracking filters central frequency can be adjusted with the tuning word RFC_CPROG. The RF tracking filter calibration (RFCAL) uses an internal tone at the input of the tracking filters (generated by CAL PLL) and finds the RFC_CPROG that corresponds to the maximum transmitted power. The RFCAL is just a small part of a more complex algorithm fully described in the flowcharts in Section 9.4.

The Power detection mode is a Normal mode in which the detector used for the calibrations is switched ON. This special mode enables power sensing at the input of the TDA18271HD and makes the power scan algorithm possible (see Section 9.4.8 "Flowchart TDA18271PowerScan").

9.3.9 Description of Easy prog byte 5

Table 19. EP5 - Easy prog byte 5 (subaddress 07h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	EXTENDED_REG	R/W		enables extended register addressing
			1	extended register (10h to 26h)
			0*	limited register (00h to 0Fh); only 1 byte can be programmed after address 0Fh within 1 transmission
6 to 4	IR_GSTEP[2:0]	R/W	011*	gain step for image rejection calibration
3	-	R/W	0*	must be set to logic 0
2 to 0	IR_MEAS[2:0]	R/W	000*	image rejection measurement frequency range (see Table 53)

9.3.10 Description of Cal post-divider byte

Table 20. CPD - Cal post-divider byte (subaddress 08h) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7 to 0	CAL_POST_DIV[7:0]	R/W	00h*	calibration synthesizer post-divider (see Table 48)

9.3.11 Description of Cal divider bytes 1, 2 and 3

Table 21. CD1, CD2 and CD3 - Cal divider bytes 1, 2 and 3 (address 09h, 0Ah and 0Bh) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
09h	CD1	7	-	R/W	0*	must be set to 0
		6 to 0	CAL_DIV[22:16]	R/W	00h*	calibration synthesizer main divider bits
0Ah	CD2	7 to 0	CAL_DIV[15:8]	R/W	00h*	
0Bh	CD3	7 to 0	CAL_DIV[7:0]	R/W	00h*	

9.3.12 Description of Main post-divider byte

Table 22. MPD - Main post-divider byte (subaddress 0Ch) bit description

*Legend: * power-on reset value.*

Bit	Symbol	Access	Value	Description
7	IF_NOTCH	R/W	0*	adds a DC notch in IF for better adjacent channels rejection; depends on standards; see Table 43
6 to 0	MAIN_POST_DIV[6:0]	R/W	000	LO synthesizer post-divider; see Table 47

9.3.13 Description of Main divider bytes 1, 2 and 3

Table 23. MD1, MD2 and MD3 - Main divider bytes 1, 2 and 3 (address 0Dh, 0Eh and 0Fh) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
0Dh	MD1	7	-	R/W	0*	must be set to 0
		6 to 0	MAIN_DIV[22:16]	R/W	00h*	LO synthesizer main divider bits
0Eh	MD2	7 to 0	MAIN_DIV[15:8]	R/W	00h*	
0Fh	MD3	7 to 0	MAIN_DIV[7:0]	R/W	00h*	

9.3.14 Description of Extended bytes 1 to 23

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
10h	EB1	7 to 3	EB1[7:3]	R	1 1111*	extended byte 1
		2	CALVCO_FORLON	R		determines VCO used during Normal mode operations
					1*	LO VCO is used
					0	CAL VCO is used
		1	AGC1_ALWAYS_MASTERN	R		enables AGC1 normal operation whatever the tuner type (master or slave)
					1*	normal operation for the master; 6 dB fixed for the slave
					0	normal operation for both the master and the slave
		0	AGC1_FIRSTN	R		determines which AGC will be updated when detectors 1 and 2 are active
					1*	AGC1 and AGC2 both updated
					0	AGC1 has priority on AGC2
11h	EB2	7 to 0	EB2[7:0]	R/W	0000 0001*	extended byte 2
12h	EB3	7 to 0	EB3[7:0]	R/W	1000 0100*	extended byte 3

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *...continued*

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
13h	EB4	7 to 6	EB4[7:6]	R/W	01*	extended byte 4
		5	LO_FORCESRCE	R/W	1	forces the main PLL charge pump to source current to the main PLL loop filter
					0*	no force
		4 to 0	EB4[4:0]	R/W	0 0001*	extended byte 4
14h	EB5	7 to 0	EB5[7:0]	R/W	0000 0001*	extended byte 5
15h	EB6	7 to 0	EB6[7:0]	R/W	1000 0100*	extended byte 6
16h	EB7	7 and 6	EB7[7:6]	R/W	01*	extended byte 7
		5	CAL_FORCESRCE	R/W	1	forces the CAL PLL charge pump to source current to the CAL PLL loop filter
					0*	no force
		4 to 0	EB7[4:0]	R/W	0 1000*	extended byte 7
17h	EB8	7	CID_ALARM	R		signal sensed by the power detector used during calibrations
					1	out of range
					0*	in range
		6 to 4	EB8[6:4]	R/W	111 0101*	extended byte 8
		3	EB8[3]	R		
		2 to 0	EB8[2:0]	R/W		
18h	EB9	7 to 0	EB9[7:0]	W	0000 0000*	extended byte 9
19h	EB10	7 and 6	EB10[7:6]	R	00*	extended byte 10
		5 to 0	CID_GAIN[5:0]	R	-	calibration power detector output
1Ah	EB11	7 to 0	EB11[7:0]	R/W	1000 0110*	extended byte 11
1Bh	EB12	7 and 6	EB12[7:6]	R	00*	extended byte 12
		5	PD_AGC1_DET	R/W		AGC1 detector
					1	power-down
					0*	no power-down
		4	PD_AGC2_DET	R/W		AGC2 detector
					1	power-down
					0*	no power-down
		3 to 0	EB12[3:0]	R/W	0111*	extended byte 12
1Ch	EB13	7	EB13[7]	R/W	1*	extended byte 13
		6 to 4	RFC_K[2:0]	R/W	100*	parameters used during the RF tracking filter calibration (see Table 46)
		3 and 2	RFC_M[1:0]	R/W	00*	
		1 to 0	EB13[1:0]	R/W	10*	extended byte 13
1Dh	EB14	7 to 0	RFC_CPROG[7:0]	R/W	0000 0000*	tuning word of the RF tracking filters
1Eh	EB15	7 to 4	EB15[7:4]	R/W	1000 XXXX*	extended byte 15
		3 to 0	EB15[3:0]	R		
1Fh	EB16	7 to 0	EB16[7:0]	W	000X XX00*	extended byte 16

Table 24. EB1 to EB23 - Extended bytes 1 to 23 (address 10h to 26h) bit description *...continued*

*Legend: * power-on reset value.*

Address	Register	Bit	Symbol	Access	Value	Description
20h	EB17	7 to 0	EB17[7:0]	W	000X XXXX*	extended byte 17
21h	EB18	7	AGC1_LOOP_OFF	R/W		turns the AGC1 loop
					1	off
					0*	on
		6 to 2	EB18[6:2]	R/W	00000*	extended byte 18
		1 and 0	AGC1_GAIN[1:0]	R/W		AGC1 gain
					00*	6 dB
					01	9 dB
					10	12 dB
					11	15 dB
22h	EB19	7 to 0	EB19[7:0]	W	000X XX00*	extended byte 19
23h	EB20	7 and 6	EB20[7:6]	W	10*	extended byte 20
		5	FORCE_LOCK	W		forces the internal lock indicator
					1	forced to logic 1
					0*	not forced
		4 to 0	EB20[4:0]	W	X XXXX*	extended byte 20
24h	EB21	7	AGC2_LOOP_OFF	R/W		turns the AGC2 loop
					1	off
					0*	on
		6 to 2	EB21[6:2]	R/W	00000*	extended byte 21
		1 and 0	AGC2_GAIN[1:0]	R/W		AGC2 gain
					00*	−15 dB
					01	−12 dB
					10	−9 dB
					11	−6 dB
25h	EB22	7	EB22[7]	R	0*	extended byte 22
		6 to 4	RF_TOP[2:0]	R/W	100*	Take-Over Point of the RF AGC, detection in RF
		3 to 0	IF_TOP[3:0]	R/W	1000*	Take-Over Point of the RF AGC, detection in IF
26h	EB23	7 to 3	EB23[7:3]	R/W	1 0110*	extended byte 23
		2	FORCELP_FC2_EN	R/W	0*	FM filter selection; see Table 25 and Table 26
		1	LP_FC	R/W	0*	
		0	EB23[0]	R/W	0*	extended byte 23

Table 25. Low-pass cut-off frequency when using RF_IN input

RF input	FORCELP_FC2_EN	LP_FC	STD[1:0]	Cut-off frequency (MHz)
RF_IN	1	1	XX	1.5
	0	X	00	6
	0	X	01	7
	0	X	10	8
	0	X	11	9

Table 26. Low-pass cut-off frequency when using FM_IN input

RF input	FORCELP_FC2_EN	LP_FC	STD[1:0]	Cut-off frequency (MHz)
FM_IN	1	0	00	6
	1	0	01	7
	1	0	10	8
	1	0	11	9
	1	1	XX	1.5

9.4 I²C-bus programming flowcharts

The following flowcharts describe how to:

- Initialize the TDA18271HD
- Launch the calibrations
- Go to Normal mode

The image rejection calibration and RF tracking filter calibration must be launched exactly as described in the flowchart, otherwise bad calibration or even blocking of the TDA18211HD can result making it impossible to communicate via the I²C-bus.

Proper internal initialization requires switching to Normal mode using a single I²C-bus sequence from subaddresses 03h to 0Fh.

9.4.1 Flowchart explanation

This section provides instructions for reading the flowcharts.

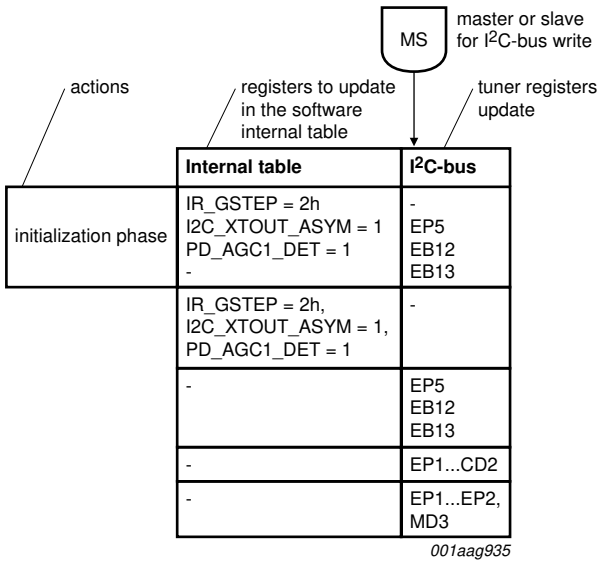


Fig 3. Programming sequence

1. I²C-bus write:
   - IR_GSTEP is updated, no immediate I²C-bus write
   - I2C_XTOUT_ASYM is updated followed by an I²C-bus write of byte EP5
   - PD_AGC1_DET is updated followed by an I²C-bus write of byte EB12
   - I²C-bus write of byte EB13 with current value of the software internal register of byte EB13

   I²C-bus read:
   - Subaddressing is not supported in read mode
   - The mandatory I²C-bus read access procedures to the TDA18271HD are described in Section 9.4.16 “Flowchart TDA18271Read” and Section 9.4.17 “Flowchart TDA18271ReadExtended”
2. Update at the same time is indicated by separation with commas:

   IR_GSTEP, I2C_XTOUT_ASYM and PD_AGC1_DET are updated, no I²C-bus registers updated
3. I²C-bus registers update bytes EP5, EB12 and EB13
4. Bytes EP1 to CD2 are written in a single I²C-bus sequence

   Example:

   Start C0 03 EP1 EP2 EP3 EP4 EP5 CPD CD1 CD2 Stop
5. Bytes EP1, EP2 and MD3 are written in as many I²C-bus sequences as needed

   Example:

   Start C0 03 EP1 EP2 Stop

   Start C0 0F MD3 Stop

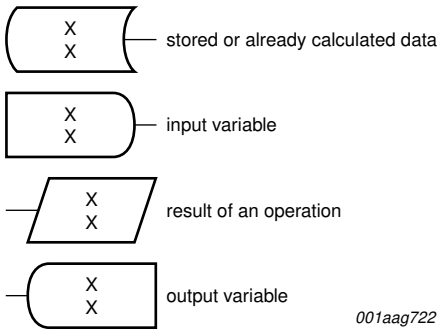
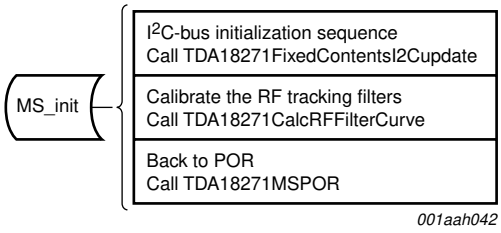
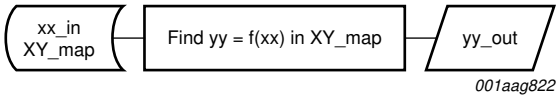


Fig 4. Blocks used in the flowcharts



Master/slave variable MS_init is input for each of the three procedures.

Fig 5. Variable used in multiple procedures

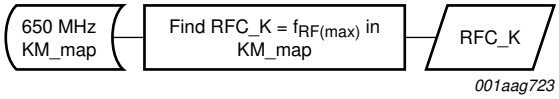


xx is a list of values stored in the first column of the map XY_map.

yy is a list of values stored in column in XY_map

yy_out is the particular value of yy to find row n. $xx(n-1) < xx\_in \leq xx(n)$

a. General description to find a value in a table



Finding the row of RFC_K: 350000 < 650000 ≤ 720000. Result n = 1. The value of RFC_K is then 3; see Table 46

b. Example to find the value RFC_K corresponding to f_{RF} = 650 MHz in the KM_map

Fig 6. Finding a value in a table

Units: In the flowcharts, hexadecimal values end with “h”, decimal values with “d”.

9.4.2 Flowchart TDA18271SetRf_dual

The initialization phase has to be launched before any SetRf.

Table 27. TDA18271SetRf_dual

Function	Description	Reference
Description	protocol top view for a dual tuner application	
Input	RF_freq, Standard (from microcontroller), MS (from microcontroller)[1]	
Table	-	
Output	-	

[1] MS = 1: master is selected for the channel configuration; MS = 0: slave is selected for the channel configuration.

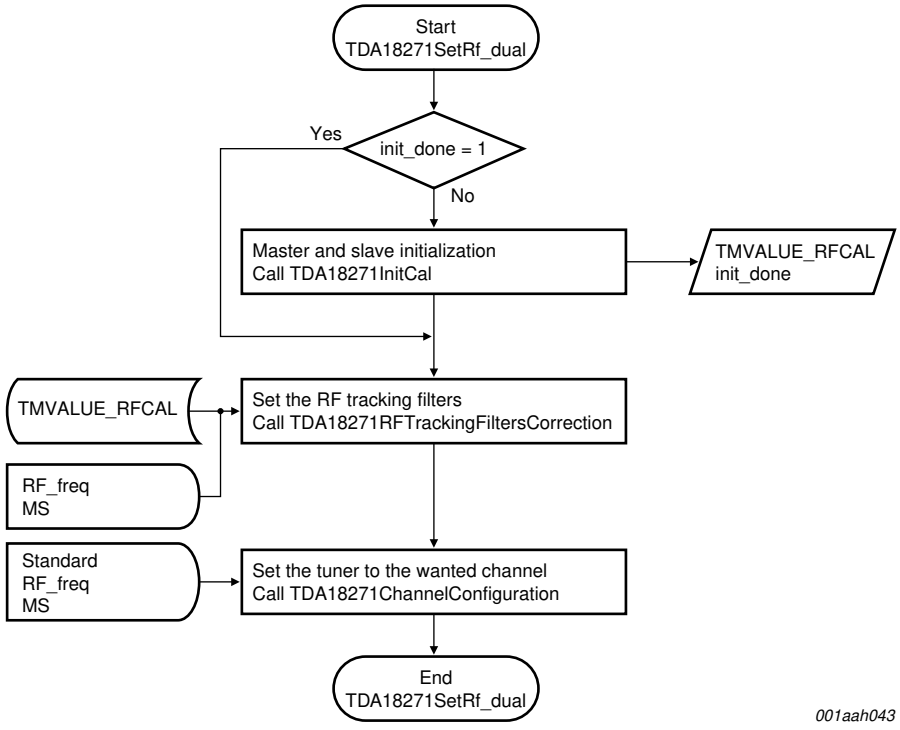


Fig 7. Flowchart TDA18271SetRf_dual

9.4.3 Flowchart TDA18271InitCal

Table 28. TDA18271InitCal

Function	Description	Reference
Description	systematic initializations for master and slave tuners	
Input	MS_init	
Table	-	
Output	TMVALUE_RFCAL, init_done	