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# TDA19988

## Low power, 150 MHz pixel rate HDMI 1.4a transmitter with 3 × 8-bit video inputs, HDCP and CEC support

Rev. 3 — 21 July 2011 Product data sheet

## 1. General description

TDA19988 is a very low power and very small size High-Definition Multimedia Interface (HDMI) 1.4a transmitter. It is backward compatible DVI 1.0 and can be connected to any DVI 1.0 or HDMI sink.

This device is primarily intended for mobile applications like Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP), Mobile Phone and Ultra-Mobile Personal Computer (UM PC), new PC tablet and MID where size and power are key for battery autonomy.

This device is also targeting STB HDMI output applications. This part replaces previous TDA9981 Transmitters with increased features and better performances.

It allows mixing 3 × 8-bit RGB or YCbCr video stream at pixel rate up to 165 MHz together with S/PDIF or I$^2$S-bus audio streams at audio sampling rate up to 192 kHz.

In order to be compatible with most applications, TDA19988 integrates a full programmable input formatter and color space conversion block. The video input formats accepted are YCbCr 4 : 4 : 4 (up to 3 × 8-bit), YCbCr 4 : 2 : 2 semi-planar (up to 2 × 12-bit) and YCbCr 4 : 2 : 2 compliant with ITU656 (up to 1 × 12-bit). In case of ITU656-like format, the input pixel clock can be made active on one (SDR mode) or both edges (DDR mode).

TDA19988AHN and TDA19988AET only include a HDCP 1.4 compliant cipher block. The HDCP keys are stored internally in a non-volatile OTP memory for maximum security.

This device provides additional embedded features like CEC (Consumer Electronic Control). CEC is a single bidirectional bus that transmits CEC commands (like Standby from remote control) over the home appliance network connected through this bus. This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials) of the whole system and enabling the connected devices (CEC enabled) to be controlled by only one remote control.

TDA19988 supports xvYCC HDMI 1.4a feature.

It can be switched to very low power Standby or Sleep modes to save power when HDMI is not used.

TDA19988 embeds I$^2$C-bus master interface for DDC-bus communication to read EDID and to manage HDCP (TDA19988AHN and TDA19988AET only).

This device can be controlled or configured via I$^2$C-bus interface.

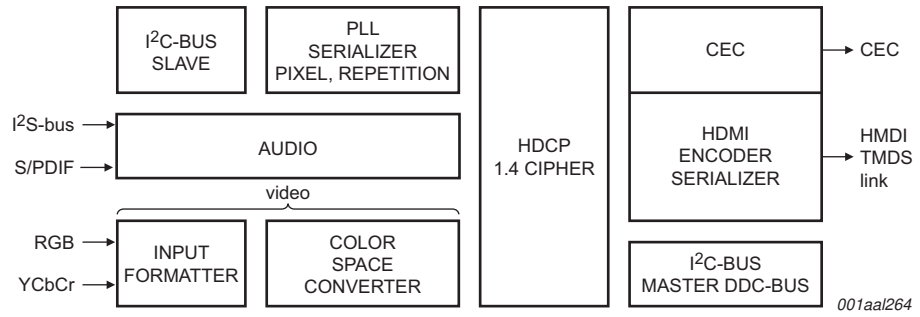



**Fig 1. TDA19988 high-level block diagram**

## 2. Features and benefits

- Compliance:
  - DVI 1.0
  - HDMI 1.4a
  - EIA/CEA-861B
  - CEC (HDMI 1.4a)
  - HDCP 1.4 (TDA19988AHN and TDA19988AET only)
- Video:
  - xvYCC HDMI 1.4a feature
  - Video formats with a pixel rate up to 165 MHz:
    RGB 4 : 4 : 4
    YCbCr 4 : 4 : 4
    YCbCr 4 : 2 : 2 semi-planar
    YCbCr 4 : 2 : 2 ITU656
  - 3D:
    Frame Packing: 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 24/30 Hz
    Side-by-Side (Half): 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 50/60 Hz
    Top-and-Bottom: 720p at 50/60 Hz, 1080i at 50/60 Hz, 1080p at 50/60 Hz
  - Maximum resolution:
    1080p at 50/60 Hz for TV
    1600 × 1200 at 60 Hz for PC (UXGA60)
    720p/1080i at 50/60 Hz in ITU656
  - Programmable color space converter:
    RGB to YCbCr
    YCbCr to RGB
  - Programmable input formatter and upsampler/interpolator allow input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656-like formats
  - Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
  - In ITU656, pixel clock input can be single or dual edges (selectable by I2C-bus)
  - Repetition of video samples as required by HDMI specification
- Audio:

- 4 × I²S-bus or one S/PDIF; audio data rate up to 192 kHz (depending on video format and on package)
- Deals with multiple levels of HDCP (TDA19988AHN and TDA19988AET only) receivers and repeaters
- Internal SHA-1 calculation
- System operation:
  - Master DDC-bus interface for EDID read
  - Controllable via I²C-bus
  - Hot Plug Detect (HPD) and receiver detection (RxSense)
- High performance power management:
  - Standby mode: 18 μW typical
  - Operation mode: 55 mW 720p 24 Hz
- Package:
  - TFBGA64, size 4.5 mm × 4.5 mm × 0.95 mm
  - HVQFN64, size 9 mm × 9 mm × 0.85 mm
- Power management:
  - External voltage supplies 1.8 V
  - Low power
  - Flexible power modes
- Miscellaneous:
  - POR (Power-On Reset)
  - Audio and video inputs LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant
  - 250 MHz to 1.5 GHz TMDS transmitter operation

## 3. Applications

- Digital Video Camera (DVC)
- Digital Still Camera (DSC)
- Portable Multimedia Player (PMP)
- Ultra-Mobile Personal Computer (UM PC)
- YCbCr or RGB high-speed video digitizer
- Blu-ray disc player
- AVR and HDMI splitter
- MID/tablet
- Media box
- Mobile Phone
- Home theater amplifier
- STB

## 4. Ordering information

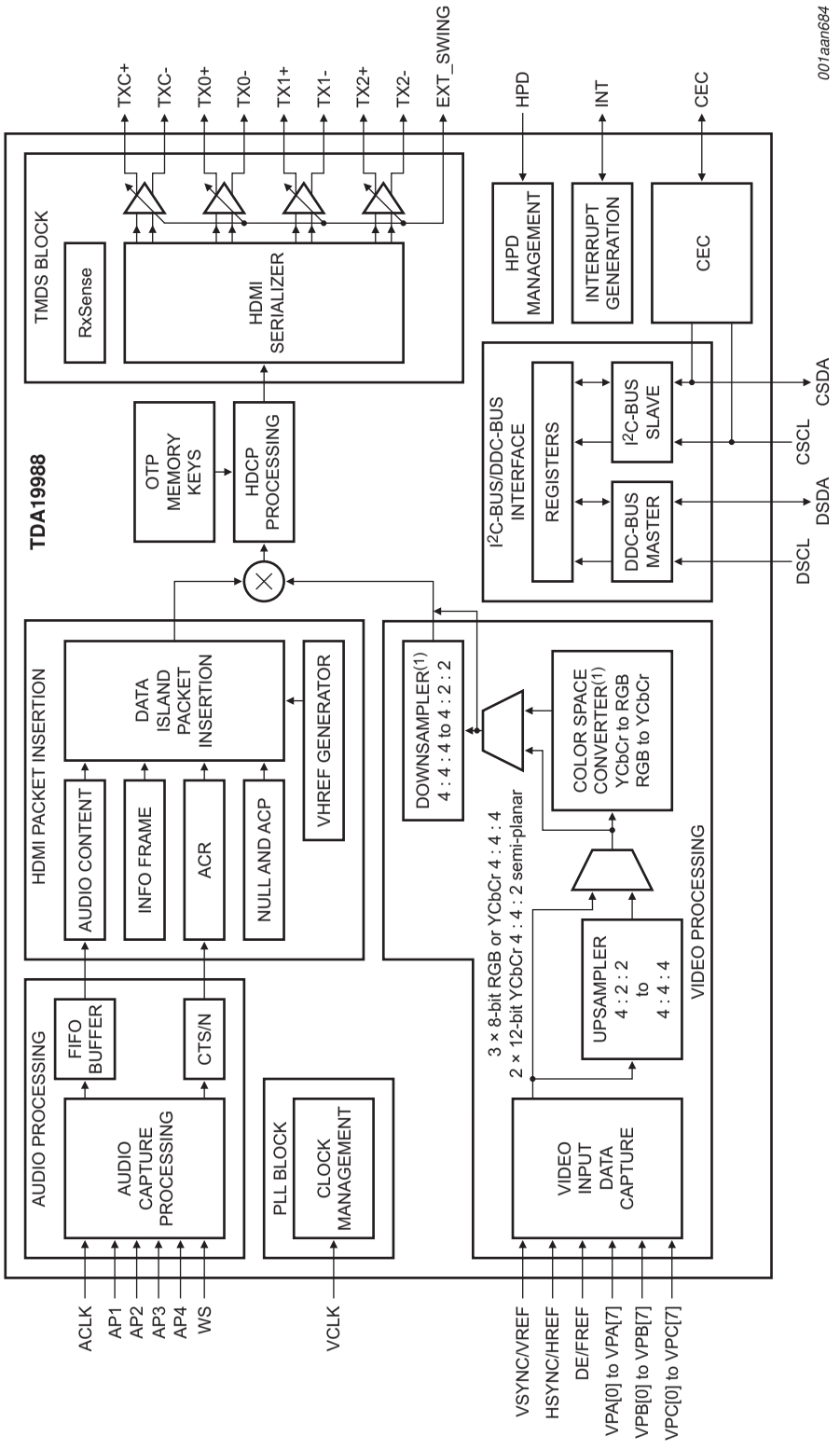
**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA19988AET/C1 | TFBGA64 | plastic thin fine-pitch ball grid array package; 64 balls | SOT962-3 |

**Table 1. Ordering information** *…continued*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TDA19988BET/C1 | TFBGA64 | plastic thin fine-pitch ball grid array package; 64 balls; without HDCP | SOT962-3 |
| TDA19988AHN/C1 | HVQFN64 | plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-4 |
| TDA19988BHN/C1 | HVQFN64 | plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm; without HDCP | SOT804-4 |

# 5. Block diagram




(1) The color space converter can be bypassed.
The device (TDA19988AHN and TDA19988AET only) can handle HDCP based on 1.4 features.

**Fig 2. TDA19988 Block diagram**

# 6. Pinning information

## 6.1 Pinning

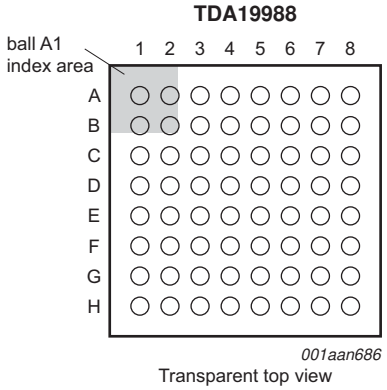



**Fig 3. Pin configuration (TFBGA64)**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| ACLK | H5 | I | audio clock input |
| AP0 | G5 | I | audio port 0 input |
| AP1 | F5 | I | audio port 1 input |
| AP2 | G6 | I | audio port 2 input |
| OSC_IN/AP3 | H6 | I | input connected to the external oscillator circuit or external clock source/audio port 3 input |
| HPD | E6 | I | hot plug detect; 5 V tolerant |
| EXT_SWING | E7 | O | TMDS output swing adjustment; place resistor ($R_{EXT\_SWING}$ = 10 kΩ ± 1 %) between this pin and analog ground. |
| DSDA | F6 | I/O | DDC-bus data input/output; 5 V tolerant |
| DSCL | F7 | I | DDC-bus clock input; 5 V tolerant |
| VCLK | D4 | I | input video pixel clock |
| HSYNC/HREF | F4 | I | input horizontal synchronization or reference input |
| VSYNC/VREF | G4 | I | input vertical synchronization or reference input |
| DE/FREF | H4 | I | data enable or field reference input |
| CSCL | B5 | I | $I^2C$-bus clock input; 1.8 V to 3.3 V tolerant |
| CSDA | A5 | I/O | $I^2C$-bus data input/output; 1.8 V to 3.3 V tolerant |
| INT | B6 | I/O | interrupt HDMI output (open-drain); this pin is used as Dual function pin selectable through $I^2C$-bus. In calibration mode only this pin is used as input for 10 ms ± 1 % calibration pulse. In operation mode this pin is used to warn the external microprocessor that a special event has occurred for HDMI or CEC |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| TX0− | E8 | O | negative data channel 0 for TMDS output |
| TX0+ | D8 | O | positive data channel 0 for TMDS output |
| TX1− | C8 | O | negative data channel 1 for TMDS output |
| TX1+ | B8 | O | positive data channel 1 for TMDS output |
| TX2− | A7 | O | negative data channel 2 for TMDS output |
| TX2+ | A6 | O | positive data channel 2 for TMDS output |
| TXC− | G8 | O | negative clock channel for TMDS output |
| TXC+ | F8 | O | positive clock channel for TMDS output |
| CEC | H7 | I/O | CEC connection (open-drain) to HDMI connector |
| VPA[0] | C1 | I | video port A input bit 0 (LSB) |
| VPA[1] | B1 | I | video port A input bit 1 |
| VPA[2] | B2 | I | video port A input bit 2 |
| VPA[3] | A2 | I | video port A input bit 3 |
| VPA[4] | B3 | I | video port A input bit 4 |
| VPA[5] | A3 | I | video port A input bit 5 |
| VPA[6] | B4 | I | video port A input bit 6 |
| VPA[7] | A4 | I | video port A input bit 7 (MSB) |
| VPB[0] | E3 | I | video port B input bit 0 (LSB) |
| VPB[1] | E2 | I | video port B input bit 1 |
| VPB[2] | E1 | I | video port B input bit 2 |
| VPB[3] | D1 | I | video port B input bit 3 |
| VPB[4] | D2 | I | video port B input bit 4 |
| VPB[5] | D3 | I | video port B input bit 5 |
| VPB[6] | C2 | I | video port B input bit 6 |
| VPB[7] | C3 | I | video port B input bit 7 (MSB) |
| VPC[0] | H3 | I | video port C input bit 0 (LSB) |
| VPC[1] | H2 | I | video port C input bit 1 |
| VPC[2] | G3 | I | video port C input bit 2 |
| VPC[3] | G2 | I | video port C input bit 3 |
| VPC[4] | G1 | I | video port C input bit 4 |
| VPC[5] | F1 | I | video port C input bit 5 |
| VPC[6] | F2 | I | video port C input bit 6 |
| VPC[7] | F3 | I | video port C input bit 7 (MSB) |
| $V_{DDA(TMDS)(1V8)}$ | A8, C7 | P | TMDS analog supply voltage (1.8 V) |
| $V_{DDD(IO)(1V8)}$ | E4 | P | I/O digital supply voltage (1.8 V) |
| $V_{DDA(PLL)(1V8)}$ | C6 | P | PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer |
| $V_{DDA(1V8)}$ | G7, H8 | P | analog supply voltage (1.8 V), is used for the serializer and miscellaneous blocks |
| $V_{DDDC}$ | E5, D5 | P | core digital supply voltage (1.8 V) |

**Table 2. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| $V_{SSD}$ | B7, C4, C5, H1 | G | digital ground supply voltage, is used for digital core and I/O |
| $V_{SSA}$ | D6, D7 | G | analog ground supply voltage, is used for PLL, serializer and transmitter |
| n.c. | A1 | | not connected |

[1] P = power supply, G = ground, I = input, O = output.

## 6.3 Pinning

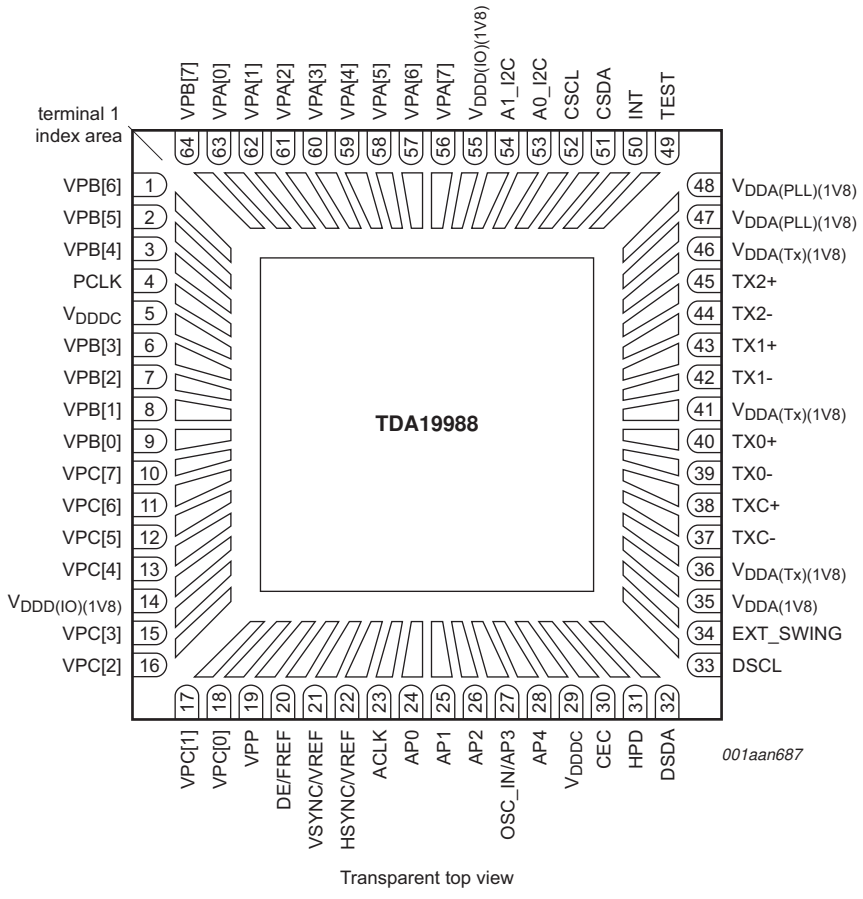



**Fig 4. Pin configuration (HVQFN64)**

## 6.4 Pin description

**Table 3. Pin description**

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| VPB[6] | 1 | I | video port B input bit 6 |
| VPB[5] | 2 | I | video port B input bit 5 |
| VPB[4] | 3 | I | video port B input bit 4 |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| PCLK | 4 | I | input video pixel clock |
| $V_{DDDC}$ | 5 | P | core digital supply voltage (1.8 V) |
| VPB[3] | 6 | I | video port B input bit 3 |
| VPB[2] | 7 | I | video port B input bit 2 |
| VPB[1] | 8 | I | video port B input bit 1 |
| VPB[0] | 9 | I | video port B input bit 0 (LSB) |
| VPC[7] | 10 | I | video port C input bit 7 (MSB) |
| VPC[6] | 11 | I | video port C input bit 6 |
| VPC[5] | 12 | I | video port C input bit 5 |
| VPC[4] | 13 | I | video port C input bit 4 |
| $V_{DDD(IO)(1V8)}$ | 14 | P | I/O digital supply voltage (1.8 V) |
| VPC[3] | 15 | I | video port C input bit 3 |
| VPC[2] | 16 | I | video port C input bit 2 |
| VPC[1] | 17 | I | video port C input bit 1 |
| VPC[0] | 18 | I | video port C input bit 0 LSB) |
| VPP | 19 | | to be connected to GND |
| DE/FREF | 20 | I | data enable or field reference input |
| VSYNC/VREF | 21 | I | input vertical synchronization or reference input |
| HSYNC/HREF | 22 | I | input horizontal synchronization or reference input |
| ACLK | 23 | I | audio clock input |
| AP0 | 24 | I | audio port 0 input |
| AP1 | 25 | I | audio port 1 input |
| AP2 | 26 | I | audio port 2 input |
| OSC_IN/AP3 | 27 | I | input connected to the external oscillator circuit or external clock source/audio port 3 input |
| AP4 | 28 | I | audio port 4 input |
| $V_{DDDC}$ | 29 | P | core digital supply voltage (1.8 V) |
| CEC | 30 | I/O | CEC connection (open-drain) to HDMI connector |
| HPD | 31 | I | hot plug detect; 5 V tolerant |
| DSDA | 32 | I/O | DDC-bus data input/output; 5 V tolerant |
| DSCL | 33 | I | DDC-bus clock input; 5 V tolerant |
| EXT_SWING | 34 | O | TMDS output swing adjustment; place resistor ($R_{EXT\_SWING}$ = 10 kΩ ± 1 %) between this pin and analog ground. |
| $V_{DDA(1V8)}$ | 35 | P | analog supply voltage (1.8 V), is used for parallel-to-serial shift register and miscellaneous blocks |
| $V_{DDA(Tx)(1V8)}$ | 36 | P | Tx analog supply voltage (1.8 V) |
| TXC− | 37 | O | negative clock channel for TMDS output |
| TXC+ | 38 | O | positive clock channel for TMDS output |
| TX0− | 39 | O | negative data channel 0 for TMDS output |
| TX0+ | 40 | O | positive data channel 0 for TMDS output |
| $V_{DDA(Tx)(1V8)}$ | 41 | P | Tx analog supply voltage (1.8 V) |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Type[1] | Description |
|---|---|---|---|
| TX1− | 42 | O | negative data channel 1 for TMDS output |
| TX1+ | 43 | O | positive data channel 1 for TMDS output |
| TX2− | 44 | O | negative data channel 2 for TMDS output |
| TX2+ | 45 | O | positive data channel 2 for TMDS output |
| $V_{DDA(Tx)(1V8)}$ | 46 | P | Tx analog supply voltage (1.8 V) |
| $V_{DDA(PLL)(1V8)}$ | 47 | P | PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer |
| $V_{DDA(PLL)(1V8)}$ | 48 | P | PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer |
| TEST | 49 | | to be connected to GND |
| INT | 50 | I/O | interrupt HDMI output (open-drain); this pin is used as Dual function pin selectable through $I^2C$-bus. In calibration mode only this pin is used as input for 10 ms ± 1 % calibration pulse. In operation mode this pin is used to warn the external microprocessor that a special event has occurred for HDMI or CEC |
| CSDA | 51 | I/O | $I^2C$-bus data input/output; 1.8 V to 3.3 V tolerant |
| CSCL | 52 | I | $I^2C$-bus clock input; 1.8 V to 3.3 V tolerant |
| A0_I2C | 53 | I | $I^2C$-bus address LSB bit 0 |
| A1_I2C | 54 | I | $I^2C$-bus address LSB bit 1 |
| $V_{DDD(IO)(1V8)}$ | 55 | P | I/O digital supply voltage (1.8 V) |
| VPA[7] | 56 | I | video port A input bit 7 (MSB) |
| VPA[6] | 57 | I | video port A input bit 6 |
| VPA[5] | 58 | I | video port A input bit 5 |
| VPA[4] | 59 | I | video port A input bit 4) |
| VPA[3] | 60 | I | video port A input bit 3 |
| VPA[2] | 61 | I | video port A input bit 2 |
| VPA[1] | 62 | I | video port A input bit 1 |
| VPA[0] | 63 | I | video port A input bit 0 (LSB) |
| VPB[7] | 64 | I | video port B input bit 7 (MSB) |
| Exposed die pad | - | G | exposed die pad; must be connected to ground |

[1] P = power supply, G = ground, I = input, O = output.

# 7. Functional description

TDA19988 is designed to convert digital data (video and audio) provided by Set-Top Boxes (STB), Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP) or DVD into an HDMI output, connected to HDMI or DVI input of a TV.

The video data input formats are:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4

- YCbCr 4 : 2 : 2 semi-planar
- YCbCr 4 : 2 : 2 ITU656-like

TDA19988 is able to output HDMI with the formats:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2

It can also handle audio formats:

- four $I^2S$-bus lanes
- one S/PDIF lane

TDA19988 is also designed to support CEC protocol. For more details about CEC, refer to *HDMI specification 1.4a*.

## 7.1 System clock

The system clock section has a PLL serializer.

It is a system clock generator which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times, or above, the sampling rate.

## 7.2 Video input formatter

### 7.2.1 Description

TDA19988 has three video input ports VPA[0] to VPA[7], VPB[0] to VPB[7] and VPC[0] to VPC[7].

TDA19988 can accept any of the following video input modes (see Table 7):

- RGB, with 8-bit for each component
- YCbCr 4 : 4 : 4, with 8-bit for each component
- YCbCr 4 : 2 : 2 semi-planar, with up to 12-bit for each component (YCbCr)
- YCbCr 4 : 2 : 2 ITU656, with up to 12-bit data depth

TDA19988 can be set to latch data at either rising or falling edge, or both.

### 7.2.2 Internal assignment

All video interfaces can be affected according to application requirements by swapping or allocating the 24-input VP ports to internal 24-video bus by block of 4-bit.

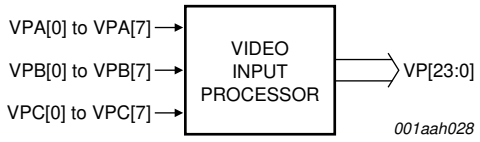



**Fig 5. Internal assignment of VP[23:0]**

**Table 4. Internal assignment**

| Internal assignment | | | | |
|---|---|---|---|---|
| **Internal port** | **RGB** | **YCbCr 4 : 4 : 4** | **YCbCr 4 : 2 : 2 semi-planar** | **YCbCr 4 : 2 : 2 ITU656** |
| VP[23] | G[7] | Y[7] | Y[11] | YCbCr[11] |
| VP[22] | G[6] | Y[6] | Y[10] | YCbCr[10] |
| VP[21] | G[5] | Y[5] | Y[9] | YCbCr[9] |
| VP[20] | G[4] | Y[4] | Y[8] | YCbCr[8] |
| VP[19] | G[3] | Y[3] | Y[7] | YCbCr[7] |
| VP[18] | G[2] | Y[2] | Y[6] | YCbCr[6] |
| VP[17] | G[1] | Y[1] | Y[5] | YCbCr[5] |
| VP[16] | G[0] | Y[0] | Y[4] | YCbCr[4] |
| VP[15] | B[7] | Cb[7] | Y[3] | YCbCr[3] |
| VP[14] | B[6] | Cb[6] | Y[2] | YCbCr[2] |
| VP[13] | B[5] | Cb[5] | Y[1] | YCbCr[1] |
| VP[12] | B[4] | Cb[4] | Y[0] | YCbCr[0] |
| VP[11] | B[3] | Cb[3] | CbCr[11] | |
| VP[10] | B[2] | Cb[2] | CbCr[10] | |
| VP[9] | B[1] | Cb[1] | CbCr[9] | |
| VP[8] | B[0] | Cb[0] | CbCr[8] | |
| VP[7] | R[7] | Cr[7] | CbCr[7] | |
| VP[6] | R[6] | Cr[6] | CbCr[6] | |
| VP[5] | R[5] | Cr[5] | CbCr[5] | |
| VP[4] | R[4] | Cr[4] | CbCr[4] | |
| VP[3] | R[3] | Cr[3] | CbCr[3] | |
| VP[2] | R[2] | Cr[2] | CbCr[2] | |
| VP[1] | R[1] | Cr[1] | CbCr[1] | |
| VP[0] | R[0] | Cr[0] | CbCr[0] | |

The device can swap and invert incoming video data using $I^2C$-bus registers VIP_CNTRL_0, VIP_CNTRL_1 and VIP_CNTRL_2 to match the expectation of the video processing block.

Table 5 shows the behavior of SWAP_A[2:0] of VIP_CNTRL_0 register, whose function is to map the 4 MSBs VP[23:20] to incoming video port

**Table 5. Video input swap to VP[23:20]**

| External assignment | | SWAP_A[2:0] selector value | Internal assignment | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin number[1] | Pin name | | Internal port | RGB | YCbCr 4 : 4 : 4 | YCbCr 4 : 2 : 2 semi-planar | | YCbCr 4 : 2 : 2 ITU656 | | | |
| F3 | VPC[7] | 000b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| F2 | VPC[6] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| F1 | VPC[5] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| G1 | VPC[4] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |
| G2 | VPC[3] | 001b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| G3 | VPC[2] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| H2 | VPC[1] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| H3 | VPC[0] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |
| C3 | VPB[7] | 010b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| C2 | VPB[6] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| D3 | VPB[5] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| D2 | VPB[4] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |
| D1 | VPB[3] | 011b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| E1 | VPB[2] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| E2 | VPB[1] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| E3 | VPB[0] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |
| A4 | VPA[7] | 100b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| B4 | VPA[6] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| A3 | VPA[5] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| B3 | VPA[4] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |
| A2 | VPA[3] | 101b | VP[23] | G[7] | Y[7] | $Y_0$[11] | $Y_1$[11] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] |
| B2 | VPA[2] | | VP[22] | G[6] | Y[6] | $Y_0$[10] | $Y_1$[10] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] |
| B1 | VPA[1] | | VP[21] | G[5] | Y[5] | $Y_0$[9] | $Y_1$[9] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] |
| C1 | VPA[0] | | VP[20] | G[4] | Y[4] | $Y_0$[8] | $Y_1$[8] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] |

[1] Only for TFBGA package.

In the same way:

- SWAP_B[2:0] is used to map incoming video port to the internal port VP[19:16].
- SWAP_C[2:0] is used to map incoming video port to the internal port VP[15:12].
- SWAP_D[2:0] is used to map incoming video port to the internal port VP[11:8].
- SWAP_E[2:0] is used to map incoming video port to the internal port VP[7:4].
- SWAP_F[2:0] is used to map incoming video port to the internal port VP[3:0].

The device expects to receive big endian incoming data. However, in cases where the input digital stream to the chip is little endian, the use of the mirror bit of the same register can help to re-order the input bits as described in Table 6.

**Table 6. TDA19988 input/output capability**

| Bit setting | Internal port | To be mapped to |
|---|---|---|
| MIRR_A = 1<br>SWAP_A[2:0] = 1 | VP[23] | VPC[0] |
| | VP[22] | VPC[1] |
| | VP[21] | VPC[2] |
| | VP[20] | VPC[3] |
| MIRR_B = 1<br>SWAP_B[2:0] = 0 | VP[19] | VPC[4] |
| | VP[18] | VPC[5] |
| | VP[17] | VPC[6] |
| | VP[16] | VPC[7] |
| MIRR_C = 1<br>SWAP_C[2:0] = 3 | VP[15] | VPB[0] |
| | VP[14] | VPB[1] |
| | VP[13] | VPB[2] |
| | VP[12] | VPB[3] |
| MIRR_D = 1<br>SWAP_D[2:0] = 2 | VP[11] | VPB[4] |
| | VP[10] | VPB[5] |
| | VP[9] | VPB[6] |
| | VP[8] | VPB[7] |
| MIRR_E = 1<br>SWAP_E[2:0] = 5 | VP[7] | VPA[0] |
| | VP[6] | VPA[1] |
| | VP[5] | VPA[2] |
| | VP[4] | VPA[3] |
| MIRR_F = 1<br>SWAP_F[2:0] = 4 | VP[3] | VPA[4] |
| | VP[2] | VPA[5] |
| | VP[1] | VPA[6] |
| | VP[0] | VPA[7] |

**Remark:** Unused input port can be set in 3-state or grounded by using appropriate configuration.

### 7.2.3 Input format mappings

Table 7 gives more information concerning input format supported.

**Table 7. Inputs of video input formatter**

| Color space | Format | Channels | Sync type | Rising edge | Falling edge | Double edge | Transmission input format | Max. pixel clock (MHz) | Max. input format | Comments | Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RGB | 4 : 4 : 4 | 3 × 8-bit | external | X | | | - | 165 | - | | Section 7.2.3.1 |
| | | | | | X | | - | 165 | - | | |
| | | | embedded | X | | | - | 165 | - | | |
| | | | | | X | | - | 165 | - | | |
| YCbCr | 4 : 4 : 4 | 3 × 8-bit | external | X | | | - | 165 | - | | Section 7.2.3.2 |
| | | | | | X | | - | 165 | - | | |
| | | | embedded | X | | | - | 165 | - | | |
| | | | | | X | | - | 165 | - | | |
| YCbCr | 4 : 2 : 2 | up to 1 × 12-bit ITU656-like | external | X | | | ITU656-like | 54.054 | 480p/576p | | Section 7.2.3.3 |
| | | | | | | | | 148.5 | 720p/1080i | | |
| | | | | | X | | ITU656-like | 54.054 | 480p/576p | | |
| | | | | | | | | 148.5 | 720p/1080i | | |
| | | | | | | X | ITU656-like | 74.25 | 720p/1080i | double edge | Section 7.2.3.4 |
| | | | embedded | X | | | ITU656-like | 54.054 | 480p/576p | | Section 7.2.3.5 |
| | | | | | | | | 148.5 | 720p/1080i | | |
| | | | | | X | | ITU656-like | 54.054 | 480p/576p | | |
| | | | | | | | | 148.5 | 720p/1080i | | |
| | | | | | | X | ITU656-like | 74.25 | 720p/1080i | double edge | Section 7.2.3.6 |
| | | up to 2 × 12-bit semi-planar | external | X | | | SMPTE293M | 148.5 | 1080p | | Section 7.2.3.7 |
| | | | | | X | | SMPTE293M | 148.5 | 1080p | | |
| | | | embedded | X | | | SMPTE293M | 148.5 | 1080p | | Section 7.2.3.8 |
| | | | | | X | | SMPTE293M | 148.5 | 1080p | | |

For all formats, active video windows can be selected using either external DE signal or internal timing generator engine.

#### 7.2.3.1 RGB 4 : 4 : 4 external synchronization (rising edge)

**Table 8. RGB (3 × 8-bit) external synchronization input (rising edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.*

| Video port A | | Video port B | | Video port C | | Control | |
|---|---|---|---|---|---|---|---|
| **Pin** | **RGB 4 : 4 : 4** | **Pin** | **RGB 4 : 4 : 4** | **Pin** | **RGB 4 : 4 : 4** | **Pin** | **RGB 4 : 4 : 4** |
| VPA[0] | B[0] | VPB[0] | G[0] | VPC[0] | R[0] | HSYNC/HREF | used |
| VPA[1] | B[1] | VPB[1] | G[1] | VPC[1] | R[1] | VSYNC/VREF | used |
| VPA[2] | B[2] | VPB[2] | G[2] | VPC[2] | R[2] | DE/FREF | used |
| VPA[3] | B[3] | VPB[3] | G[3] | VPC[3] | R[3] | | |
| VPA[4] | B[4] | VPB[4] | G[4] | VPC[4] | R[4] | | |
| VPA[5] | B[5] | VPB[5] | G[5] | VPC[5] | R[5] | | |
| VPA[6] | B[6] | VPB[6] | G[6] | VPC[6] | R[6] | | |
| VPA[7] | B[7] | VPB[7] | G[7] | VPC[7] | R[7] | | |

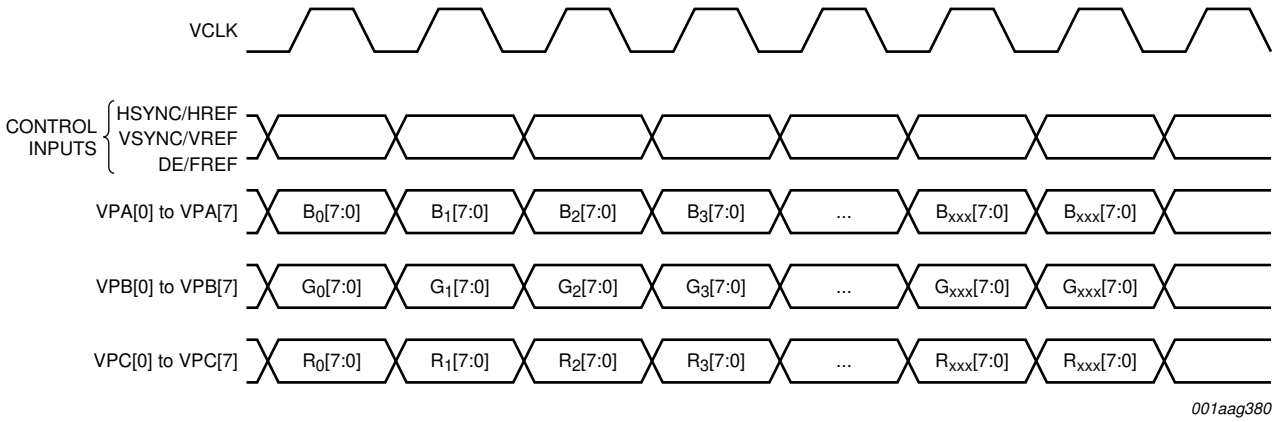



**Fig 6. Pixel encoding RGB 4 : 4 : 4 external synchronization input (rising edge)**

#### 7.2.3.2 YCbCr 4 : 4 : 4 external synchronization (rising edge)

**Table 9. YCbCr 4 : 4 : 4 (3 × 8-bit) external synchronization input (rising edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.*

| Video port A | | Video port B | | Video port C | | Control | |
|---|---|---|---|---|---|---|---|
| **Pin** | **YCbCr 4 : 4 : 4** | **Pin** | **YCbCr 4 : 4 : 4** | **Pin** | **YCbCr 4 : 4 : 4** | **Pin** | **YCbCr 4 : 4 : 4** |
| VPA[0] | Cb[0] | VPB[0] | Y[0] | VPC[0] | Cr[0] | HSYNC/HREF | used |
| VPA[1] | Cb[1] | VPB[1] | Y[1] | VPC[1] | Cr[1] | VSYNC/VREF | used |
| VPA[2] | Cb[2] | VPB[2] | Y[2] | VPC[2] | Cr[2] | DE/FREF | used |
| VPA[3] | Cb[3] | VPB[3] | Y[3] | VPC[3] | Cr[3] | | |
| VPA[4] | Cb[4] | VPB[4] | Y[4] | VPC[4] | Cr[4] | | |
| VPA[5] | Cb[5] | VPB[5] | Y[5] | VPC[5] | Cr[5] | | |
| VPA[6] | Cb[6] | VPB[6] | Y[6] | VPC[6] | Cr[6] | | |
| VPA[7] | Cb[7] | VPB[7] | Y[7] | VPC[7] | Cr[7] | | |

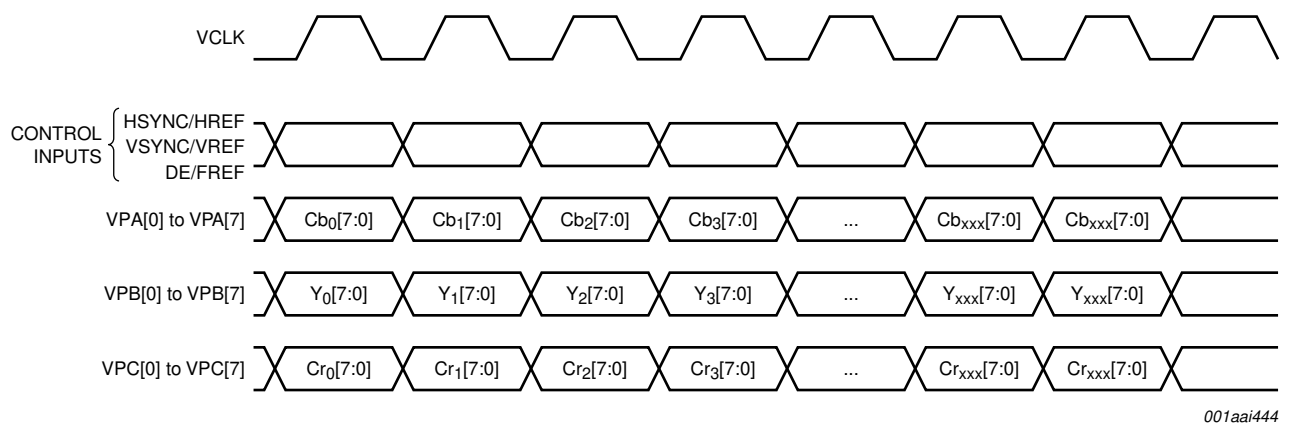



**Fig 7. Pixel encoding YCbCr 4 : 4 : 4 external synchronization input (rising edge)**

#### 7.2.3.3 YCbCr 4 : 2 : 2 ITU656-like external synchronization (rising edge)

**Table 10. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.*

| Video port A | | | | | Video port B | | | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | Cb[0] | $Y_0$[0] | Cr[0] | $Y_1$[0] | VPB[0] | Cb[4] | $Y_0$[4] | Cr[4] | $Y_1$[4] | HSYNC/HREF | used |
| VPA[1] | Cb[1] | $Y_0$[1] | Cr[1] | $Y_1$[1] | VPB[1] | Cb[5] | $Y_0$[5] | Cr[5] | $Y_1$[5] | VSYNC/VREF | used |
| VPA[2] | Cb[2] | $Y_0$[2] | Cr[2] | $Y_1$[2] | VPB[2] | Cb[6] | $Y_0$[6] | Cr[6] | $Y_1$[6] | DE/FREF | used |
| VPA[3] | Cb[3] | $Y_0$[3] | Cr[3] | $Y_1$[3] | VPB[3] | Cb[7] | $Y_0$[7] | Cr[7] | $Y_1$[7] | | |
| VPA[4] | - | - | - | - | VPB[4] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] | | |
| VPA[5] | - | - | - | - | VPB[5] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] | | |
| VPA[6] | - | - | - | - | VPB[6] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] | | |
| VPA[7] | - | - | - | - | VPB[7] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] | | |

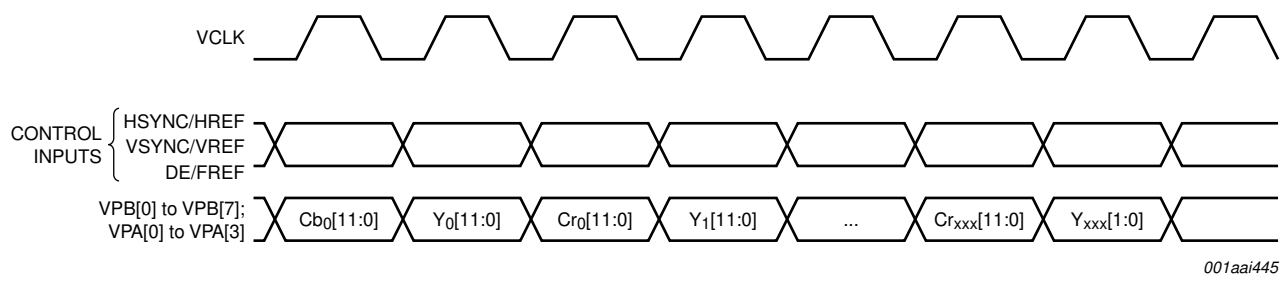



**Fig 8. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge)**

#### 7.2.3.4 YCbCr 4 : 2 : 2 ITU656-like external synchronization (double edge)

**Table 11. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.*

| Video port A | | | | | Video port B | | | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | Cb[0] | $Y_0$[0] | Cr[0] | $Y_1$[0] | VPB[0] | Cb[4] | $Y_0$[4] | Cr[4] | $Y_1$[4] | HSYNC/HREF | used |
| VPA[1] | Cb[1] | $Y_0$[1] | Cr[1] | $Y_1$[1] | VPB[1] | Cb[5] | $Y_0$[5] | Cr[5] | $Y_1$[5] | VSYNC/VREF | used |
| VPA[2] | Cb[2] | $Y_0$[2] | Cr[2] | $Y_1$[2] | VPB[2] | Cb[6] | $Y_0$[6] | Cr[6] | $Y_1$[6] | DE/FREF | used |
| VPA[3] | Cb[3] | $Y_0$[3] | Cr[3] | $Y_1$[3] | VPB[3] | Cb[7] | $Y_0$[7] | Cr[7] | $Y_1$[7] | | |
| VPA[4] | - | - | - | - | VPB[4] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] | | |
| VPA[5] | - | - | - | - | VPB[5] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] | | |
| VPA[6] | - | - | - | - | VPB[6] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] | | |
| VPA[7] | - | - | - | - | VPB[7] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] | | |

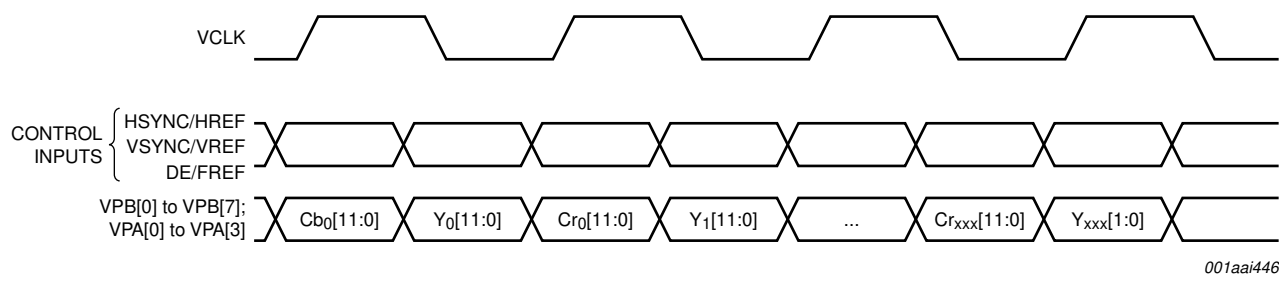



**Fig 9. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge)**

#### 7.2.3.5 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (rising edge)

**Table 12. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge) mappings**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.*

| Video port A | | | | | Video port B | | | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | Cb[0] | $Y_0$[0] | Cr[0] | $Y_1$[0] | VPB[0] | Cb[4] | $Y_0$[4] | Cr[4] | $Y_1$[4] | HSYNC/HREF | not used |
| VPA[1] | Cb[1] | $Y_0$[1] | Cr[1] | $Y_1$[1] | VPB[1] | Cb[5] | $Y_0$[5] | Cr[5] | $Y_1$[5] | VSYNC/VREF | not used |
| VPA[2] | Cb[2] | $Y_0$[2] | Cr[2] | $Y_1$[2] | VPB[2] | Cb[6] | $Y_0$[6] | Cr[6] | $Y_1$[6] | DE/FREF | not used |
| VPA[3] | Cb[3] | $Y_0$[3] | Cr[3] | $Y_1$[3] | VPB[3] | Cb[7] | $Y_0$[7] | Cr[7] | $Y_1$[7] | | |
| VPA[4] | - | - | - | - | VPB[4] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] | | |
| VPA[5] | - | - | - | - | VPB[5] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] | | |
| VPA[6] | - | - | - | - | VPB[6] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] | | |
| VPA[7] | - | - | - | - | VPB[7] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] | | |

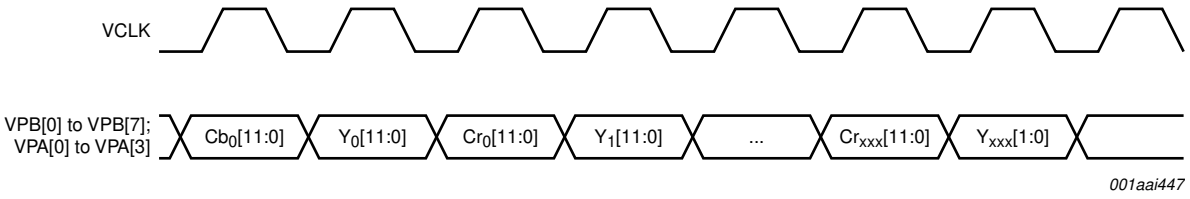



**Fig 10. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge)**

#### 7.2.3.6 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (double edge)

**Table 13. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.*

| Video port A | | | | | Video port B | | | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 (ITU656-like) | | | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | Cb[0] | $Y_0$[0] | Cr[0] | $Y_1$[0] | VPB[0] | Cb[4] | $Y_0$[4] | Cr[4] | $Y_1$[4] | HSYNC/HREF | not used |
| VPA[1] | Cb[1] | $Y_0$[1] | Cr[1] | $Y_1$[1] | VPB[1] | Cb[5] | $Y_0$[5] | Cr[5] | $Y_1$[5] | VSYNC/VREF | not used |
| VPA[2] | Cb[2] | $Y_0$[2] | Cr[2] | $Y_1$[2] | VPB[2] | Cb[6] | $Y_0$[6] | Cr[6] | $Y_1$[6] | DE/FREF | not used |
| VPA[3] | Cb[3] | $Y_0$[3] | Cr[3] | $Y_1$[3] | VPB[3] | Cb[7] | $Y_0$[7] | Cr[7] | $Y_1$[7] | | |
| VPA[4] | - | - | - | - | VPB[4] | Cb[8] | $Y_0$[8] | Cr[8] | $Y_1$[8] | | |
| VPA[5] | - | - | - | - | VPB[5] | Cb[9] | $Y_0$[9] | Cr[9] | $Y_1$[9] | | |
| VPA[6] | - | - | - | - | VPB[6] | Cb[10] | $Y_0$[10] | Cr[10] | $Y_1$[10] | | |
| VPA[7] | - | - | - | - | VPB[7] | Cb[11] | $Y_0$[11] | Cr[11] | $Y_1$[11] | | |

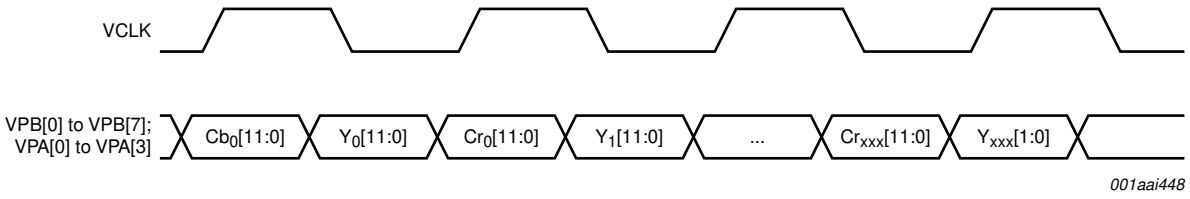



**Fig 11. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge)**

### 7.2.3.7 YCbCr 4 : 2 : 2 semi-planar external synchronization (rising edge)

**Table 14. YCbCr 4 : 2 : 2 semi-planar external synchronization input (rising edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.*

| Video port A | | | Video port B | | | Video port C | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | $Y_0$[0] | $Y_1$[0] | VPB[0] | $Y_0$[4] | $Y_1$[4] | VPC[0] | Cb[4] | Cr[4] | HSYNC/HREF | used |
| VPA[1] | $Y_0$[1] | $Y_1$[1] | VPB[1] | $Y_0$[5] | $Y_1$[5] | VPC[1] | Cb[5] | Cr[5] | VSYNC/VREF | used |
| VPA[2] | $Y_0$[2] | $Y_1$[2] | VPB[2] | $Y_0$[6] | $Y_1$[6] | VPC[2] | Cb[6] | Cr[6] | DE/FREF | used |
| VPA[3] | $Y_0$[3] | $Y_1$[3] | VPB[3] | $Y_0$[7] | $Y_1$[7] | VPC[3] | Cb[7] | Cr[7] | | |
| VPA[4] | Cb[0] | Cr[0] | VPB[4] | $Y_0$[8] | $Y_1$[8] | VPC[4] | Cb[8] | Cr[8] | | |
| VPA[5] | Cb[1] | Cr[1] | VPB[5] | $Y_0$[9] | $Y_1$[9] | VPC[5] | Cb[9] | Cr[9] | | |
| VPA[6] | Cb[2] | Cr[2] | VPB[6] | $Y_0$[10] | $Y_1$[10] | VPC[6] | Cb[10] | Cr[10] | | |
| VPA[7] | Cb[3] | Cr[3] | VPB[7] | $Y_0$[11] | $Y_1$[11] | VPC[7] | Cb[11] | Cr[11] | | |

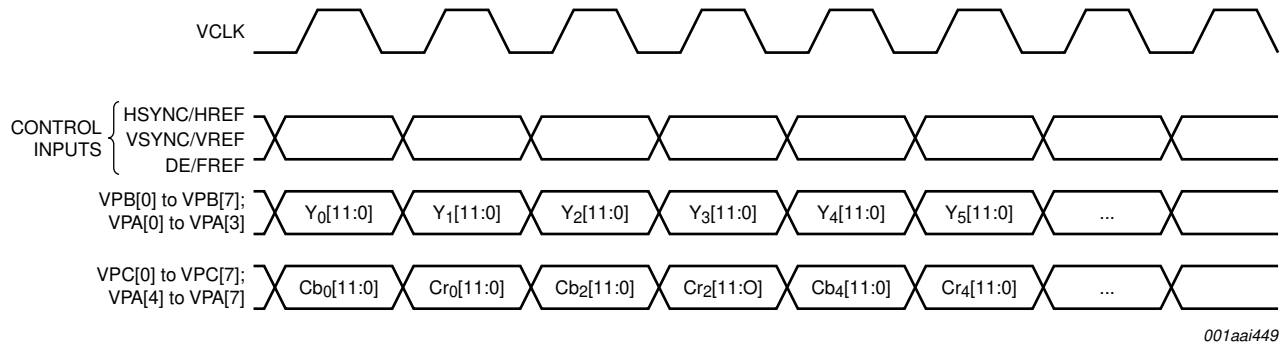



**Fig 12. Pixel encoding YCbCr 4 : 2 : 2 semi-planar external input synchronization (rising edge)**

#### 7.2.3.8 YCbCr 4 : 2 : 2 semi-planar embedded synchronization (rising edge)

**Table 15. YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge) mapping**

*Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.*

| Video port A | | | Video port B | | | Video port C | | | Control | |
|---|---|---|---|---|---|---|---|---|---|---|
| Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 semi-planar | | Pin | YCbCr 4 : 2 : 2 |
| VPA[0] | $Y_0$[0] | $Y_1$[0] | VPB[0] | $Y_0$[4] | $Y_1$[4] | VPC[0] | Cb[4] | Cr[4] | HSYNC/HREF | not used |
| VPA[1] | $Y_0$[1] | $Y_1$[1] | VPB[1] | $Y_0$[5] | $Y_1$[5] | VPC[1] | Cb[5] | Cr[5] | VSYNC/VREF | not used |
| VPA[2] | $Y_0$[2] | $Y_1$[2] | VPB[2] | $Y_0$[6] | $Y_1$[6] | VPC[2] | Cb[6] | Cr[6] | DE/FREF | not used |
| VPA[3] | $Y_0$[3] | $Y_1$[3] | VPB[3] | $Y_0$[7] | $Y_1$[7] | VPC[3] | Cb[7] | Cr[7] | | |
| VPA[4] | Cb[0] | Cr[0] | VPB[4] | $Y_0$[8] | $Y_1$[8] | VPC[4] | Cb[8] | Cr[8] | | |
| VPA[5] | Cb[1] | Cr[1] | VPB[5] | $Y_0$[9] | $Y_1$[9] | VPC[5] | Cb[9] | Cr[9] | | |
| VPA[6] | Cb[2] | Cr[2] | VPB[6] | $Y_0$[10] | $Y_1$[10] | VPC[6] | Cb[10] | Cr[10] | | |
| VPA[7] | Cb[3] | Cr[3] | VPB[7] | $Y_0$[11] | $Y_1$[11] | VPC[7] | Cb[11] | Cr[11] | | |

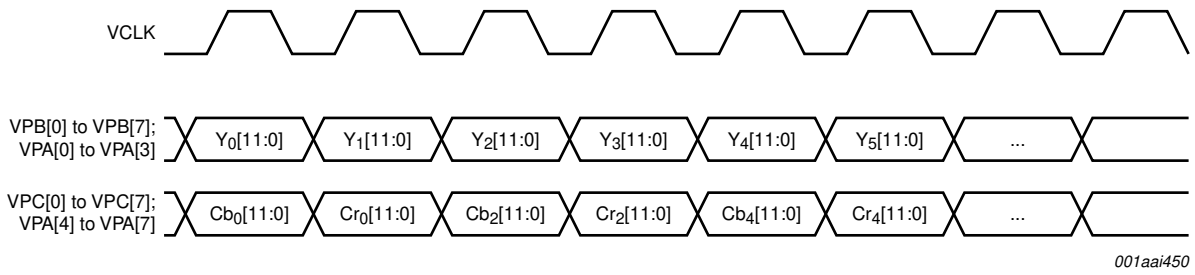



**Fig 13. Pixel encoding YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge)**

### 7.2.4 Synchronization

TDA19988 can be synchronized with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream or with external HSYNC/VSYNC inputs.

#### 7.2.4.1 Timing extraction generator

Synchronization signals can be extracted from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream.

Synchronization signals can be embedded or external.

#### 7.2.4.2 Data enable generator

TDA19988 contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

## 7.3 Input and output video format

Thanks to the flexible video input formatter, TDA19988 can accept a large range of input formats. This flexibility allows TDA19988 to be compatible with the maximum possible number of audio/video processors. Moreover, these input formats may be changed in many ways (color space converter, upsampler, downsampler) before it is transmitted across the HDMI link. Table 16 gives the possible inputs and outputs.

**Table 16. Use of color space converter, upsampler and downsampler**

| Input | | | Output | | |
|---|---|---|---|---|---|
| **Color space** | **Format** | **Channels** | **Color space** | **Format** | **Channels** |
| RGB | 4 : 4 : 4 | 3 × 8-bit | RGB | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 2 : 2 | 2 × 12-bit |
| YCbCr | 4 : 4 : 4 | 3 × 8-bit | RGB | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 2 : 2 | 2 × 12-bit |
| YCbCr | 4 : 2 : 2 | up to 2 × 12-bit semi-planar | RGB | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 2 : 2 | 2 × 12-bit |
| YCbCr | 4 : 2 : 2 | up to 1 × 12-bit ITU656 | RGB | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 4 : 4 | 3 × 8-bit |
| | | | YCbCr | 4 : 2 : 2 | 2 × 12-bit |

## 7.4 Upsampler

The incoming YCbCr 4 : 2 : 2 (2 × 12-bit) data stream format may be upsampled into YCbCr 4 : 4 : 4 (3 × 8-bit) data stream by repeating or linearly interpolating the chrominance pixels.

## 7.5 Color space converter

The color space converter is used to convert input video data from one type to another color space (e.g. RGB to YCbCr and YCbCr to RGB). This block can be bypassed and each coefficient is programmable via the $I^2C$-bus register.

$$\begin{bmatrix} Y\backslash G \\ Cr\backslash R \\ Cb\backslash B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left( \begin{bmatrix} Y \\ R/Cr \\ B/Cb \end{bmatrix} + \begin{bmatrix} Oin_{G/Y} \\ Oin_{R/Cr} \\ Oin_{B/Cb} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y\backslash G} \\ Oout_{Cr\backslash R} \\ Oout_{Cb\backslash B} \end{bmatrix} \quad (1)$$

## 7.6 Gamut-related metadata

Gamut-related metadata is an enhanced colorimetry beyond the default standard with higher definition colorimetries. Profile P0 is supported, which means that only one packet per video field is sent.

Examples:

- xvYCC601 (IEC 61966-2-4 – SD) (using YCbCr)
- xvYCC709 (IEC 61966-2-4 – HD) (using YCbCr)
- AdobeYCC601 (IEC 61966-2-5) (using YCbCr)
- AdobeRGB (IEC 61966-2-5) (using RGB)

**Remark:** Gamut-related metadata is an HDMI 1.4a feature.

## 7.7 Downsampler

This block works only with YCbCr input format; the filters downsample the Cb and Cr signals by a factor of 2. A delay is added on the Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the Cb-Cr channel.

## 7.8 Audio input format

TDA19988 is compatible with the following audio features described in the *"HDMI specification 1.4a"*:

- S/PDIF
- I²S-bus up to four stereo channels (depending on package)

TDA19988 can carry audio in I²S-bus format (one stereo to four stereo channels) or in S/PDIF format through audio pins named AP1, AP2, AP3 and AP4 (depending on package). S/PDIF or I²S-bus format can be selected via the I²C-bus. Only one audio format can be used at a time: either S/PDIF or I²S-bus. Table 17 shows the audio port allocation and Section 7.8.3 gives more details.

**Table 17. Audio port configuration**

| Audio port | Input configuration | |
|---|---|---|
| | S/PDIF | I²S-bus |
| AP0 | - | WS (word select) |
| AP1 | S/PDIF input | I²S-bus channel 0 |
| AP2 | S/PDIF input | I²S-bus channel 1 |
| AP3[1] | | I²S-bus channel 2 |
| AP4[1] | | I²S-bus channel 3 |
| ACLK | - | SCK (I²S-bus clock) |

[1] Depending on package.

All audio ports are LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant. It is possible to deactivate unused ports via I²C-bus with ENA_AP register on page 00h for both audio and clock inputs.

### 7.8.1 S/PDIF

In this format TDA19988 supports 2-channel uncompressed PCM data (IEC 60958) layout 0, or compressed bit stream (Dolby Digital, DTS, AC3 etc.) layout 1.

Only one S/PDIF input can be used at the same time. The selection is done by register.

TDA19988 is able to recover the original clock from the S/PDIF signal (no need of external clock). In addition, it can also use an external clock to decode the S/PDIF signal.

### 7.8.2 I²S-bus

There are 2 × I²S-bus or 4 × I²S-bus (depending on package) stereo input, which enables 4 or 8 (depending on package) PCM channels to be carried. The I²S-bus input interface receives an I²S-bus signal including serial data, word select and serial clock.

Typical waveforms for the I²S-bus signals at $64f_s$ are given by Figure 14.