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TDA19989

150 MHz pixel rate HDMI 1.3 transmitter with 3 × 8-bit video inputs, HDCP and CEC support

Rev. 01 — 15 February 2010 Preliminary data sheet

1. General description

TDA19989 is a very low power and very small size High-Definition Multimedia Interface (HDMI) v. 1.3a transmitter. It is backward compatible DVI 1.0 and can be connected to any DVI 1.0 and HDMI sink.

This device is primarily intended for mobile applications like Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP), Mobile Phone and Ultra-Mobile Personal Computer (UM PC) where size and very low power are mandatory for battery autonomy.

It allows mixing 3 × 8-bit RGB or YCbCr video stream with a pixel rate up to 150 MHz together with one S/PDIF or one I²S-bus audio streams with an audio sampling rate up to 192 kHz.

In order to be compatible with most applications, TDA19989 integrates a full programmable input formatter and color space conversion block. The video input formats accepted are YCbCr 4 :4 : 4 (up to 3 × 8-bit), YCbCr 4 : 2 : 2 semi-planar (up to 2 × 12-bit) and YCbCr 4 : 2 : 2 compliant with ITU656 (up to 1 × 12-bit). In case of ITU656-like format, the input pixel clock can be made active on one (SDR mode) or both edges (DDR mode).

TDA19989 includes a HDCP 1.3 compliant cipher block. The HDCP key are stored internally in a non-volatile OTP memory for maximum security.

This device provides additional embedded feature like CEC (Consumer Electronic Control). CEC is a single bidirectional wire that transmits CEC commands (like Standby from remote control) over the home appliance network connected through this wire. This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials) of the whole system and enable the connected devices (CEC enabled) to be controlled by only one remote control.

TDA19989 supports xvYCC HDMI 1.3a feature.

It can be switched to very low power Standby or Sleep modes to save power when HDMI is not used.

TDA19989 includes I²C-bus master interface for DDC-bus communication for EDID reading and HDCP purpose.

This device can be controlled or configured via I²C-bus interface.

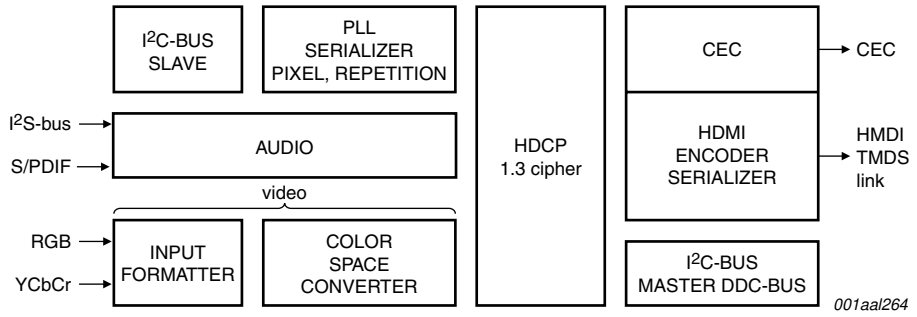


Fig 1. TDA19989 high-level block diagram

2. Features

- Compliance:
  - DVI 1.0
  - HDMI 1.3a
  - EIA/CEA-861B
  - CEC (HDMI 1.3)
  - SimplayHD
  - HDCP 1.3
- Video:
  - xvYCC HDMI 1.3 feature
  - Video formats with a pixel rate up to 150 MHz:
    RGB 4 : 4 : 4
    YCbCr 4 : 4 : 4
    YCbCr 4 : 2 : 2 semi-planar
    YCbCr 4 : 2 : 2 ITU656
  - Maximum resolution:
    1080p for TV
    1600 × 1200 at 60 Hz for PC (UXGA60)
    720p/1080i in ITU656
  - Programmable color space converter:
    RGB to YCbCr
    YCbCr to RGB
  - Programmable input formatter and upsampler/interpolator allows input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656-like formats
  - Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
  - Pixel clock input can be made active on one or both edges (selectable by I2C-bus)
  - Repetition of video samples as required by HDMI specification
- Audio:
  - 2 × I2S-bus 2 channels and S/PDIF; audio data rate up to 192 kHz per input for both standards
- Deals with multiple levels of HDCP receivers and repeaters

- Internal SHA-1 calculation
- System operation:
  - Master DDC-bus interface for EDID read
  - Controllable via I^2C-bus
  - Downstream availability through the use of hot plug detect (HPD) and receiver detection (RxSense)
  - Deals with multiple levels of receivers and repeaters
- Package:
  - TFBGA64
  - Size 4.5 × 4.5 × 0.95 mm
- Power management:
  - External voltage supplies 1.8 V
  - Low power
  - Flexible power modes
- Miscellaneous:
  - POR (Power-On Reset)
  - Audio and video inputs LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant
  - 250 MHz to 1.5 GHz TMDS transmitter operation

3. Applications

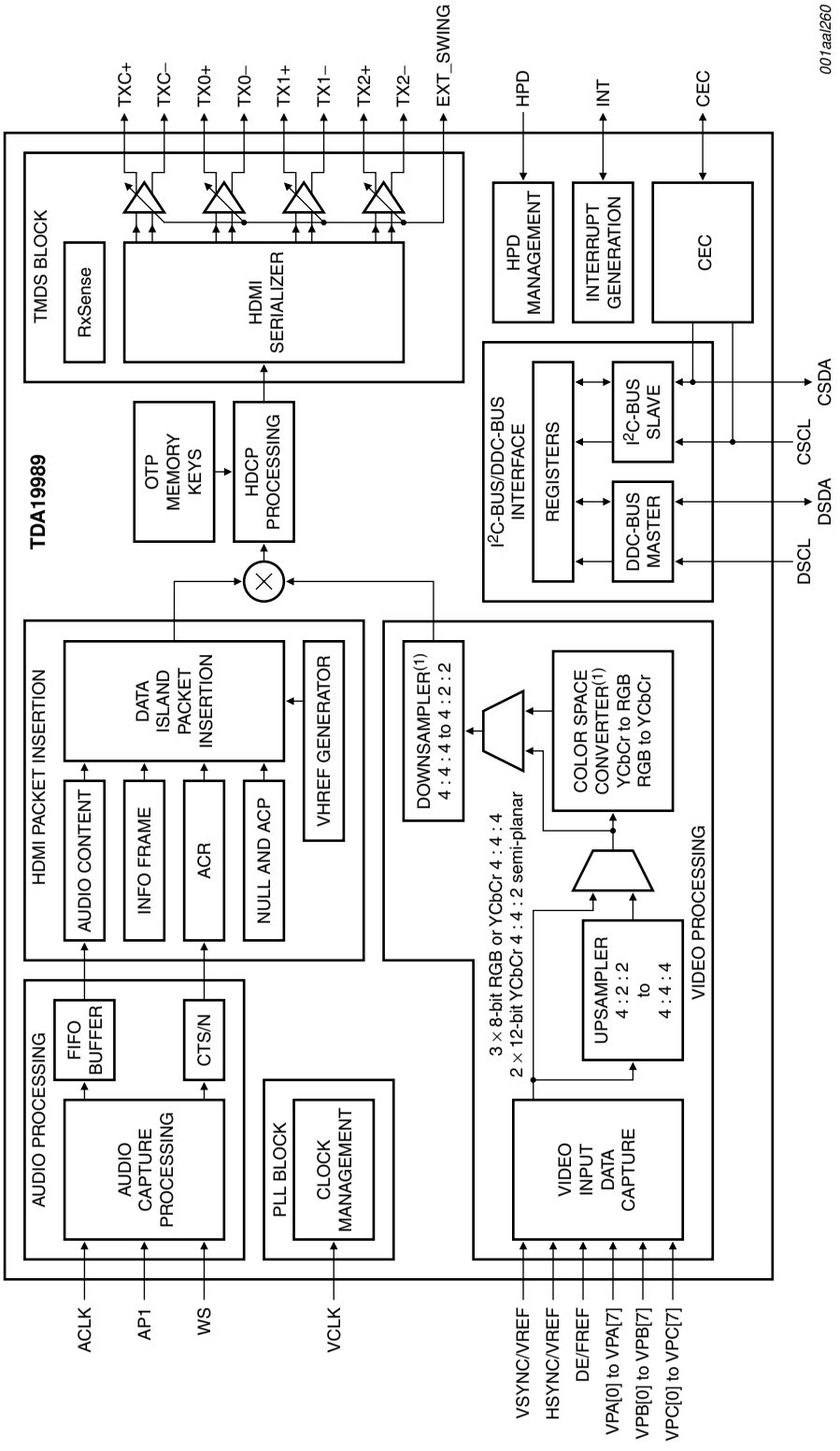
- Digital Video Camera (DVC)
- Digital Still Camera (DSC)
- Portable Multimedia Player (PMP)
- Mobile Phone
- Ultra-Mobile Personal Computer (UM PC)

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDA19989AET	TFBGA64	plastic thin fine-pitch ball grid array package; 64 balls	SOT962-3

5. Block diagram



(1) The color space converter can be bypassed.
The device can handle HDCP based on 1.3 features.

Fig 2. TDA19989 Block diagram

6. Pinning information

6.1 Pinning

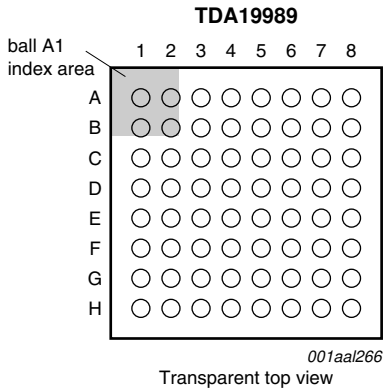


Fig 3. Pin configuration (TFBGA64)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
ACLK	H5	I	audio clock input
AP0	G5	I	audio port 0 input
AP1	F5	I	audio port 1 input
HPD	E6	I	hot plug detect; 5 V tolerant
EXT_SWING	E7	O	TMDS output swing adjustment; place resistor (R_{EXT_SWING} = 10 kΩ ± 1 %) between this pin and analog ground.
DSDA	F6	I/O	DDC-bus data input/output; 5 V tolerant
DSCL	F7	I	DDC-bus clock input; 5 V tolerant
VCLK	D4	I	input video pixel clock
HSYNC/HREF	F4	I	input horizontal synchronization or reference input
VSYNC/VREF	G4	I	input vertical synchronization or reference input
DE/FREF	H4	I	data enable or field reference input
CSCL	B5	I	I^2C-bus clock input; 1.8 V to 3.3 V tolerant
CSDA	A5	I/O	I^2C-bus data input/output; 1.8 V to 3.3 V tolerant
INT	B6	I/O	interrupt HDMI output (open-drain); this pin is used as Dual function pin selectable through I^2C-bus. In calibration mode only this pin is used as input for 10 ms ± 1 % calibration pulse. In operation mode this pin is used to warn the external microprocessor that a special event has occurred for HDMI or CEC
TX0−	E8	O	negative data channel 0 for TMDS output
TX0+	D8	O	positive data channel 0 for TMDS output
TX1−	C8	O	negative data channel 1 for TMDS output

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
TX1+	B8	O	positive data channel 1 for TMDS output
TX2−	A7	O	negative data channel 2 for TMDS output
TX2+	A6	O	positive data channel 2 for TMDS output
TXC−	G8	O	negative clock channel for TMDS output
TXC+	F8	O	positive clock channel for TMDS output
CEC	H7	I/O	CEC connection (open-drain) to HDMI connector
OSC_IN/AP3	H6	I	input connected to the external oscillator circuit or external clock source/audio port 3 input
AP2	G6	I	audio port 2 input
VPA[0]	C1	I	video port A input bit 0 (LSB)
VPA[1]	B1	I	video port A input bit 1
VPA[2]	B2	I	video port A input bit 2
VPA[3]	A2	I	video port A input bit 3
VPA[4]	B3	I	video port A input bit 4
VPA[5]	A3	I	video port A input bit 5
VPA[6]	B4	I	video port A input bit 6
VPA[7]	A4	I	video port A input bit 7 (MSB)
VPB[0]	E3	I	video port B input bit 0 (LSB)
VPB[1]	E2	I	video port B input bit 1
VPB[2]	E1	I	video port B input bit 2
VPB[3]	D1	I	video port B input bit 3
VPB[4]	D2	I	video port B input bit 4
VPB[5]	D3	I	video port B input bit 5
VPB[6]	C2	I	video port B input bit 6
VPB[7]	C3	I	video port B input bit 7 (MSB)
VPC[0]	H3	I	video port C input bit 0 (LSB)
VPC[1]	H2	I	video port C input bit 1
VPC[2]	G3	I	video port C input bit 2
VPC[3]	G2	I	video port C input bit 3
VPC[4]	G1	I	video port C input bit 4
VPC[5]	F1	I	video port C input bit 5
VPC[6]	F2	I	video port C input bit 6
VPC[7]	F3	I	video port C input bit 7 (MSB)
$V_{DDA(TMDS)(1V8)}$	A8, C7	P	TMDS analog supply voltage (1.8 V)
$V_{DDD(IO)(1V8)}$	E4	P	I/O digital supply voltage (1.8 V)
$V_{DDA(PLL)(1V8)}$	C6	P	PLL analog supply voltage (1.8 V), this PLL provides the clock for the serializer
$V_{DDA(1V8)}$	G7, H8	P	analog supply voltage (1.8 V), is used for parallel-to-serial shift register and miscellaneous blocks
V_{DDDC}	E5	P	core digital supply voltage (1.8 V)

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
V_{DDDC}	D5	P	core digital supply voltage (1.8 V)
V_{SSD}	B7, C4, C5	G	digital ground supply voltage, is used for digital core; I/O
V_{SSA}	D6, D7	G	analog ground supply voltage, is used for PLL; serializer, transmitter, and parallel-to-serial shift register

[1] P = power supply, G = ground, I = input, O = output.

7. Functional description

TDA19989 is designed to convert digital data (video and audio) provided by Set-Top Boxes (STB), Digital Video Camera (DVC), Digital Still Camera (DSC), Portable Multimedia Player (PMP) or DVD into an HDMI output, which can be used by a TV with either an HDMI or DVI input.

The video data input formats are:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2 semi-planar
- YCbCr 4 : 2 : 2 ITU656-like

TDA19989 is able to output HDMI with the formats:

- RGB 4 : 4 : 4
- YCbCr 4 : 4 : 4
- YCbCr 4 : 2 : 2

It can also handle audio formats:

- two I^2S-bus channels
- one S/PDIF channel

TDA19989 is also designed to support CEC protocol. For more details about CEC, refer to *HDMI 1.3a specification*.

7.1 System clock

The system clock section has a PLL serializer.

It is a system clock generator which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times, or above, the sampling rate.

7.2 Video input formatter

7.2.1 Description

TDA19989 has three video input ports VPA[0] to VPA[7], VPB[0] to VPB[7] and VPC[0] to VPC[7].

TDA19989 can accept any of the following video input modes (see Table 6):

- RGB, with 8-bit for each component
- YCbCr 4 : 4 : 4, with 8-bit for each component
- YCbCr 4 : 2 : 2 semi-planar, with up to 12-bit for each component (YCbCr)
- YCbCr 4 : 2 : 2 ITU656, with up to 12-bit data depth

TDA19989 can be set to latch data at either rising or falling edge, or both.

7.2.2 Internal assignment

The aim of the video input processor is to internally map the incoming data to the corresponding mode, which can be handled by the video processing. The internal signal named VP[23:0] is assigned depending on the input mode as defined below.

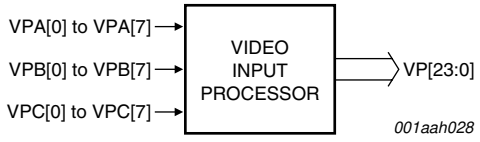


Fig 4. Internal assignment of VP[23:0]

Table 3. Internal assignment

Internal assignment				
Internal port	**RGB**	**YCbCr 4 : 4 : 4**	**YCbCr 4 : 2 : 2 semi-planar**	**YCbCr 4 : 2 : 2 ITU656**
VP[23]	G[7]	Y[7]	Y[11]	YCbCr[11]
VP[22]	G[6]	Y[6]	Y[10]	YCbCr[10]
VP[21]	G[5]	Y[5]	Y[9]	YCbCr[9]
VP[20]	G[4]	Y[4]	Y[8]	YCbCr[8]
VP[19]	G[3]	Y[3]	Y[7]	YCbCr[7]
VP[18]	G[2]	Y[2]	Y[6]	YCbCr[6]
VP[17]	G[1]	Y[1]	Y[5]	YCbCr[5]
VP[16]	G[0]	Y[0]	Y[4]	YCbCr[4]
VP[15]	B[7]	Cb[7]	Y[3]	YCbCr[3]
VP[14]	B[6]	Cb[6]	Y[2]	YCbCr[2]
VP[13]	B[5]	Cb[5]	Y[1]	YCbCr[1]
VP[12]	B[4]	Cb[4]	Y[0]	YCbCr[0]

Table 3. Internal assignment *…continued*

Internal assignment				
Internal port	**RGB**	**YCbCr 4 : 4 : 4**	**YCbCr 4 : 2 : 2 semi-planar**	**YCbCr 4 : 2 : 2 ITU656**
VP[11]	B[3]	Cb[3]	CbCr[11]	
VP[10]	B[2]	Cb[2]	CbCr[10]	
VP[9]	B[1]	Cb[1]	CbCr[9]	
VP[8]	B[0]	Cb[0]	CbCr[8]	
VP[7]	R[7]	Cr[7]	CbCr[7]	
VP[6]	R[6]	Cr[6]	CbCr[6]	
VP[5]	R[5]	Cr[5]	CbCr[5]	
VP[4]	R[4]	Cr[4]	CbCr[4]	
VP[3]	R[3]	Cr[3]	CbCr[3]	
VP[2]	R[2]	Cr[2]	CbCr[2]	
VP[1]	R[1]	Cr[1]	CbCr[1]	
VP[0]	R[0]	Cr[0]	CbCr[0]	

The device can swap and invert, in the event of a little endian stream, the incoming video data using I^2C-bus registers VIP_CNTRL_0, VIP_CNTRL_1 and VIP_CNTRL_2 (page 00h) to match the expectation of the video processing block. Table 4 shows the behavior of SWAP_A[2:0] of VIP_CNTRL_0 register, whose function is to map the 4 MSBs VP[23:20] to the incoming video port.

Table 4. Video input swap to VP[23:20]

External assignment		SWAP_A[2:0] selector value	Internal assignment								
Pin number	Pin name		Internal port	RGB	YCbCr 4 : 4 : 4	YCbCr 4 : 2 : 2 semi-planar		YCbCr 4 : 2 : 2 ITU656			
F3	VPC[7]	000b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
F2	VPC[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
F1	VPC[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
G1	VPC[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
G2	VPC[3]	001b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
G3	VPC[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
H2	VPC[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
H3	VPC[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
C3	VPB[7]	010b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
C2	VPB[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
D3	VPB[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
D2	VPB[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
D1	VPB[3]	011b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
E1	VPB[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
E2	VPB[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
E3	VPB[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
A4	VPA[7]	100b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
B4	VPA[6]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
A3	VPA[5]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
B3	VPA[4]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]
A2	VPA[3]	101b	VP[23]	G[7]	Y[7]	Y_0[11]	Y_1[11]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]
B2	VPA[2]		VP[22]	G[6]	Y[6]	Y_0[10]	Y_1[10]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]
B1	VPA[1]		VP[21]	G[5]	Y[5]	Y_0[9]	Y_1[9]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]
C1	VPA[0]		VP[20]	G[4]	Y[4]	Y_0[8]	Y_1[8]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]

In the same way:

- SWAP_B[2:0] is used to map incoming video port to the internal port VP[19:16].
- SWAP_C[2:0] is used to map incoming video port to the internal port VP[15:12].
- SWAP_D[2:0] is used to map incoming video port to the internal port VP[11:8].
- SWAP_E[2:0] is used to map incoming video port to the internal port VP[7:4].
- SWAP_F[2:0] is used to map incoming video port to the internal port VP[3:0].

The device expects to receive big endian incoming data. However, in cases where the input digital stream to the chip is little endian, the use of the mirror bit of the same register can help to re-order the input bits as described in Table 5.

Table 5. TDA19989 input/output capability

Bit setting	Internal port	To be mapped to
MIRR_A = 1 SWAP_A[2:0] = 1	VP[23]	VPC[0]
	VP[22]	VPC[1]
	VP[21]	VPC[2]
	VP[20]	VPC[3]
MIRR_B = 1 SWAP_B[2:0] = 0	VP[19]	VPC[4]
	VP[18]	VPC[5]
	VP[17]	VPC[6]
	VP[16]	VPC[7]
MIRR_C = 1 SWAP_C[2:0] = 3	VP[15]	VPB[0]
	VP[14]	VPB[1]
	VP[13]	VPB[2]
	VP[12]	VPB[3]
MIRR_D = 1 SWAP_D[2:0] = 2	VP[11]	VPB[4]
	VP[10]	VPB[5]
	VP[9]	VPB[6]
	VP[8]	VPB[7]
MIRR_E = 1 SWAP_E[2:0] = 5	VP[7]	VPA[4]
	VP[6]	VPA[5]
	VP[5]	VPA[6]
	VP[4]	VPA[7]
MIRR_F = 1 SWAP_F[2:0] = 4	VP[3]	VPA[0]
	VP[2]	VPA[1]
	VP[1]	VPA[2]
	VP[0]	VPA[3]

When input ports are not used, it is possible to deactivate them via the I^2C-bus with the appropriate set of registers ENA_VP_0, ENA_VP_1 and ENA_VP_2 on page 00h.

7.2.3 Input format mappings

Table 6 gives more information concerning input format supported.

Table 6. Inputs of video input formatter

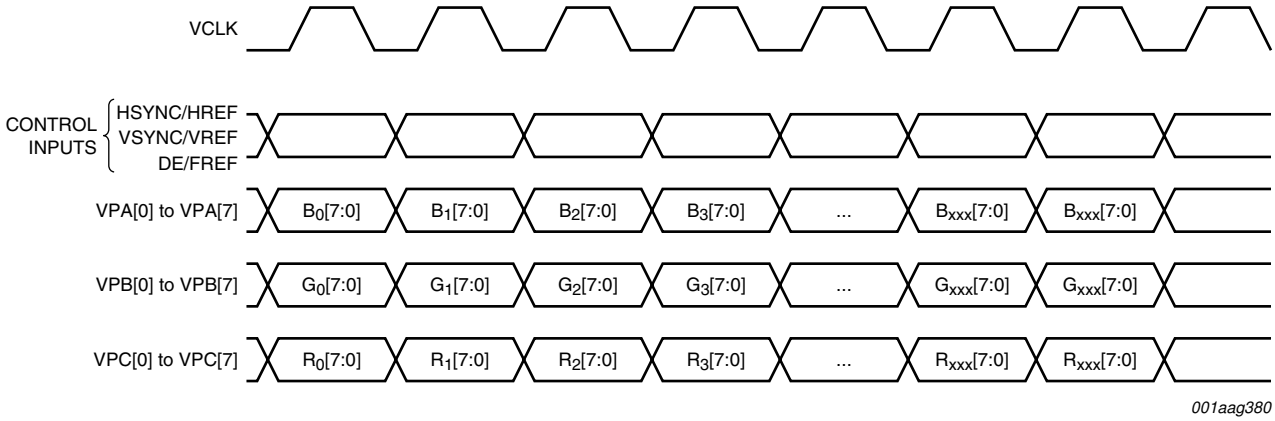
Color space	Format	Channels	Sync type	Rising edge	Falling edge	Double edge	Transmission input format	Max. pixel clock (MHz)	Max. input format	Comments	Reference
RGB	4 : 4 : 4	3 × 8-bit	external	X			-	150	-		Section 7.2.3.1
					X		-	150	-		
			embedded	X			-	150	-		
					X		-	150	-		
YCbCr	4 : 4 : 4	3 × 8-bit	external	X			-	150	-		Section 7.2.3.2
					X		-	150	-		
			embedded	X			-	150	-		
					X		-	150	-		
YCbCr	4 : 2 : 2	up to 1 × 12-bit ITU656-like	external	X			ITU656-like	54.054	480p/576p		Section 7.2.3.3
								148.5	720p/1080i		
					X		ITU656-like	54.054	480p/576p		
								148.5	720p/1080i		
						X	ITU656-like	74.25	720p/1080i	double edge	Section 7.2.3.4
			embedded	X			ITU656-like	54.054	480p/576p		Section 7.2.3.5
								148.5	720p/1080i		
					X		ITU656-like	54.054	480p/576p		
								148.5	720p/1080i		
						X	ITU656-like	74.25	720p/1080i	double edge	Section 7.2.3.6
		up to 2 × 8-bit semi-planar	external	X			SMPTE293M	148.5	1080p		Section 7.2.3.7
					X		SMPTE293M	148.5	1080p		
			embedded	X			SMPTE293M	148.5	1080p		Section 7.2.3.8
					X		SMPTE293M	148.5	1080p		

7.2.3.1 RGB 4 : 4 : 4 external synchronization (rising edge)

Table 7. RGB (3 × 8-bit) external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF.

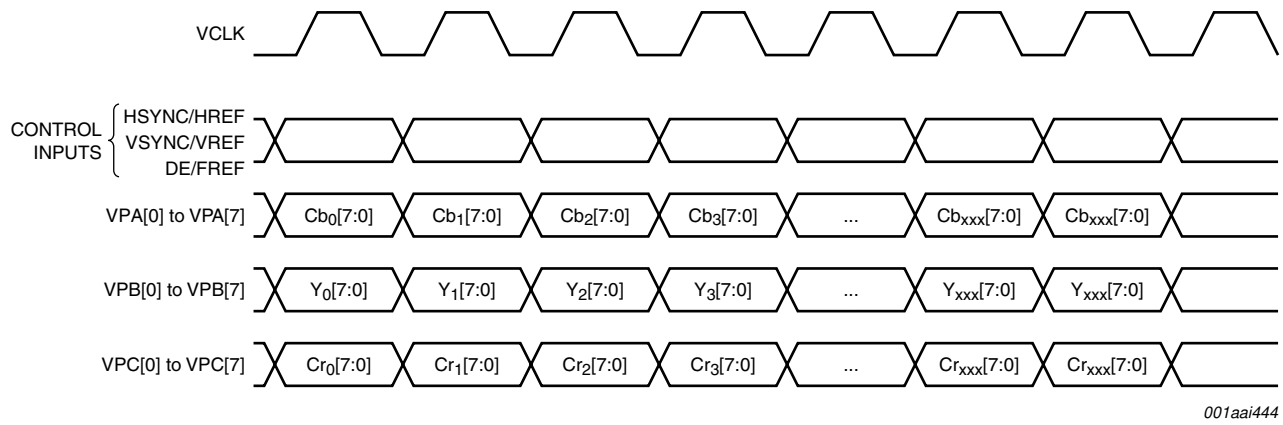
Fig 5. Pixel encoding RGB 4 : 4 : 4 external synchronization input (rising edge)

7.2.3.2 YCbCr 4 : 4 : 4 external synchronization (rising edge)

Table 8. YCbCr 4 : 4 : 4 (3 × 8-bit) external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**	**Pin**	**YCbCr 4 : 4 : 4**
VPA[0]	Cb[0]	VPB[0]	Y[0]	VPC[0]	Cr[0]	HSYNC/HREF	used
VPA[1]	Cb[1]	VPB[1]	Y[1]	VPC[1]	Cr[1]	VSYNC/VREF	used
VPA[2]	Cb[2]	VPB[2]	Y[2]	VPC[2]	Cr[2]	DE/FREF	used
VPA[3]	Cb[3]	VPB[3]	Y[3]	VPC[3]	Cr[3]		
VPA[4]	Cb[4]	VPB[4]	Y[4]	VPC[4]	Cr[4]		
VPA[5]	Cb[5]	VPB[5]	Y[5]	VPC[5]	Cr[5]		
VPA[6]	Cb[6]	VPB[6]	Y[6]	VPC[6]	Cr[6]		
VPA[7]	Cb[7]	VPB[7]	Y[7]	VPC[7]	Cr[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF.

Fig 6. Pixel encoding YCbCr 4 : 4 : 4 external synchronization input (rising edge)

7.2.3.3 YCbCr 4 : 2 : 2 ITU656-like external synchronization (rising edge)

Table 9. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

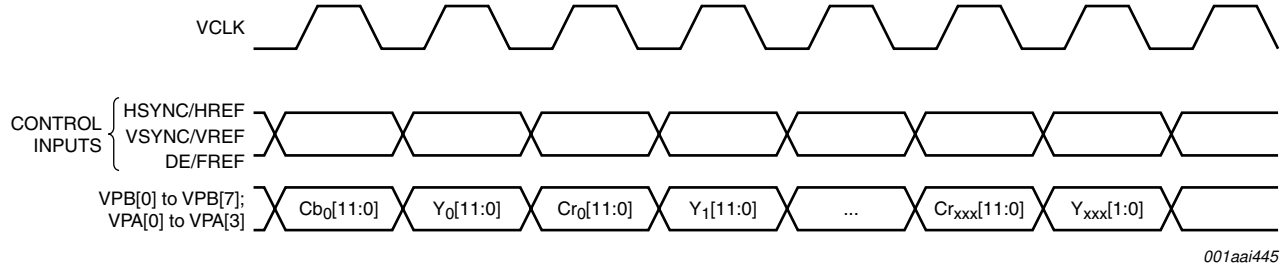


Fig 7. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (rising edge)

7.2.3.4 YCbCr 4 : 2 : 2 ITU656-like external synchronization (double edge)

Table 10. YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

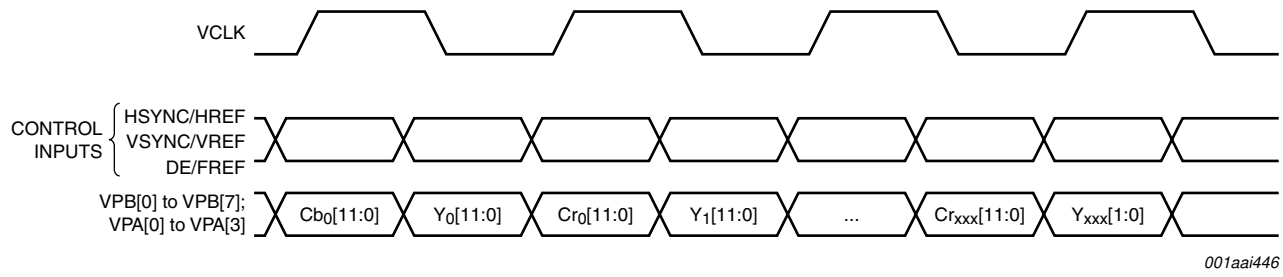


Fig 8. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like external synchronization input (double edge)

7.2.3.5 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (rising edge)

Table 11. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge) mappings

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr11]	Y_1[11]		

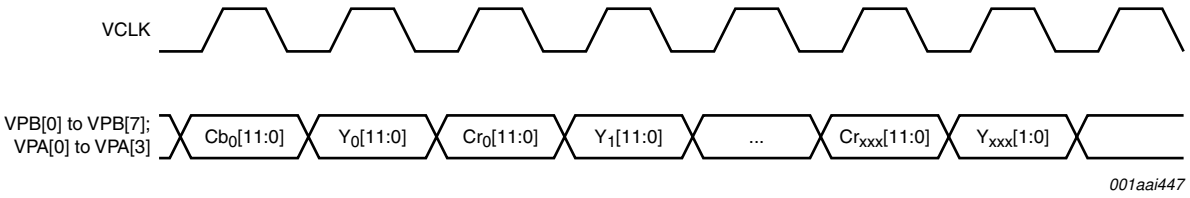


Fig 9. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (rising edge)

7.2.3.6 YCbCr 4 : 2 : 2 ITU656-like embedded synchronization (double edge)

Table 12. YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2 (ITU656-like)				Pin	YCbCr 4 : 2 : 2
VPA[0]	Cb[0]	Y_0[0]	Cr[0]	Y_1[0]	VPB[0]	Cb[4]	Y_0[4]	Cr[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	Cb[1]	Y_0[1]	Cr[1]	Y_1[1]	VPB[1]	Cb[5]	Y_0[5]	Cr[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	Cb[2]	Y_0[2]	Cr[2]	Y_1[2]	VPB[2]	Cb[6]	Y_0[6]	Cr[6]	Y_1[6]	DE/FREF	not used
VPA[3]	Cb[3]	Y_0[3]	Cr[3]	Y_1[3]	VPB[3]	Cb[7]	Y_0[7]	Cr[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	Cb[8]	Y_0[8]	Cr[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	Cb[9]	Y_0[9]	Cr[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	Cb[10]	Y_0[10]	Cr[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	Cb[11]	Y_0[11]	Cr[11]	Y_1[11]		

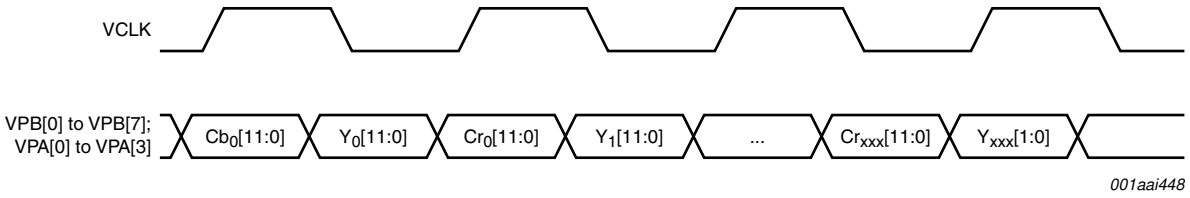


Fig 10. Pixel encoding YCbCr 4 : 2 : 2 ITU656-like embedded synchronization input (double edge)

7.2.3.7 YCbCr 4 : 2 : 2 semi-planar external synchronization (rising edge)

Table 13. YCbCr 4 : 2 : 2 semi-planar external synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

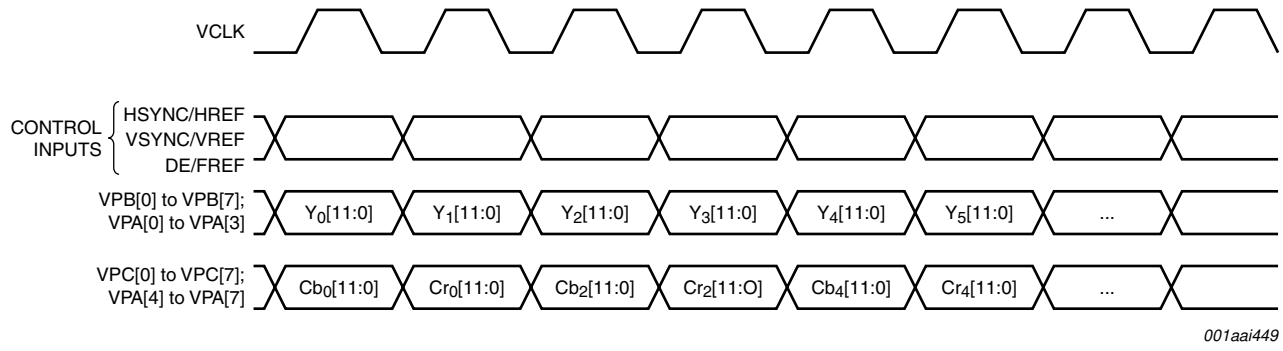


Fig 11. Pixel encoding YCbCr 4 : 2 : 2 semi-planar external input synchronization (rising edge)

7.2.3.8 YCbCr 4 : 2 : 2 semi-planar embedded synchronization (rising edge)

Table 14. YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge) mapping

Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2 semi-planar		Pin	YCbCr 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	Cb[4]	Cr[4]	HSYNC/HREF	not used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	Cb[5]	Cr[5]	VSYNC/VREF	not used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	Cb[6]	Cr[6]	DE/FREF	not used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	Cb[7]	Cr[7]		
VPA[4]	Cb[0]	Cr[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	Cb[8]	Cr[8]		
VPA[5]	Cb[1]	Cr[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	Cb[9]	Cr[9]		
VPA[6]	Cb[2]	Cr[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	Cb[10]	Cr[10]		
VPA[7]	Cb[3]	Cr[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	Cb[11]	Cr[11]		

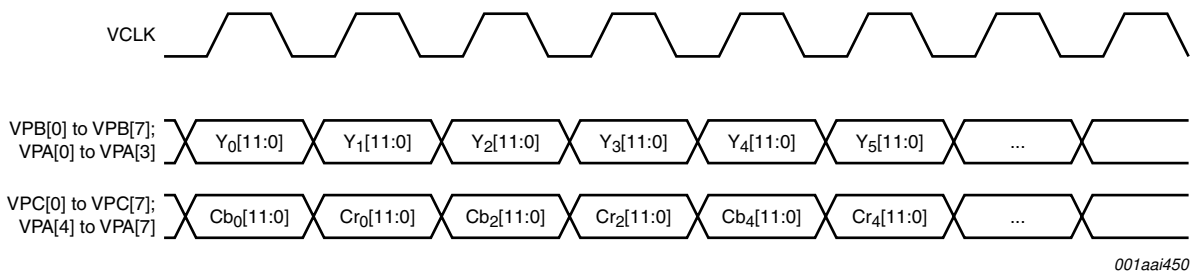


Fig 12. Pixel encoding YCbCr 4 : 2 : 2 semi-planar embedded synchronization input (rising edge)

7.2.4 Synchronization

TDA19989 can be synchronized with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream or with external HSYNC/VSYNC inputs.

7.2.4.1 Timing extraction generator

Synchronization signals can be extracted from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream.

Synchronization signals can be embedded in YCbCr 4 : 2 : 2 ITU656 (up to 1 × 12-bit) and YCbCr 4 : 2 : 2 semi-planar (up to 2 × 12-bit).

7.2.4.2 Data enable generator

TDA19989 contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

7.3 Input and output video format

Due to the flexible video input formatter, TDA19989 can accept a large range of input formats. This flexibility allows TDA19989 to be compatible with the maximum possible number of MPEG decoders. Moreover, these input formats may be changed in many ways (color space converter, upsampler, downsampler) before it is transmitted across the HDMI link. Table 15 gives the possible inputs and outputs.

Table 15. Use of color space converter, upsampler and downsampler

Input			Output		
Color space	**Format**	**Channels**	**Color space**	**Format**	**Channels**
RGB	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 4 : 4	3 × 8-bit	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit
YCbCr	4 : 2 : 2	up to 1 × 12-bit semi-planar	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit

Table 15. Use of color space converter, upsampler and downsampler *...continued*

Input			Output		
Color space	**Format**	**Channels**	**Color space**	**Format**	**Channels**
YCbCr	4 : 2 : 2	up to 2 × 12-bit semi-planar	RGB	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 4 : 4	3 × 8-bit
			YCbCr	4 : 2 : 2	2 × 12-bit

7.4 Upsampler

The incoming YCbCr 4 : 2 : 2 (2 × 12-bit) data stream format could be upsampled into YCbCr 4 : 4 : 4 (3 × 8-bit) data stream by repeating or linearly interpolating the chrominance pixels.

7.5 Color space converter

The color space converter is used to convert input video data from one type to another color space (e.g. RGB to YCbCr and YCbCr to RGB). This block can be bypassed and each coefficient is programmable via the I²C-bus register.

$$\begin{bmatrix} Y\backslash G \\ Cr\backslash R \\ Cb\backslash B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} Y \\ R/Cr \\ B/Cb \end{bmatrix} + \begin{bmatrix} Oin_{G/Y} \\ Oin_{R/Cr} \\ Oin_{B/Cb} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y\backslash G} \\ Oout_{Cr\backslash R} \\ Oout_{Cb\backslash B} \end{bmatrix} \quad (1)$$

7.6 Gamut-related metadata

Gamut-related metadata is an enhanced colorimetry beyond the default standard with higher definition colorimetries. Profile P0 is supported, which means that only one packet per video field is sent. Color gamut boundary data are defined the standards:

- xvYCC601 (IEC 61966-2-4 – SD) (using YCbCr)
- xvYCC709 (IEC 61966-2-4 – HD) (using YCbCr)

Remark: Gamut-related metadata is an HDMI 1.3a feature.

7.7 Downsampler

This block works only with YCbCr input format; the filters downsample the Cb and Cr signals by a factor of 2. A delay is added on the Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the Cb-Cr channel.

7.8 Audio input format

TDA19989 is compatible with the following audio features described in the HDMI 1.3 specification:

- S/PDIF
- I²S-bus up to four stereo channels

TDA19989 can carry audio in I²S-bus format (one stereo to two stereo channels) or in S/PDIF format through one audio pin named AP1. S/PDIF or I²S-bus format can be selected via the I²C-bus. Only one audio format can be used at a time: either S/PDIF or I²S-bus. Table 16 shows the audio port allocation and Section 7.8.3 gives more details.

Table 16. Audio port configuration

Audio port	Input configuration	
	S/PDIF	I²S-bus
AP0	-	WS (word select)
AP1	S/PDIF input	I²S-bus channel 0
AP2	S/PDIF input	I²S-bus channel 1
AP3	MCLK	
ACLK	-	SCK (I²S-bus clock)

All audio ports are LV-CMOS 1.8 V compatible and LV-CMOS 3.3 V tolerant. It is possible to deactivate unused ports via I²C-bus with ENA_AP register on page 00h for both audio and clock inputs.

7.8.1 S/PDIF

In this format TDA19989 supports 2-channel uncompressed PCM data (IEC 60958) layout 0, or compressed bit stream up to 8 multi channels (Dolby Digital, DTS, AC3 etc.) layout 1.

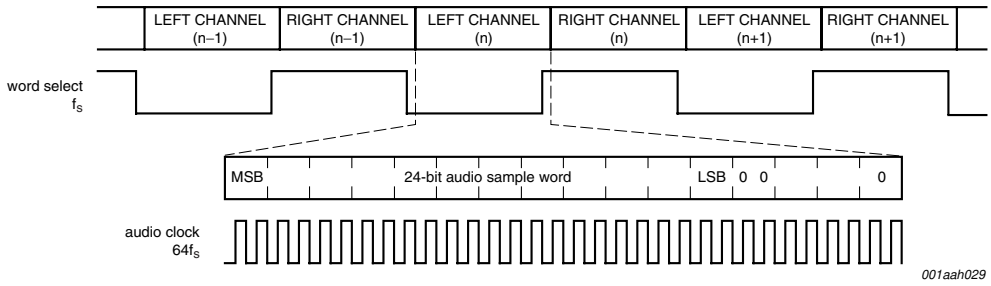
Only one S/PDIF input can be used at the same time. The selection is done by register.

TDA19989 is able to recover the original clock from the S/PDIF signal (no need of external clock). In addition, it can also use an external clock to decode the S/PDIF signal.

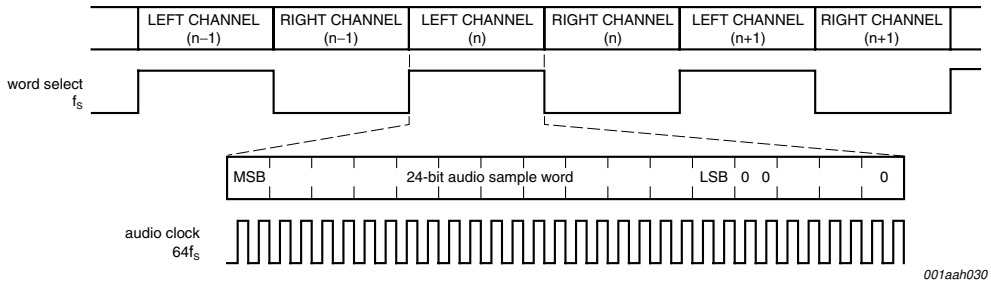
7.8.2 I²S-bus

There are 2 × I²S-bus stereo input, which enables 2 uncompressed audio channels to be carried. The I²S-bus input interface receives an I²S-bus signal including serial data, word select and serial clock.

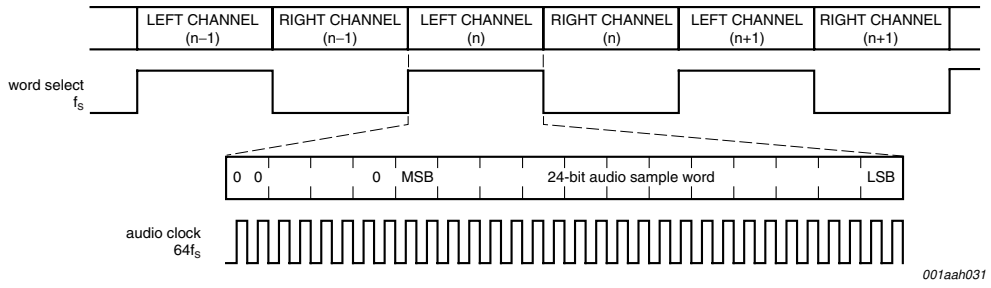
Typical waveforms for the I²S-bus signals at $64f_s$ are given by Figure 13.



a. Philips format.



b. Left justified format.



c. Right justified format.

Fig 13. I^2S-bus formats

The I^2S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency f_s.

Audio samples with a precision better than 24-bit are truncated to 24-bit. If the input clock has a frequency of $32f_s$, only 16-bit audio-samples can be received. In this case, the 8 LSBs will be set to 0. If the input clock has a frequency of $64f_s$ and is left justified or Philips, the audio word is truncated to 24-bit format and other bits padded with zeros. If the input clock has a frequency of $64f_s$ and is right justified, audio sample size has to be specified via software drivers.

The serial data signal carries the serial baseband audio data, sample by sample left/right interleaved.

The word select signal indicates whether left or right channel information is transferred over the serial data line.

7.8.3 Audio port internal assignment

The aim of the internal audio input assignment is to internally map any of the incoming data from the audio port AP1 or AP2 to I²S-bus channel 0 or S/PDIF internal ports by setting the appropriate I²C-bus register.

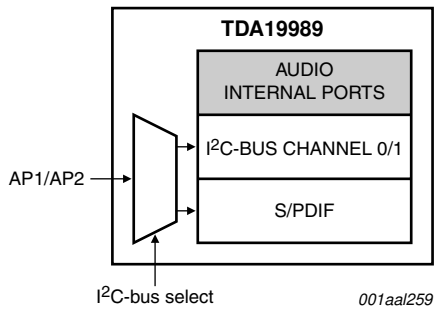


Fig 14. Audio input swap to I²S-bus channel 0 or S/PDIF

7.9 Power management

TDA19989 HDMI and CEC cores can be independently powered down by the I²C-bus register. In Standby mode all activities are reduced by switching off all PLLs, HDMI and CEC cores and disconnecting the biasing structure of the output stage. TDA19989 has a very low power consumption, which is suitable for portable applications.

Table 17 gives the typical power consumption of the device in different configurations.

Table 17. TDA19989 typical power consumption in different configurations

Typical power	Configuration	Comment
400 μW	Standby mode: • I²C-bus ON	default configuration: after power-up; PLLs HDMI and CEC cores are OFF; can be switched ON via I²C-bus register
1.3 mW	Sleep mode without CEC: • HDMI interruption (HPD, RxSense only)	no sink connected; CEC is OFF
1.8 mW	Sleep mode with CEC: • HDMI interruption (HPD, RxSense only) • CEC interruption	no sink connected; CEC is ON
90 mW	Low power 1080i mode: • Video format 1080i • Video input RGB 4 : 4 : 4 • No CEC	sink connected; CEC is OFF; 30 % activity on video input ports
155 mW	Full speed mode: • Video format 1080p	all blocks enabled and running; 30 % activity on video input ports

7.10 Interrupt controller

Pin INT is used to alert the system microcontroller that a critical event concerning the HDMI or CEC has occurred. The software provided with the device read a status register (I^2C-bus) to determine which block between HDMI and CEC has caused the interruption before processing it. Some of theses interrupts are maskable. The interrupt types are described in Table 18.

Table 18. Interruptions

Interrupt domain	Interrupt name	Definition	Maskable feature
HDCP	r0	r0 = R'0 check done	maskable
	pj	pj = P'j check fails	
	sha-1	V = V' check success	
	bstatus	bstatus available	
	bcaps	bcaps available	
	t0	HDCP goes to initial state	
	security	HDCP encryption is off or blue screen removed	not maskable
HPD	hpd	transition on HPD input	maskable
RxSense	rx_sense	transition on RxSense	maskable
Interrupt	sw_intsoftware	test purpose (output an interrupt signal)	maskable
EDID	edid_block_rd	EDID block read finished	maskable
CEC	cec_int	CEC message received	not maskable

7.10.1 Hot plug/unplug detect

The hot plug detect (HPD) pin is 5 V input tolerant. The HPD signal, when asserted, tells the transmitter that the receiver is connected. When changing from LOW-to-HIGH, TDA19989 has to read the EDID of the receiver in order to select the video format that the receiver can handle.

7.10.2 Receiver sensitivity

TDA19989 has the capability to sense the receiver connectivity and working behavior. This feature (RxSense) detects the presence of the 50 Ω pull-up resistor R_T on the TMDS clock channel of the downstream side.

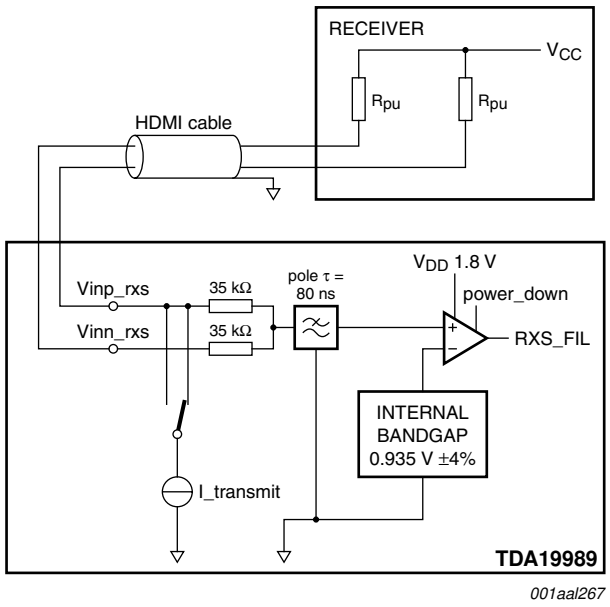


Fig 15. Receiver sensitivity detection

As long as the receiver is connected to the transmitter and powered-up, bit RXS_FIL is set to logic 1.

As soon as the cable is unplugged or receiver side powered off (assuming in this case that V_{CC} is switched off), the RxSense generates an interrupt inside TDA19989, changing the value of bit RXS_FIL to logic 0 (See Table 19). This allows the application to stop sending unnecessary video content.

This feature is very useful when the receiver recovers from an off-state and does not generate a HPD transition HIGH-to-LOW-to-HIGH. In this particular case, RxSense will generate an interrupt so that the chip restarts sending video.

Table 19. Receiver detection according to averaged terminal voltage

Average voltage (Vinp_rxs + Vinn_rxs) / 2	bit RXS_FIL: receiver powered on	bit RXS_FIL: receiver powered off
$V \geq 1$ V	1	0
0.8 V < V < 1 V	undefined	0
$V \leq 0.8$ V	0	0

Remark: According to the HDMI specification, only the HPD interrupt allows the application to read the EDID. The RxSense interrupt is not mandatory to initialize the EDID reading procedure.

7.11 HDCP processing

7.11.1 High-bandwidth digital content protection

TDA19989 contains an HDCP function, which encrypts the transmitted stream content (both video and audio). This function can be enabled and disabled via the I^2C-bus.

The keys can be stored internally in OTP non-volatile memory or can be loaded via the I^2C-bus. As the keys are stored internally, the security is maximized.

7.11.1.1 Repeater function

TDA19989 can be used in a repeater device according to the *HDCP specification, Rev 1.3*. TDA19989 is able to store the KSV list of a maximum of 127 devices in a register memory.

7.11.1.2 SHA-1

To deal with repeater, a SHA-1 calculation is performed by the transmitter and by the downstream repeater. For security purposes and in order to relieve the microcontroller, the SHA-1 has been implemented within TDA19989.

This calculation is worked out after the transmitter has loaded the KSV list (see *HDCP specification, Rev 1.3*). If SHA-1 calculated by transmitter equals the SHA-1 calculated by repeater, then an interrupt is sent.

7.12 CEC

TDA19989 with its embedded CEC block provides a complete solution to enable Consumer Electronic Control (CEC) in product (DSC, DVC, PMP, UM PC). This eliminates the need of any additional device to handle this feature thus improving BOM (Bill Of Materials). CEC capability allows AV products (CEC enable) to communicate together over the home appliance network which could be controlled using only one remote control.

The CEC block manages low level transactions (compliant to CEC timing specification) over the one bidirectional line. It translates CEC protocol in I^2C-bus for the host processor and vice versa. It manages CEC message reception and transmission compliant to CEC protocol and provides the message to the system microcontroller (host processor).

For power consumption optimization purpose CEC could be enable or disable through I^2C-bus register. The following sections describe CEC:

- Features
- Clocking scheme

7.12.1 Features

- Receive and transmit CEC messages to host processor
- Supports multiple CEC logical addresses
- Supports CEC messages up to 16 bytes long
- Programmable retry count
- Comprehensive arbitration and collision handling