Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

1 Applications

- Desktop and Server VR buck-converter
- Single Phase and Multiphase POL
- CPU/GPU Regulation in Notebook, Desktop Graphics Cards, DDR Memory, Graphic Memory
- High Power Density Voltage Regulator Modules (VRM)
- Qualified for DCDC industrial applications based on JEDEC (JESD47, JESD22, J-STD20)

2 Features

- For synchronous buck converter step down voltage applications
- Maximum average current of 40 A
- Input voltage range +4.5 V to +16 V
- Power MOSFETs rated 25 V
- Fast switching technology for improved performance at high switching frequencies (> 500 kHz)
- Remote driver disable function
- Includes bootstrap diode
- Undervoltage lockout
- Shoot through protection
- +5 V high side and low side MOSFETs driving voltage
- Compatible to standard +3.3 V PWM controller integrated circuits
- Tri-state PWM input functionality
- Small package: PG-IQFN-30-2 (4 x 4 x 1 mm³)
- RoHS compliant
- Thermal warning

Table 1 Product Identification

Part Number	Temp Range	Package	Marking
TDA21240	-40 to 125°C	PG-IQFN-30-2 (4 x 4 x 1 mm³)	21240

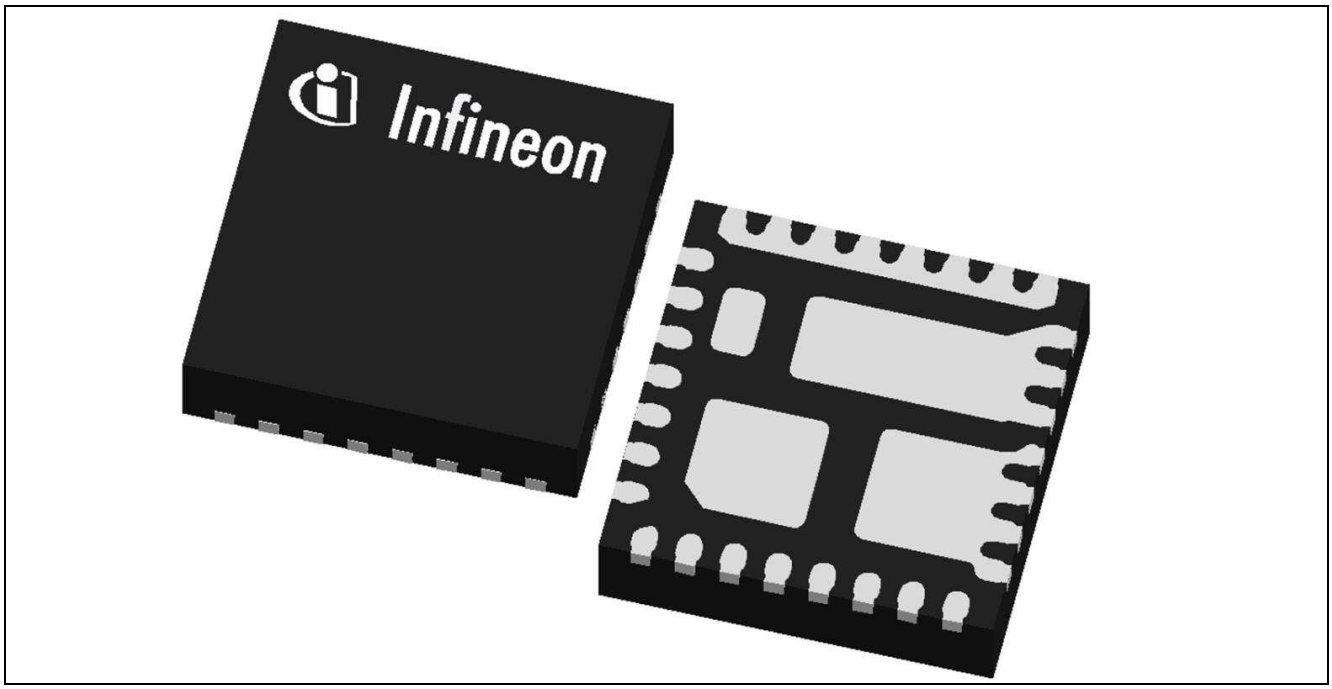


Figure 1 Picture of the Product

3 Description

3.1 Pinout

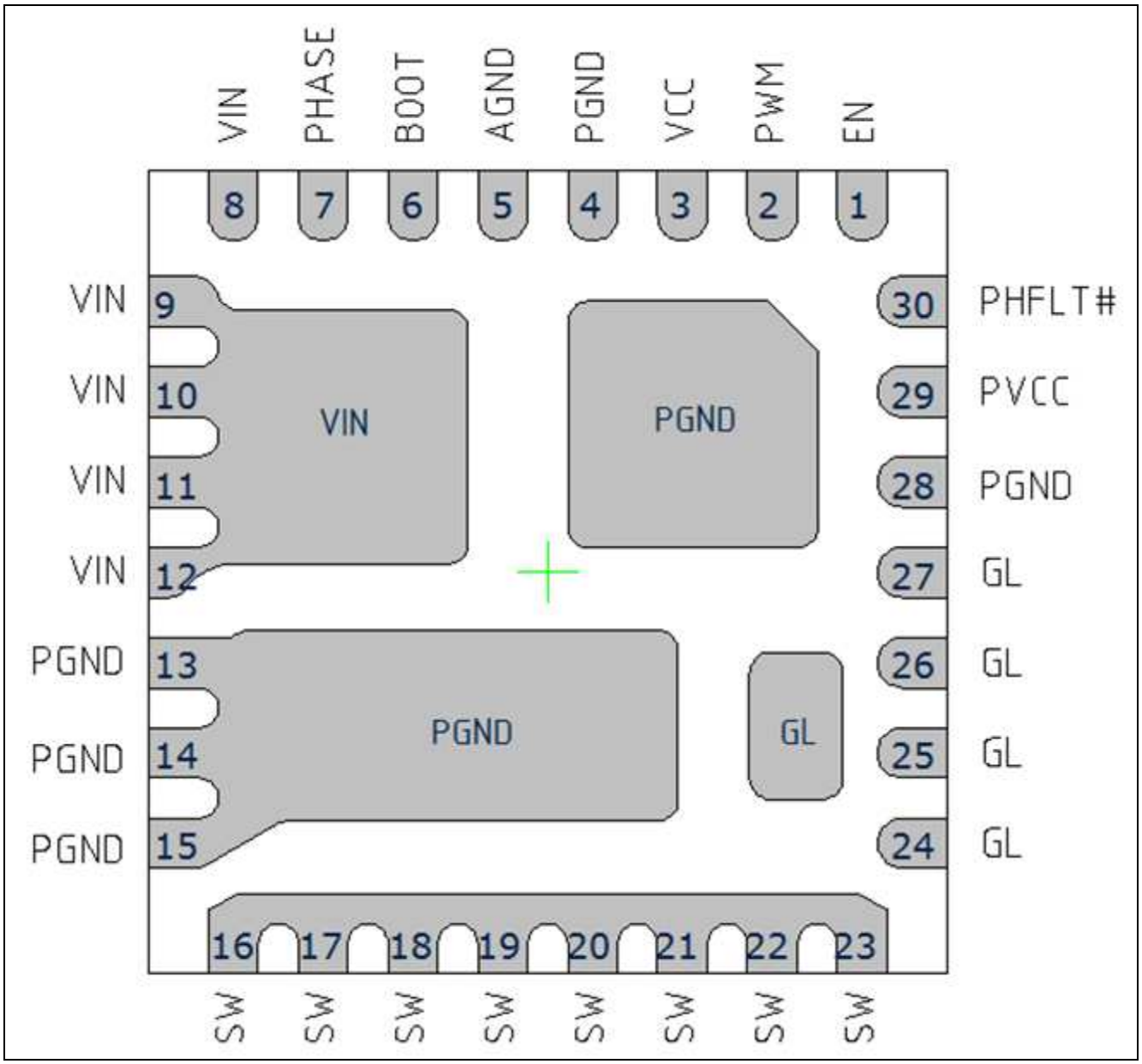


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
2	PWM	I	+3.3 V logic	**PWM drive logic input** The tri-state PWM input is compatible with 3.3 V.
6	BOOT	I	Analog	**Bootstrap voltage pin** Connect to BOOT capacitor
7	PHASE	I	Analog	**Switch node** (reference for Boot voltage) internally connected to SW pin, connect to BOOT capacitor
16 – 23	SW	O	Analog	**Switch node output** High current output switching node
24 – 27	GL	O	Analog	**Low-Side Gate** Test point for Low Side MOSFET gate signal
30	PHFLT#	O	+3.3 V logic	**Thermal Warning** Connect through a resistor to 3.3V. When the thermal protection threshold is tripped, the PHFLT# pin is being pulled low. Leave open if not used.
1	EN	I	+3.3 V logic	**Enable signal (active high)** Connect to GND to disable the IC.

Table 3 Power Supply

Pin No.	Name	Pin Type	Function
8 - 12, Vin pins and pad	VIN	POWER	**Input voltage** Supply of the drain of the high-side MOSFET
29	PVCC	POWER	**FET gate supply voltage** High- and low-side gate drive supply
3	VCC	POWER	**Logic supply voltage** Bias voltage for the internal logic

Table 4 Ground Pins

Pin No.	Name	Pin Type	Function
5	AGND	GND	**Control signal ground** Should be connected to PGND externally
4, 13 – 15, 28 PGND pins and pads	PGND	GND	**Power ground** All these pins must be connected to the power GND plane through multiple low inductance vias.

3.2 General Description

The Infineon TDA21240 is a multichip module that incorporates Infineon's premier MOSFET technology for a single high-side and a single low-side MOSFET coupled with a robust, high performance, high switching frequency gate driver in a single PG-IQFN-30-2 package. The optimized gate timing allows for significant light load efficiency improvements over discrete solutions.

When combined with Infineon's family of digital multi-phase controllers, the TDA21240 forms a complete core-voltage regulator solution for advanced micro and graphics processors as well as point-of-load applications.

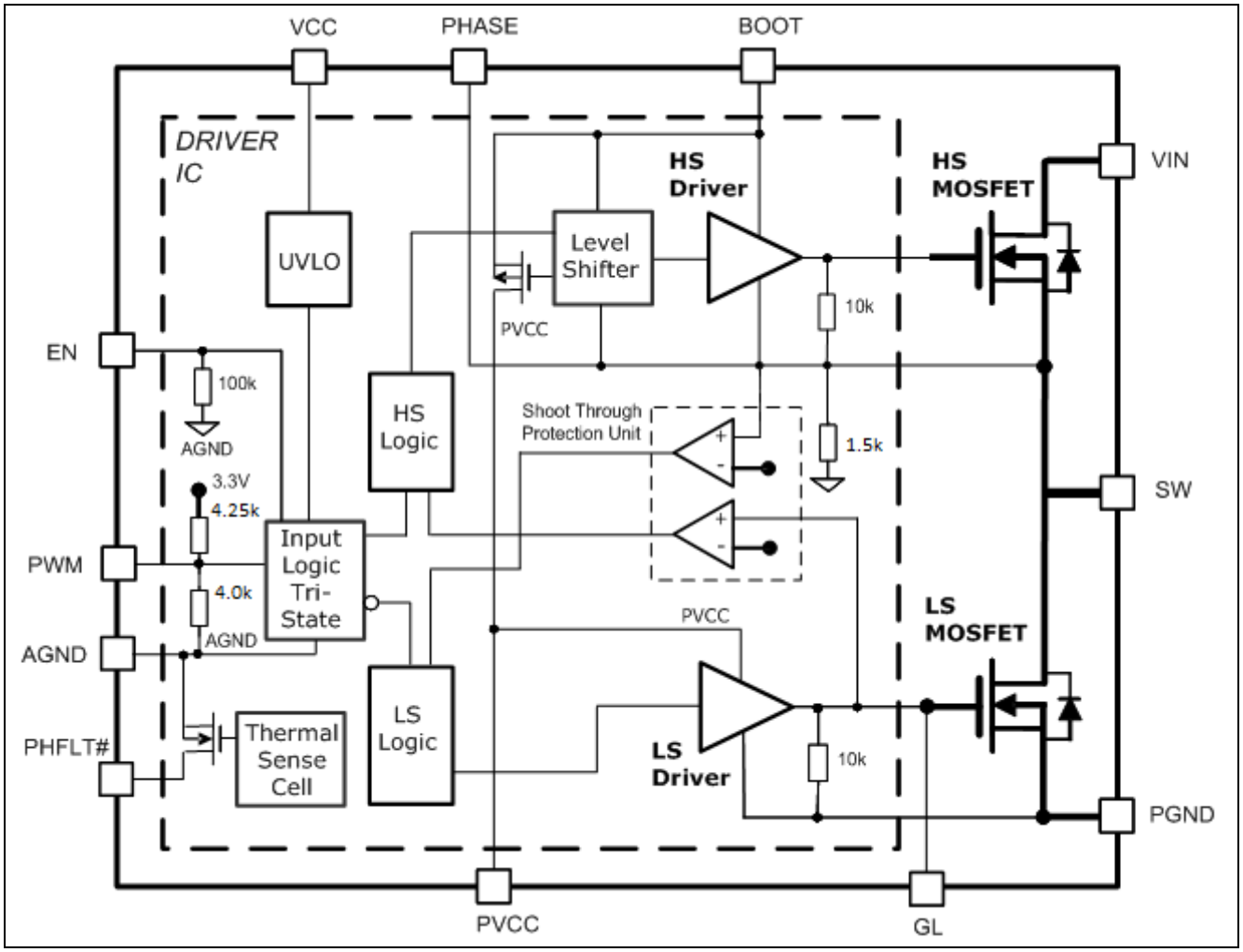


Figure 3 Simplified Block Diagram

4 Electrical Specification

4.1 Absolute Maximum Ratings

Note: T_A = 25°C

Stresses above those listed in Table 5 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings (Table 8) for extended periods may adversely affect the operation and reliability of the device.

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum average load current	I_{OUT}	–	–	40	A	
Input Voltage	V_{IN} (DC)	-0.30	–	21	V	
Logic supply voltage	V_{VCC} (DC)	-0.30	–	8		
High- and low-side driver voltage	V_{PVCC} (DC)	-0.30	–	8		
Switch / Phase node voltage	$V_{SW/PHASE}$ (DC)	-1	–	25		
	V_{PHASE} (AC)	-8[1]	–	–		Driver limitation
HS-MOSFET voltage spike	V_{IN}-V_{PHASE} (AC)	–	–	32[2]		2 ns above 25 V
LS-MOSFET voltage spike	V_{SW}-V_{PGND} (AC)	–	–	32[2]		
BOOT voltage	V_{BOOT} (DC)	-0.3	–	25		
	V_{BOOT} (AC)	–	–	30[1]		
	$V_{BOOT-PHASE}$ (DC)	-0.3	–	8		
EN voltage	V_{EN}	-0.3	–	4		Maximum value valid for operation up to 1h accumulated over lifetime, else the maximum value is 3.6V
PWM voltage	V_{PWM}	-0.3	–	4		
PHFLT#	$V_{PHFLT\#}$	-0.3	–	4		
Junction temperature	T_{Jmax}	-40	–	150	°C	
Storage temperature	T_{STG}	-55	–	150		

Note: All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

[1] AC is limited to 10 ns
[2] AC is limited to 2 ns

4.2 Thermal Characteristics

Table 6 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance to case (soldering point)	θ_{JC}	–	–	1	K/W	–
Thermal resistance to top of package	θ_{JCtop}	–	–	36		–
Thermal resistance to ambient (P_{loss} = 4.5 W,T_A = 70 °C, 8 layer server board with 2 oz copper per layer)	θ_{JA}	–	13	–		Still air

4.3 Recommended Operating Conditions and Electrical Characteristics

Note: V_{DRV} = V_{CIN} = 5 V, T_A = 25°C

Table 7 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	5	–	16[3]	V	For telecom applications see note 3
MOSFET driver voltage	V_{PVCC}	4.5	5	7		
Logic supply voltage	V_{VCC}	4.5	5	7		
Frequency of the PWM	f_{SW}	–	–	1.0	MHz	
Junction temperature	T_{jOP}	-40	–	125	°C	

[3] In telecom applications the recommended maximum voltage for V_{IN} is 13.2V unless a boot resistor is used (in series with C_{BOOT} in Figure 6) to limit the voltage spike V_{PHASE}-V_{PGND} (AC) to 26V.

Table 8 Voltage Supply And Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO BOOT rising	$V_{UVLOBOOT\_R}$	–	4.0	–	V	V_{BOOT}-V_{SW} rising
UVLO BOOT falling	$V_{UVLOBOOT\_F}$	–	3.8	–		V_{BOOT}-V_{SW} falling
UVLO rising	V_{UVLO_R}	–	–	4.2	V	VCC rising
UVLO falling	V_{UVLO_F}	3.7	–	–		VCC falling
Driver current	I_{PVCC_300kHz}	–	9	–	mA	EN = 3.3 V, f_{SW} = 300 kHz
	I_{PVCC_1MHz}	–	30	–		EN = 3.3 V, f_{SW} = 1 MHz
	I_{PVCC_PWML}	–	710	–	µA	EN = 3.3 V, PWM = 0V
	I_{PVCC_PWMH}	–	210	–		EN = 0V, PWM=3.3V,
IC current (control)	I_{VCC_PWML}	–	1	–	mA	EN = 3.3 V, PWM = 0 V
	I_{VCC_O}	–	630	–	µA	EN = 3.3 V, PWM = Open
IC quiescent	I_{CC} + I_{PVCC}	–	840	–		EN = 0V, PWM = Open
Pre-Bias at SW	V_{SW_0}	–	160	180	mV	VCC and PVCC present

Table 9 Logic Inputs And Threshold

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Input low	V_{EN_L}	–	–	0.8	V	V_{EN} falling
	Input high	V_{EN_H}	2.0	–	–		V_{EN} rising
	Sink current	I_{EN}	–	10	–	µA	V_{EN} = 1 V
PWM	Input low	V_{PWM_L}	–	–	0.6	V	V_{PWM} falling
	Input high	V_{PWM_H}	2.6	–	–		V_{PWM} rising
	Input resistance	$R_{IN\text{-}PWM}$	–	2	–	kΩ	V_{PWM} = 1 V
	Open voltage	V_{PWM_O}	–	1.6	–	V	V_{PWM_O}
	Tri-state shutdown window[4]	V_{PWM_S}	1.2	–	2.0		
PHFLT#	Warning Temperature[5]	$T_{PHFLT\#\_T}$	–	140	–	°C	
	Thermal warning accuracy5	$dT_{PHFLT\#\_T}$	-10	–	10	K	
	Hysteresis5	$T_{PHFLT\#\_H}$	–	10	–		
	On resistance	$R_{PHFLT\#\_PD}$	–	37.5	80	Ω	I_{LOAD} = 8mA
	Leakage current	$I_{PHFLT\#\_LK}$	–	0.1	5	µA	

[4] Maximum voltage range for tri-state

[5] The thresholds for temperature warning are verified by design and not subject to production test.

Table 10 Timing Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PWM tri-state to SW rising delay	t_pts	–	15	–	ns	
PWM tri-state to SW falling delay	t_pts2	–	15	–		
SW Shutdown hold-Off time from PWM low	t_tsshd	–	50	–		
SW Shutdown hold-Off time from PWM high	t_tssh	–	50	–		
PWM to SW turn-off propagation delay	t_pdlu	–	20	–		
PWM to SW turn-on propagation delay	t_pdll	–	10	–		
DR_EN turn-off propagation delay falling	t_pdl_DR_EN	–	20	–		
DR_EN turn-on propagation delay rising	t_pdh_DR_EN	–	20	–		
UVLO-BOOT-on time	t_UVLOBOOTon	–	200	–		Pulse pattern issued to GL in UVLO-BOOT
UVLO-BOOT-off time	t_UVLOBOOToff	–	200	–		
PWM minimum pulse width	ton_min_PWM	–	25	–		When PWM change is recognized, the output remains in the new state for these minimum times.
PWM minimum off time	toff_min_PWM	–	30	–		

5 Theory of Operation

The TDA21240 incorporates a high performance gate driver, one high-side power MOSFET and one low-side power MOSFET in a single PG-IQFN-30-2 package. The advantages of this arrangement are found in the areas of increased performance, increased efficiency and lower overall package and layout inductance.This module is ideal for use in Synchronous Buck Regulators.

The power MOSFETs are optimized for 5 V gate drive enabling excellent high load and light load efficiency. The gate driver is a robust high-performance driver rated at the switching node for DC voltages ranging from -1 V to +21 V. The power density for transmitted power of this approach is approximately 60 W within a 16 mm^2 area.

5.1 Driver Characteristics

The gate driver of the TDA21240 has 2 voltage inputs, VCC and PVCC. VCC is the 5 V logic supply for the driver. PVCC sets the driving voltage for the high side and low side MOSFETs. The reference for the gate driver control circuit (VCC) is AGND. To decouple the sensitive control circuitry (logic supply) from a noisy environment a ceramic capacitor must be placed between VCC and AGND close to the pins. PVCC needs also to be decoupled using a ceramic capacitor (MLCC) between PVCC and PGND in close proximity to the pins. PGND serves as reference for the power circuitry including the driver output stage.

Referring to the block diagram page 4, VCC is internally connected to the UVLO circuit. It will force shut-down for insufficient VCC voltage. PVCC supplies the floating high-side drive – consisting of an active boot circuit - and the low side drive circuit. During undervoltage both GH and GL are driven low actively; further passive pull-down (10 kΩ) is placed across gate-source of both FETs.

An additional UVLO circuitry, sensing the BOOT voltage level, is implemented to enable a recharge of the boot capacitor when its voltage is too low for a complete turn-on of the HS-MOSFET.

Proper response of the driver to the PWM signal is only guaranteed when UVLO and UVLO BOOT have been cleared by their respective supply voltages (Table 8). Therefore, it is strongly recommended to only issue pulses to PWM when no UVLO conditions are present. The power down sequence should set PWM to HiZ with regard to the internal threshold before ramping down VIN, PVCC and VCC respectively.

5.2 Inputs to the Internal Control Circuits

The **PWM** is the control input to the IC from an external PWM controller and is compatible with 3.3 V.

The PWM input has tri-state functionality. When the voltage remains in the specified PWM-shutdown-window for at least the PWM-shutdown-holdoff time t_tsshd, the operation will be suspended by keeping both MOSFET gate outputs low. Once left open, the pin is held internally at a level of V_{PWM_O} = 1.6 V level.

Table 11 PWM Pin Functionality

PWM logic level	Driver output
Low	GL= High, GH = Low
High	GL = Low, GH = High
Open (left floating, or High impedance)	GL = Low, GH = Low

The PWM threshold voltages V_{PMW_O}, V_{PWM_H}, V_{PWM_L} do not vary over the wide range of VCIN supply voltages (4.5 V to 8 V).

The **EN** is an active high signal. When EN is being pulled low, the power stage will be disabled.

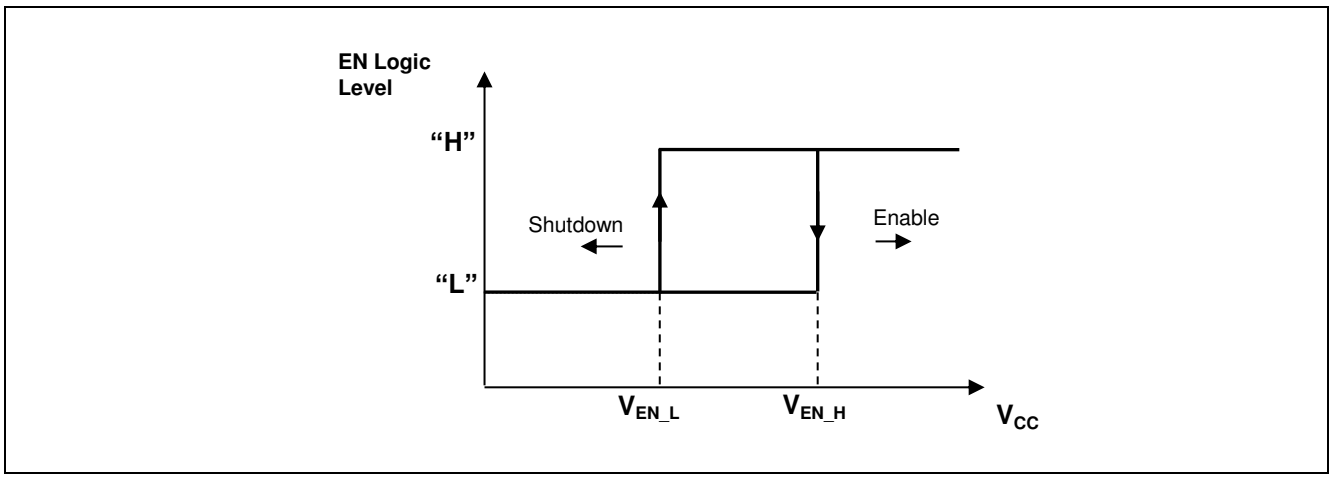


Figure 4 Enable (EN) signal logic levels

Table 12 EN Pin Functionality

EN logic level	Driver output
Low	Shutdown : GL = GH = Low
High	Enable : GL = Active, GH = Active
Open (left floating, or High impedance)	Shutdown : GL = GH = Low

5.3 Thermal protection

The **PHFLT#** pin is a digital monitoring output for the thermal warning. It does not affect the operation of the driver nor does it shut down the device.

When the driver junction temperature exceeds the thermal warning threshold of 140 °C (typ) the open drain output PHFLT# will be pulled low. Externally PHFLT# has to be connected to a supply (e.g. +3.3 V) by a resistor in the range of 10 kΩ. When the temperature of the driver junction decreases below the level of thermal warning threshold minus hysteresis (10 K typ.), the pin **PHFLT#** is released. $V_{PHFLT\#}$ is being pulled up by the external resistance. If the thermal warning feature is not used the pin can be left floating.

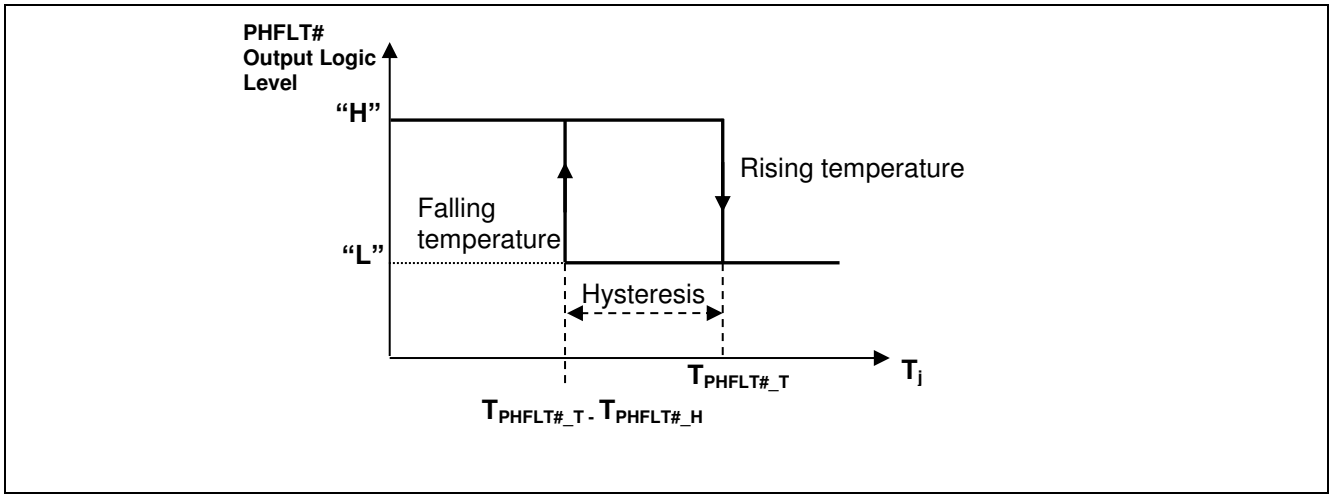


Figure 5 Thermal warning

5.4 Shoot Through Protection

The TDA21240 driver includes gate drive functionality to protect against shoot through. In order to protect the power stage from overlap, both high-side and low-side MOSFETs being on at the same time, the adaptive control circuitry monitors specific voltages. When the PWM signal transitions to low, the high-side MOSFET will begin to turn off after the propagation delay time t_pdlu. When V_{GS} of the high-side MOSFET is discharged below 1 V (a threshold below which the high-side MOSFET is off), a secondary delay t_pdhl is initiated. After that delay the low-side MOSFET turns on regardless of the state of the “SW” pin. It ensures that the converter can sink current efficiently and the bootstrap capacitor will be refreshed appropriately during each switching cycle. See Figure 8 for more detail.

5.5 UVLO – BOOT Protection

After long tristate conditions the voltage of the boot capacitor may be too small to completely enhance the HS-MOSFET when PWM enables GH directly after. Therefore, a monitoring circuit is being implemented to detect a lower threshold at which GH can safely be turned on. If the voltage across the boot capacitor has been dropping to this threshold a boot refresh circuit engages until an upper threshold has been reached.

The recharge is being done by intervals of repetitively pulling GL high for t_UVLOBOOTon followed by t_UVLOBOOToff driving GL low to reset the output current to zero. When the voltage across the boot capacitor has reached an upper threshold the recharge cycles stop.

The PWM input always takes priority over the boot refresh circuit when it is logic “H” or logic “L”.

6 Application

6.1 Implementation

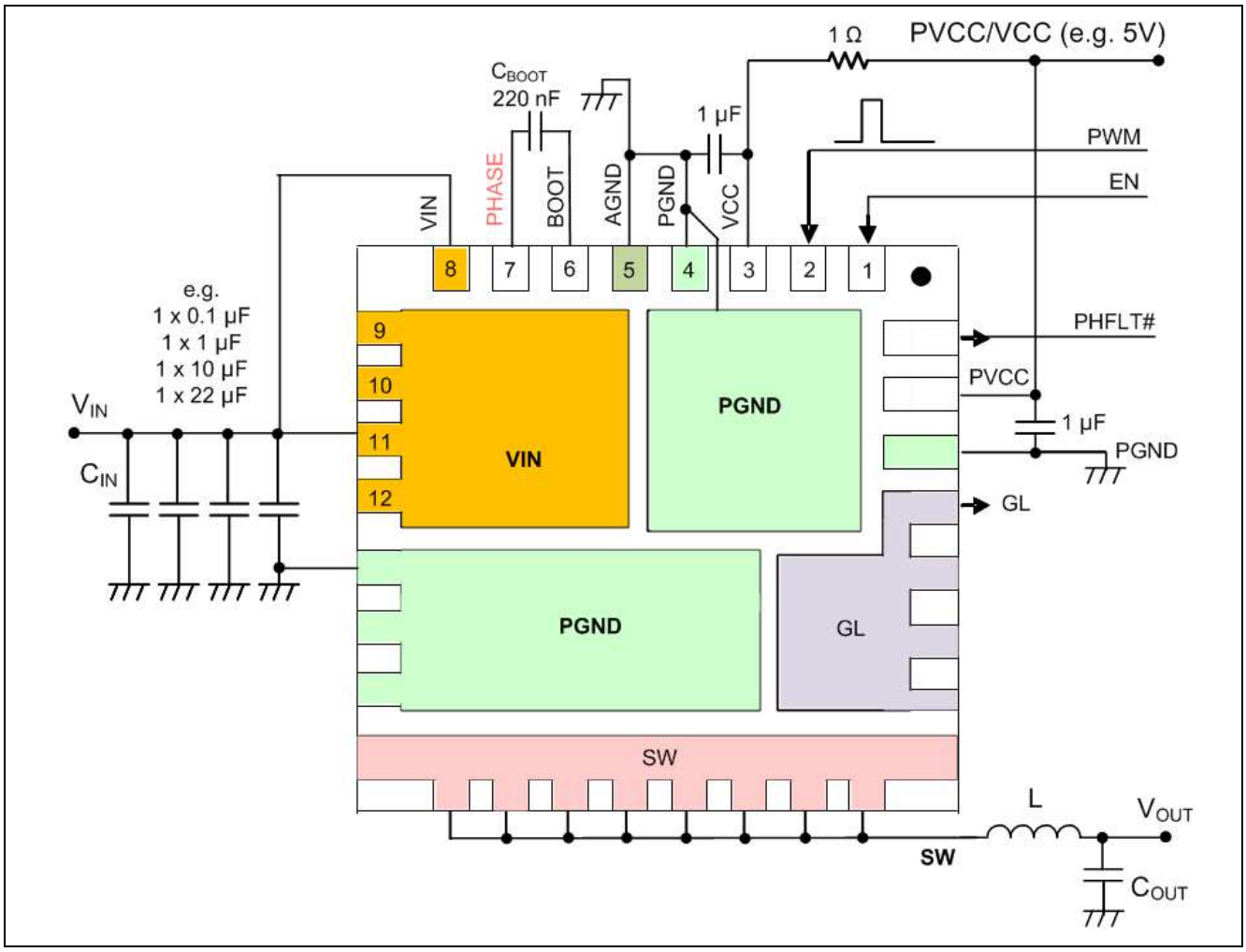


Figure 6 Pin Interconnection Outline (example, transparent top view)

Note:

1. *Pin PHASE is internally connected to SW node*
2. *It is recommended to place a RC filter between VCC and PVCC as shown.*

6.2 Typical Application

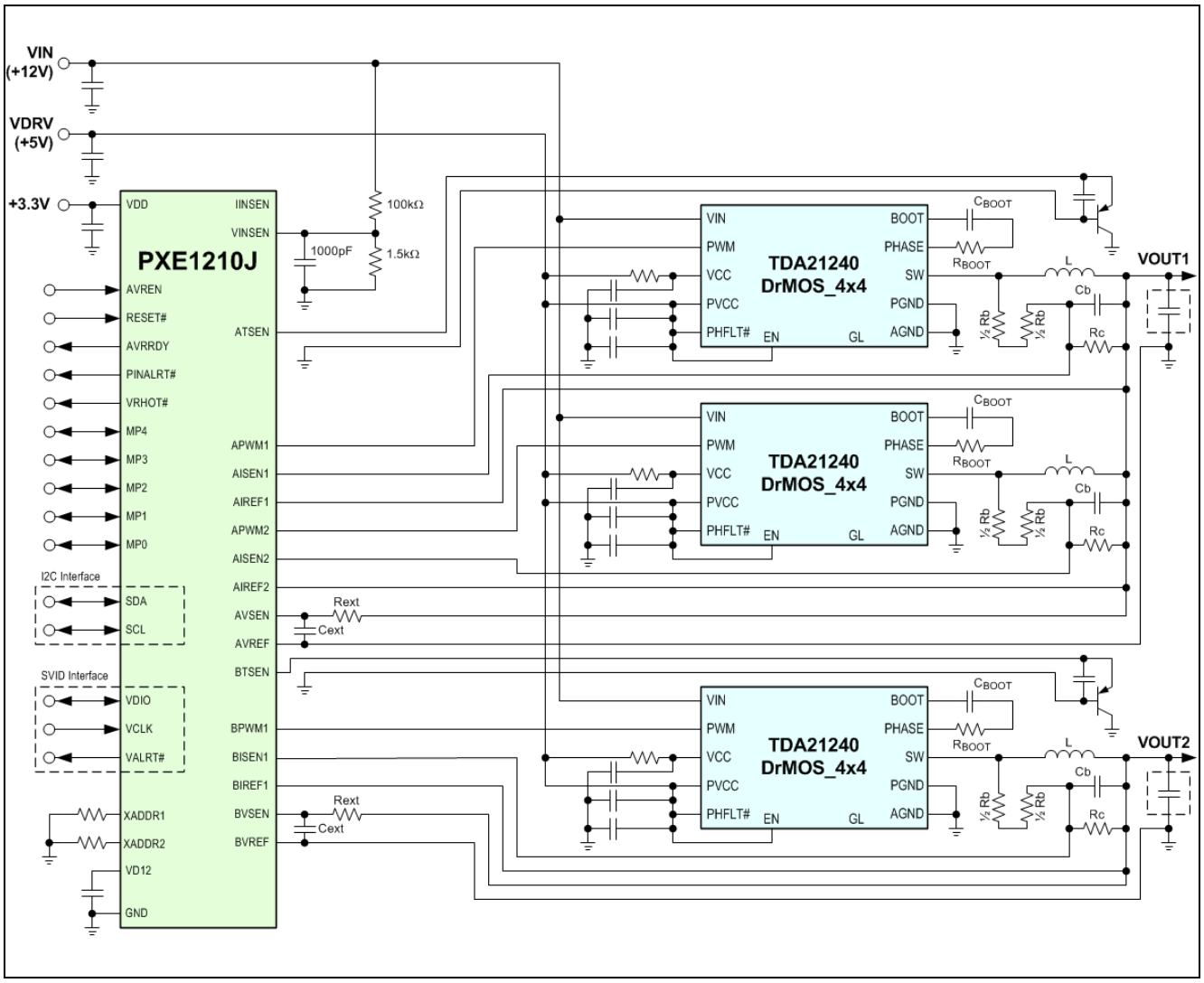


Figure 7 2+1 - phase voltage regulator - typical application (simplified schematic)

7 Gate Driver Timing Diagram

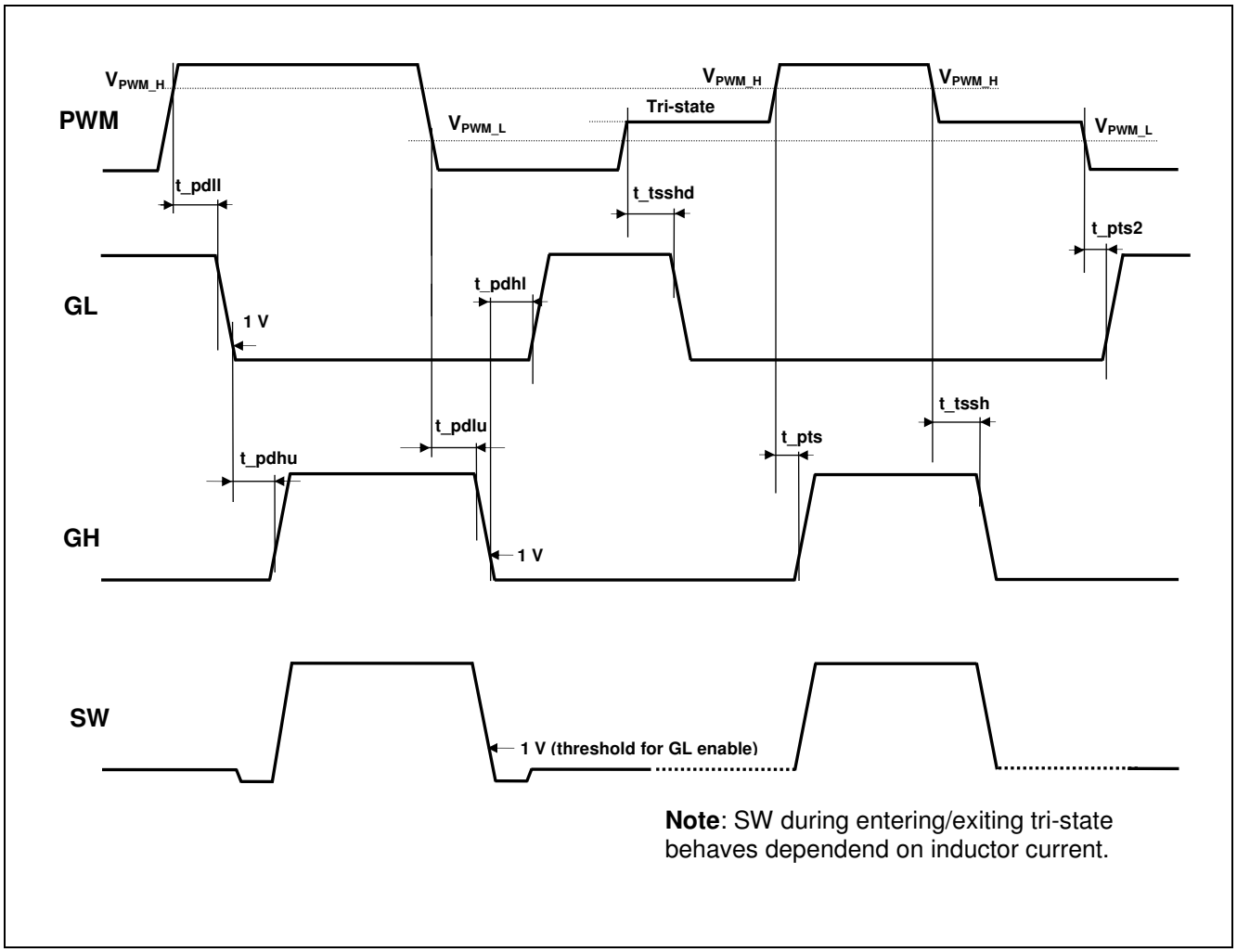


Figure 8 Adaptive Gate Driver Timing Diagram

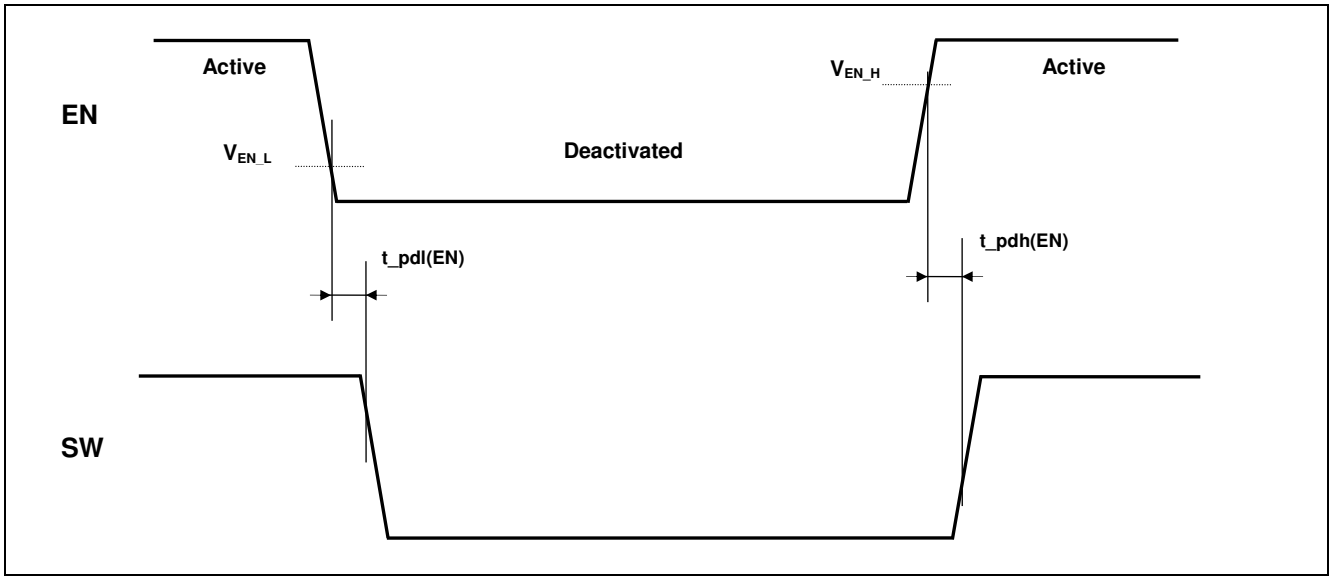


Figure 9 EN Timing Diagram

8 Performance Curves – Typical Data

Operating conditions (unless otherwise specified): VIN = +12 V, VCC = PVCC = +5 V, VOUT = +1.8 V, f_{SW} = 600 kHz, 150nH (Cooper, FP0906R1-R15, DCR = 0.29 mΩ) inductor, T_A = 25 °C, airflow = 300 LFM, no heatsink. Efficiency and power loss reported herein include only TDA21240 losses for a single phase on an 8-layer server board.

8.1 Driver Current versus Switching Frequency

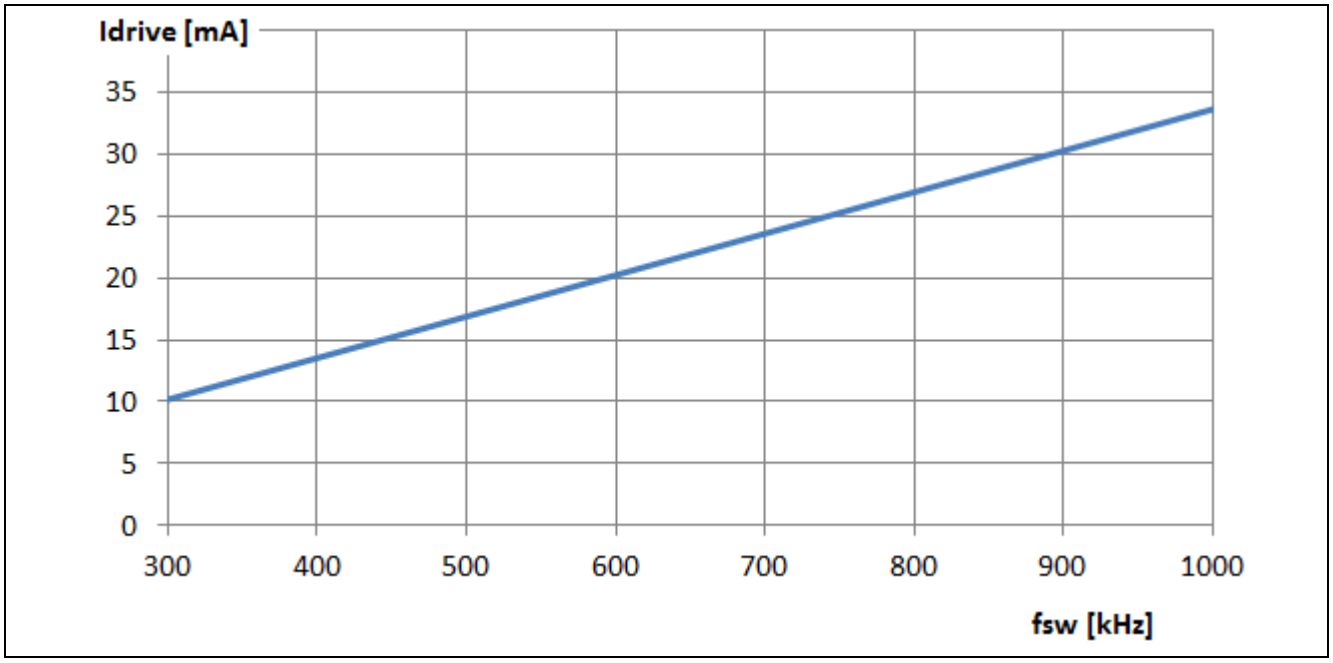


Figure 10 Driver Current over Switching Frequency in CCM Operation

8.2 Efficiency and Power Loss

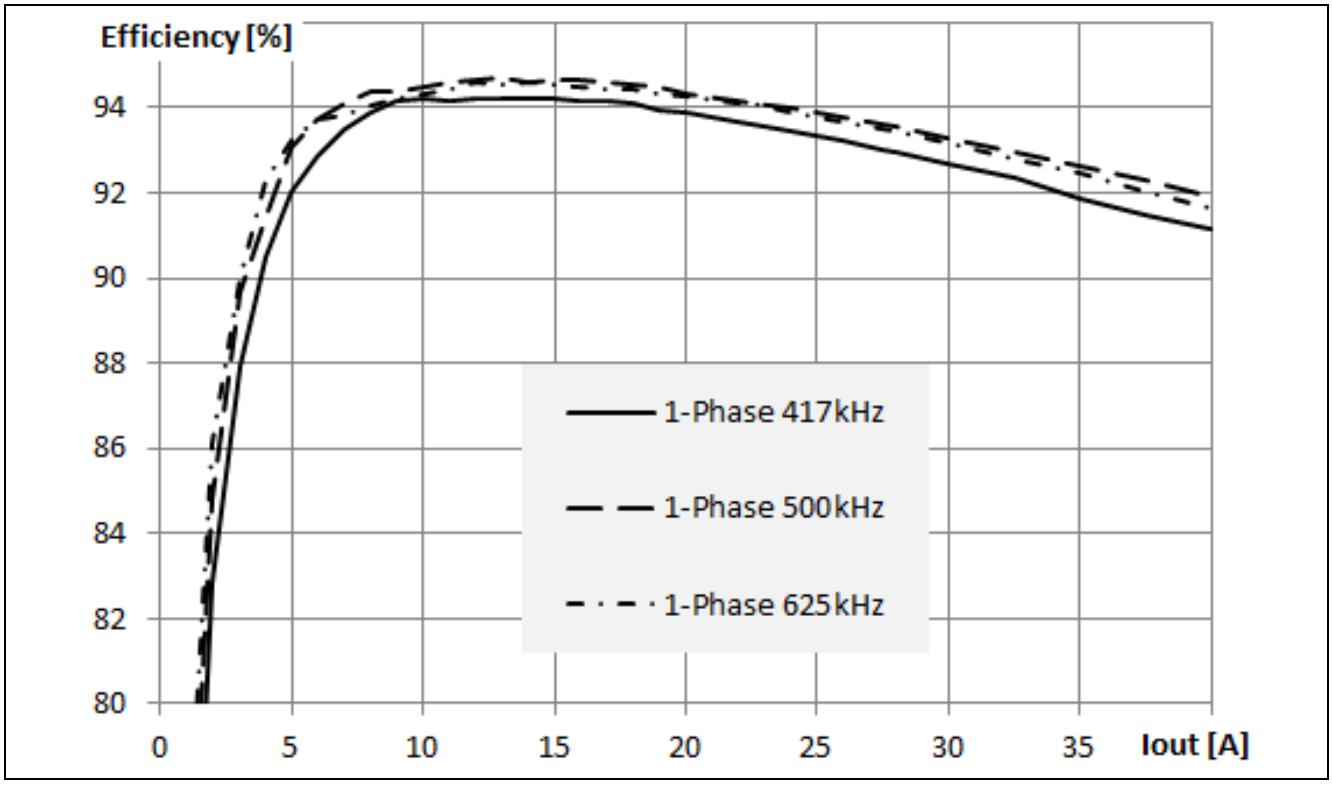


Figure 11 Efficiency at VIN = 12 V, VCC = PVCC = 5 V, Single Phase, VOUT = 1.8 V

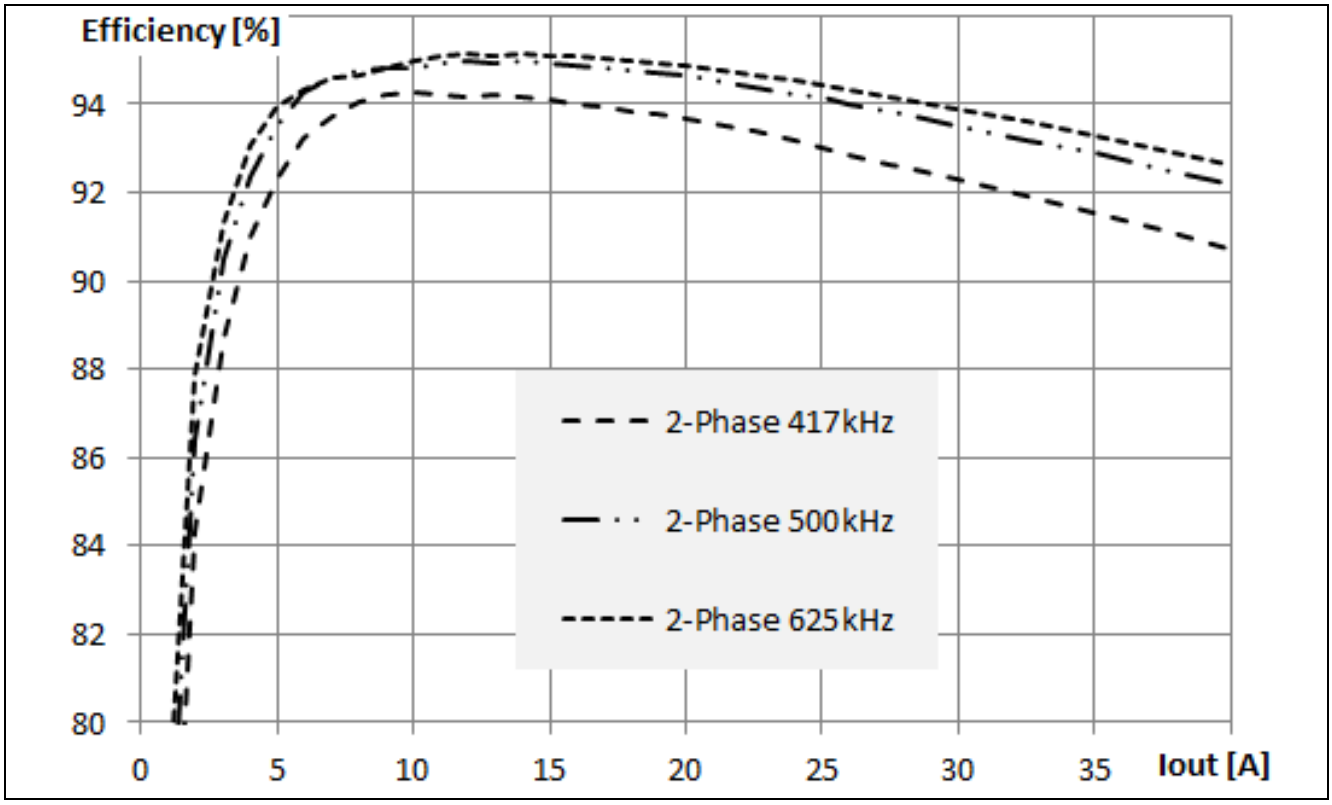


Figure 12 Efficiency at VIN = 12 V, VCC = PVCC = 5 V, Dual Phase, VOUT = 1.8 V

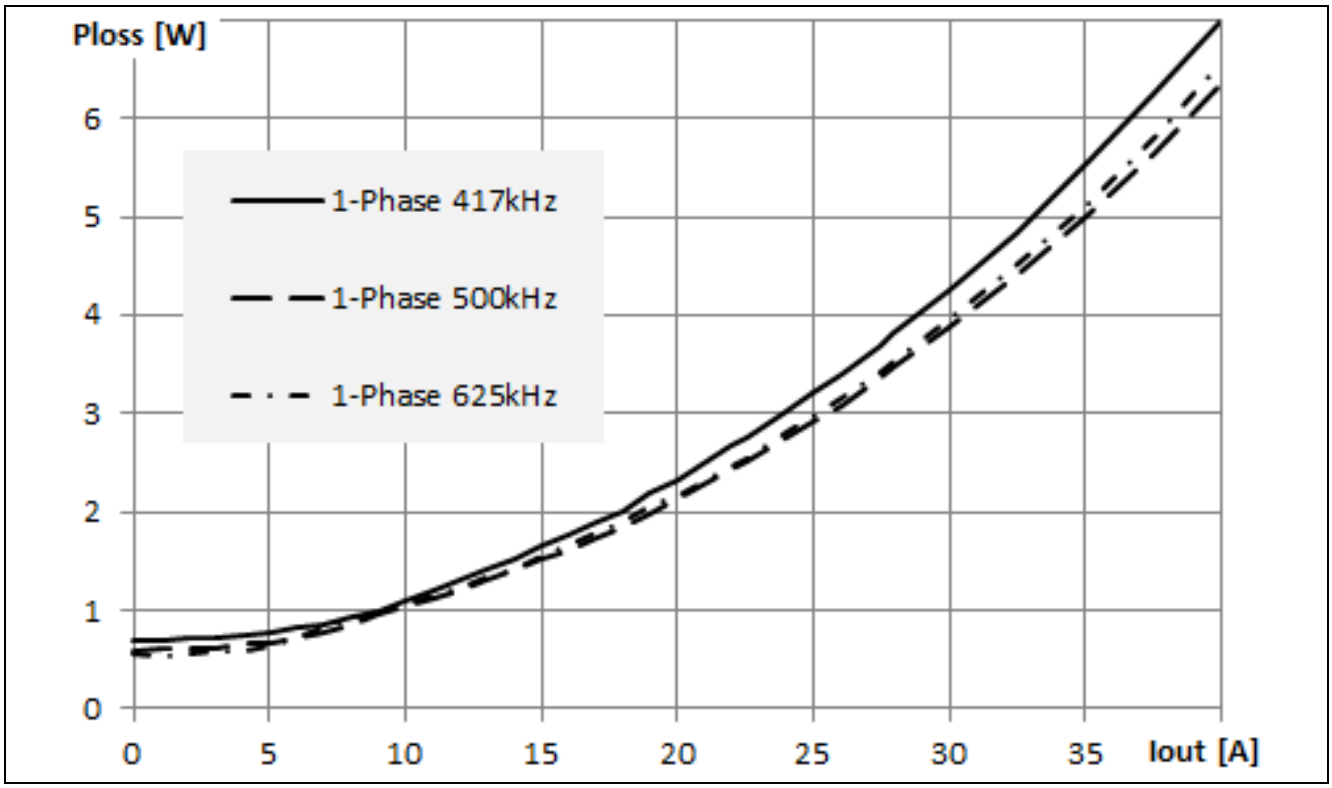


Figure 13 Power Loss at VIN = 12 V, VCC = PVCC = 5 V, Single Phase, VOUT = 1.8 V

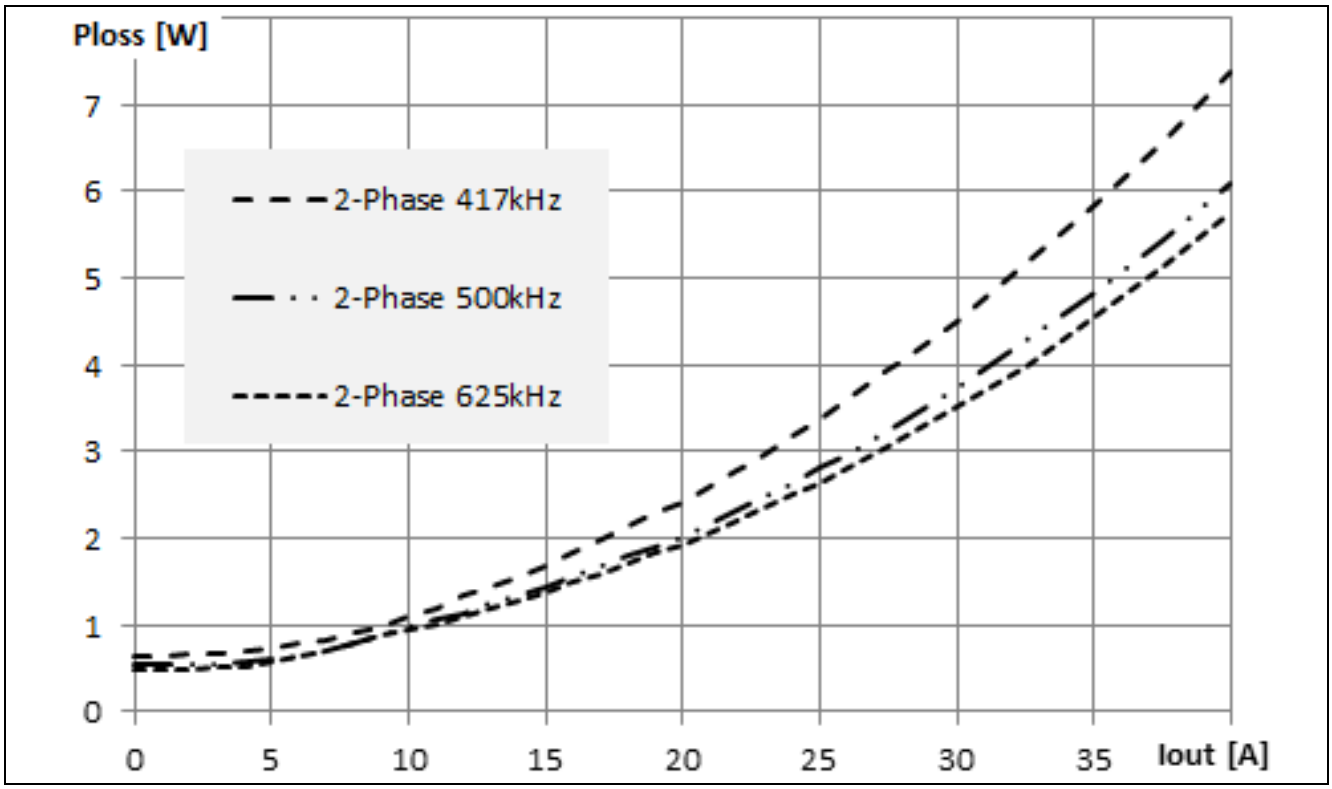


Figure 14 Power Loss at VIN = 12 V, VCC = PVCC = 5 V, Dual Phase, VOUT = 1.8 V

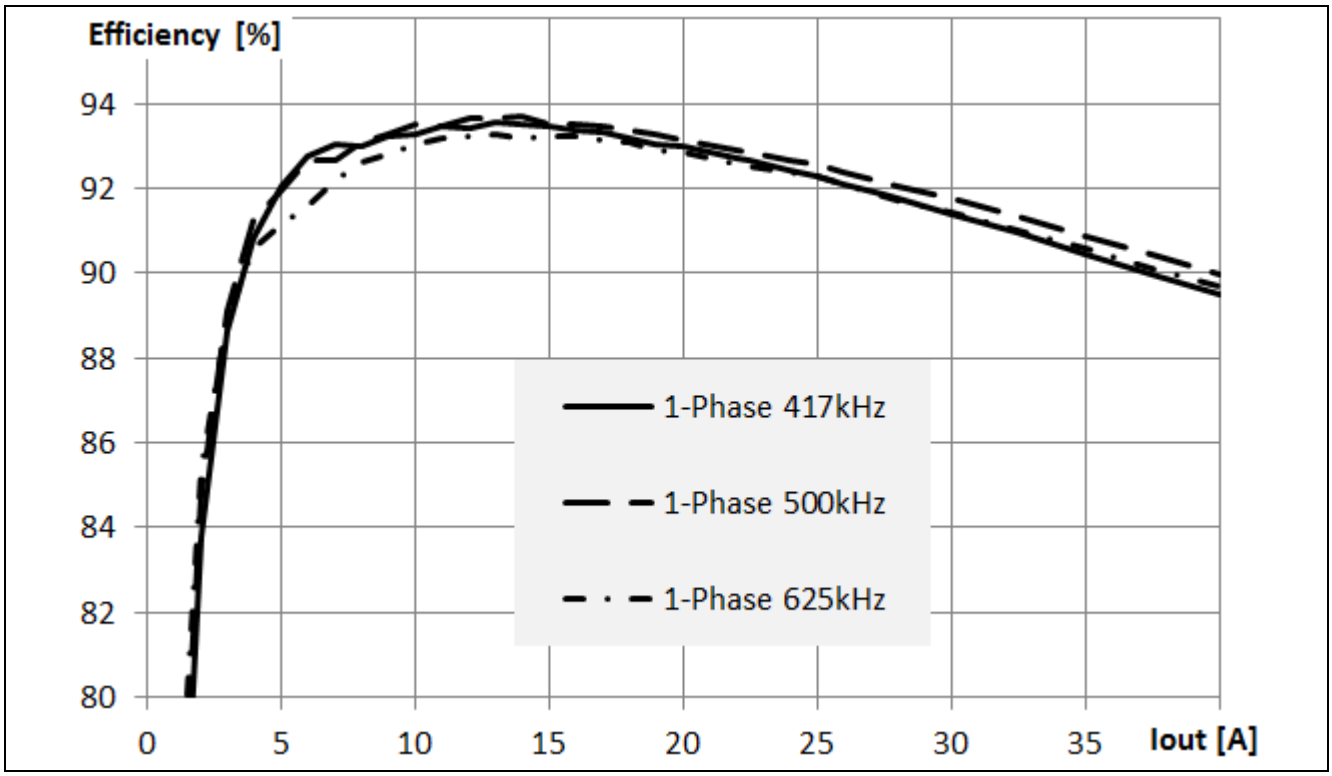


Figure 15 Efficiency at VIN = 12 V, VCC = PVCC = 5 V, Single Phase, VOUT = 1.2 V

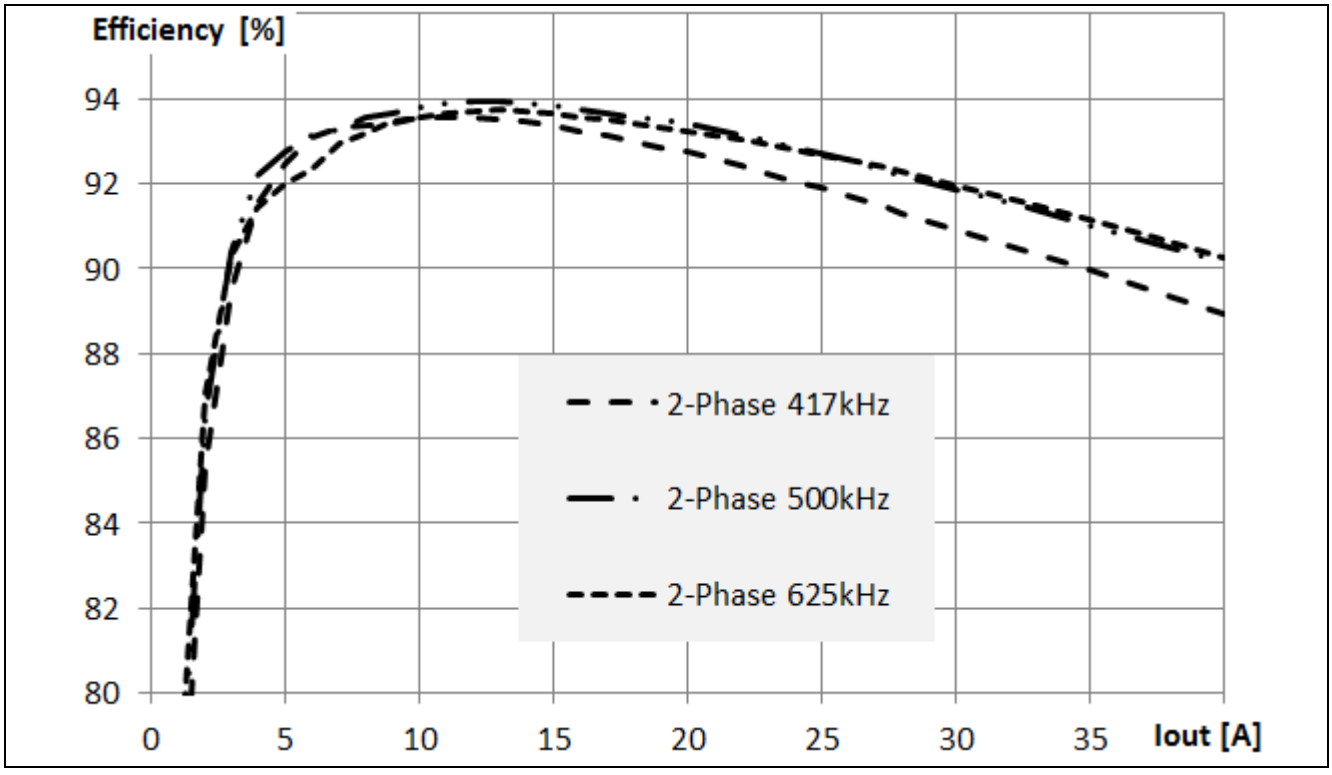


Figure 16 Efficiency at VIN = 12 V, VCC = PVCC = 5 V, Dual Phase, VOUT = 1.2 V

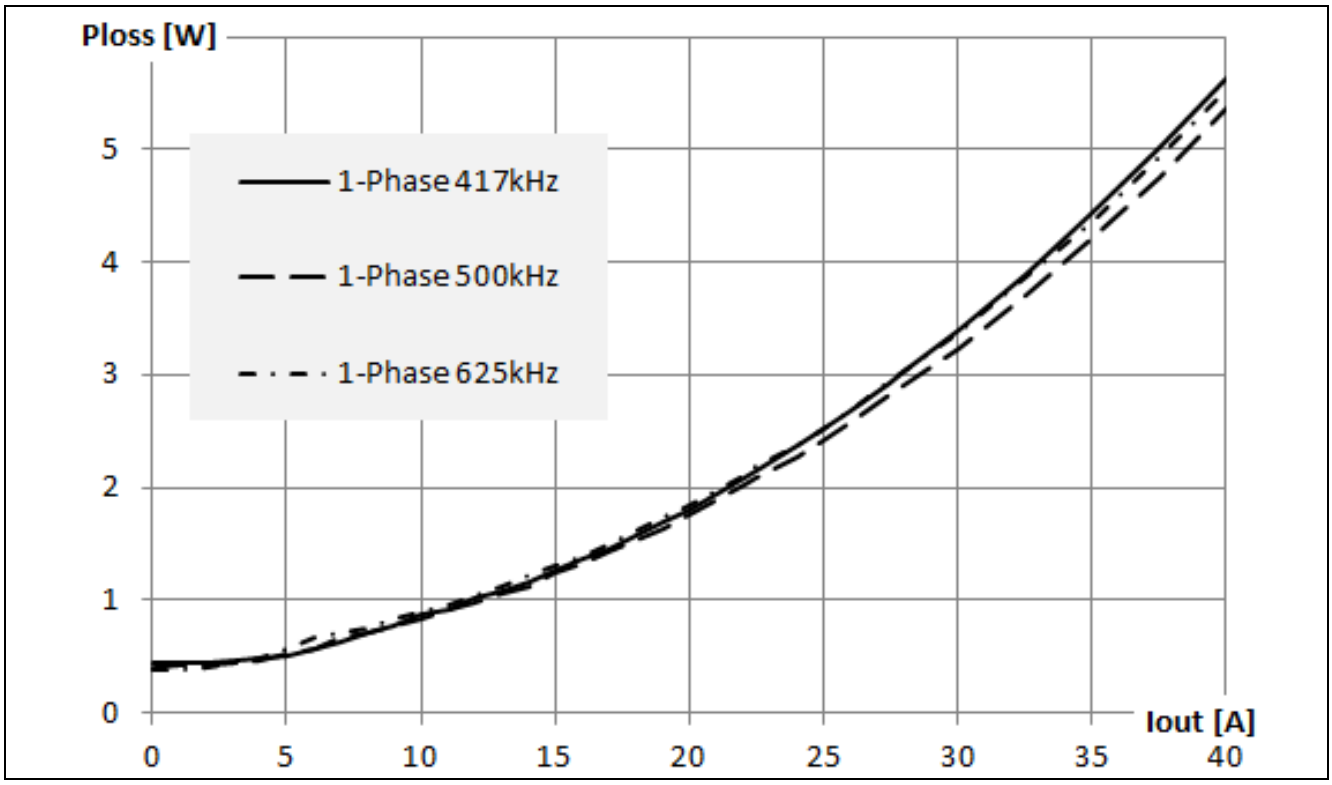


Figure 17 Power Loss at VIN = 12 V, VCC = PVCC = 5 V, Single Phase, VOUT = 1.2 V

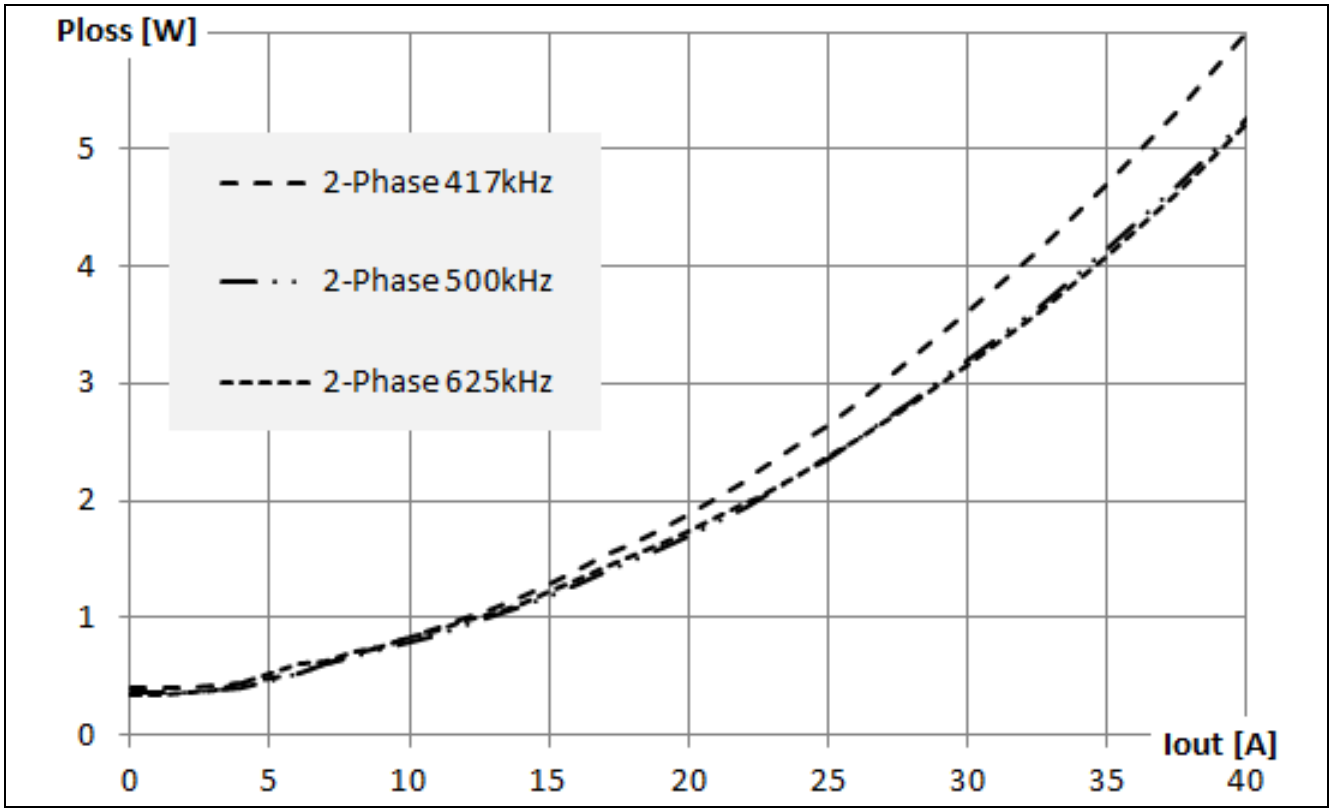
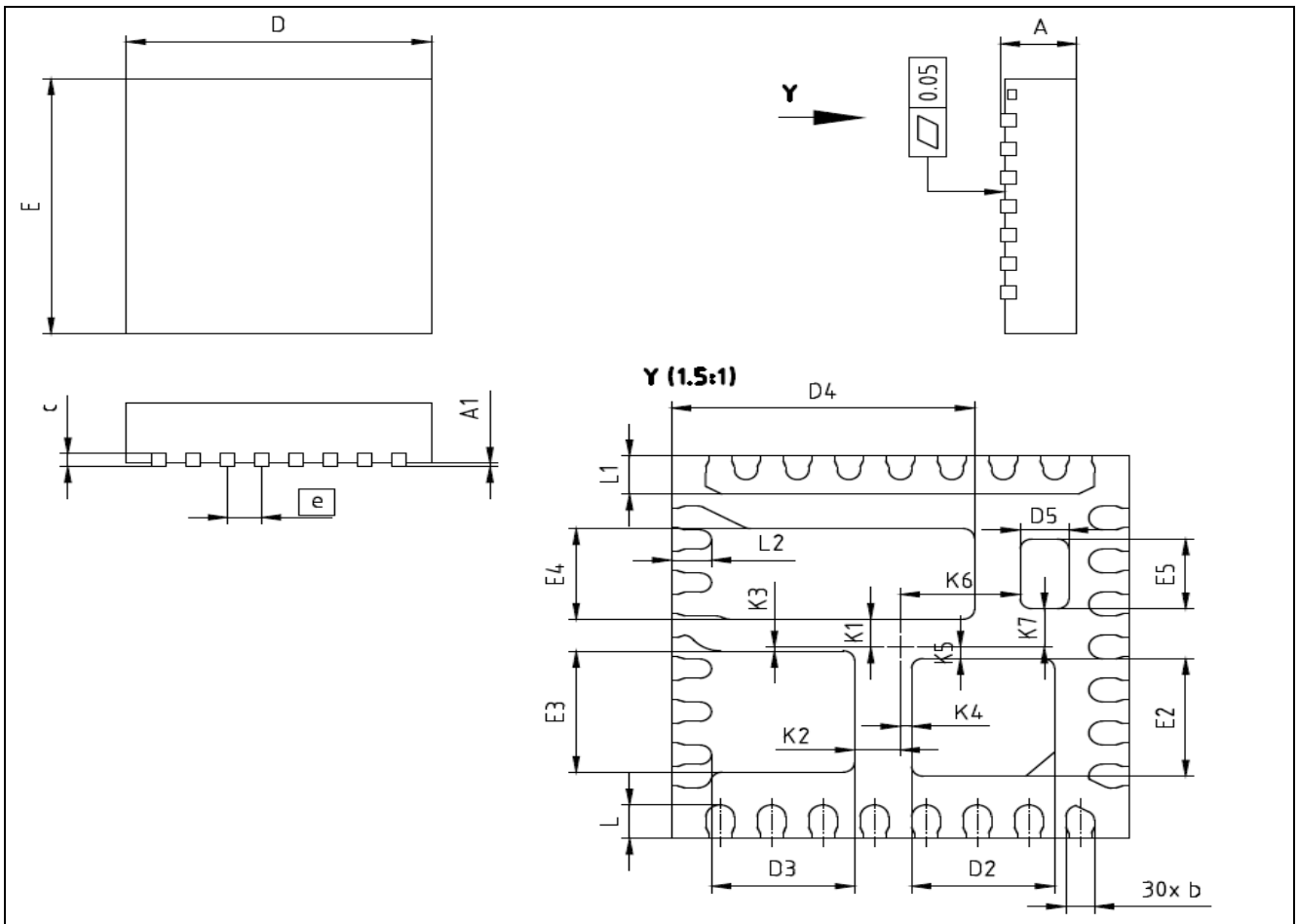


Figure 18 Power Loss at VIN = 12 V, VCC = PVCC = 5 V, Dual Phase, VOUT = 1.2 V

9 Mechanical Drawing PG-IQFN-30-2



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	1.10	0.033	0.043
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
c	0.10	0.30	0.004	0.012
D	3.90	4.10	0.154	0.161
D2	1.15	1.35	0.045	0.053
D3	1.15	1.35	0.045	0.053
D4	2.55	2.75	0.100	0.108
D5	0.33	0.53	0.013	0.021
E	3.90	4.10	0.154	0.161
E2	1.13	1.33	0.044	0.052
E3	1.17	1.37	0.046	0.054
E4	0.85	1.05	0.033	0.041
E5	0.63	0.83	0.025	0.033
e	0.45		0.018	
N	30		30	
L	0.25	0.45	0.010	0.018
L1	0.30	0.50	0.012	0.020
L2	0.25	0.45	0.010	0.018
K1	0.19	0.39	0.007	0.015
K2	0.30	0.50	0.012	0.020
K3	-0.06	0.14	-0.002	0.006
K4	0.00	0.20	0.000	0.008
K5	0.02	0.22	0.001	0.009
K6	0.95	1.15	0.037	0.045
K7	0.30	0.50	0.012	0.020

Figure 19 Mechanical Dimensions – Top and Side Views (in mm)

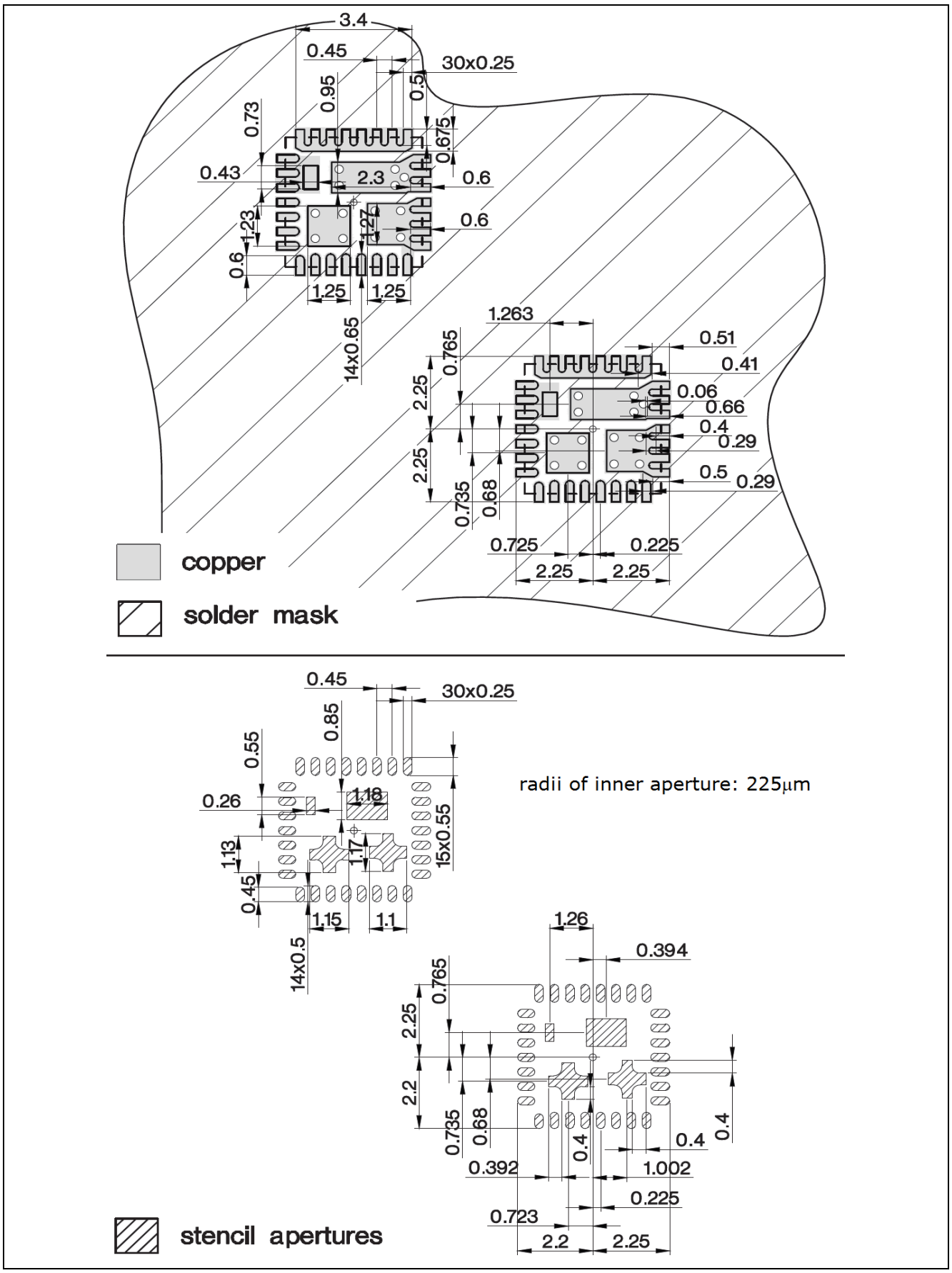
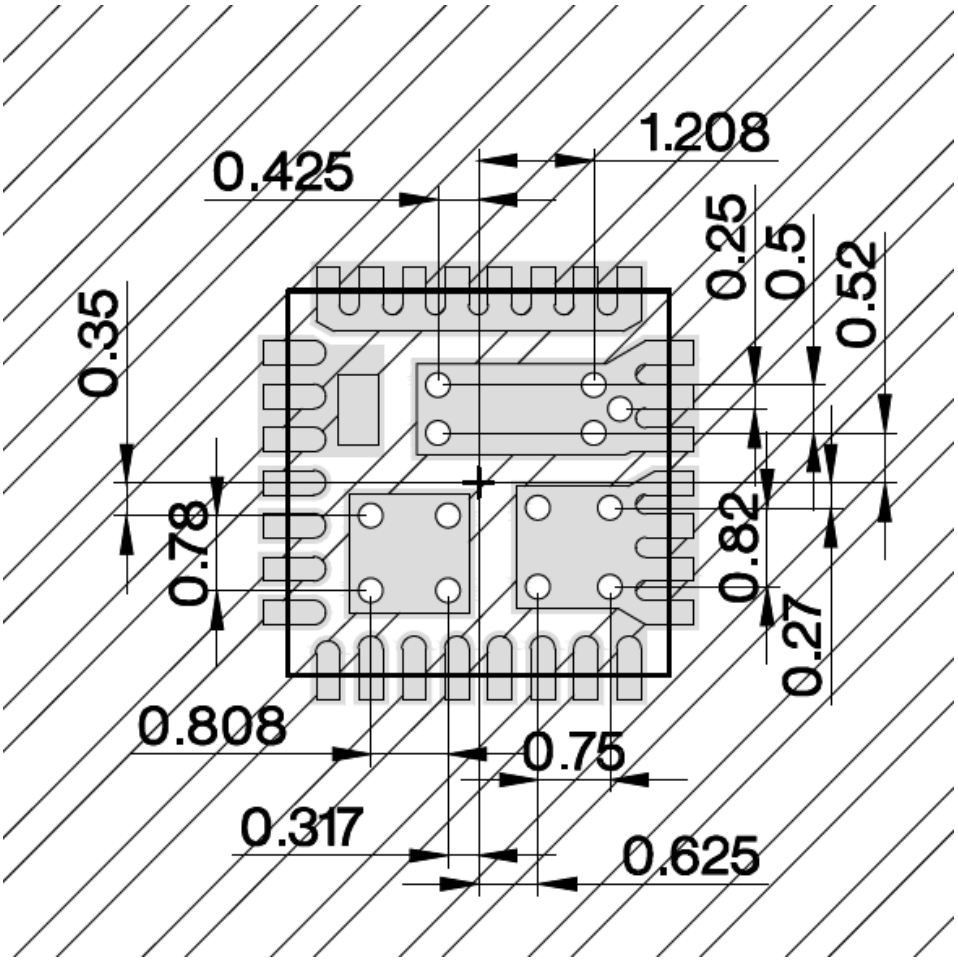


Figure 20 Recommended Landing Pattern and Stencil Dimensions (in mm)



Via diameter: 250 µm or 10 mil

Figure 21 Recommended Via Pattern (in mm)

10 Board Layout Recommendations

The PCB (printed circuit board) layout design follows the listed industry standards:

- Recommended vias: 10 mil[6] hole with 20 mil via pad diameter, 12 mil hole with 24 mil via pad diameter
- Minimum (typical) via to via center distance: 18 mil (18 … 25 mil)
- Minimum feature width: 5 mil
- Minimum (typical) clearance: 5 mil (15 … 20 mil)

Commonly, 10 mil via drill diameters are used for PCBs up to 150 mil thicknesses (usually 22 layers). For thicker boards, 12 mil vias are recommended. To reduce voltage spikes caused by parasitic circuit inductance, all primary decoupling capacitors for VIN, PVCC, BOOT and VCC should be of MLCC type, X6S or X7R rated and located at the same board side as the powerstage close to their respective pins. This is especially important for the VIN to PGND MLCCs.

Electrical and thermal connection of the powerstage to the PCB is crucial for achieving high efficiency. Therefore, vias in VIN and PGND pads are required in the pad areas to connect most effectively to other power and PGND layers. Bigger value MLCC input capacitors should be placed at the bottom side of the PCB close to the vias of the powerstage's VIN and PGND pads. To reduce the stray inductance in the current commutation loop it is strongly recommended to have the 2nd layers from the top and the bottom of the board to be monolithic ground planes. All logic and signal connections between powerstage and controller should be embedded between two ground layers. The routing of the current sense lines back to the controller has to be done differentially, for example with 5 mil spacing and 10 – 15 mil distances to other potentials. If the PCB features more than 10 layers, the passive components associated with the current sense lines should be located only at the top side of the board. All resistors and capacitors near the powerstage should be in 0402 case size. For minimizing distribution loss to the load and maintaining signal integrity, have multiple layers/planes in parallel and ensure that the copper cross section for PGND is at least as big as it is for Vout.

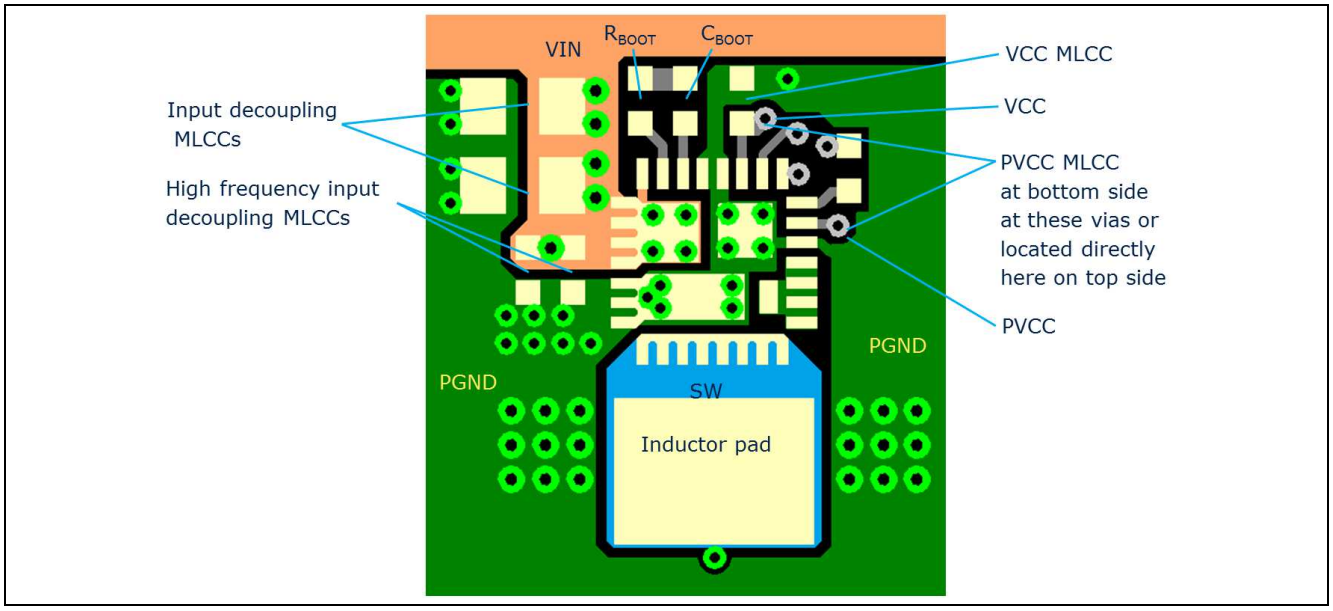


Figure 22 Generic Board Design

[6] Unit conversion: 1 mil = 25.4 µm

Revision History

TDA21240

Revision: 2017-03-07, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2016-11-10	Release of final version
2.1	2017-03-07	Update of marking info

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.
In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.
The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.