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Datasheet, V2.0, 1 May 1996

PWM-FF IC

TDA4916GG

SMPS IC with MOSFET Driver Output

Power Management & Supply

Never stop thinking.

Revision History: **1996-05-01** Datasheet

Previous Version:

Page	Subjects (major changes since last revision)

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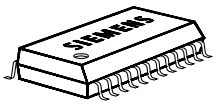
Features

- High clock frequency
- Low current drain
- High reference accuracy
- All monitoring functions



P-DSO-24-1

Type	Ordering Code	Package
TDA 4916 GG	Q67000-A9230	P-DSO-24-1

Functional Description and Application

The general-purpose single-ended switch-mode power supply device for the direct control of SIPMOS power transistors incorporates both digital and analog functions. These are required for the construction of high-quality flyback, forward and choke converters. The device can be likewise used for transformer-less voltage multipliers and variable-speed motors.

Faults occurring during operation of the switch-mode power supply are detected by comparators integrated in the device which initiate protective functions.

In addition, pairs of power supplies can be synchronized in antiphase. In-phase or antiphase synchronization is possible when more than two power supplies are involved.

Pin Configuration
(top view)

P-DSO-24-1

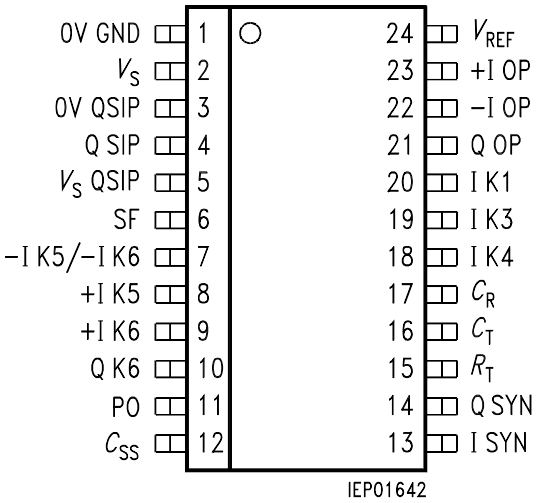


Figure 1

Pin Definitions and Functions

Pin No.	Symbol	Function
1	0V GND	GND
2	V_S	Supply voltage
3	0V QSIP	Ground QSIP
4	Q SIP	SIPMOS driver
5	V_S QSIP	Supply voltage driver
6	SF	Series feed
7	– I K5/– I K6	Current sensor negative input
8	+ I K5	Current sensor K5
9	+ I K6	Current turn-OFF K6
10	Q K6	Output K6
11	PO	Pulse omission
12	C_{SS}	Soft start
13	I SYN	Input synchronization
14	Q SYN	Output synchronization
15	R_T	Frequency generator
16	C_T	Frequency generator
17	C_R	Ramp generator
18	I K4	Input undervoltage
19	I K3	Input overvoltage
20	I K1	Input K1
21	Q OP	Output operational amplifier
22	– I OP	Input operational amplifier
23	+ I OP	Input operational amplifier
24	V_{REF}	Reference voltage

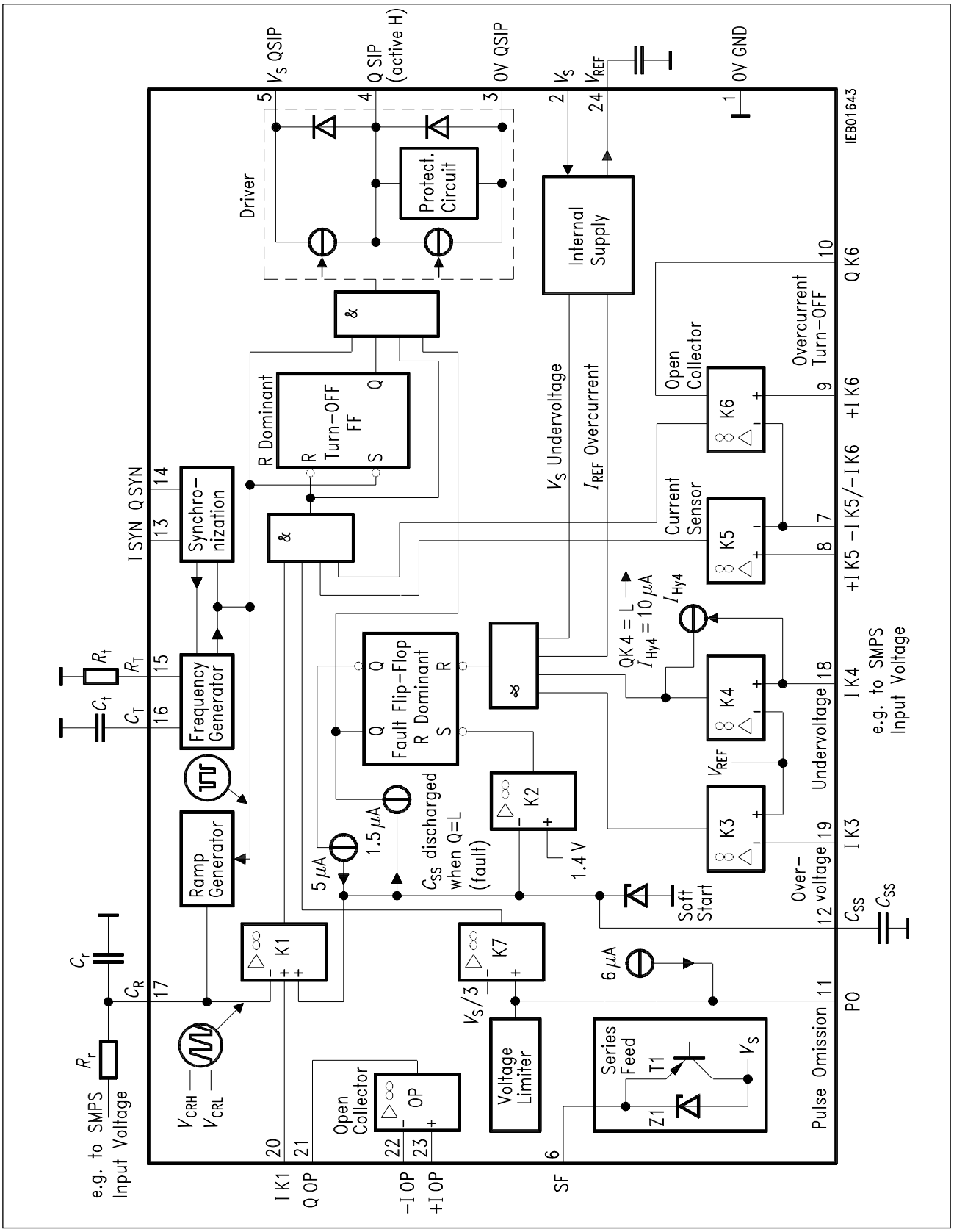


Figure 2
Block Diagram

Circuit Description

The individual functional sections of the device and their interactions are described below.

Power Supply at V_S

The device does not enable the output until the turn-ON threshold of V_S is exceeded. The duty factor (active time/period) can then rise from zero to the value set with K1 in the time determined by the soft start. The turn-OFF threshold lies below the turn-ON threshold. Below the turn-OFF threshold the output Q SIP is reliably low.

Frequency Generator

The frequency is mainly determined by close-tolerance external components and the calibrated reference voltage.

The switching frequency at the output can be set by suitable choice of R_t and C_t.

The maximum possible duty factor can be reduced by a defined amount by means of a resistor from C_T to 0V GND. The maximum possible duty factor can be increased by a defined amount by means of a resistor from C_T to V_S.

Ramp Generator

The ramp generator is controlled by the frequency generator and operates with the same frequency. Capacitor C_r on the ramp generator is discharged by an internally-set current and charged via a current set externally. The duration of the falling edge of the ramp generator output must be shorter than its rise time. Only then do the upper and lower switching levels of the ramp generator signal have their nominal values.

In “voltage mode control” operation, the rising edge of the ramp generator signal is compared with an externally set dc voltage in comparator K1 for pulse-width control at the output. The slope of the rising edge is set by the current through R_r. The voltage source connected to R_r can be the SMPS input voltage. This makes it possible to control the duty factor for a constant volt-second product at the output. This control option (precontrol) permits equalization of known disturbances (e.g. input voltage ripple).

Superimposed load current control (current mode control) can also be implemented. For this purpose the actual current at the source of the SIPMOS transistor is sensed and compared with the specified value in comparator K5.

Comparator K1 (duty factor setting for voltage mode control)

The two plus inputs of the comparator are so connected that the lower plus level is always compared with the minus input level. As soon as the voltage of the rising edge of the sawtooth (minus input) exceeds the lower of the two plus input levels, the output is inhibited via the turn-OFF Flip-Flop, that is to say the High time of the output can be continuously varied. Since the frequency remains constant, this corresponds to a duty factor change.

Comparator K2

The comparator has a switching threshold at 1.5 V. Its output sets the fault Flip-Flop when the voltage on capacitor C_a lies below 1.5 V. However, the fault Flip-Flop accepts the setting pulse only if no reset pulse (fault) is applied. This prevents resetting of the output as long as a fault signal is present.

Comparators K3 (overvoltage), K4 (undervoltage), V_S Undervoltage, V_{REF} Overcurrent

These are fault detectors which cause the output to be inhibited immediately by the fault Flip-Flop when faults occur. When faults are no longer present, the duty factor is reestablished via the soft start C_{SS}. In the event of undervoltage, a current is injected at the input of K4 with the aid of which an adjustable hysteresis or latching is made possible. The value of the hysteresis is determined by the internal resistance of the external drive source and the current injected internally at the input of K4. In the event of undervoltage at K4, the injected current flows into the device.

Comparator K5 (duty factor setting for current mode control)

K5 is used to sense the source current at the switching transistor. The plus input of the comparator is fed out. Enabling of output Q SIP after cessation of the fault is effected with an H signal at the turn-OFF Flip-Flop output.

Comparator K6 (overcurrent turn-OFF)

The turn-OFF Flip-Flop is reset when overcurrent is detected by K6. In combination with the pulse-omission facility, individual pulses can then be omitted. This then results in a limited rise in the output current with a rising overload at the output.

Operational Amplifier OP

Opamp OP is a high-quality operational amplifier. It can be used in the control circuit to transfer the variations in the voltage to be regulated in amplified form to the free plus input of comparator K1. As a result, a voltage change is converted into a duty factor change. The output of OP is an open collector. The frequency response of OP is already corrected. The plus input is connected internally via a capacitor to ground. This gives the inverting amplifier a more favorable phase response.

Turn-OFF Flip-Flop AFF

A pulse is fed to the set input of the turn-OFF Flip-Flop with the falling edge of the frequency generator signal. However, it can only really be set if no reset signal is applied. With a set turn-OFF Flip-Flop, the output is enabled and can be active. The Flip-Flop inhibits the output in the event of a turn-OFF signal from K1, K5, K6 or K7.

Fault Flip-Flop

Fault signals fed to the reset input of the fault Flip-Flop cause the output to be immediately disabled (Low), and to be turned on again via the soft start C_{SS} after removing fault-condition.

Soft Start C_{SS}

The smaller of the two voltages at the plus inputs of K1 - compared with the ramp generator voltage - is a measure of the duty factor at the output. At the instant the device is turned-ON, the voltage on capacitor C_{SS} equals zero. Provided no fault exists, the capacitor is charged up to its maximum value.

C_{SS} is discharged in the event of a fault. However, the fault Flip-Flop inhibits the output immediately. Below a charging voltage of approx. 1.5 V, a set signal is applied to the fault Flip-Flop and the output is enabled, provided a reset signal is not applied simultaneously. However, since the minimum ramp generator voltage is about 1.8 V, the duty factor at the output is not actually slowly and continuously increased until the voltage on C_{SS} exceeds a value of 1.8 V.

The Z-diode limits the voltage on capacitor C_{SS}. The voltage at the ramp generator can reach a higher level than the Zener voltage. With a suitable ramp generator rising edge slope, the duty factor can be limited to a wanted maximum value.

Pulse Omission PO

In the event of overcurrent in the SIPMOS transistors it is frequently necessary to omit pulses even with minimum duty factor. Only this measure ensures that the SIPMOS transistors cannot be overloaded. This wanted function can be achieved with Pulse Omission PO and Overcurrent Comparator K7 by means of a suitable external circuit.

Reference Voltage V_{REF}

The reference voltage source makes available a source with a high-stability temperature characteristic which can be used for external connection to the operational amplifier, the fault comparators, the frequency generator, or to other external units. The voltage source is short-circuit-proof to ground.

Synchronization I SYN, Q SYN

The device has an input and an output for synchronization. In the case of a synchronized device (slave), its output Q SIP is in phase opposition to the output Q SIP of the synchronizing device (master). In the case of an unconnected input I SYN, or with connection to V_{REF}, or also when a series capacitor (without switching transitions) is connected, the device receives its clock from the internal frequency generator in accordance with the circuit connected to it. As soon as switching transitions appear at I SYN, switchover to external synchronization and vice versa takes place after a delay. After a switchover process, a few clock cycles must elapse in addition to the delay before the frequency and phase achieve their steady states.

Series Feed SF

The Series Feed circuit section is used to turn-OFF the external series-feed transistor when energy recovery commences. As a result there is minimum power loss in the supply to the device. With the series-feed transistor turned-OFF, its drive current flows via VS to V_S.

SIPMOS Driver Output Q SIP

The output is High active. The time during which the output is active can be continuously varied.

The duration of the rising edge of the frequency generator signal is the minimum time during which the output can be Low.

The duration of the falling edge of the frequency generator signal is the maximum time during which the output can be High.

The output driver is designed as a push-pull stage. The output current is limited internally to the specified values.

Output Q SIP is connected via diodes to the supply V_S QSIP and 0V QSIP.

A protection circuit SS lies between Q SIP and GND to clamp the output to ground at low impedance in the event of undervoltage at V_S.

When the supply to the switch-mode power supply is switched on, the capacitive displacement current from the gate of the SIPMOS transistor is conducted to the smoothing capacitor at V_S QSIP by the diode connected to V_S QSIP. The voltage at V_S QSIP may reach about 2.3 V in the process without the SIPMOS transistor being turned-ON.

The diode connected to ground clamps negative voltages at Q SIP to minus 0.7 V. Capacitive currents which occur with voltage dips at the drain terminal of the SIPMOS transistor can then flow away unimpeded.

The output is active Low with supply voltages at V_S and V_S QSIP from about 4 V on. The function of the diode connected to V_S QSIP and the resistor are then taken over by the pull-down source.

The two ground terminals 0V SQIP and 0V GND can lie at different levels. This permits connections to be made to the SIPMOS transistor in such a way that the drive currents for the gate do not flow to the source via the current-sensing resistor. The maximum permissible level differences between 0V GND and 0V SQIP are given under Functional Range. If greater level differences are anticipated, it is better to join the two terminals.

Absolute Maximum Ratings

T_A = – 40 to 85 °C

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply voltage; V_S,$V_{S\ QSIP}$	V_S,$V_{VS\ QSIP}$	– 0.3	17	V	
I OP, I K1, I K3, I K4, I K5, I K6,	V_I	– 0.3	17	V	
I SYN	$V_{I\ SYN}$	0	5	V	
	$I_{I\ SYN}$	– 3	3	mA	$V_{I\ SYN}$ > 5 V or $V_{I\ SYN}$ < 0 V
Q SYN	$V_{Q\ SYN}$	– 0.3	5	V	
Frequency Generator; C_T, R_T	$V_{CT,\ RT}$	– 0.3	5	V	
	$I_{CT,\ RT}$	0	3	mA	V_{CT} > 5 V
Ramp Generator; C_R	V_{CR}	– 0.3	V_{CRH}	V	V_{CRH} (see charact.)
	I_{CR}	0	3	mA	V_{CR} > V_{CRH}
Reference voltage; V_{REF}	V_{REF}	– 0.3	6	V	
	I_{REF}	– 10	10	mA	V_{REF} > 6 V or V_{REF} < – 0.3 V
Output Opamp; Q OP					
Inhibited	$V_{Q\ OP}$	– 0.3	17	V	
Conducting	$I_{Q\ OP}$	0	5	mA	
Output Overcurrent Turn-OFF; Q K6					
Inhibited	$V_{Q\ K6}$	– 0.3	17	V	
Conducting	$I_{Q\ K6}$	0	5	mA	
Driver output; Q SIP	$V_{Q\ SIP}$	– 0.3	V_S	V	1)
Q SIP clamping diodes	$I_{Q\ SIP}$	– 10	10	mA	$V_{Q\ SIP}$ > V_S or $V_{Q\ SIP}$ < – 0.3 V
Soft start; C_{SS}	V_{CSS}	– 0.3	V_{SSH}	V	V_{SSH} (see charact.)
	I_{CSS}	0	100	µA	V_{SS} > V_{SSH}
Pulse omission; PO	V_{PO}	– 0.3	V_{POH}	V	V_{POH} (see charact.)
	I_{PO}	0	3	mA	V_{PO} > V_{POH}
Series feed; SF	V_{SF}	– 0.3	17	V	
Junction temperature	T_j	– 65	150	°C	
Storage temperature	T_s	– 65	150	°C	
Thermal resistance system - ambient	$R_{th\ S/A}$		60	K/W	

The values refer to the two connected ground terminals.
1) Important: observe max. power loss or junction temperature.

Operating Range

Function	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	V_S $V_{VS\ QSIP}$	0 0	15 15	V V
Frequency generator	f	0.05	400	kHz
Ramp generator	f	0.05	400	kHz
Ambient temperature	T_A	– 40	+ 100	°C
Ground Q SIP	$V_{0V\ QSIP}$	GND – 300 mV	GND + 2 V	V
Resistor at R_T	R_{RT}	27	1000	kΩ

Characteristics

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current in V_S	I_{VS}			7 8 8 9	mA[1)] mA[1)] mA[1)] mA[1)]	FG at 100 kHz FG at 300 kHz Q SYN unconnected FG at 100 kHz FG at 300 kHz Q SYN to 0V GND
Current in V_S QSIP	$I_{VS\ QSIP}$		2.5 5.5		mA[1)] mA[1)]	FG at 100 kHz FG at 300 kHz
Current in $V_S + V_S$ QSIP	I_{Sum}			9 13 10 14	mA[1)] mA[1)] mA[1)] mA[1)]	FG at 100 kHz FG at 300 kHz Q SYN unconnected FG at 100 kHz FG at 300 kHz Q SYN to 0 V GND

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Drain[2]						
Hysteresis at V_S						
Turn-ON threshold for V_S rising	V_{SH}	8.0	9.1	10	V	
Turn-OFF threshold for V_S falling	V_{SL}	7.9	9.0	9.9	V	

[1] C_T; R_T (see oscillator nomogram).
[2] The currents as V_S and V_S QSIP are in each case without loads and without internal discharge to C_R, as well as with active output Q SIP.

Reference Voltage

Voltage	V_{REF}	2.460	2.500	2.540	V	I_{REF} = 250 µA; V_S = 12 V
Load current	$-I_{REF}$	0		3	mA	ΔV_{REF} < 30 mV
Voltage change	ΔV_{REF}			5	mV	0 mA < I_{REF} < 500 µA
Voltage change	ΔV_{REF}			3	mV	12 V < V_S < 14 V
Temperature response	$\Delta V_{REF}/\Delta T$		0.1		mV/K	
Operate threshold V_{REF} overcurrent	$-I_{REFO}$	3	6	10	mA	

Frequency Generator

Nominal frequency spread	$\Delta f_F/f_O$	– 4		4	%	20 kHz < f_O < 150 kHz; Q SYN to GND; V_S = 12 V; T_A = 25 °C
Voltage dependence of nominal frequency	$\Delta f_V/f_O$	– 1		1	%	10 V < V_S < 14.4 V; T_A = 25 °C; relative to f_O at 12 V; 20 kHz < f_O < 150 kHz

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Temperature-dependence of nominal frequency	$\Delta f_\tau/f_O$	– 3		3	%	-25 °C $< T_A <$ + 85 °C; V_S = 12 V; relative to f_O at 25 °C; 20 kHz $< f_O <$ 150 kHz
Nominal frequency	f_{20150}	0.92 f_O	f_O	1.08 f_O	kHz[1]	20 kHz to 150 kHz
Nominal frequency	f_{150250}	0.88 f_O	f_O	1.12 f_O	kHz[1),2)]	150 kHz to 250 kHz
Nominal frequency	f_{250300}	0.85 f_O	f_O	1.15 f_O	kHz[1),2)]	250 kHz to 300 kHz
Maximum duty cycle	ν_{20150}	48		52	%[2)]	20 kHz to 150 kHz
Maximum duty cycle	ν_{150200}	46		54	%[2)]	150 kHz to 250 kHz
Maximum duty cycle	ν_{250300}	44		56	%[2)]	250 kHz to 300 kHz

Ramp Generator

Frequency range	f	0.05		300	kHz	
Maximum voltage at C_R	V_{CRH}	4.8	5.8	6.8	V	
Minimum voltage at C_R	V_{CRL}	1.4	1.8	2.2	V	
Discharge current at C_R	I_{dis}	0.75	1.00	1.25	mA	internally fixed
Capacitance at C_R	C_R	10			pF	
ON-time spread (limited by C_{SS})	$\Delta t_{Ot}/t_{Ot}$	– 9		9	%	C_r = 200 pF; $V_{IK1} > V_{SSH}$; I_{Rr} = 150 µA; T_A = 25 °C; relative to t_{Ot} = 4.0 µs

[1] C_T; R_T (see oscillator nomogram).
[2] See diagram: Tolerance of oscillator frequency, duty cycle.

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
ON-time drift	$\Delta t_{Ot}/t_{Ot}$	– 2		2	%	C_r = 200 pF; $V_{IK1} > V_{CAH}$; I_{Rr} = 150 µA; relative to t_{Ot} = 25 °C
ON-time spread	t_{Ot}	3.6	4.0	4.4	µs	C_r = 200 pF; $V_{IK1} > V_{CAH}$; I_{Rr} = 150 µA
Operational Amplifier OP						
Open-loop gain	G_o	60	80	100	dB	$I_{Q\,OP}$ = 100 µA
Input offset voltage	V_{io}	– 5		+ 5	mV	$I_{Q\,OP}$ = 100 µA
Input current	$-I_i$			1	µA	
Input common-mode range	V_{cm}	– 0.2		4	V	
Output current	$I_{Q\,OP}$	– 3			mA	0.5 < $V_{Q\,OP}$ < 15 V
Output voltage	$V_{Q\,OP}$	0.5		15	V	0 mA < $I_{Q\,OP}$ < 2 mA
Transit frequency	f_t	2	5	8	MHz	
Transit phase	ϕ_t	90	120	150	Deg.	
Temp. coeff. of V_{io}	T_c	– 10		+ 10	µV/K	
Rate of rise of voltage at output	$\Delta V/\Delta t$	1	± 3	6	V/µs	$I_{Q\,OP}$ = 100 µA
Comparator K1						
Input current	$-I_{K1}$			1	µA	
Input common-mode range	V_{cm}	0		V_{CAH}	V	
Turn-OFF delay	t_{OFF}		200	400	ns[1)]	Nominal load 1 nF at Q SIP

[1)] Step function ΔV – 100 mV ⌐→ ΔV + 100 mV (for delay from comparator input to Q SIP).

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overvoltage K3						
Input current	$-I_i$			0.2	µA	
Switching voltage	V_{SW}	V_{REF} – 5 mV		V_{REF} + 5 mV	V	
Turn-OFF delay	t_{OFF}	1	2	4	µs	
Undervoltage K4						
Input current at K4	$-I_i$			0.2	µA	
Switching voltage at K4	V_{SW}	V_{REF} – 5 mV		V_{REF} + 5 mV	V	
Hysteresis current	I_{hy4H} I_{hy4L}	5	10	15 0.1	µA µA	$V_{+\,IK4} < V_{sw}$ $V_{+\,IK4} > V_{sw}$
Turn-OFF delay	t_o	1	2	4	µs[1]	
Current Sensor K5; Overcurrent Turn-OFF K6						
Input current	$-I_{dyn}$			1	µA	
Input offset voltage	V_{io}	– 5		+ 5	mV	
Input common-mode range	V_{cm}	0		4	V	
Turn-OFF delay	t_{OFF}		150 250	300 400	ns[2] ns[3]	Load 1 nF at Q SIP
Output K6 inhibited	I_{QK6}			2	µA	V_{QK6} = 5 V
Conducting	V_{QK6}			1.2	V	I_{QK6} = 1 mA

[1] Step function V_{REF} – 100 mV $\rightarrow$ V_{REF} + 100 mV (for delay from comparator input to Q SIP).
[2] Step function ΔV – 100 mV $\rightarrow$ ΔV + 100 mV (for delay from comparator input to Q SIP).
[3] Step function ΔV – 10 mV $\rightarrow$ ΔV + 10 mV (for delay from comparator input to Q SIP).

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft Start C_{SS}						
Charging current at C_{SS}	$-I_{ch}$	4	5	8	µA	
Discharge current at C_{SS}	I_{dis}	0.8	1.5	3.0	µA	
Upper clamping voltage	V_{SSH}	4.4	4.8	5.2	V	
Difference $V_{CRH} - V_{SSH}$	V_{DSS}	0.1			V	$V_{CRH} - V_{SSH}$
Switching voltage of K2	V_{K2}	1.1	1.4	1.7	V	
Pulse Omission PO						
Charging current at PO int.	$-I_{ch}$	4	6	9	µA	
Charging current at PO ext.	I_{ch}			1	mA	
Voltage at – K7	V_{-K7}	$V_S/3$ – 5 %	$V_S/3$	$V_S/3$ + 5 %	V	
Upper clamping voltage at + K7	V_{POH}	V_{-K7} + 0.2	V_{-K7} + 0.7	V_{-K7} + 1.2	V	0 mA $< I_{PO} <$ 1 mA
Minimum voltage applied to PO	V_{POM}	1			V	
Synchronization						
Input I SYN	$I_{I\,SYN}$	– 70		200	µA	0 V$< V_{I\,SYN} <$ 4.5 V
Switching threshold at I SYN Open Rising edge Falling edge	 $V_{I\,SYNO}$ $V_{I\,SYNR}$ $V_{I\,SYNF}$	 1.5 2.5 1.0	 2.7 3.4 2.0	 3.5 4.0 3.0	 V V V	

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Switchover delay int. free-running - synchronized	$t_{df\text{-}s}$	15	35	60	µs	
synchronized - free-running	$t_{ds\text{-}f}$	9	18	35	µs	
Limiting diodes	$-I_{I\,SYN}$ $I_{I\,SYN}$	0 0		2 2	mA mA	$V_{I\,SYN} < 1$ V $V_{I\,SYN} > 5$ V
Output Q SYN High	$V_{Q\,SYNH}$	4.1			V	-500 µA $< I_{Q\,SYN} < 0$ µA
Low	$V_{Q\,SYNL}$			0.6	V	0 µA$< I_{Q\,SYN} <$ 500 µA
Fan-out of Q SYN for control I SYN		2				Q SYN to 0V GND allowed

Series Feed

Series Feed Threshold at V_S	V_{SFTH}	9.0	10.0	10.5	V	$I_{SF} > 5$ µA; $V_{SF} = 13$ V
V_{SH} to V_{SFTH} Gap	V_{SFGAP}	500	–	–	mV	
Maximum current	$I_{SF\,max}$	500	–	–	µA	$V_S = 11.5$ V; $V_{SF} = 12.5$ V
Voltage at Z1	V_{Z11}	5	–	–	V	$I_{Z1} = 20$ µA; $0 \le V_S \le 8$ V
Voltage at Z1	V_{Z12}	–	–	8	V	$I_{Z1} = 500$ µA $0 \le V_S \le 8$ V

Output Driver Q SIP

Saturation voltage source	$V_{Q\,SIPH}$ $V_{Q\,SIPH}$ $V_{Q\,SIPH}$		1.8 2.2 2.5	2.0 2.5 3.0	V V V	$I_{Q\,SIP} = 0$ mA $I_{Q\,SIP} = -1$ mA $I_{Q\,SIP} = -200$ mA $V_S = V_{Q\,SIP} > V_{Son}$
Saturation voltage sink	$V_{Q\,SIPL}$ $V_{Q\,SIPL}$		0.1 1.7	0.5 2.2	V V	$I_{Q\,SIP} = 10$ mA $I_{Q\,SIP} = 200$ mA $V_S = V_{Q\,SIP} > V_{Son}$

Characteristics (cont'd)

$V_{Son} < V_S < 15$ V, -25 °C $< T_A <$ 85 °C; V_{Son} means that V_S has exceeded V_{SH}, but has not gone below V_{SL}.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Saturation voltage sink	$V_{Q\,SIPP}$			1.5	V	$I_{Q\,SIP}$ = + 5 mA IC passive
Output current Falling edge Rising edge	 $I_{Q\,SIP}$ $-I_{Q\,SIP}$	 0.7 0.7	 1.0 1.0	 1.5 1.5	 A[1] A[1]	 $C_{Q\,SIP}$ = 10 nF; $V_S = V_{Q\,SIP}$ = 12 V $C_{Q\,SIP}$ = 10 nF; $V_S = V_{Q\,SIP}$ = 12 V
Output voltage Fall time Rise time	 $t_{Q\,SIPF}$ $t_{Q\,SIPR}$			 200 200	 ns[2] ns[2]	 $C_{Q\,SIP}$ = 10 nF; $V_S = V_{Q\,SIP}$ = 12 V $C_{Q\,SIP}$ = 10 nF; $V_S = V_{Q\,SIP}$ = 12 V

[1] Maximum dynamic current during rising or falling edge.
[2] Voltage level 10 %/90 %.

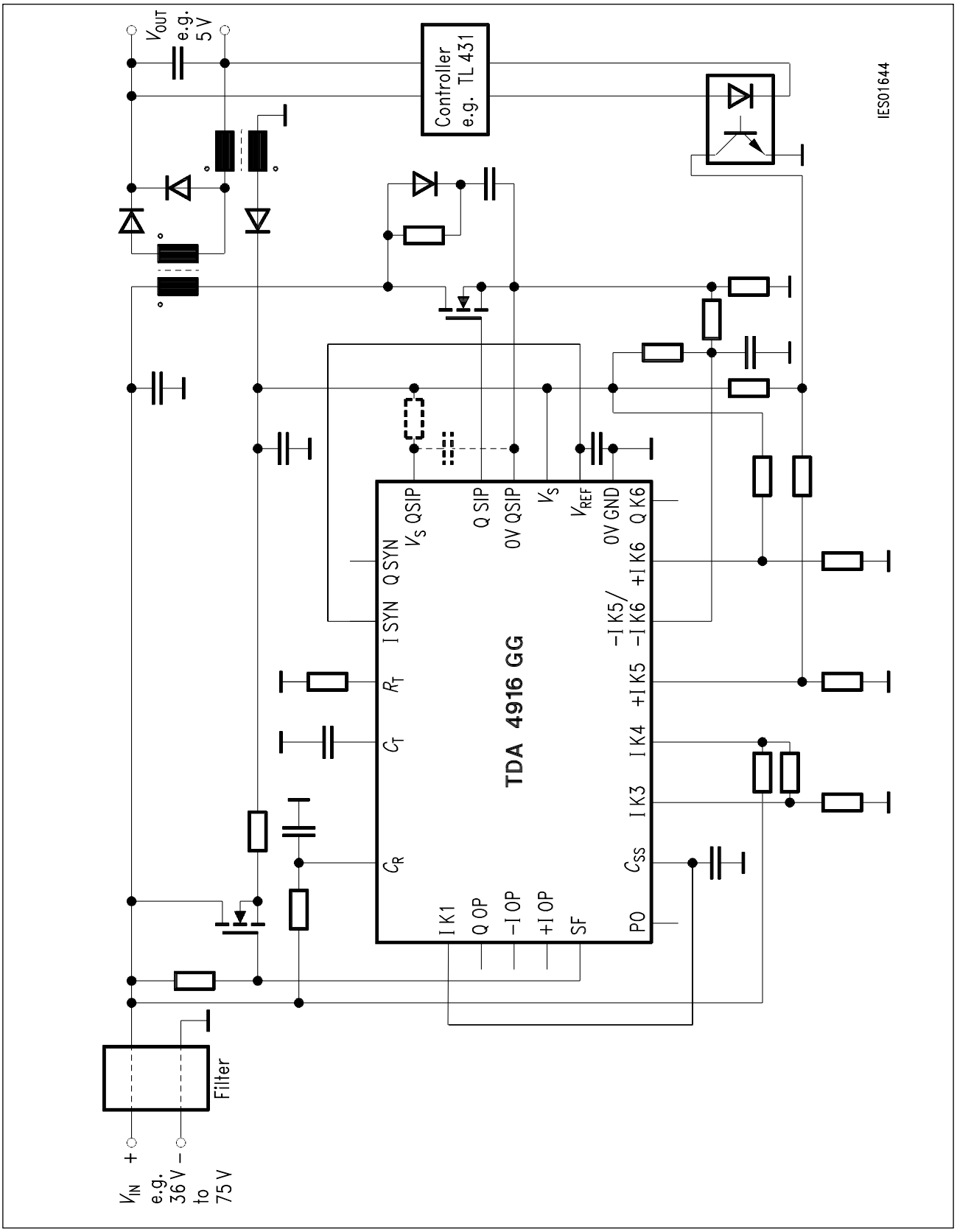


Figure 3
Application Circuit 1: Forward Converter with Output Regulation

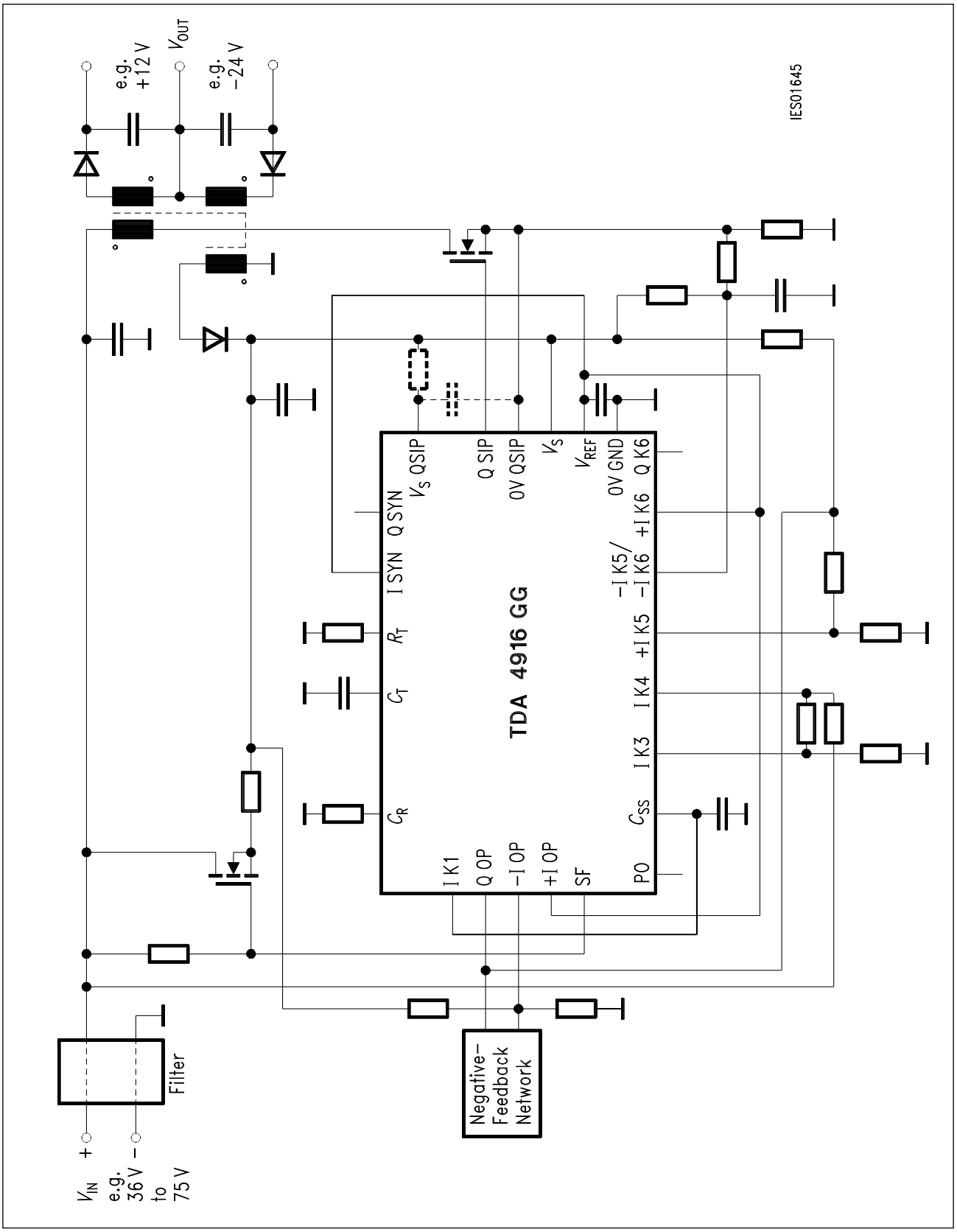


Figure 4
Application Circuit 2: Flyback Converter with EMF Regulation

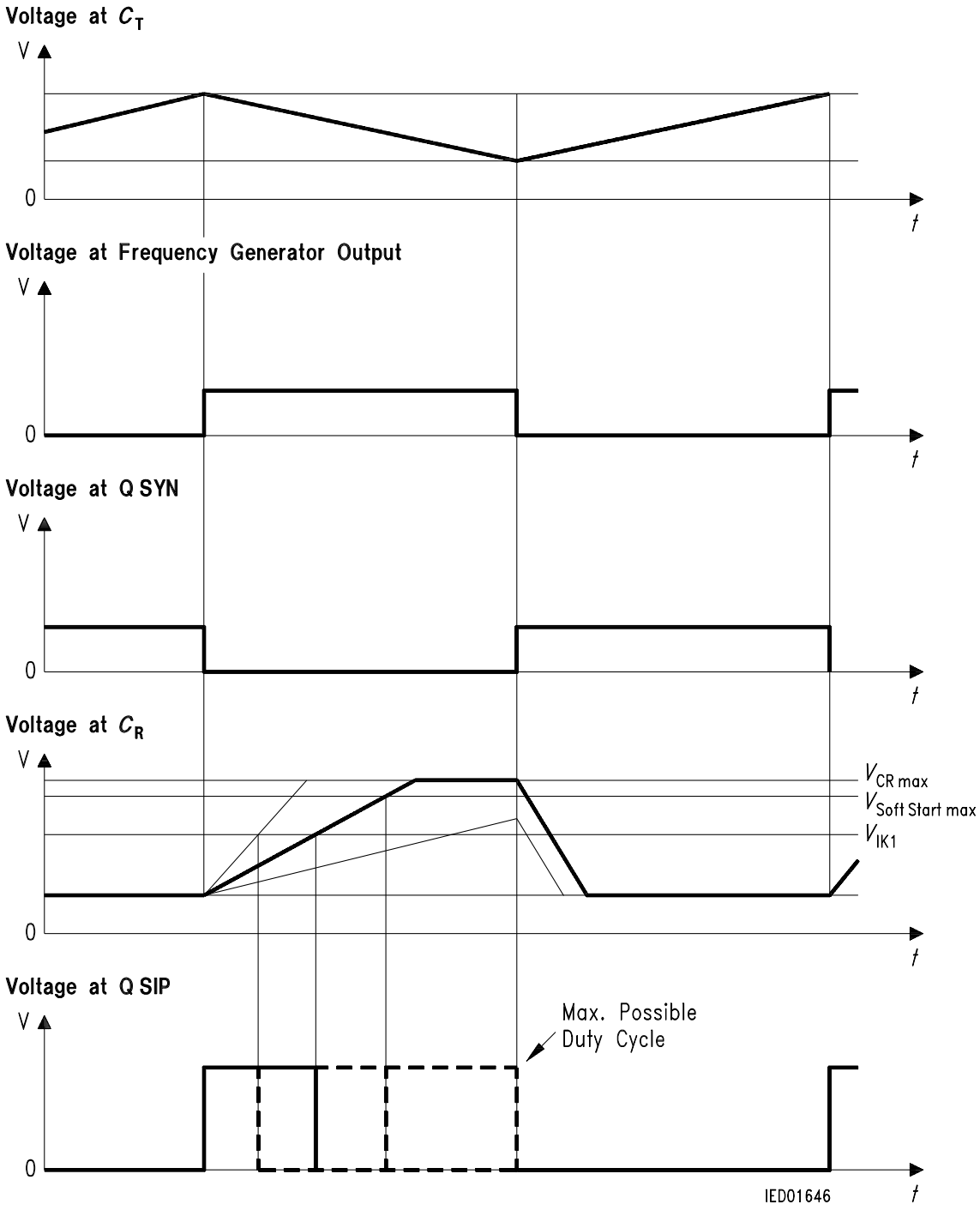


Figure 5
Timing Diagram

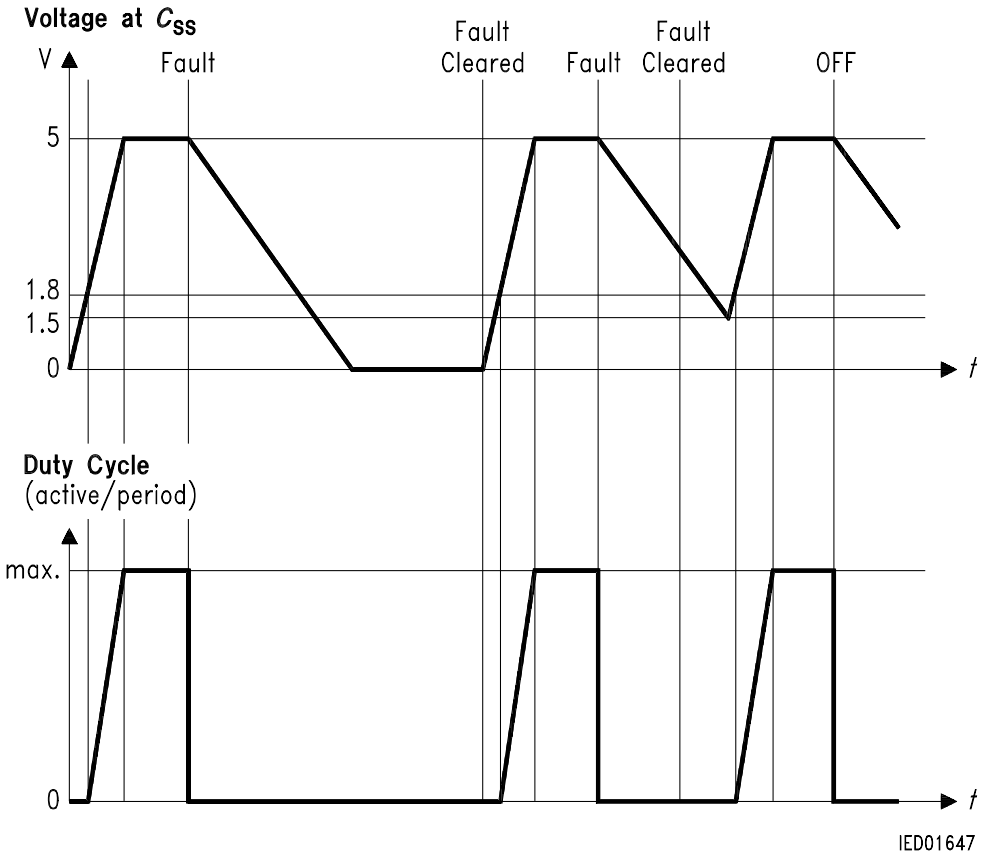


Figure 6
Soft Start C_{SS} / Fault/ON - OFF

Nomogram for FG

f_o = 97.5 kHz @ T_j = 25 °C; R_T = 40.2 kΩ; C_T = 560 pF