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V1.1 June 2012

TDA5150

Multichannel / Multiband Transmitter

Multichannel / Multiband RF Transmitter for 300-928 MHz bands

On-chip, high resolution fractional-N synthesizer and
Sigma-Delta modulator with ASK, FSK, GFSK options

Wireless Control

Never stop thinking.

Edition June 2012

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TDA5150
Revision History: **V1.1**

Previous Version:	**V1.0** issued July 2009
433 MHz band lower limit changed	433 MHz frequency band lower limit (min), referred in several paragraphs changed from previous value of **425** MHz to **433** MHz, recent value
Chapter 2.4.5	Detailed explanations about avoidance of fractional spurs added to **Crystal Oscillator and Clock Divider** subchapter
Chapter 2.4.11.2	Detailed description of chip-internal synchronization mechanism added to **Synchronous Transmission** subchapter
Table 4 four individual bits in synthesizer register bank (SFRs) reassigned to *reserved* class	Four bits (previously referenced as FRACCOMPx) reassigned to **reserved** class. **Notes**: *1. The affected bits are 0x0C.5 0x10.5 0x14.5 and 0x18.5* *2. The change has no impact on chip functionality* *3. After-reset state of all four above mentioned bits is 0 (i.e. no change versus previous Datasheet V1.0)*
Description of Evaluation Board V2 added to **Chapter 3.2**	Description of **Evaluation Board V2** added, see **Infineon Evaluation Board V2** Description of former board version moved to subchapter **Schematics of Infineon Evaluation board V1.1**
Values in **Table "PLLBW TRIM" on Page 84** and associated ***Note*** on same page updated in accordance with the PLL settings listed in **Table 2**	Range of nominal PLL Bandwidth values (PLLBW) Listed in **Datasheet V1.0** 90 120 150 180 210 240 270 [kHz] Listed in **Datasheet V1.1** 150 175 230 270 335 375 410 [kHz] by chargepump current of 5 7.5 12.5 17.5 25 32.5 40 [µA] *Note:* *1. chargepump current values are unchanged and the same in both Datasheets.* *2. no changes operated in **Table 2** regarding the PLL bandwidth or chargepump current settings.*
Data regarding load drive capability of **SDIO** pin added	Data regarding load drive capability of **SDIO** pin added to **Table 13**

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1 Product Description

1.1 Overview

The TDA5150 is a low cost, multi-channel ASK/FSK/GFSK RF transmitter for the 300-320 MHz, 433-450 MHz, 863-928 MHz frequency bands with low power consumption and programmable RF-output power of up to +10 dBm. Radio systems built around this transmitter are easy to be designed and to be implemented.

The IC offers a high level of integration and needs only a few external components, such as a crystal, blocking capacitors and the necessary matching elements between the power amplifier output and the antenna.

An integrated high-resolution fractional-N PLL synthesizer interconnected with a sigma-delta modulator covers all of the above listed frequency bands, using the same crystal for reference frequency and Baud-rate generation.

All the major functions of the chip are controlled over SFR registers, which at their turn are accessible over a 3-wire SPI bus (Serial Peripheral Interface).

The user-configurable digital modulator allows precise settings of FSK modulation parameters and Gaussian shaping (GFSK), which directly contributes to reduction of occupied bandwidth and efficient spectrum usage.

The output power of the integrated C-class RF power amplifier is controlled over SFR registers and if necessary, the power can be downsized (reduced) in digital steps. The ASK shaping option contributes to reduced harmonics and minimized spectral splatter.

On-chip antenna tuning capacitors are available, the capacitor bank switching (for antenna tuning) is accomplished over SFR registers.

The data encoder supports NRZ, Manchester, Bi-Phase, and Miller encoding.

1.2 Features

- High resolution Sigma-Delta fractional-N PLL synthesizer (frequency step size down to 7 Hz)
- Multiband/Multichannel capability for the 300-320 MHz, 433-450 MHz and 863-928 MHz bands
- Modulation types ASK (OOK) with ASK shaping, FSK (CPFSK) and GFSK
- Multi-channel and channel hopping capability, 4 register banks for fast Tx frequency switching
- Configurable via 3-wire serial interface bus (SPI)
- Manchester, Bi-Phase, and Miller encoding, on-chip PRBS9 scrambler
- Continuous checking of chip status by Fail-Safe mechanism
- Transparent and synchronized RF modulation mode
- Programmable clock divider output
- Configurable output power level from -10 dBm to +10 dBm, in 2 dB nominal steps
- Supply voltage range 1.9 V - 3.6 V, 2 low battery detection thresholds, preset to 2.4 V and 2.1 V
- Low supply current (Sleep Mode < 0.8 µA, RF transmission 9 mA @ +5 dBm)
- ESD protection up to $\pm$ 4 kV at all pins
- Operating temperature range -40° C to +85° C
- Green Package TSSOP-10

1.3 Applications

- Short range wireless data transmission
- Remote keyless entry transmitters
- Remote control units
- Wireless alarm systems
- Remote metering
- Garage door openers

1.4 Order Information

Type	Ordering Code	Package
TDA5150	SP000300415	PG-TSSOP-10

1.5 Key Features overview

1.5.1 Typical Application Circuit

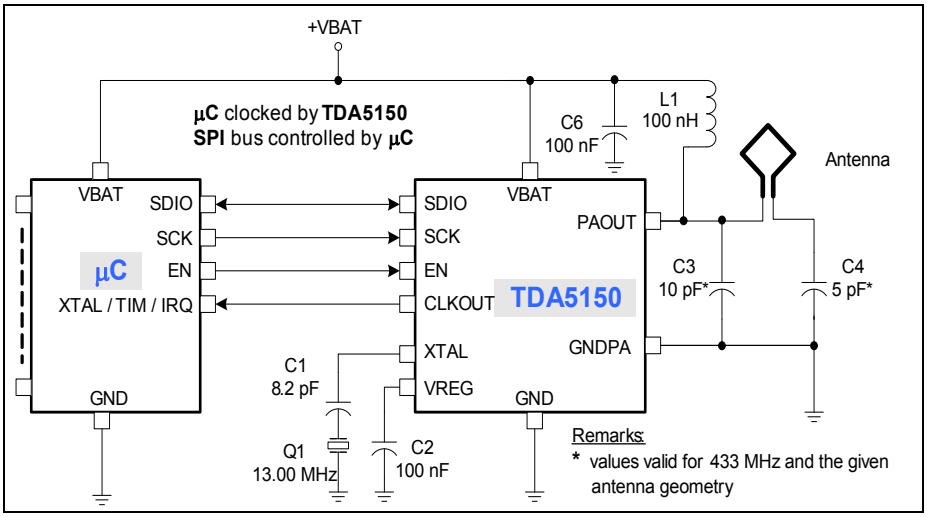


Figure 1 Minimum component count application circuit

The TDA5150 application circuit shown demonstrates the ease and simplicity of an intelligent transmitter implementation. The µC configures the TDA5150 via 3-wire SPI, the SDIO line is used at the same time to transfer data on SPI bus and as digital data input into the RF modulator. The CLKOUT line may be used as clock source for the µC or as a timer for bitrate generation.

The matching shown is an example for a loop antenna application. Different antenna types (electrical monopole or dipole, magnetic loop etc.) as well as different layout versions might require component values which can differ from those given in above example. The antenna geometry has a major influence on the antenna impedance and consequently on the component values in the matching network.

1.5.2 Sigma-Delta fractional-N PLL with High Resolution

This type of PLL offers a multitude of advantages compared to fixed, integer division ratio PLLs.

In the reference oscillator circuit the same crystal can be used for all of the RF bands and channel frequencies (for example 13 MHz and alternatively 13.56 MHz crystals are listed in the Evaluation Board descriptions **Chapter 3.2 Infineon Evaluation Board V2** and **Chapter 3.3 Infineon Evaluation board V1.1** for all versions, independently of intended operating frequency band).

Thus dedicated crystals for each carrier frequency (like by integer-N type synthesizers) are no longer required, and this is a significant advantage for systems based on the TDA5150 transmitter chip.

However by choice of crystal frequency the phenomenon known as occurrence of fractional-N spurs, shall be considered and the reference frequency selected in such way, to avoid it. The phenomenon and the countermeasures which should be taken are described in detail in **Chapter 2.4.6.1 Fractional Spurs**.

The PLL allows a direct and highly accurate (G)FSK digital modulation. This leads to reduction of spurs and harmonics versus performance of legacy transmitters, devices which are mainly using crystal frequency pulling in order to achieve FSK modulation.

Synthesizer resolution down to 7 Hz for carrier frequency generation makes possible accurate adjustments and fine tuning. It allows at least the partial correction and reduction of inherent frequency tolerances, which are due to crystal manufacturing process.

In the same way it is possible to cancel the effects of temperature dependent frequency drift (introduced by the crystal used for reference frequency generation) and a temperature-dependent retune process could be applied, by means of small frequency steps, at the carrier frequency level.

Note: the correction of the temperature related frequency drift (caused by the quartz crystal) assumes the availability of a temperature measurement sensor in the host system.

1.5.3 Reduction of Spurs and Occupied Bandwidth

The direct FSK modulation and in addition the Gaussian FSK (GFSK) reduces spurs and occupied bandwidth. Bandwidth reduction is exemplified below.

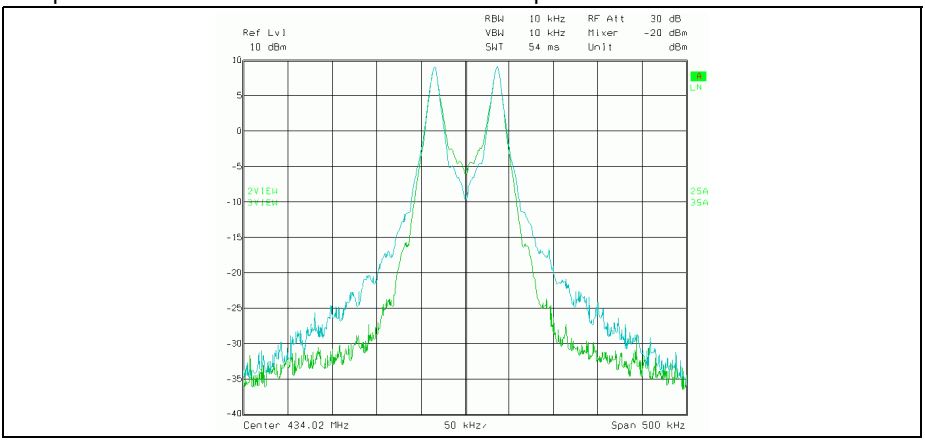


Figure 2 Spectrum of RF-signals with equal frequency deviations (± 35kHz), same 20 kBit/s datarate and encoding (NRZ). Blue plot corresponds to FSK modulation and green to GFSK. Observe the difference in terms of occupied bandwidth between the signals.

1.5.4 Asynchronous and Synchronous Transmission

TDA5150 offers a simple asynchronous transmission mode (transparent modulation), whereby after the configuration word is downloaded into the transmitter's SFRs (via SPI bus) the data bitstream is output on the SDIO line and fed into the transmitter's RF modulator.

The CLKOUT signal can be used either as clock line for host µC or, alternatively, as timer base (flag) for bitrate generator (this last function have to be implemented in the µC).

In this mode, the bitrate is solely imposed and controlled by the µC software.

GFSK modulation and ASK shaping options are allowed in Asynchronous Mode.

In Synchronous Transmission Mode the bitrate is solely under the transmitter's control and fully timed by the TDA5150. The CLKOUT is used to alert the µC about the request for next data bit.

The µC may have a higher allowable processing delay tolerance, typically the duration of 1/2 bit, before sending the corresponding bit via SDIO line to transmitter.

Usage of data encoding option is allowed in Synchronous Mode.

1.5.5 Integrated Data Encoder

TDA5150 comprises a Data Encoder which automatically generates encoded data from a regular (NRZ) bitstream. The supported data encoding modes are:

- Manchester code
- Differential Manchester code
- Bi-phase space code
- Bi-phase mark code
- Miller code (Delay modulation)
- NRZ
- Scrambling (PRBS9 generator)

All the encoded bitstreams can be level inverted (as part of the encoding option). The scrambling module (PRBS9 generator) is intended to be used for generation of pseudo-random data patterns (rather for Tx test scopes) or for basic level data encryption.

1.5.6 Fail-Safe Mechanism

The Transmitter Status Register reports about failures such as: Brownout event, PLL lock error, VCO auto-calibration error and Register Parity error.

The Register Parity is a special safety feature. Each SFR (Special Function Register) has an extra parity bit which is automatically calculated and stored during a SFR write operation. During transmitter active state these parity bits, belonging to SFR content are continuously recalculated and compared against the stored values. Changes in the contents of writable SFRs without write command generate an SFR error event and an error flag is set.

To prevent erroneous transmissions (on wrong frequency or with erroneous modulation parameters) the activation of Fail-Safe mechanism is coupled with deactivation (switching off) of the RF Power Amplifier stages.

This additional feature inhibits the transmission if errors occur, thus preventing the transmission of erroneous datagrams or on false frequency

For details see the associated SFR description, and their interaction with the Fail-Safe Mechanism, as described in **Chapter 2.4.10**.

1.5.7 TESEUS - Configuration and Evaluation Tool

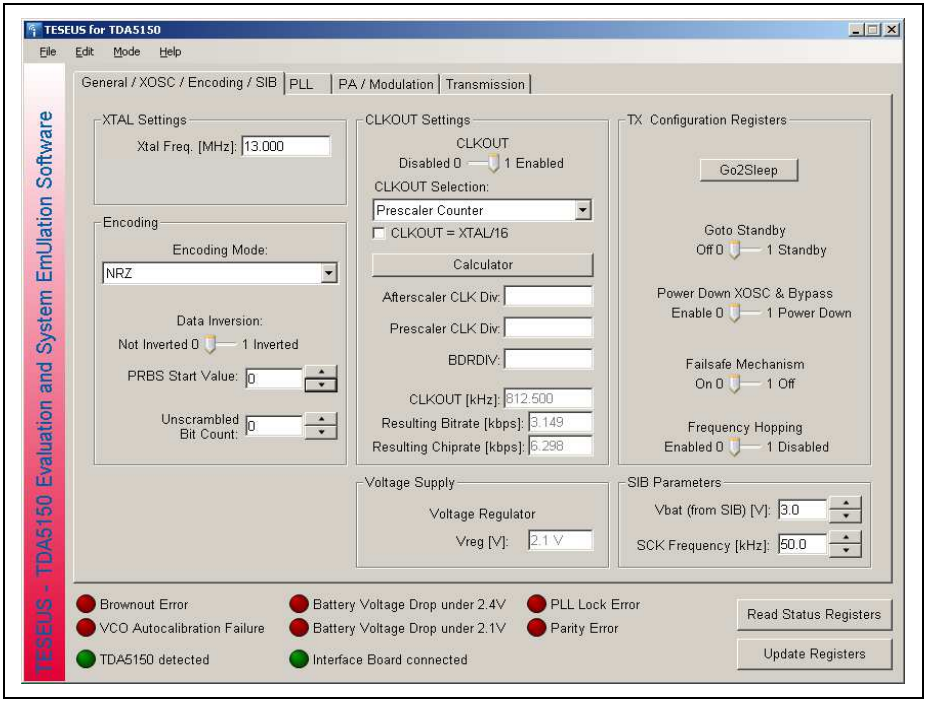


Figure 3 TESEUS - First Tab of User Interface screen

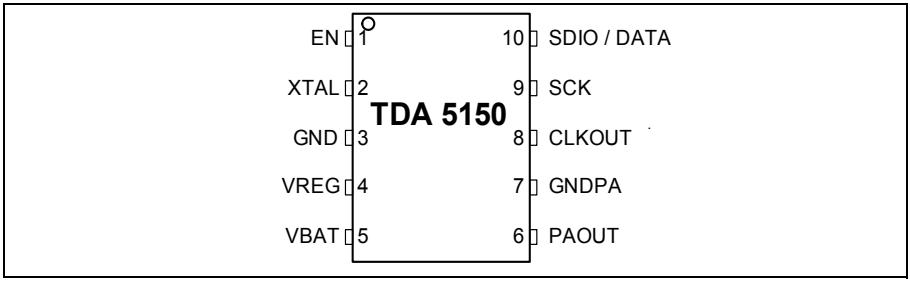
TESEUS is a user-friendly, comfortable tool, suitable for generation of TDA5150 configurations and testing them using a TDA5150 Evaluation Board. Configurations can be automatically converted into register lists and implemented in C-code.

The pattern to be transmitted is written into a datagram or TX-file. A commented example TX-file can be generated by TESEUS. This file might be edited using a standard text file editor, if changes of the transmit parameters and data patterns are required.

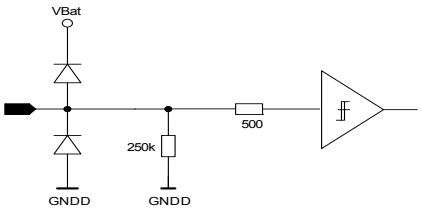
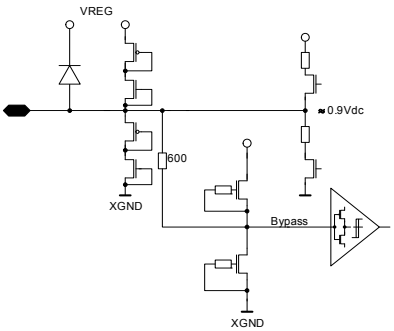
***Note:** for further details please consult the **TESEUS User's Manual** document, downloadable from Infineon Technologies AG web-page, free of charge.*

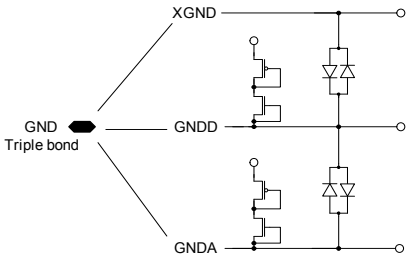
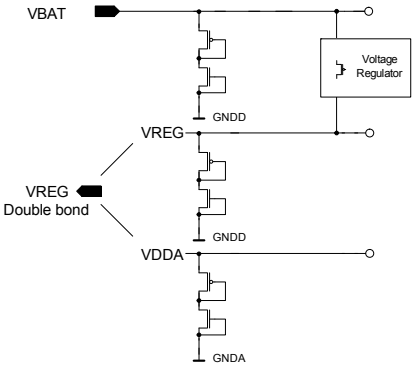
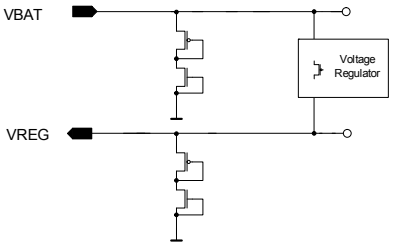
2 TDA5150 Functional Description

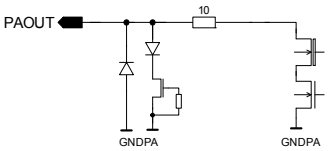
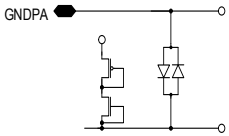
2.1 PIN Configuration, Pin-out

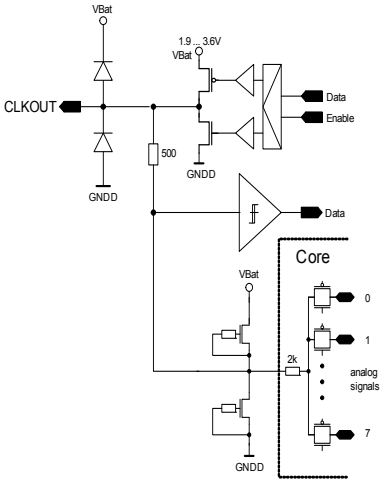


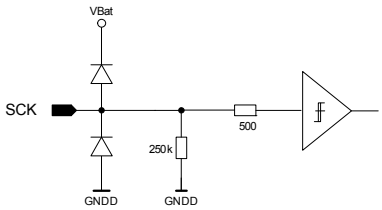
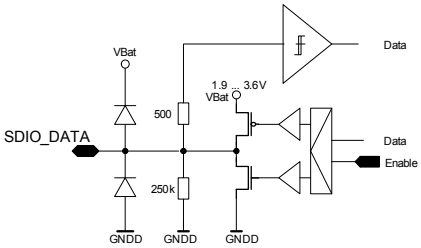
2.2 Pin Definition and Pin Functionality

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
1	EN	Digital Input		Enable 3-wire bus
2	XTAL	Analog Input		Crystal Oscillator

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
3	GND	Supply		Power supply ground
4	VREG	Analog Output		Voltage Regulator output
5	VBAT	Supply		Power supply (+)

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
6	PAOUT	RF-PA Output		RF Power Amplifier Output (open drain)
7	GNDPA	Analog GND		RF Power Amplifier Ground return

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
8	CLKOUT	Digital Output		Programmable Divided Clock

Pin No.	Name	Pin Type	Equivalent I/O Schematic	Function
9	SCK	Digital Input		Clock 3-wire bus
10	SDIO	Digital Input/ Output		Data 3-wire bus

2.3 Functional Block Diagram

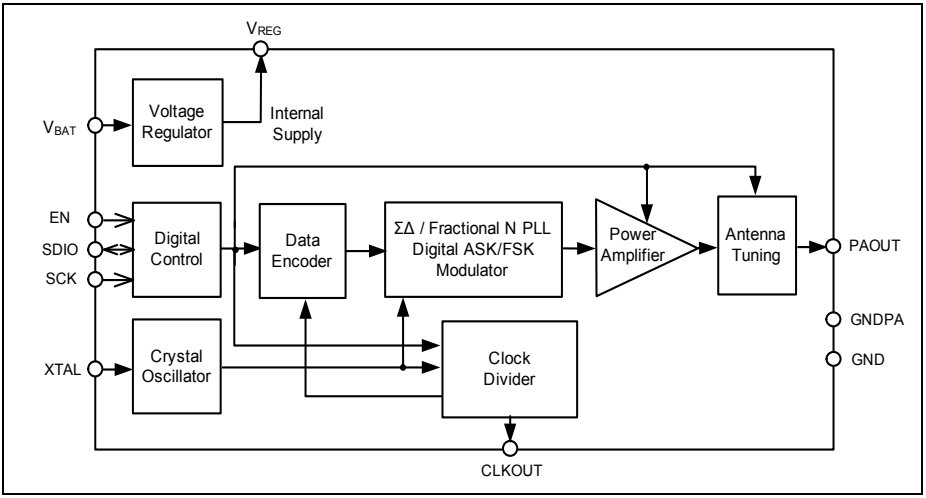


Figure 4 TDA5150 Block Diagram

TDA5150 is an SPI configurable fully integrated ASK/FSK/GFSK RF transmitter for the 300-320 MHz, 433-450 MHz and 863-928 MHz frequency bands. The input datastream, applied to the digital SDIO line is transposed and appears as modulated RF-signal, at the output of the integrated RF power amplifier. Signal encoding and spectrum is in accordance with the chosen modulation type (i.e ASK, FSK or GFSK) and encoding scheme.

TDA5150 contains following major blocks which extend the functionality compared to legacy RF transmitters:

- An on-chip voltage regulator is delivering 2.1 V nominal supply voltage for the transmitter's functional units. In addition, the battery voltage is monitored and battery low and brown out flags are set, if a critical supply voltage drop event occurs.
- For avoidance of erroneous transmissions, the brownout flag is coupled with the RF Power Amplifier state control. If a brownout or critical voltage drop event occurs, the RF Power Amplifier is automatically switched off, as part of the Fail-Safe philosophy. The mechanism is explained in detail in **Chapter 2.4.8.5**
- The crystal oscillator and the associated clock divider(s) generate the required clock signals. There is an output line (CLKOUT) which may be used to clock a host µC, or for bit rate generation.
- A digital control logic, accessible for user via the SPI bus allows flexible and fast (re)configuration. At the same time it offers a simple but powerful Fail-Safe mechanism, which enhances the reliability of the transmissions

- The data encoder synchronizes the bitstream to be transmitted with the internal bit clock. It supports different types of Manchester and Bi-Phase encodings and is able to generate PRBS9 pseudo-random patterns. The internal data encoder can be bypassed, allowing transmissions in direct (transparent) mode.
- The core element of the transmitter is the sigma-delta fractional-N PLL Synthesizer, used for carrier frequency control and as part of the digital modulator as well. It covers the frequency bands 300-320 MHz, 433-450 MHz and 863-928 MHz with outstanding frequency resolution. Only one, fixed frequency crystal (e.g. 13 MHz) is required for reference frequency generation. The synthesizer is characterized by short settling time. It is also used as direct FSK modulator, and together with a Gaussian filter, implemented by means of lookup table offers the functionality of a direct GFSK modulator.
- The integrated Power Amplifier is able to deliver up to +10 dBm output power into a 50 Ω load (usually the antenna) via an external impedance matching network. In addition there are integrated capacitors, connected between GND and the RF-PA output, over SFR controlled on/off switches. These capacitors are elements of a software controlled antenna tuner. They may be used to fine-tune (adjust) the PA-output to Load matching network impedance, and thus to maintain good VSWR values over a wider frequency band. This is particularly useful if the transmitter is operated not only on a single frequency but in multichannel mode, with considerable spread between the channels.

2.4 Functional Description

2.4.1 Special Function Registers

TDA5150 is configurable by programming the Special Function Register bank (abbreviated SFRs) via the SPI interface.

Terminology and notations related to TDA5150 SFR set, list of symbols and programming restrictions are given in **Chapter 22 Register Terminology**.

Detailed description of SFR map, programming, usage and content explanations are found in **Chapter 2.4 Functional Description** and **Chapter 2.5 Digital Control (SFR Registers)**.

2.4.2 Power Supply Circuit

An internal **voltage regulator** generates a constant supply voltage (2.1 V nominal) for most of the analog and digital blocks.

An external capacitor (100 nF nominal value) connected between VREG (pin 4) and GND (pin 3) is necessary to guarantee stable functionality of the regulator.

The regulated voltage on VREG pin is not adjustable by user and it is not allowed to connect any additional, external loads to this pin, but the above mentioned decoupling capacitor.

In **STANDBY** state, a special low-power voltage regulator is activated, which is supplying only the SPI bus interface, the SFR registers and the system controller.

In order to further reduce the current consumption, and keeping in mind that leakage currents can steeply increase by high temperatures, an additional low-power state, denoted **SLEEP** was defined. In this state most of the digital part is disconnected from the regulator (VREG). Only the SPI bus interface remains active. As a consequence, further power saving is achieved, but register content is lost by entering this mode.

See **Chapter 2.4.9 Operating Modes** for further informations.

2.4.2.1 Brownout Detector

A **Brownout Detector** (abbreviated **BOD**) is integrated into the TDA5150 transmitter.

Brownout is a condition where the supply voltage drops below a certain threshold level. By brownout events the integrity of SFRs can not be guaranteed, even if the dropout's duration is very short.

During active states, BOD monitors the VREG pin; during **STANDBY**, it monitors VBAT and VREG supply lines.

Table 1 BOD Thresholds

Description		Monitored @	min	max
Brownout Detection Level—Active State	VBDR	VREG	1.7 V	1.8 V
Brownout Detection Level—StandBy State	VPDBR	VREG & VBAT	0.7 V	1.7 V

If the BOD detects a brownout, the Power Amplifier is switched off and the SFRs are reset. The device is then forced to restart from the Power Up Reset condition. This ensures that the device is always in a well-defined logic state.

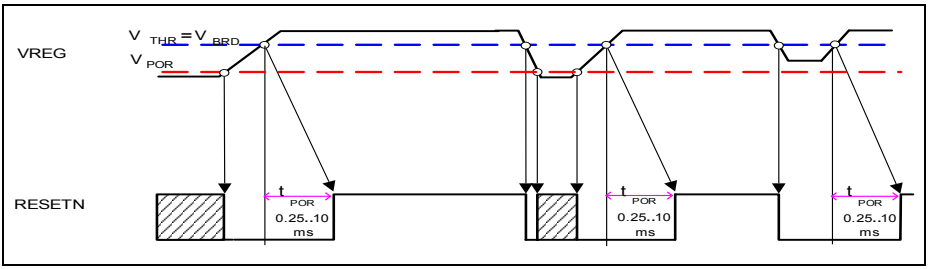


Figure 5 Power-on Reset/Brownout Detector

Brownout is indicated by bit BROUTERR (0x01.2) within SFR *TXTSTAT* (0x01).

Note: The BOD itself can not be used to guarantee the correct operation of analog sections, where the minimum operating voltage is defined to be 1.9 V; as this is larger than the maximum BOD voltage. In other words, in case of a supply voltage drop, the voltage region which is critical for reliable operation of the analog sections (min 1.9V) is reached before the brownout detector triggers (between 1.8 - 1.7V).

See also **Chapter 4.2** for operating voltage limits.

2.4.2.2 Low Battery Detector

TDA5150 has an embedded **Low Battery Detector** (**LBD**) block. In active modes, **LBD** monitors the voltage on VBAT supply line (pin 5). **LBD** has two activation thresholds, set to 2.4 V and 2.1 V. The status regarding supply voltage below threshold events can be updated by reading from SFR *TXSTAT*, bits 4 and 5 (0x01.5:4). These LBD flags are cleared after every transmission start. The LBD might be used as early warning for low battery voltage state (but before the battery voltage is dropping below the critical value, which renders normal operation capability).

2.4.2.3 SFRs related to Supply Voltage monitoring

ADDR 0x01		TXSTAT—Transmitter Status Register					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	n.u.	LBD_2V1	LBD_2V4	VAC_FAIL	BROUTERR	PARERR	PLLLDER
/	/	r/0	r/0	c/0	c/1	c/0	c/0

Bit 7	1		Set to 1, mandatory
Bit 5	LBD_2V1		battery low detected, threshold at 2.1 V -
Bit 4	LBD_2V4		battery low detected, threshold at 2.4 V
Bit 3	reserved		reserved
Bit 2	BROUTERR		Brown out event
Bit 1	PARERR		Parity error
Bit 0	PLLLDER		PLL lock detector error

Comments	
LBD_2V1	Battery voltage drop below 2.1 V detected if **1**. In standby mode, this bit is invalid.
LBD_2V4	Battery voltage drop below 2.4 V detected if **1**. In standby mode, this bit is invalid.
BROUTERR	Brownout event detected if **1**.
PARERR	Parity error detected if **1**.
PLLLDERR	PLL lock error detected if **1**.

2.4.3 Digital Control (3-wire SPI Bus)

The control interface is a 3-wire Serial Peripheral Interface (SPI), which is used for device control and data transmission.

2.4.3.1 SPI Pin Description

- **EN - enable input** with embedded pull-down resistor. High level on EN input enables the SPI transmission. The rising edge of the EN signal triggers the selection of the active SCK edge (for the consequent data transfer, until the EN line goes again in low state) and transmission/ sampling of data between the device and the microcontroller can start. For details refer to **Figure 6** and **Figure 7**.
- **SDIO - 3-state input/output** This bidirectional line is used for data transfer between the TDA5150 and external host (usually a µC). On-chip pull-down resistor is connected to this pin. The load drive capability is listed in **Table 4.3**.

- **SCK - clock input** pin with embedded pull-down resistor. If SCK is at low level while EN goes high, the incoming SDIO data is sampled by falling edge of the SCK and the output SDIO data is set by the rising edge of SCK. Contrariwise, If SCK is at high level when EN goes high, the SDIO data is sampled with the rising edge of the SCK clock and output on SDIO by falling edge of the SCK clock. For details refer to **Figure 6** and **Figure 7**.

SPI commands are started by the rising edge on the EN line and terminated by the falling edge on EN.

The available Burst Write mode allows configuration of several SFRs within one block access, without cycling the EN line Low - High - Low for each individual byte. By keeping the EN line at High level, subsequent bytes could be sent, and the byte address counter is autoincremented, thus speeding up the transfer on the SPI bus.

A self-explaining diagram is found here: **Chapter 9 Timing Diagrams of 3-wire SPI**.

The active edge of SCK (during SPI commands) is programmable, and it is determined by the level on SCK line at the moment of activation of the EN line (rising edge on EN).

If SCK is low at that moment, the incoming SDIO data will be sampled with the falling edge of SCK, and output by rising edge of SCK (see **Figure 6** below).

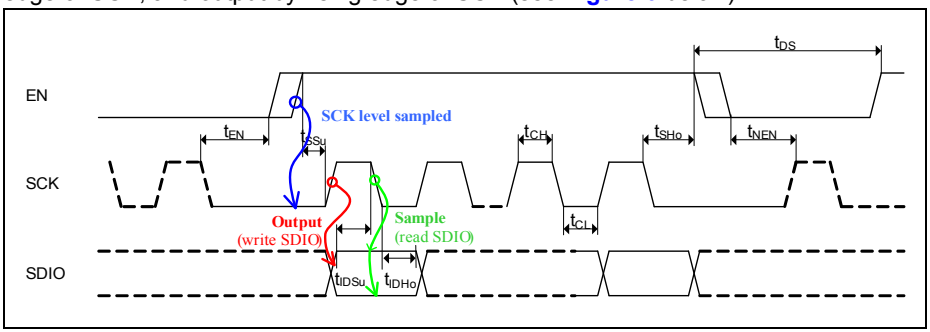


Figure 6 SPI Timing — SCK low at rising edge of EN

If SCK is high during occurrence of rising edge on EN, incoming SDIO data is sampled with the rising edge on SCK, and output by falling edge of SCK, as illustrated in **Figure 7**.

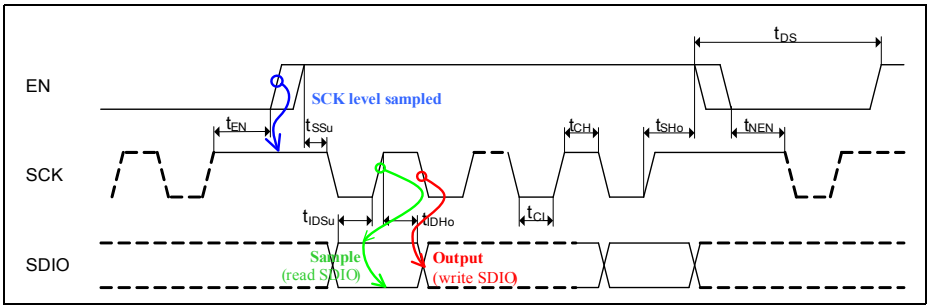


Figure 7 SPI Timing — SCK high at rising edge of EN

2.4.3.2 SPI XOR Checksum

The SPI block includes a safety feature for checksum calculation. This is achieved by means of XOR operation between the address and the data during write operation of SFR registers. The checksum is in fact the XOR of the data 8-bitwise after every 8 bits of the SPI write command. The calculated checksum value is then automatically written into SFR *SPICHKSUM* (0x00) and can be compared with the expected value. By executing a read operation of SFR *SPICHKSUM* (0x00) the register content is automatically cleared (after read). Read access to any of the other readable SFRs does not influence the SFR *SPICHKSUM*.

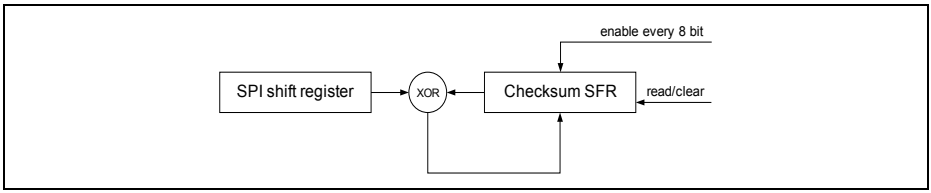


Figure 8 Generating the Checksum of SFRs, block diagram

Example:

Write to SFR address 0x04, data 0x02, address 0x05, data 0x01

Bytes transmitted via SPI	Result in Checksum Register
0000 0100	0000 0100
0000 0010	0000 0110
0000 0101	0000 0011
0000 0001	0000 0010

After writing into the registers, content of checksum SFR *SPICHKSUM* (0x00) will be 0x02.

2.4.3.3 Command Byte Structure

First byte of each SPI sequence is the **Command Byte**, with the following structure:

Function Code		Command Byte Configuration					
C1	C0	Address					
x	x	A5	A4	A3	A2	A1	A0

The first 2 bits **C1, C0** of the Command Byte are the function code field**.**

They define the command to be performed, according to the following table:

C1	C0	Function Code Configuration Bits
0	0	**Write** data into SFR register <A5:A0> field contains the SFR register's address There are 2 possible write modes (controlled by state of EN line): 1. write to a single address 2. burst mode write (with address auto increment)
0	1	**Read** data from SFR, <A5:A0> points to register address
1	0	**Reserved** (do not use)
1	1	**Transmit Command Byte** Bits <A5:A0> within this byte define the transmission parameters (see **Chapter 2.4.3.4 Transmit Command** for command fields).

The **Write / Read Command** bytes are used for device control. Bit fields <A5:A0> within **Command Byte** are used to specify the addressed SFR register. An overview and register map is given in **Chapter 2.5.1 SFR Register List**.

There are two ways to program the SFR registers:

1. by sending Write commands individually, for each register which should be written.
2. by sending a Burst Write command, which allows sequential programming (of registers found at subsequent addresses).

Attention: Writing to the address space beyond the valid SFR address range [0x04 - 0x27] is prohibited, as it may lead to system malfunction.

2.4.3.4 Transmit Command

The **Transmit Command Byte** is used for **data transmission**. It precedes the datagram to be transmitted. The Transmit Command Byte format is described in the following table:

C1	C0	Transmit Command Configuration		
		Bit	**Function**	**Value, description**
1	1	A	Data sync	0: off 1: on (at the same time Bit C - Encoding must be set also to 1 --> Int. Encoding)
1	1	B	PA mode	0: PA off at the falling edge of EN (synchronized with bit-rate if bit A is high) 1: SDIO/DATA is latched at the falling edge of EN, PA stays on, TX data are kept constant. After the time-out of 65536 / f_{sys} which is ~5 ms for a 13 MHz crystal, PA and PLL are switched off.
1	1	C	Encoding	0: off 1: on (selects SFR register for encoding Bit A must be also set to1 --> Data sync)
1	1	D	Pwr. level/ ModSetting	0: selects **PowerLevel/Modulation Setting1** 1: selects **Power Level/Modulation Setting2**
1	1	<E,F>	Frequency selection	0 (00): frequency channel **A** selected 1 (01): frequency channel **B** selected 2 (10): frequency channel **C** selected 3 (11): frequency channel **D** selected (for description of programming the frequency channels **A**..**D** consult **Chapter 2.4.11.3 Channel Hopping**)

Note: After the last configuration bit for a new transmission was sent, a break of at least 100 µs must be provided in order to achieve PLL settling and lock on the selected channel frequency.

2.4.3.5 Timing Diagrams

In the following timing diagrams the 4 possible SPI commands are shown. The examples are valid for the case of SCK is low when EN line goes from Low to High (rising edge).