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TDA 5200

ASK Single Conversion Receiver
Version 3.0

Data Sheet

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Wireless Components

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Previous Revision: 2.9	
Revision 3.0, 2010-12-28	
all	Converted into structured FrameMaker (EDD 3.4)
4-3	More detailed explanation of AGC
5-6, 5-8	More detailed information of LNA high gain mode and LNA low gain mode

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1 Product Info

General Description

The IC is a very low power consumption single chip ASK Single Conversion Receiver for receive frequencies bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Features

- Low supply current (I_s = 4.8 mA typ. at 868 MHz, I_s = 4.6 mA typ. at 434 MHz)
- Supply voltage range 5 V ±10 %
- Power down mode with very low supply current (50 nA typ)
- Fully integrated VCO and PLL Synthesizer
- RF input sensitivity < – 107 dBm
- Selectable frequency ranges around 868-870 MHz and 433-435 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7 MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Package

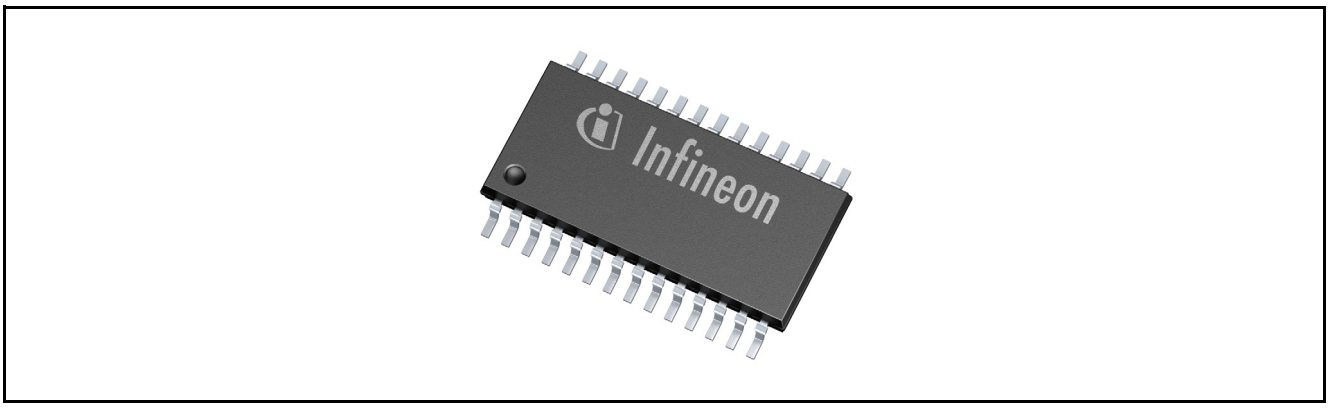


Figure 1 PG-TSSOP-28

Ordering Information

Type	Ordering Code	Package[1)]
TDA5200	SP000016381	PG-TSSOP-28

1) Available on tape and reel

2 Product Description

2.1 Overview

The IC is a very low power consumption single chip ASK Superheterodyne Receiver (SHR) for the frequency bands 868-870 MHz and 433-435 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

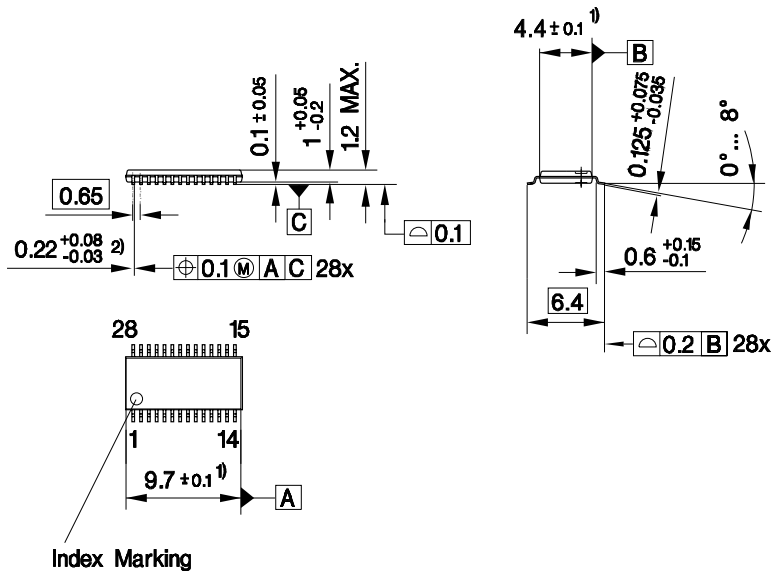
2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (I_s = 4.8 mA typ. at 868 MHz, I_s = 4.6 mA typ. at 434 MHz)
- Supply voltage range 5 V ±10 %
- Power down mode with very low supply current (100 nA typ.)
- Fully integrated VCO and PLL Synthesizer
- RF input sensitivity < – 107 dBm
- Selectable receive frequency bands 868-870 MHz and 433-435 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7 MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

Figure 2 PG-TSSOP-28 Package Outlines

3 Functional Description

3.1 Pin Configuration

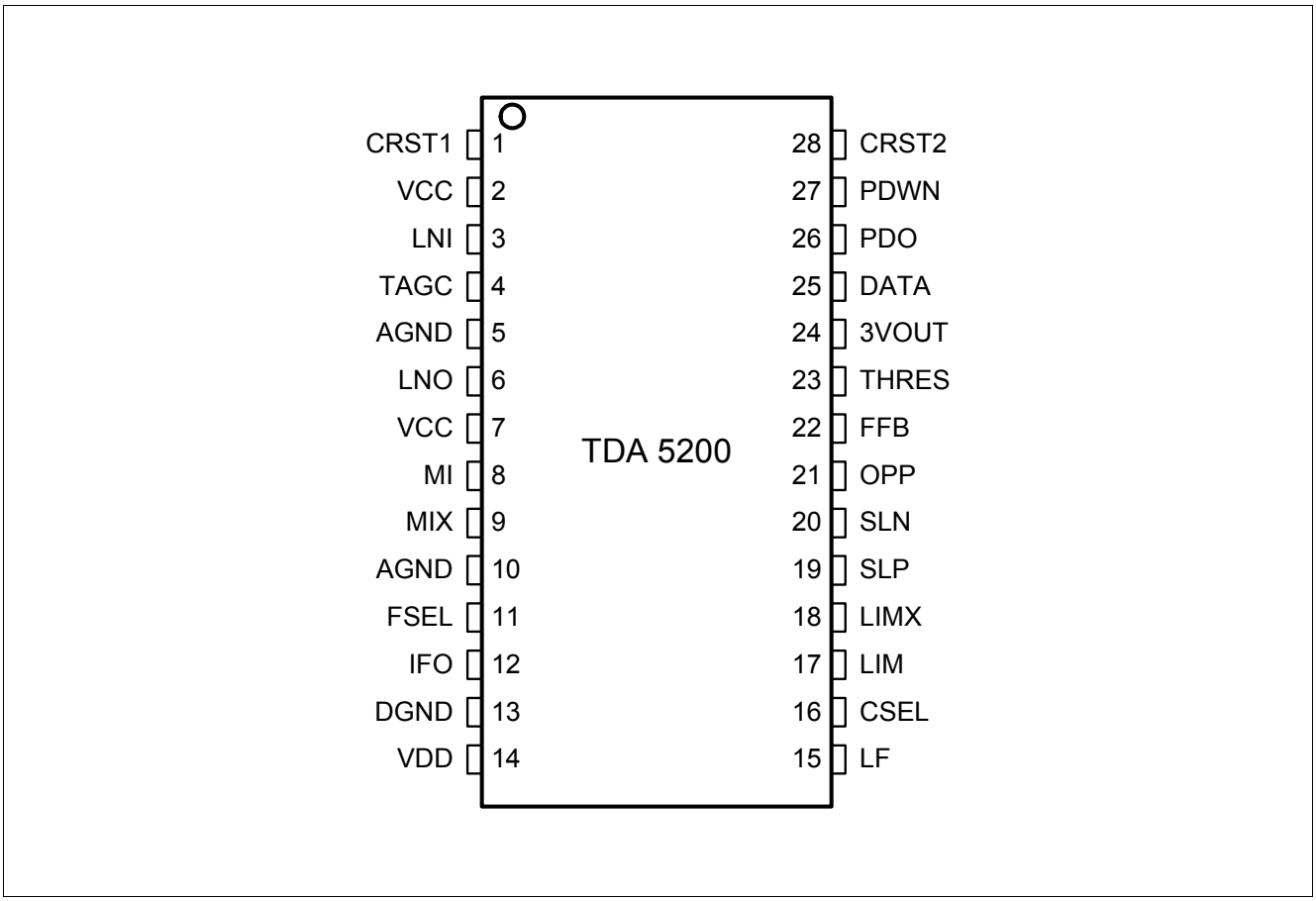


Figure 3 IC Pin Configuration

3.2 Pin Definition and Function

Table 1 Pin Definition and Function

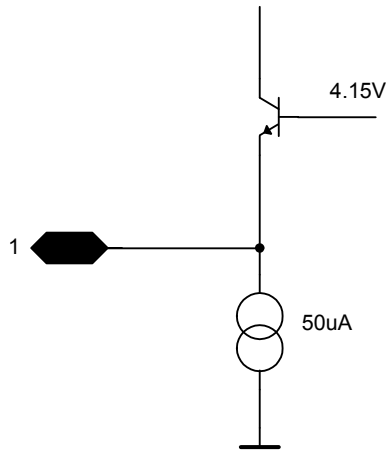
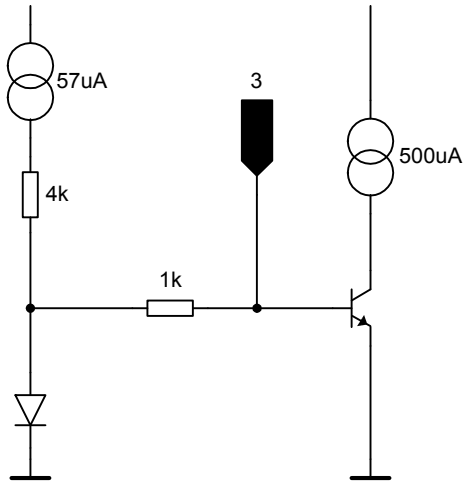
Pin No.	Name	Pin Type	Buffer Type	Function
1	CRST1	In/Out		**External Crystal Connector 1**
2	VCC	In		**5 V Supply**
3	LNI	In		**LNA Input**

Table 1 Pin Definition and Function (cont'd)

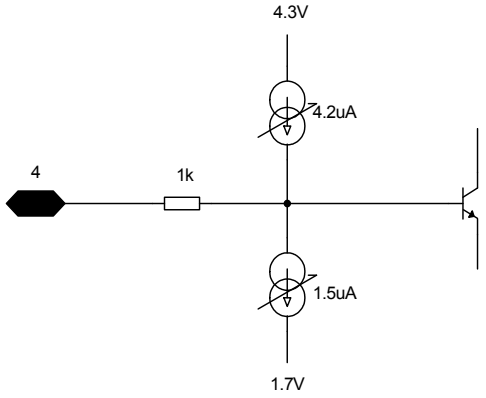
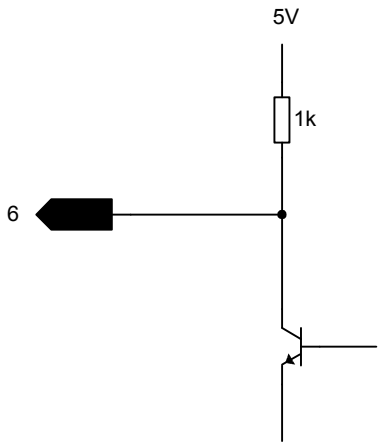
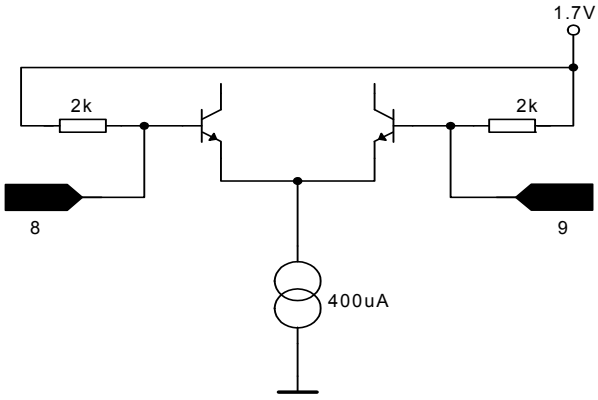
Pin No.	Name	Pin Type	Buffer Type	Function
4	TAGC	In/Out		**AGC Time Constant Control**
5	AGND	In		**Analogue Ground Return**
6	LNO	Out		**LNA Output**
7	VCC	In		**5 V Supply**
8	MI	In		**Mixer Input**

Table 1 Pin Definition and Function (cont'd)

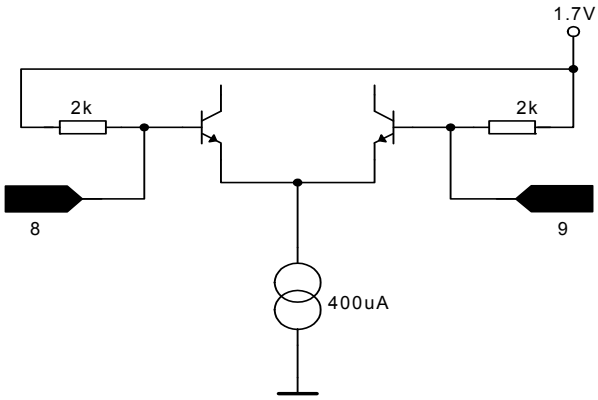
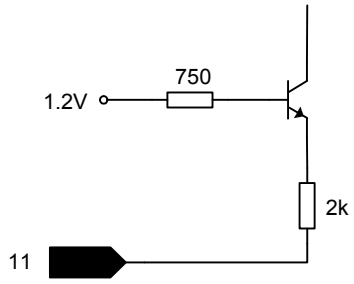
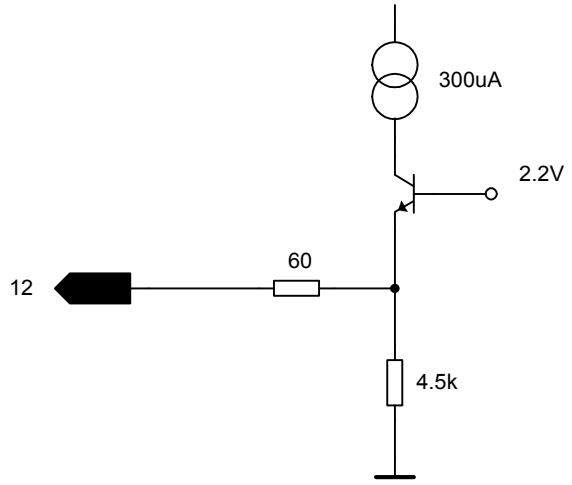
Pin No.	Name	Pin Type	Buffer Type	Function
9	MIX	In		**Complementary Mixer Input**
10	AGND	In		**Analogue Ground Return**
11	FSEL	In		**Operating Frequency Selector** 869/434 MHz
12	IFO	Out		**IF Mixer Output** 10.7 MHz
13	DGND	In		**Digital Ground Return**
14	VDD	In		**5 V Supply** PLL Counter Circuitry

Table 1 Pin Definition and Function (cont'd)

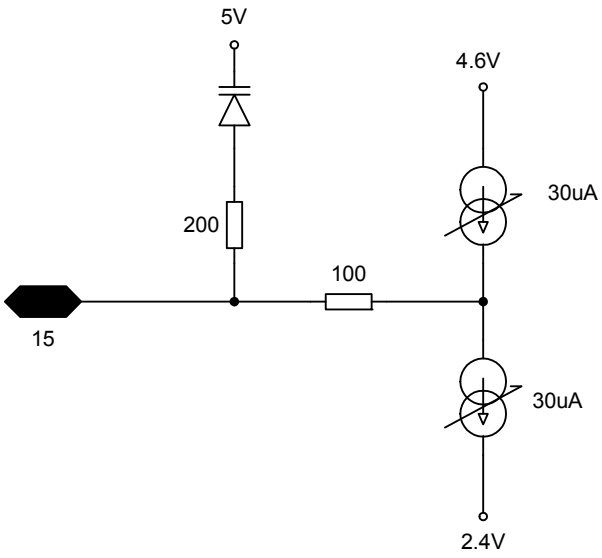
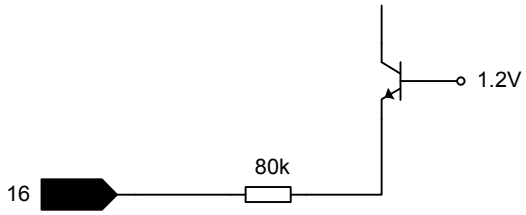
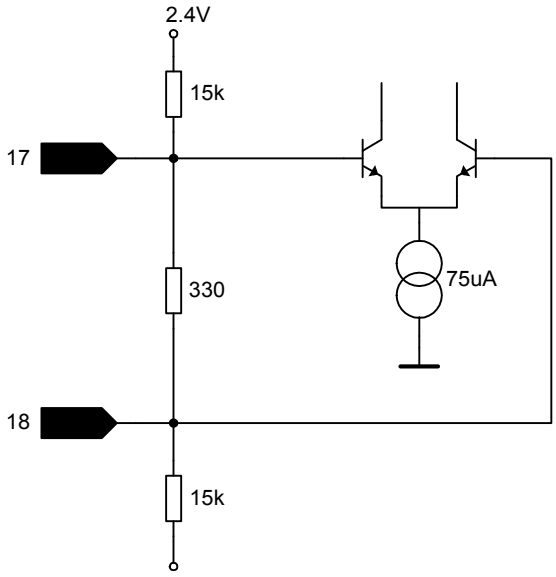
Pin No.	Name	Pin Type	Buffer Type	Function
15	LF	In/Out		**PLL Filter Access Point**
16	CSEL	In		**Quartz Selector** 6.xx MHz or 13.xx MHz
17	LIM	In		**Limiter Input**

Table 1 Pin Definition and Function (cont'd)

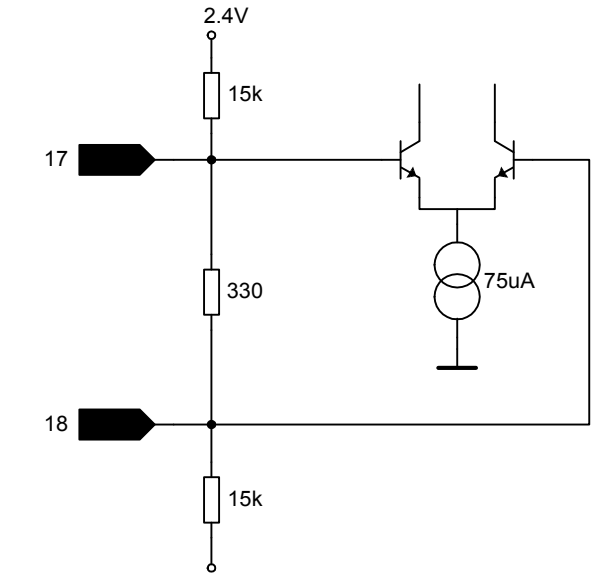
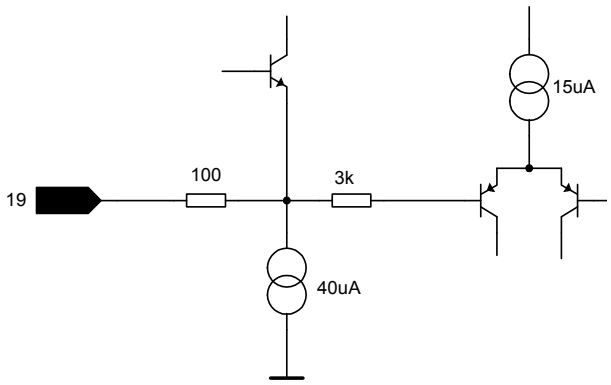
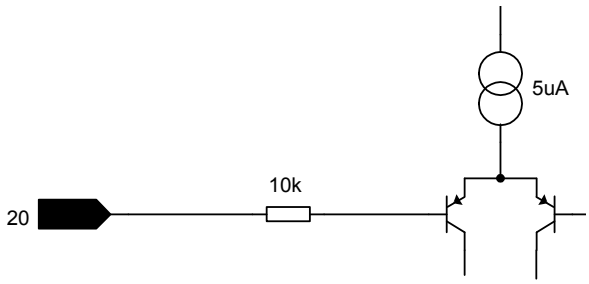
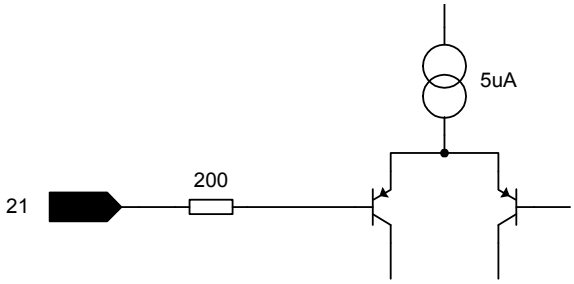
Pin No.	Name	Pin Type	Buffer Type	Function
18	LIMX	In		**Complementary Limiter Input**
19	SLP	In		**Data Slicer Positive Input**
20	SLN	In		**Data Slicer Negative Input**
21	OPP	In		**OpAmp Noninverting Input**

Table 1 Pin Definition and Function (cont'd)

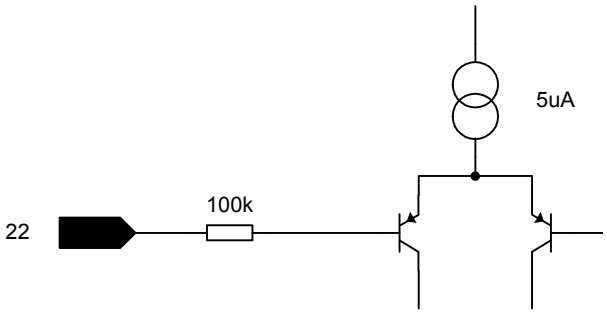
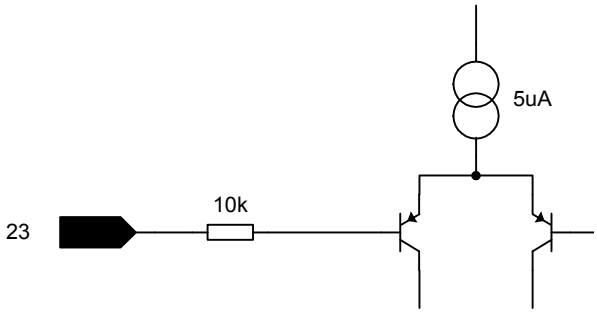
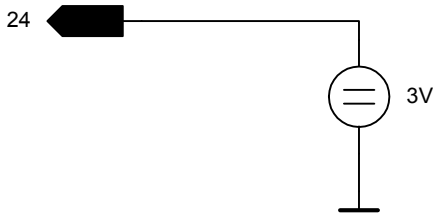
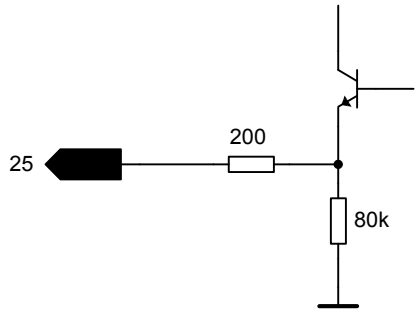
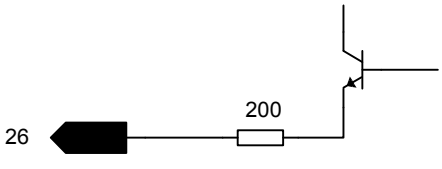
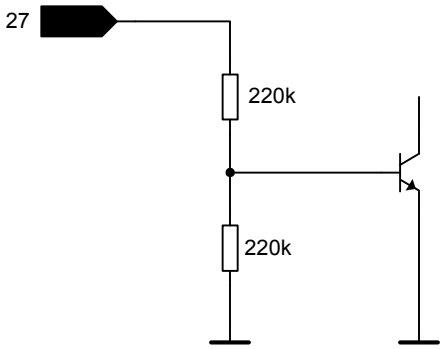
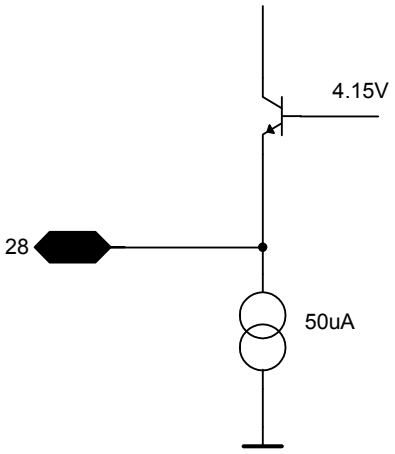
Pin No.	Name	Pin Type	Buffer Type	Function
22	FFB	In		**Data Filter Feedback Pin**
23	THRES	In		**AGC Threshold Input**
24	3VOUT	Out		**3 V Reference Output**
25	DATA	Out		**Data Output**
26	PDO	Out		**Peak Detector Output**

Table 1 Pin Definition and Function (cont'd)

Pin No.	Name	Pin Type	Buffer Type	Function
27	PDWN	In		**Power Down Input**
28	CRST2	In/Out		**External Crystal Connector 2**

3.3 Functional Block Diagram

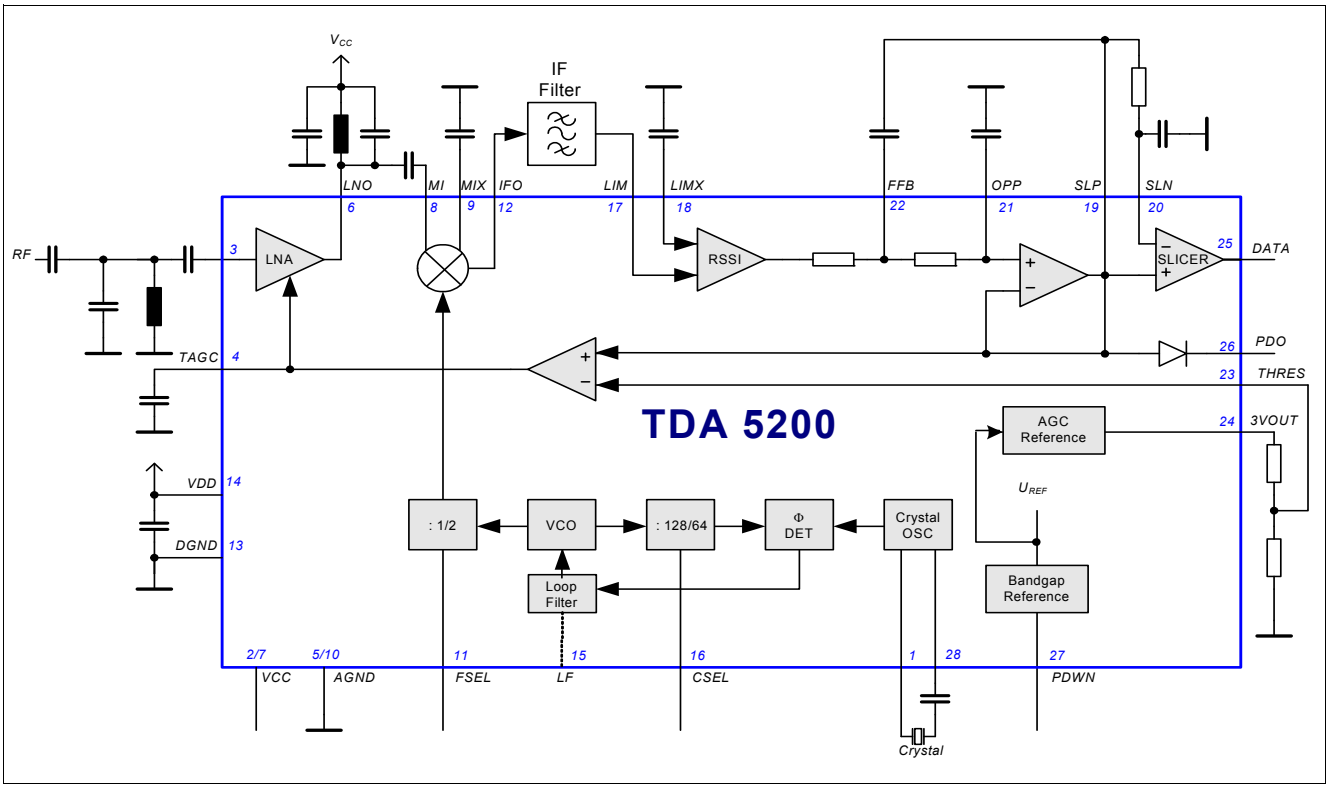


Figure 4 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 dB to 20 dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pin 8 and Pin 9). The noise figure of the LNA is approximately 3.2 dB, the current consumption is 500 µA. The gain can be reduced by approximately 18 dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the **THRES** pin as described in **Chapter 4.1**. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in **Chapter 4.1**.

3.4.2 Mixer

The Double Balanced Mixer down-converts the input frequency (RF) in the range of 433-435 MHz / 868-870 MHz to the intermediate frequency (IF) at 10.7 MHz with a voltage gain of approximately 21 dB. A low pass filter with a corner frequency of 20 MHz is built on chip in order to suppress RF signals to appear at the IF output (IFO pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330 Ω to facilitate interfacing the pin directly to a standard 10.7 MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 840 MHz. No additional components are necessary.
Local oscillator high side injection has to be used for receive frequencies below approximately 420 MHz or 840 MHz, low side injection for receive frequencies above approximately 420 MHz or 840 MHz - see also **Chapter 4.4**. Therefore low-side injection of the local oscillator has to be used for operation both in the 868 MHz and the 434 MHz ISM bands.
The oscillator signal is fed both to the synthesizer divider chain and to the down-converting mixer. In case of operation in the 433-435 MHz range, the signal is divided by two before it is fed to the mixer. This is controlled by the selection pin FSEL (Pin 11) as described in the following table. The overall division ratio of the divider chain can be selected to be either 128 or 64, depending on the frequency of the reference oscillator quartz (see below). The loop filter is also realized fully on-chip.

Table 2 FSEL Pin Operating States

FSEL	RF Frequency
Open	433-435 MHz
Shorted to ground	868-870 MHz

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilization of quartzes both in the 6 MHz and 13 MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	13.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in **Chapter 4.3**, the quartz frequency calculation is explained in **Chapter 4.4**.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centered around 10.7 MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in **Figure 6**. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 17 dB in case the input signal strength is too strong as described in **Chapter 3.4.1** and **Chapter 4.1**.

3.4.6 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100 kHz used as a voltage follower and two 100 kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in **Chapter 4.2**.

3.4.7 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120 kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 is generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in **Chapter 4.5**.

3.4.8 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is 500 µA.

3.4.9 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all sub-circuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50 nA.

Table 4 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Power Down Mode
Tied to V_{CC}	Receiver On

4 Applications

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.

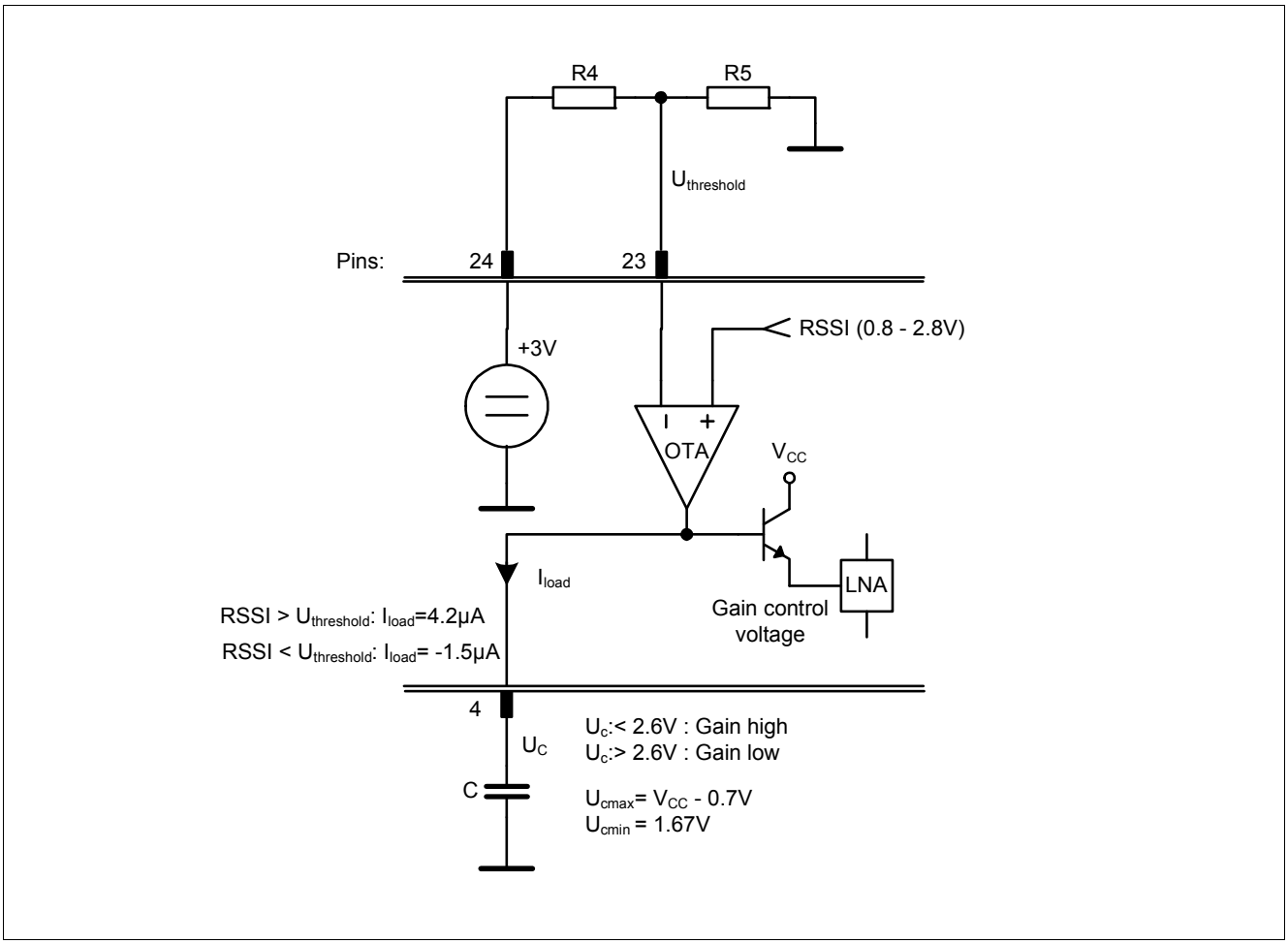


Figure 5 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately typically 0.8 V and 2.8 V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23). The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3 V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

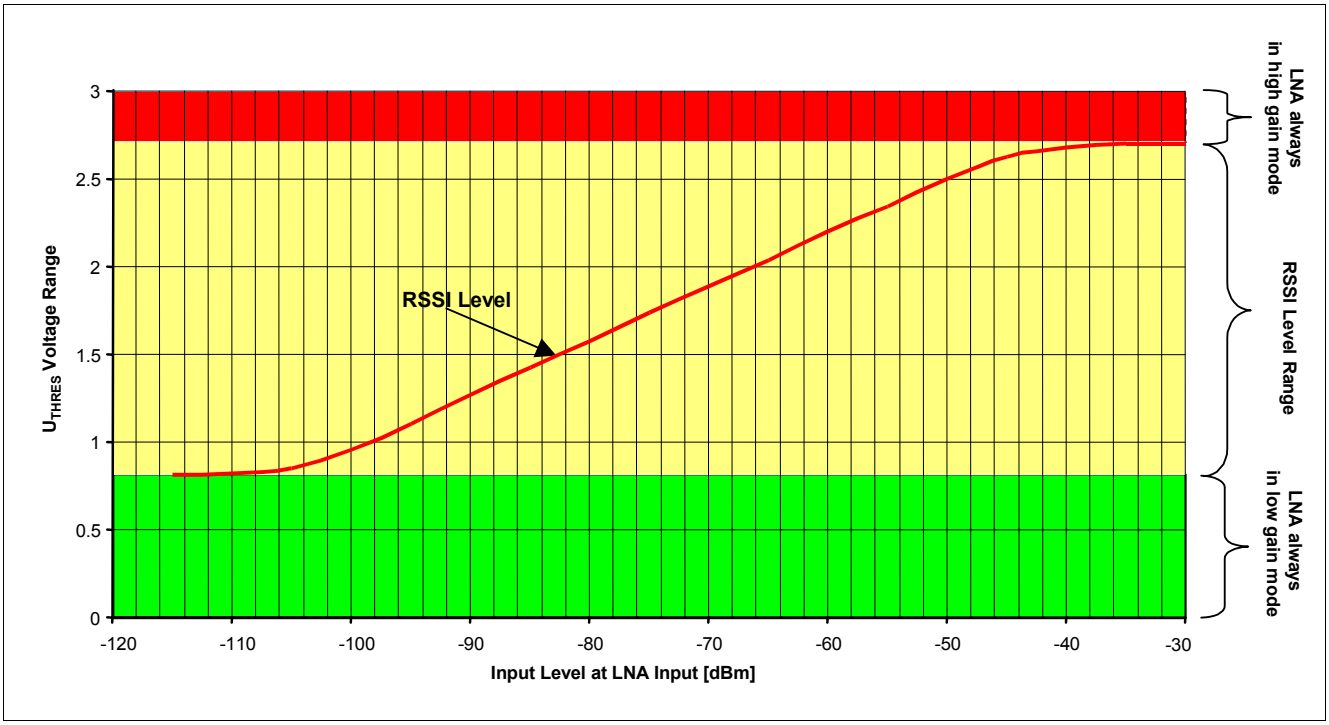


Figure 6 Typical Curve of RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8 V is apparently a viable choice. It should be noted that the output of the 3VOUT pin is capable of driving up to 50 µA, but that the THRES pin input current is only in the region of 40 nA. As the current drawn out of the 3VOUT pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. R4 can be chosen as 120 kΩ, R5 as 180 kΩ to yield an overall 3VOUT output current of 10 µA.

Notes

1. *To keep the LNA in high gain mode for the complete RF-input level range a voltage equal or higher than 3.3 V has to be applied at pin 23. Alternatively, pin 23 has to be connected to pin 24 and pin 4 has to be connected to GND. In addition this would save an external capacitor.*
2. *To keep the LNA in low gain mode for the complete RF-input level range a voltage lower than 0.7 V has to be applied to the THRES pin (e.g. THRES connected to GND). In the above-mentioned mode pin 4 has to be connected by a capacitor to GND.*
3. *As stated above, the gain control voltage of the LNA is generated at the capacitor connected to the TAGC pin by the charging and discharging currents of the OTA. Consequently this capacitor is responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47 nF.*

4.2 Data Filter Design

Utilizing the on-board voltage follower and the two 100 kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pin 19 (SLP) and pin 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].

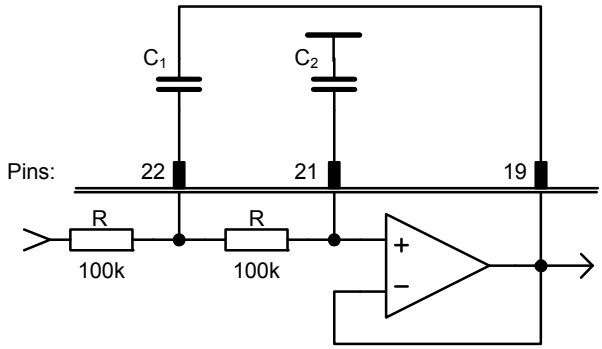


Figure 7 Data Filter Design

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \quad (1)$$

$$C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}} \quad (2)$$

with

$$Q = \frac{\sqrt{b}}{a} \quad (3)$$

the quality factor of the poles where

in case of a **Bessel** filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a **Butterworth** filter a = 1.141, b = 1

and thus Q = 0.71

Example

Butterworth filter with f_{3dB} = 5 kHz and R = 100 kΩ

C_1 = 450 pF, C_2 = 225 pF

1) Taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in **Chapter 5.1.3** and by the quartz specifications given by the quartz manufacturer.

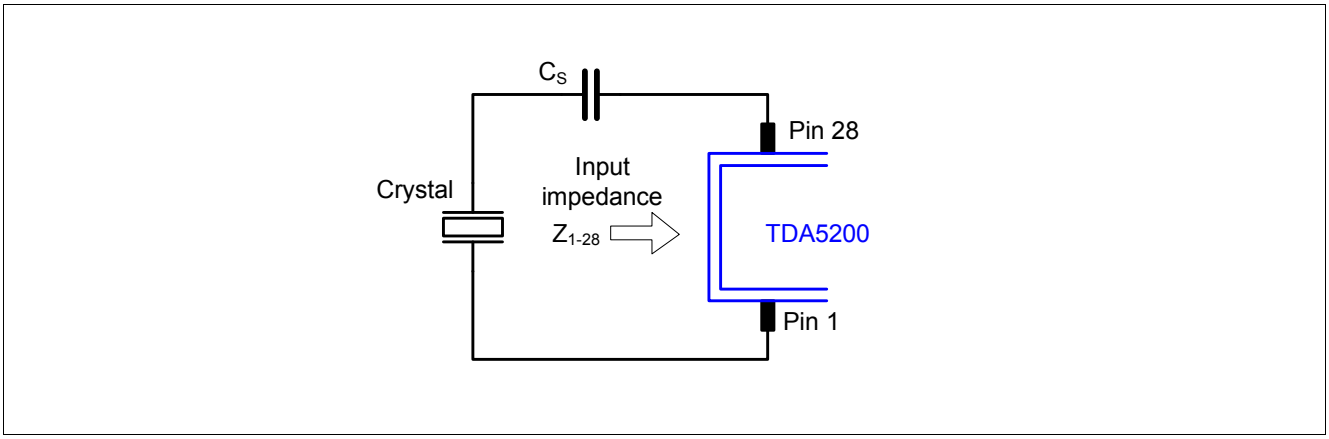


Figure 8 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L} \tag{4}$$

with C_L the load capacitance (refer to the quartz crystal specification).

Examples

6.7 MHz	C_L = 12 pF	X_L = 750 Ω	C_S = 8.7 pF
13.401 MHz	C_L = 12 pF	X_L = 1250 Ω	C_S = 5.3 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 20 pF and 15 pF in the 6.7 MHz case and 15 pF and 8.2 pF in the 13.401 MHz case.

But please note that the calculated value of C_S includes the parasitic capacitors also.