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Wireless Components

ASK Single Conversion Receiver 390MHz

TDA 5204 E1

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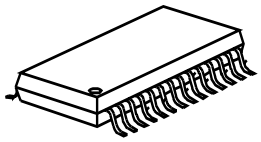
Product Info

General Description

The IC is a very low power consumption single chip ASK Single Conversion Receiver for receive frequencies between 385 and 406MHz. The Receiver offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (I_s = 4.8mA typ.)
- Supply voltage range 5V ±10%
- Temperature range -40°C...+85°C
- Power down mode with very low supply current (50nA typ)
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity < –110dBm
- 390MHz band
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

Application

- Keyless Entry Systems
- Remote Control Systems
- Fire Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5204	Q67037-A1169	P-TSSOP-28-1
available on tape and reel		

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2 Product Description

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2.1 Overview

The IC is a very low power consumption single chip ASK Superheterodyne Receiver (SHR) for the frequency band 390MHz. The SHR offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Fire Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (Is = 4.8mA typ.)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity < –110dBm
- frequency band 390MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- Temperature range -40°C...+85°C

2.4 Possible Receive Ranges

- **385...406MHz (high-side injected)**
- 406...428MHz (low-side injected)
- 781...823MHz (high-side injected)
- 803...844MHz (low-side injected)

2.5 Package Outlines

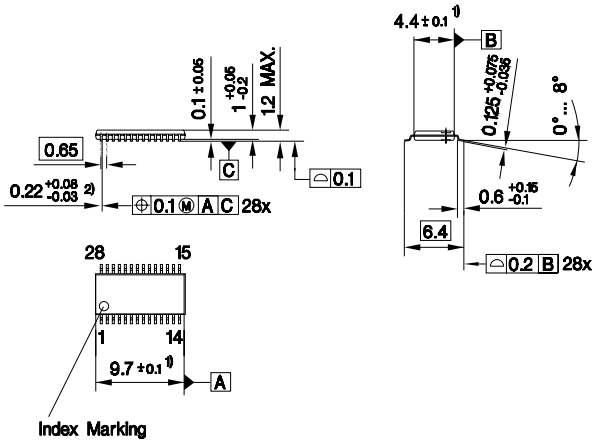

Figure 2-1 P-TSSOP-28-1 package outlines

3 Functional Description

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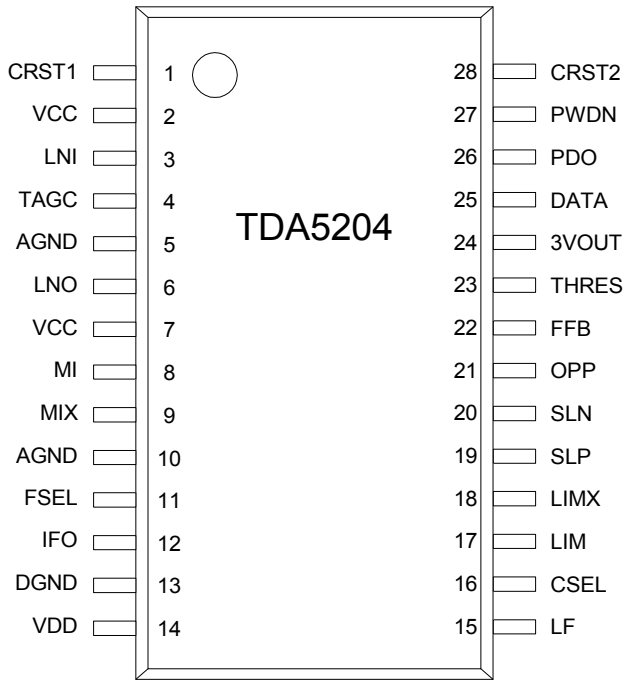
3.1 Pin Configuration

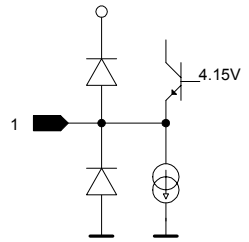
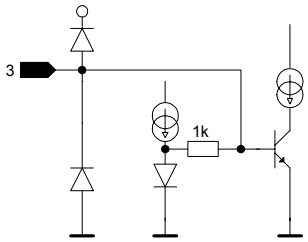
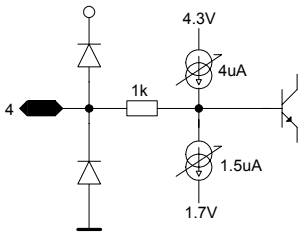
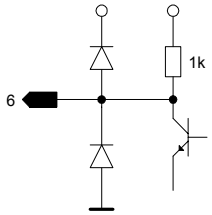


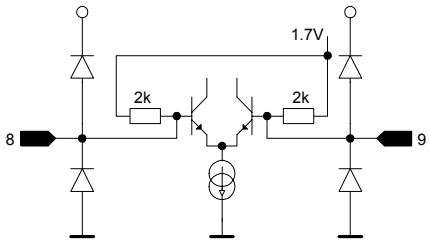
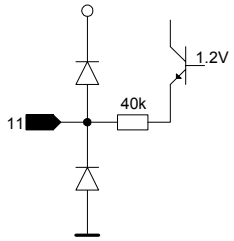
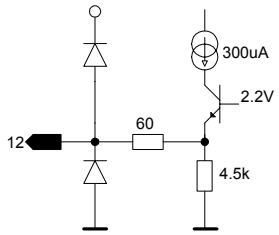
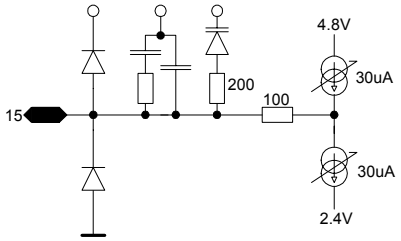
Pin_Configuration.wmf

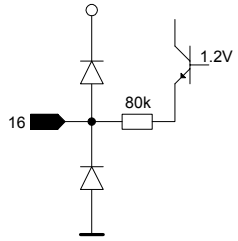
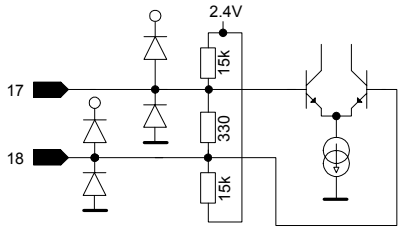
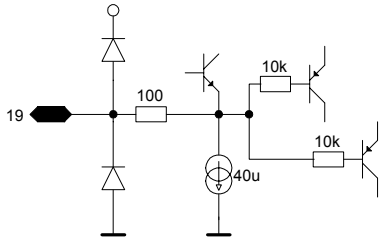
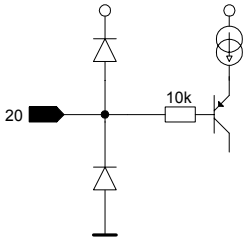
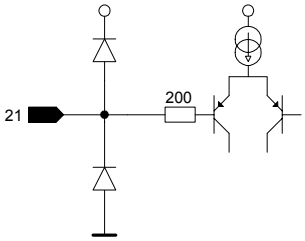
Figure 3-1 IC Pin Configuration

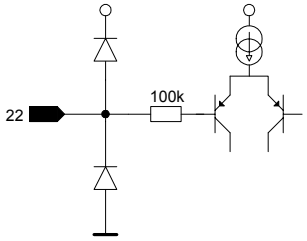
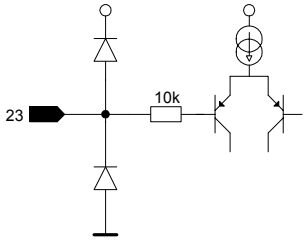
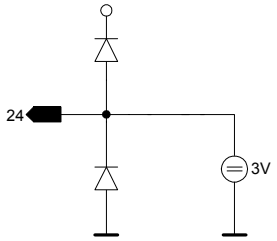
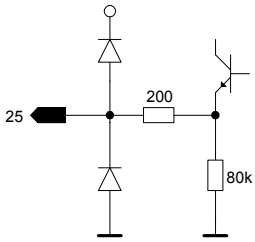
3.2 Pin Definition and Function

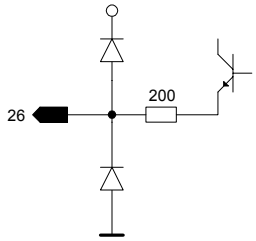
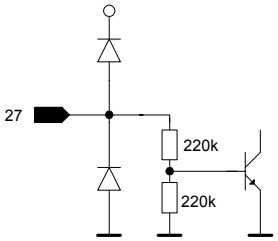
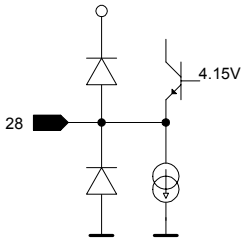
Table 3-1 Pin Definition and Function

Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input
4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply

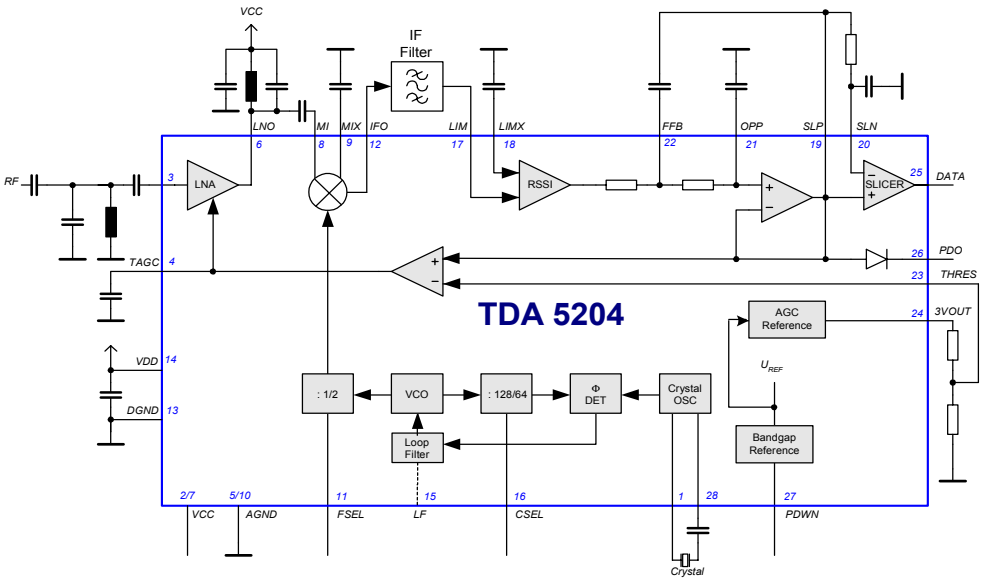
8 9	MI MIX		Mixer Input Complementary Mixer Input
10	AGND		Analogue Ground Return
11	FSEL		390MHz: not applicable - has to be left open
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	LF		PLL Filter Access Point (Loop Filter)

16	CSEL		6.xx or 12.xx MHz Quartz Selector
17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Filter Output Data Slicer Positive Input Peak Detector Input
20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input

22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output

26	PDO		Peak Detector Output
27	PDWN		Power Down Input Vs --> Power ON GND---> Power Down
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram



Function_5204.wmf

Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 2dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operat-

ing case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) 390MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB. A low pass filter with a corner frequency of 20MHz is built on chip in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. It's nominal centre frequency is 800MHz. The **FSEL** pin (Pin 11) has to be left open. No additional components are necessary. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. The VCO signal is divided by two before it is fed to the mixer. The loop filter is also realised fully on-chip.

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 6 and 12MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-2 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	6.xx MHz
Shorted to ground	12.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is expained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80dB that has a bandpass-characteristic centred around 10.7MHz. It has an input impedance of 330 Ω to allow for easy interfacing to a 10.7MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4.1. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 18dB in case the input signal strength is too strong as described in Section 3.4.1 and Section 4.1.

3.4.6 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.7 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on **pin SLN** (pin 20) its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.8 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The output can be used as an indicator for the signal strength and also as a reference for the data slicer. The maximum output current is approx. 900µA.

3.4.9 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the **PWDN pin** (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 3-3 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

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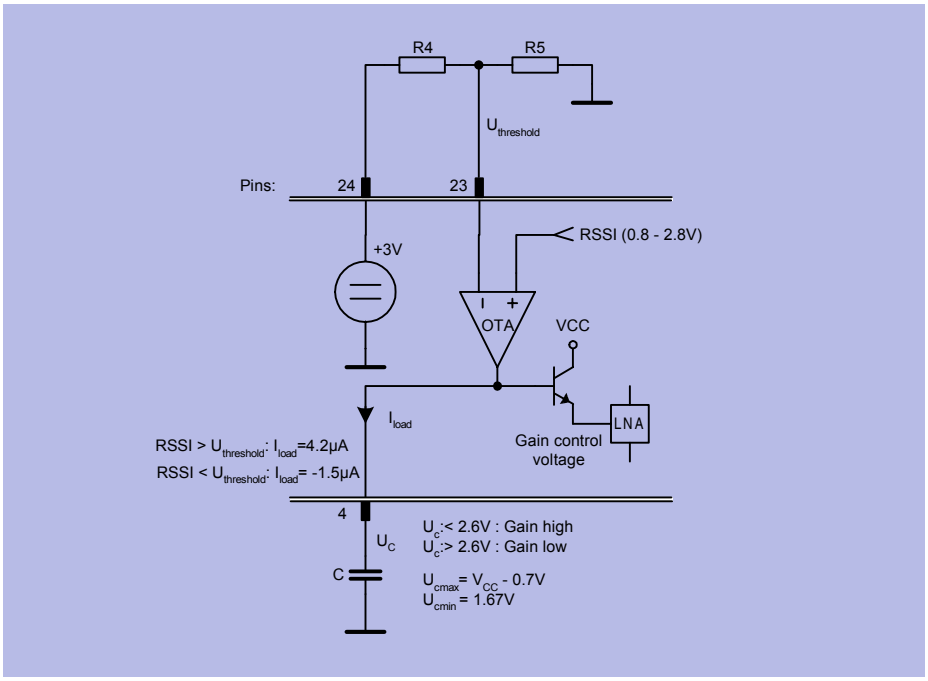
4.1 LNA and Automatic Gain Control (AGC) 4-2
4.2 Data Filter Design 4-4
4.3 Quartz Load Capacitance Calculation 4-5
4.4 Quartz Frequency Calculation 4-6
4.5 Data Slicer Threshold Generation 4-7

4.1 LNA and Automatic Gain Control (AGC)

The AGC extends the dynamic range of the receiver.

The automatic gain control in the TDA5204 is a narrow-band control loop which compares the receive signal strength signal (RSSI, 0.8V to 2.8V) from the limiter with a fixed threshold voltage applied to **pin 23** (THRES).

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The fixed voltage on **pin 23** is generated on the external voltage divider. The comparator is a transimpedance amplifier (OTA), which creates a positive current (+4.2uA) in the case the RSSI level is larger than the threshold voltage. Otherwise the current is -1.5uA. This leads to an asymmetric fast-attack and slow-release behaviour and thus to fast reaction to the low gain mode and slow reaction to the high gain mode.

This current is converted into a control voltage over an external capacitor C attached to **pin 4** (TAGC) which defines the gain of the LNA. The limits of the control voltages for the LNA on pin4 are 1.67V for high gain mode and Vcc-0.7V for low gain mode.

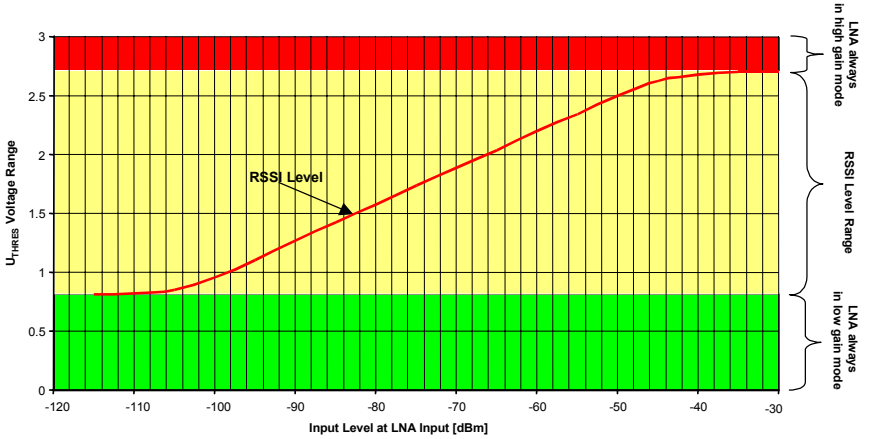


Figure 4-2 RSSI Level an Permissive AGC Threhold Level

The value of the capacitor defines the response time of the AGC. For a stable control loop the capacitor value should be at least 47nF.

The AGC can be disabled by tying the THRES-pin either to GND or to VCC as show here:

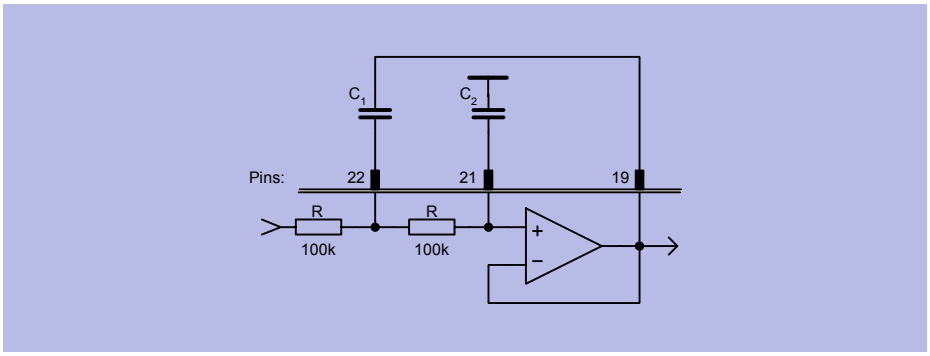
LNA high gain: - **pin 23** (THRES) shorted to VCC

LNA low gain: - **pin 23** (THRES) shorted to GND

In these cases capacitor and voltage divider are not necessary.

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between **pins 19** (SLP) and **22** (FFB) and to **pin 21** (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

(1) (2)

$$C1 = \frac{2 \cdot Q\sqrt{b}}{R \cdot 2\pi f_{3dB}} \qquad C2 = \frac{\sqrt{b}}{4Q \cdot R \cdot \pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$ (3) the quality factor of the poles

where

in case of a Bessel filter	a = 1.3617, b = 0.618
and thus	Q = 0.577
and in case of a Butterworth filter	a = 1.41, b = 1
and thus	Q = 0.71

Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.

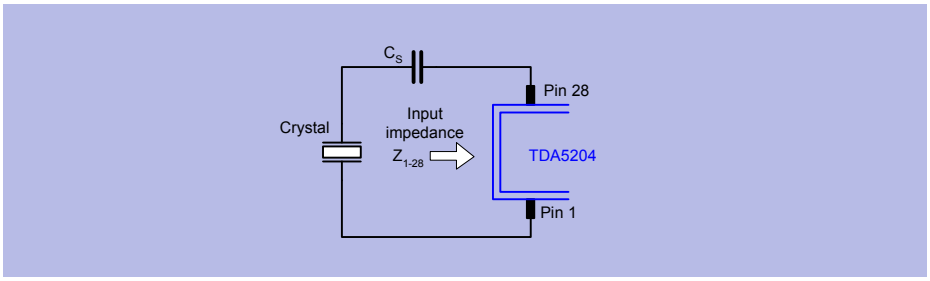


Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

The quartz oscillator input impedance consists of a negative resistance and an inductance L.

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + (2\pi f)^2 L}$$

with C_L the load capacitance (refer to the quartz crystal specification).

Examples with typ. values:

6.26 MHz:	C_L = 12 pF	L=21uH	C_S = 8.6 pF
12.52 MHz:	C_L = 12 pF	L=19uH	C_S = 5 pF

These values may be obtained by putting two capacitors in series to the quartz.

4.4 Quartz Frequency Calculation

The quartz frequency is calculated by using the following formula:

$f_{QU} = (f_{RF} \pm 10.7\text{MHz}) / r$ (1),

with
- f_{RF} .... receive frequency
- +/- ... high-side / low-side injected
- f_{LO} .... local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)
- f_{QU} .... quartz oscillator frequency
- r .... ratio of local oscillator (PLL) frequency and quartz frequency as shown in the subsequent table.

Table 4-1

frequency range f_{RF}	high-side injected	low-side injected	FSEL Pin11
385...406MHz	**X**		**open**
406...428MHz		X	open
781...823MHz	X		GND
803...844MHz		X	GND

Table 4-2

quartz crystal range	CSEL Pin16
6.xx MHz	open
12.xx MHz	GND

Table 4-3

FSEL	CSEL	Ratio r (f_{LO}/f_{QU})
open	**open**	**64**
open	**GND**	**32**
GND	open	128
GND	GND	64

Example: f_{RF}=390MHz

f_{QU}=(390MHz+10.7MHz) / 64 = 6.2609375MHz

f_{QU}=(390MHz+10.7MHz) / 32 = 12.521875MHz