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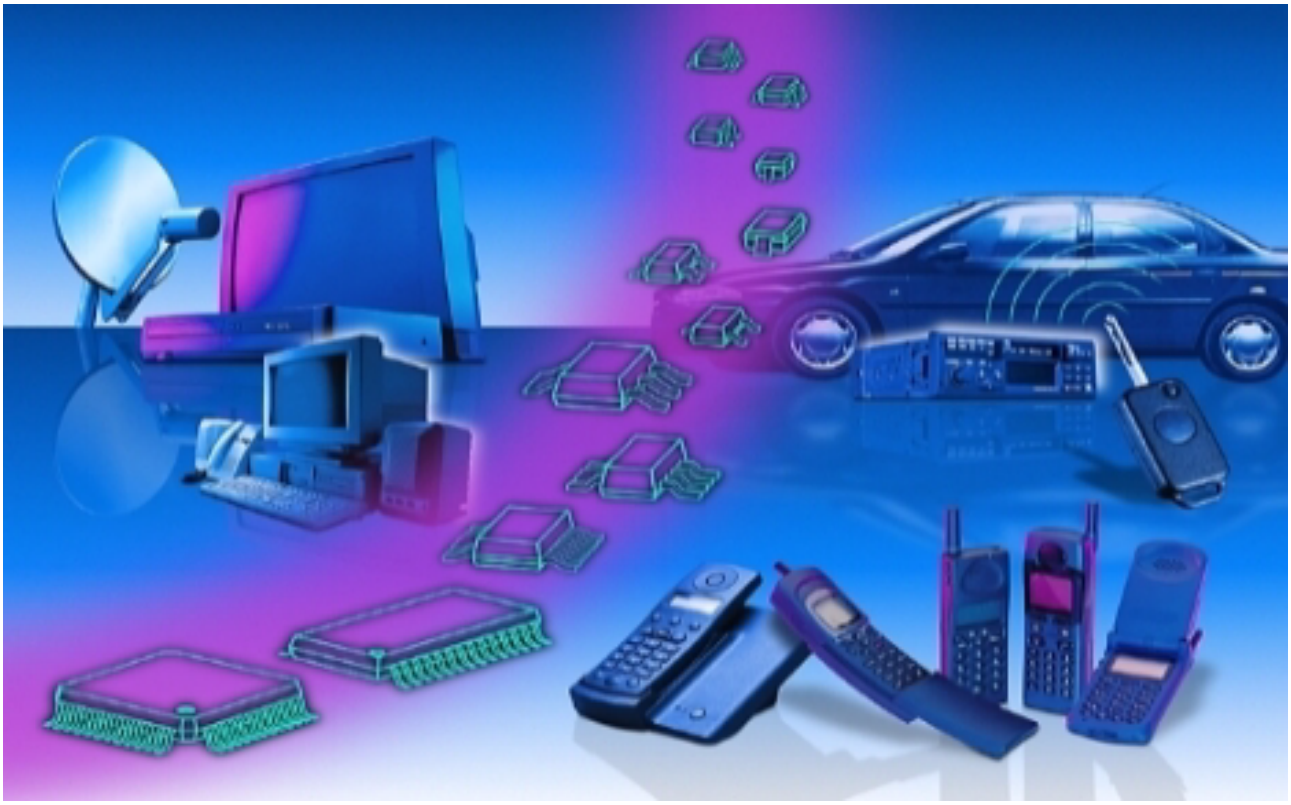

Wireless Components

ASK/FSK Single Conversion Receiver

TDA 5211 Version 2.0

Specification May 2001

Revision History

Current Version: 2.0 as of 18.05.01

Previous Version: 1.1, Dec. 2000

Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3-12	3-12	Sec. 3.4.8: max. datarate changed, Sec. 3.4.9: max. output current changed
4-4	4-4	value of a changed to 1.414
4-13	4-13	value for C2 changed to 22nF according to bill of materials, τ_2 and T_2 changed
5-3	5-3	min. supply current limits added, max. limits changed
5-4	5-4	supply current max. limit changed, min. limit added
5-5	5-5	3VOUT min. & max. limits changed, TAGC typ. & max. values changed
5-6	5-6	Section “SLICER” reworked, max. datarate at given load capacitance quoted, high output voltage limits changed, precharge current: min., max. limits changed
5-7	5-7	PDO load and leakage currents limits and typ. values changed, FSK demodulation gain min. limit changed
5-9	5-9	PDWN-current max. limit changed, supply currents min. limits added, max. limits changed, 3VOUT min. & max. limits changed, I_{TAGC_out} limits changed
5-10	5-10	Section “SLICER” reworked, max. datarate at given load capacitance quoted, high output voltage limits changed, precharge current: min., max. limits changed, PDO output voltage removed
5-15	5-15	C18 value changed

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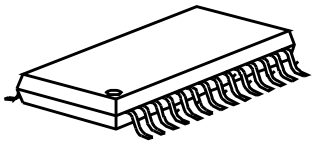
Product Info

General Description

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency band 310 to 350 MHz that is pin compatible with the ASK Receiver TDA5201. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (Is = 5.7 mA typ. in FSK mode, Is = 5 mA typ. in ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -110 dBm over specified temperature range (- 40 to +105°C)
- Selectable frequency ranges 310-330 MHz and 330-350 MHz
- Limiter with RSSI generation, operating at 10.7MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- FSK sensitivity better than -102 dBm over specified temperature range (- 40 to +105°C)

Applications

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5211	Q67037-A1147	P-TSSOP-28-1
samples available		

1 Table of Contents

2 Product Description

Contents of this Chapter

2.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for receive frequencies between 310 and 350 MHz that is pin compatible to the ASK Receiver TDA5201. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

2.3 Features

- Low supply current (I_S = 5.7 mA typ.FSK mode, 5mA typ. ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity ASK -113dBm typ. at 25°C, better than -110dBm over complete specified operating temperature range (-40 to +105°C)
- RF input sensitivity FSK -105dBm typ. at 25°C, better than -102dBm over complete specified operating temperature range (-40 to +105°C)
- Receive frequency range between 310 and 350 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

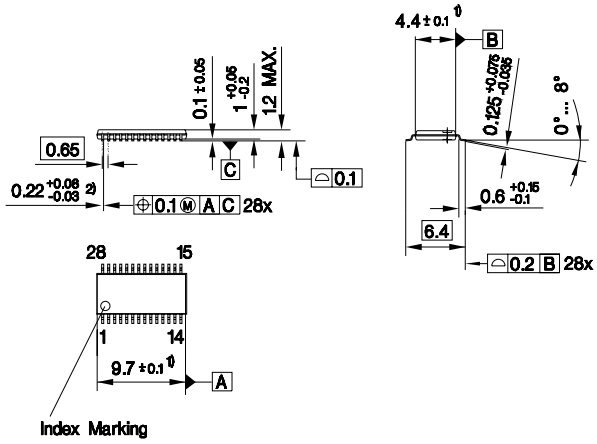
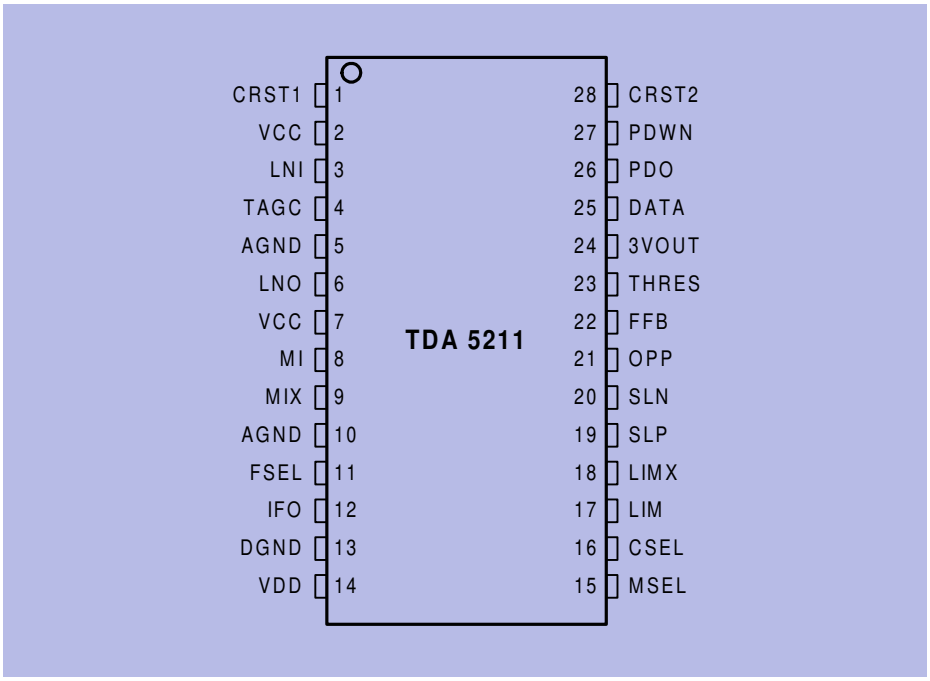


Figure 2-1 P-TSSOP-28-1 package outlines

3 Functional Description

Contents of this Chapter

3.1 Pin Configuration



Pin_Configuration_5211.wmf

Figure 3-1 IC Pin Configuration

3.2 Pin Definition and Function

In the subsequent table the internal circuits connected to the pins of the device are shown. ESD-protection circuits are omitted to ease reading.

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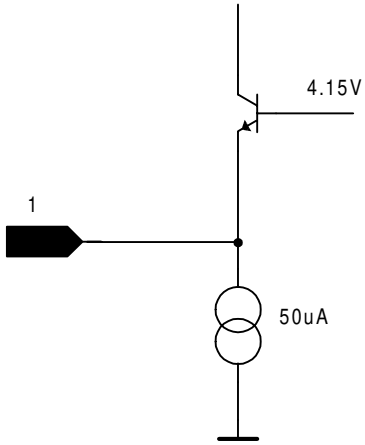
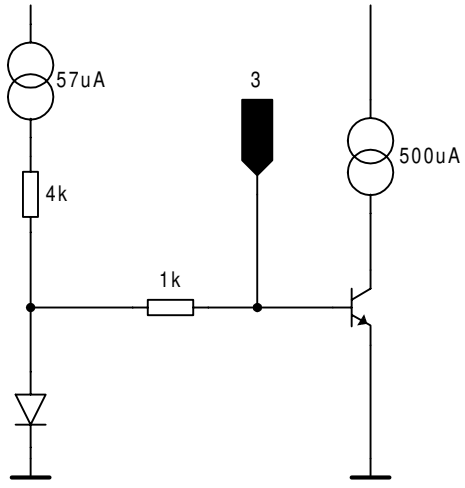
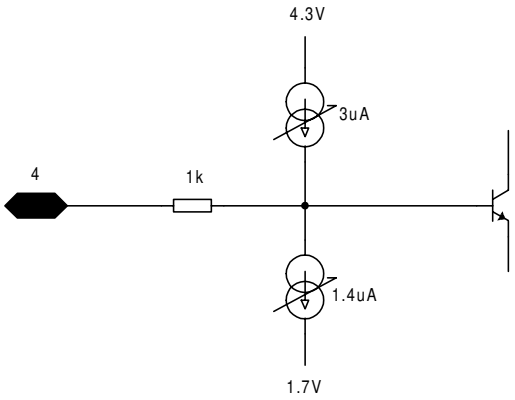
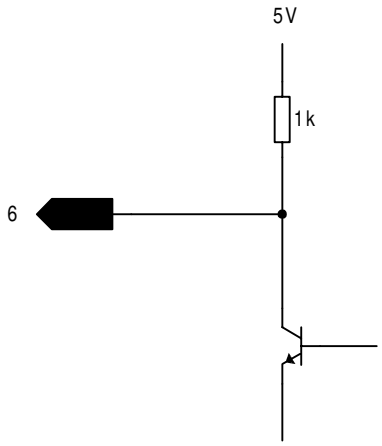
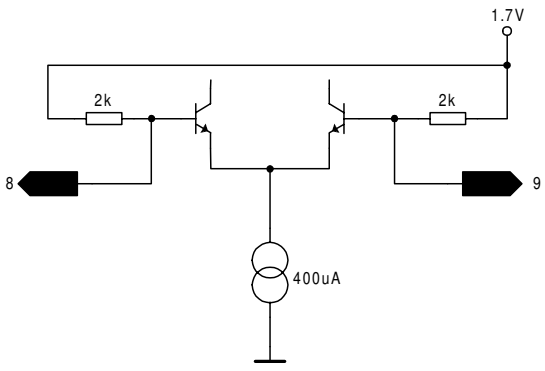
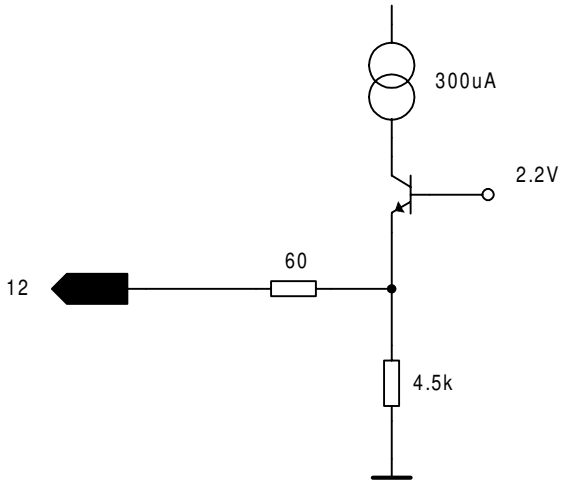
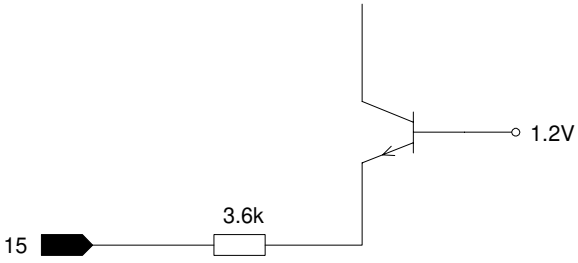
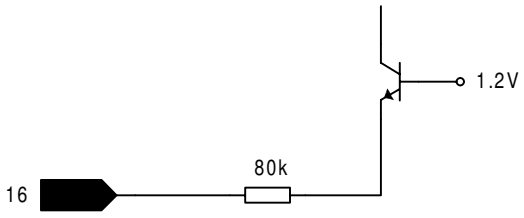
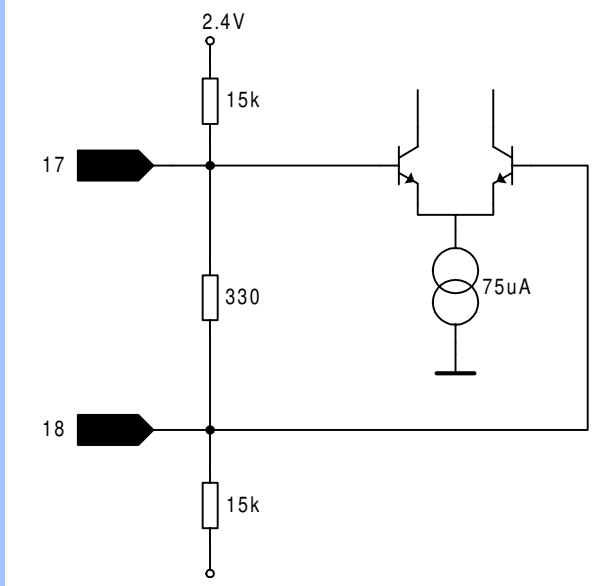
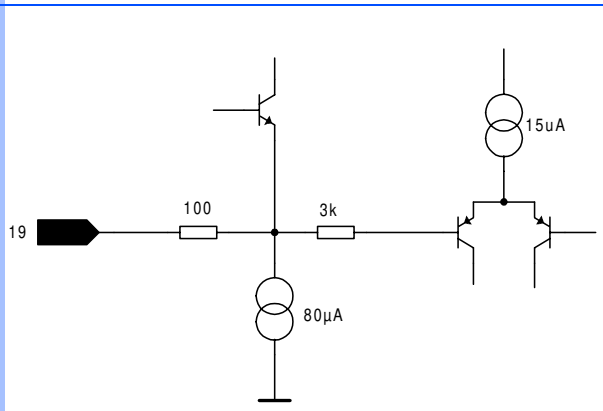
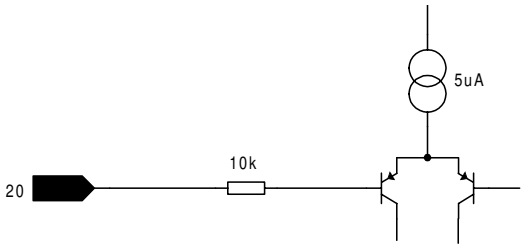
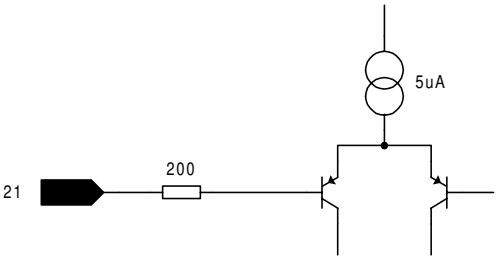
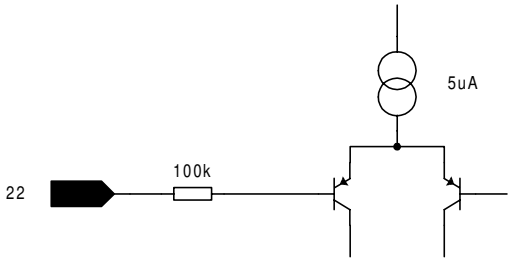
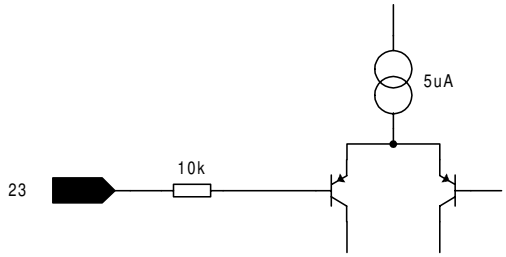
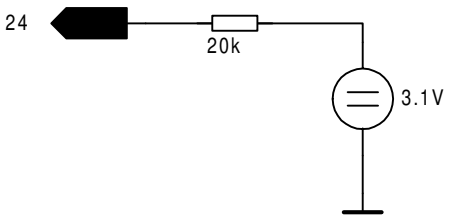
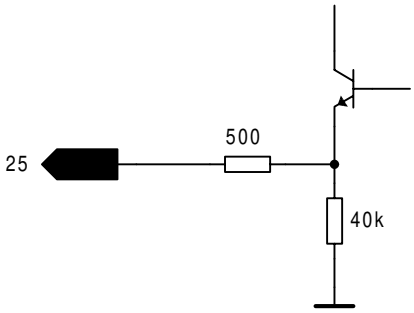
Table 3-1 Pin Definition and Function

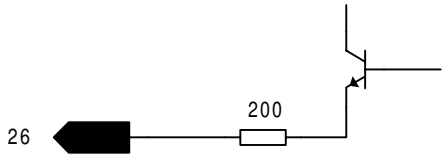
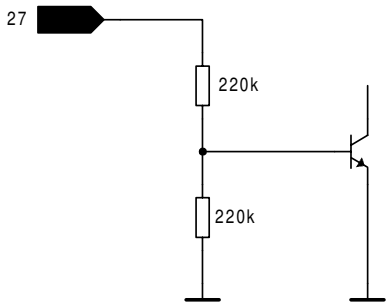
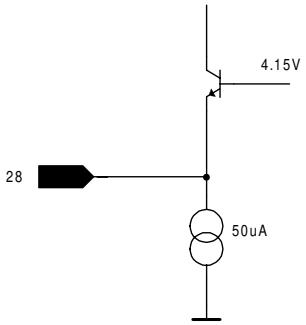
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	FSEL		not applicable - has to be left open

12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	MSEL		ASK/FSK Modulation Format Selector
16	CSEL		6.xx or 13.xx MHz Quartz Selector

17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input

22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output

26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram

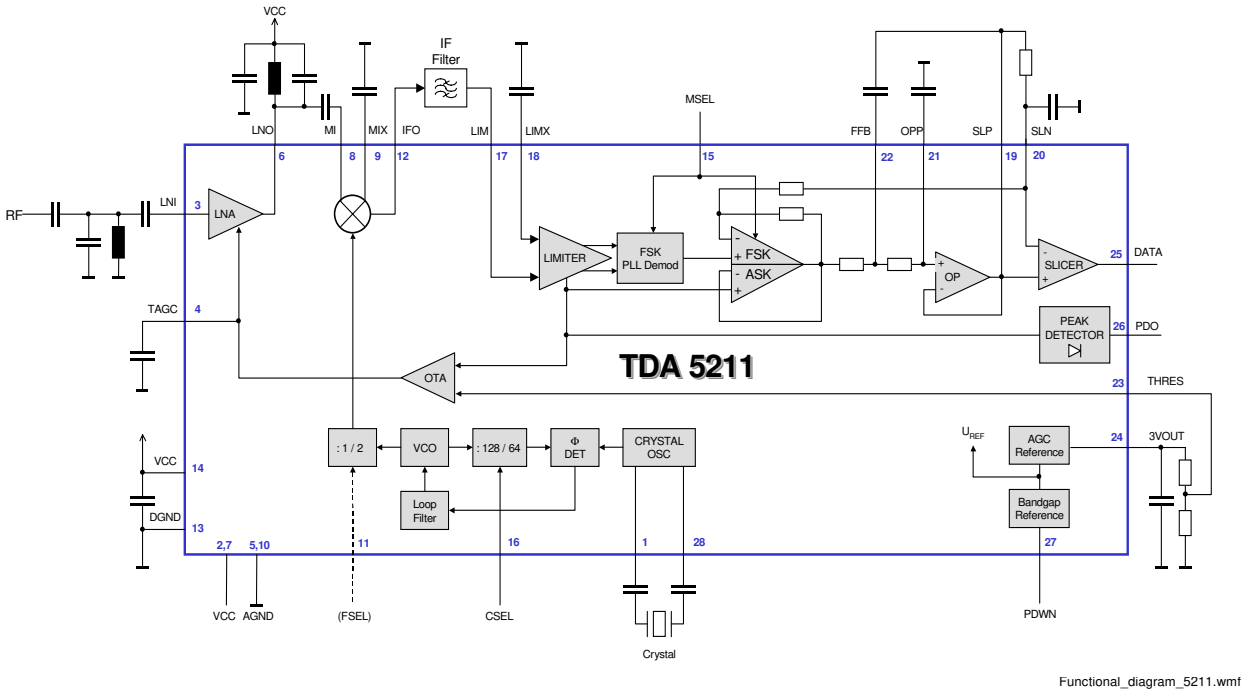


Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be deter-

mined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 310-350MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The **FSEL** pin (Pin11) has to be left open. The tuning range of the VCO was designed to guarantee over production spread and the specified temperature range a receive frequency range between 310 and 350MHz depending on whether high- or low-side injection of the local oscillator is used. The oscillator signal is fed both to the synthesiser divider chain and to a divider that is dividing the signal by 2 before it is applied to the downconverting mixer. Local oscillator high side injection has to be used for receive frequencies between approximately 310 and 330 MHz, low side injection for receive frequencies between 330 and 350MHz - see also Section 4.4..

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 5 and 10MHz range as the overall division ratio of the PLL can be switched between 32 and 64 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-2 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	5.xx MHz
Shorted to ground	10.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is explained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4-2. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be left open as described in the next chapter.

3.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 140µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic ones and high frequencies demodulated to logic zeroes. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 330MHz (e.g. 345MHz). In case of receive frequencies below 330MHz (e.g.315MHz) high frequencies are demodulated as logical ones due to a sign inversion in the downconversion mixing process. See also Section 4.4.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 4.6.

Table 3-3 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

3.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for sbsequent circuits. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. The output current is typically 950µA, the discharge current is lower than 2µA. Note that the RSSI level is also output in case of FSK mode.

3.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 3-4 PDWN Pin Operating States

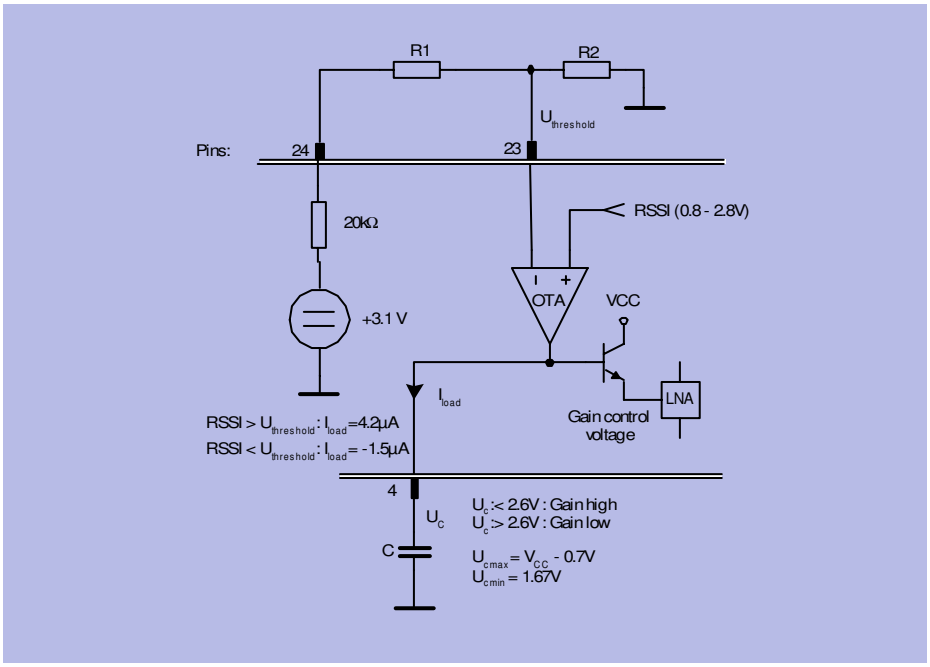
PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

Contents of this Chapter

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

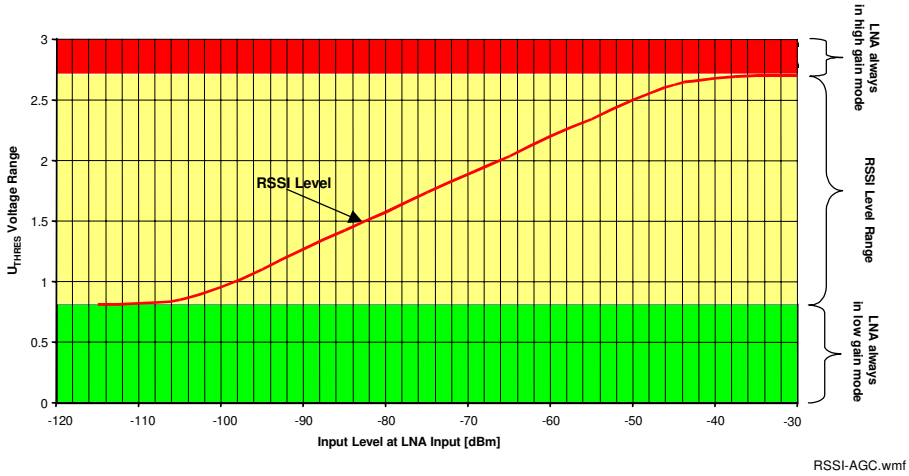


Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1] and a threshold voltage of 1.8V

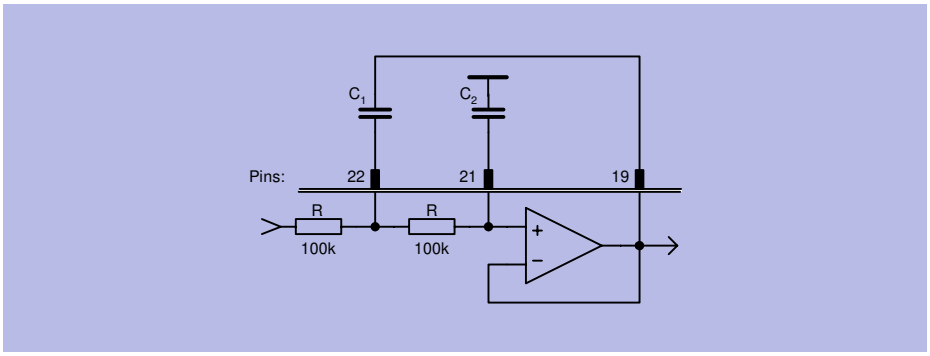
Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1. note the 20kΩ resistor in series with the 3.1V internal voltage source

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

(1)(2)

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \qquad C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$ (3)the quality factor of the poles

where

in case of a Bessel filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a Butterworth filtera = 1.414, b = 1

and thus Q = 0.71

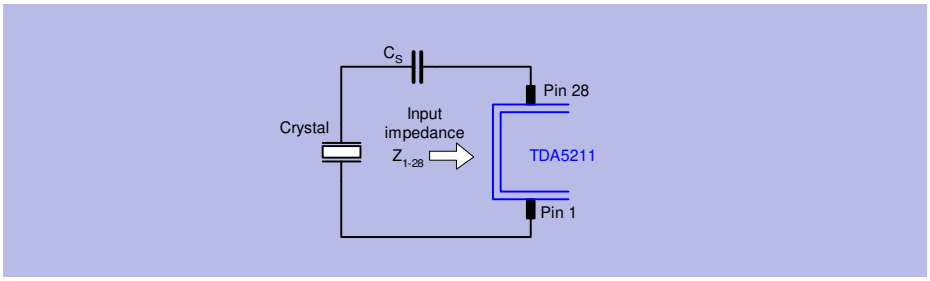
Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Quartz Load Capacitance Calculation

The value of the capacitor necessary to achieve that the quartz oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the quartz specifications given by the quartz manufacturer.



Quartz_load_5211.wmf

Figure 4-4 Determination of Series Capacitance Value for the Quartz Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_l} + 2\pi f X_L}$$

with C_l the load capacitance (refer to the quartz crystal specification).

Example:

10.18 MHz: C_L = 12 pF X_L=870 Ω C_S = 7.2 pF

This value may be obtained by putting two capacitors in series to the quartz, such as 18pF and 22pF in the 5.1MHz case and 18pF and 12pF in the 10.2MHz case.