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Data Sheet, V1.0, February 2010

SmartLEWIS™ RX+ TDA5225

Enhanced Sensitivity Multi-Channel Quad-Configuration Receiver with Digital Slicer

Wireless Control

Never stop thinking.

Edition February 19, 2010

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Data Sheet, V1.0, February 2010

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Enhanced Sensitivity Multi-Channel Quad-Configuration Receiver with Digital Slicer

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TDA5225

Revision Number: **010**
Revision History: **2010-02-19** V1.0

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Page	Subjects (major changes since last revision)
Page 26	Update of Figure 9
Page 28	Update of Figure 10
Page 30	AFC limitation added
Page 32	AGC setting proposal added
Page 33	New Section 2.4.6.5 ADC added
Page 34	Additional information on RSSIPRX register inserted
Page 40	Update of Figure 19
Page 41	Update of Figure 20
Page 45	Additional hint on clock and data recovery algorithm of the user software inserted
Page 49	Limitation for ISx readout and Burst-read function added
Page 51	Limitation for Burst-read function added
Page 77	Additional hints added
Page 79	Adaption of Section 4.1
Page 82	New item C7 added
Page 90 f	Comments added for items I6, I7, I8, I9, J11, J12
Page 90	Item J1 updated
Page 95	BOM components C7, C8, L1, R2 and R3 updated

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1 Product Description

1.1 Overview

The IC is a low power ASK/FSK Receiver for the frequency bands 300-320, 425-450, 863-870 and 902-928 MHz.

The chip offers a very high level of integration and needs only a few external components.

The device is qualified to automotive quality standards and operates between -40 and +105°C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

The receiver is realized as a double down conversion super-heterodyne/low-IF architecture each with image rejection. A fully integrated Sigma-Delta Fractional-N PLL Synthesizer allows for high-resolution frequency generation and uses a crystal oscillator as the reference. The on-chip temperature sensor may be utilized for temperature drift compensation via the crystal oscillator.

The high performance down converter is the key element for the exceptional sensitivity performance of the device which take it close to the theoretical top-performance limits. It demodulates the received ASK or FSK data stream independently which can then be accessed via separate pins. The RSSI output signal is converted to the digital domain with an ADC. All these signals are accessible via the 4-wire SPI interface bus. Up to 4 pre-configured telegram parameters can be stored into the device offering independent pre-processing of the received data to an extent not available till now. The down converter can be also configured in single-conversion mode at moderately reduced selectivity performance but at the advantage of omitting the IF ceramic filter.

1.2 Features

- Enhanced sensitivity receiver
- Multi-band/Multi-Channel (300-320, 425-450, 863-870 and 902-928 MHz)
- One crystal frequency for all supported frequency bands
- 21-bit Sigma-Delta Fractional-N PLL synthesizer with high resolution of 10.5 Hz
- Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources
- Up to 12 different frequency channels are supported with 10.5 Hz resolution each
- Ultrafast Wake-up on RSSI
- Selectable IF filter bandwidth and optional external filters possible
- Double down conversion image reject mixer
- ASK and FSK capability
- Automatic Frequency Control (AFC) for carrier frequency offset compensation
- NRZ data processing capability
- Sliced data output
- RSSI peak detectors
- Wake-up generator and polling timer unit
- Unique 32-bit serial number
- On-chip temperature sensor
- Integrated timer usable for external watch unit
- Integrated 4-wire SPI interface bus
- Supply voltage range 3.0 Volts to 3.6 Volts or 4.5 Volts to 5.5 Volts
- Operating temperature range -40 to +105°C
- ESD protection +/- 2 kV on all pins
- Package PG-TSSOP-28

1.3 Applications

- Remote keyless entry systems
- Remote start applications
- Tire pressure monitoring
- Short range radio data transmission
- Remote control units
- Cordless alarm systems
- Remote metering

2 Functional Description

2.1 Pin Configuration

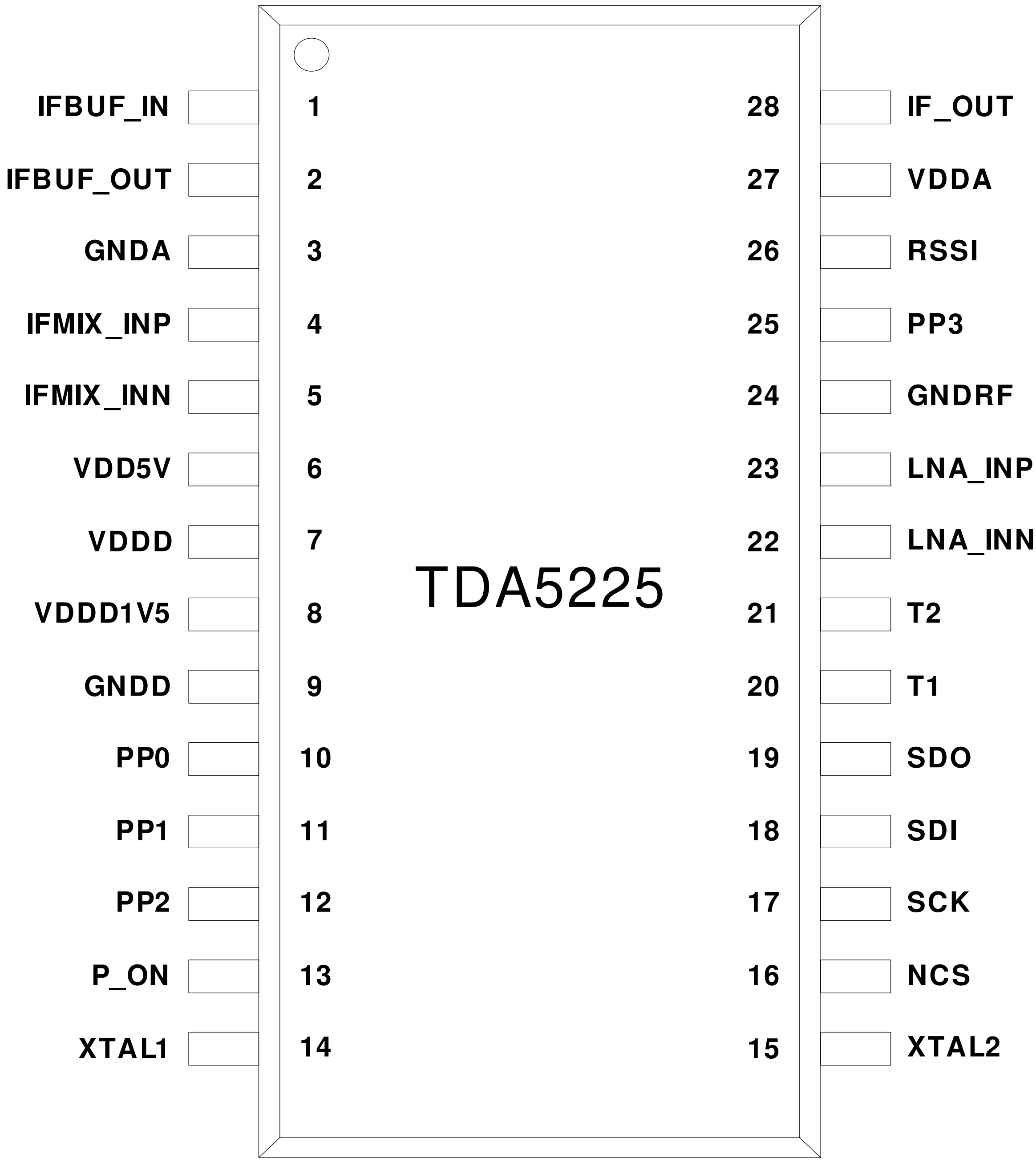
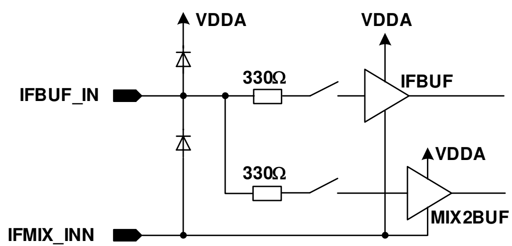
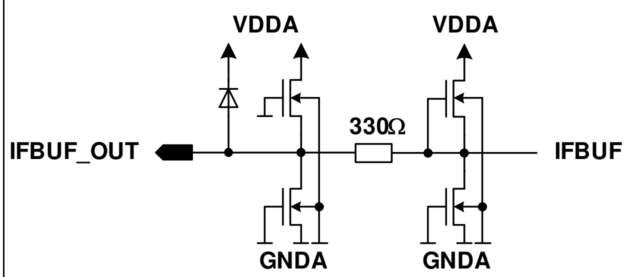
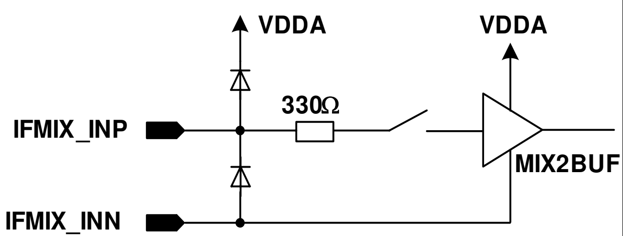
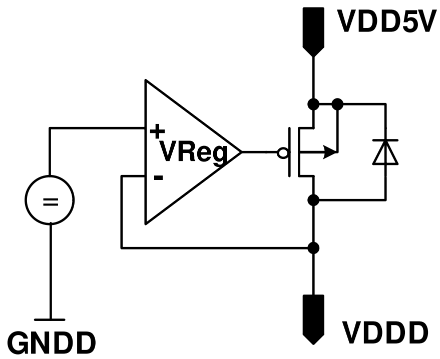
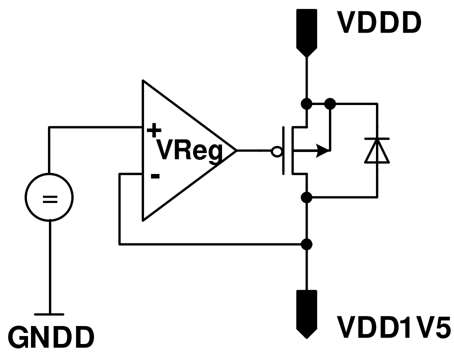
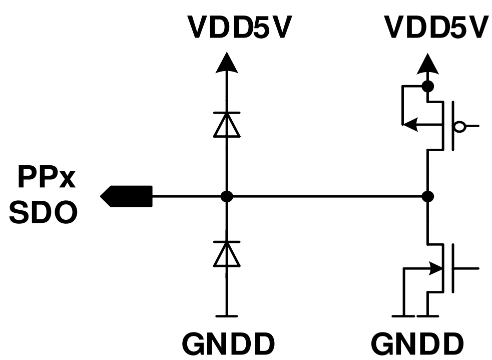


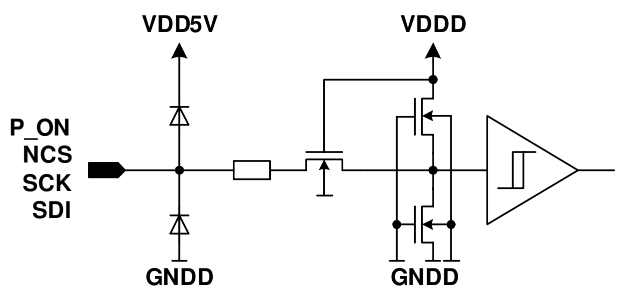
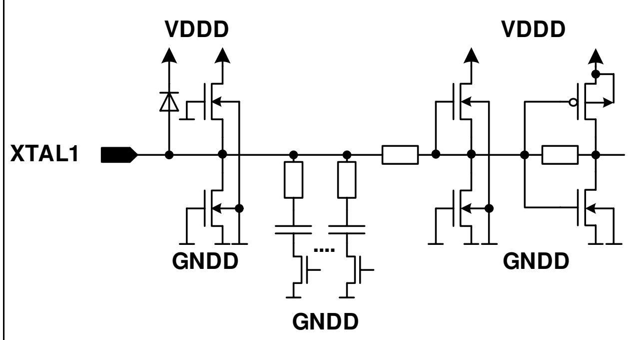
Figure 1 Pin-out

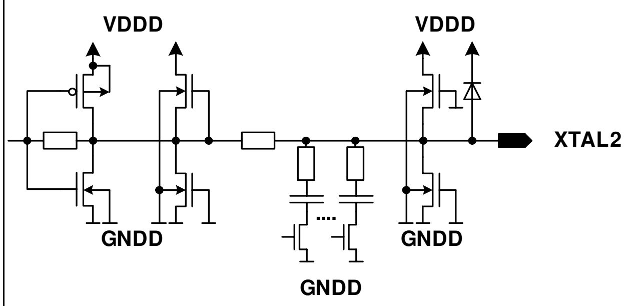
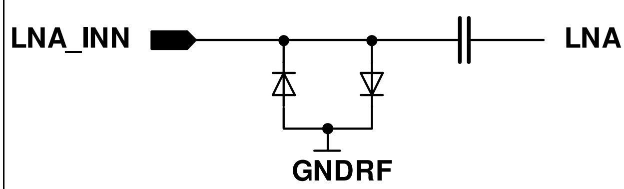
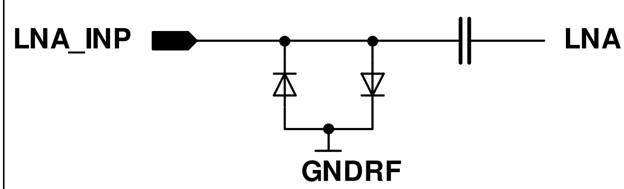
2.2 Pin Definition and Pin Functionality

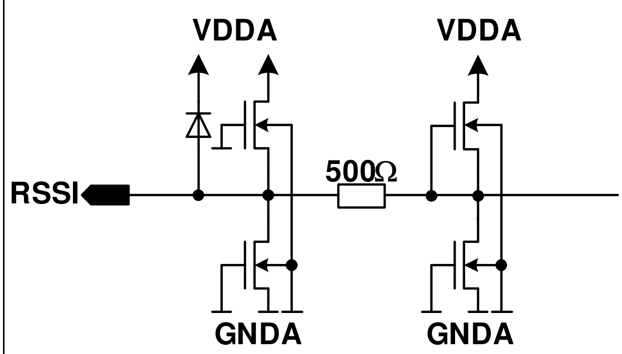
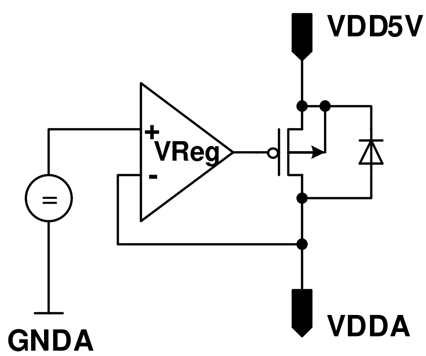
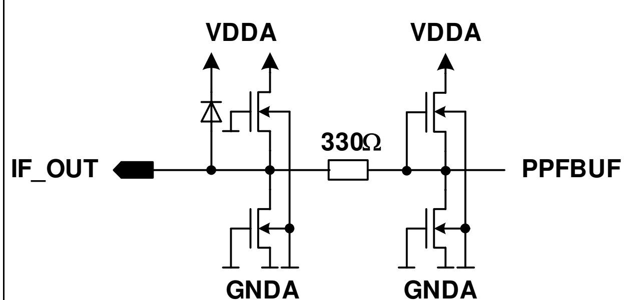
Table 1 Pin Definition and Function

Pin No.	Pad name	Equivalent I/O Schematic	Function
1	IFBUF_IN		Analog input IF Buffer input Note: Input is biased at VDDA/2
2	IFBUF_OUT		Analog output IF Buffer output
3	GNDA		Analog ground
4	IFMIX_INP		Analog input + IF mixer input Note: Input is biased at VDDA/2
5	IFMIX_INN	see schematic of Pin 1 and 4	Analog input. - IF mixer input
6	VDD5V		Analog input 5 Volt supply input

Pin No.	Pad name	Equivalent I/O Schematic	Function
7	VDDD		Analog input digital supply input
8	VDDD1V5		Analog output 1.5 Volt voltage regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR (Special Function Register), default = CLK_OUT

Pin No.	Pad name	Equivalent I/O Schematic	Function
11	PP1	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = DATA
12	PP2	see schematic of Pin 10	Digital output CLK_OUT, RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = NINT
13	P_ON		Digital input power-on reset
14	XTAL1		Analog input crystal oscillator input

Pin No.	Pad name	Equivalent I/O Schematic	Function
15	XTAL2		Analog output crystal oscillator output
16	NCS	see schematic of Pin 13	Digital input SPI enable
17	SCK	see schematic of Pin 13	Digital input SPI clock
18	SDI	see schematic of Pin 13	Digital input SPI data in
19	SDO	see schematic of Pin 10	Digital output SPI data out
20	T1		Digital input, connect to Digital Ground
21	T2		Digital input, connect to Digital Ground
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input + RF input
24	GNDRF		RF analog ground

Pin No.	Pad name	Equivalent I/O Schematic	Function
25	PP3	see schematic of Pin 10	Digital output RX_RUN, NINT, LOW, HIGH, DATA and DATA_MATCHFIL are programmable via a SFR, default = RX_RUN
26	RSSI		Analog output analog RSSI output/ analog test pin ANA_TST
27	VDDA		Analog input Analog supply
28	IF_OUT		Analog output IF output

2.3 Functional Block Diagram

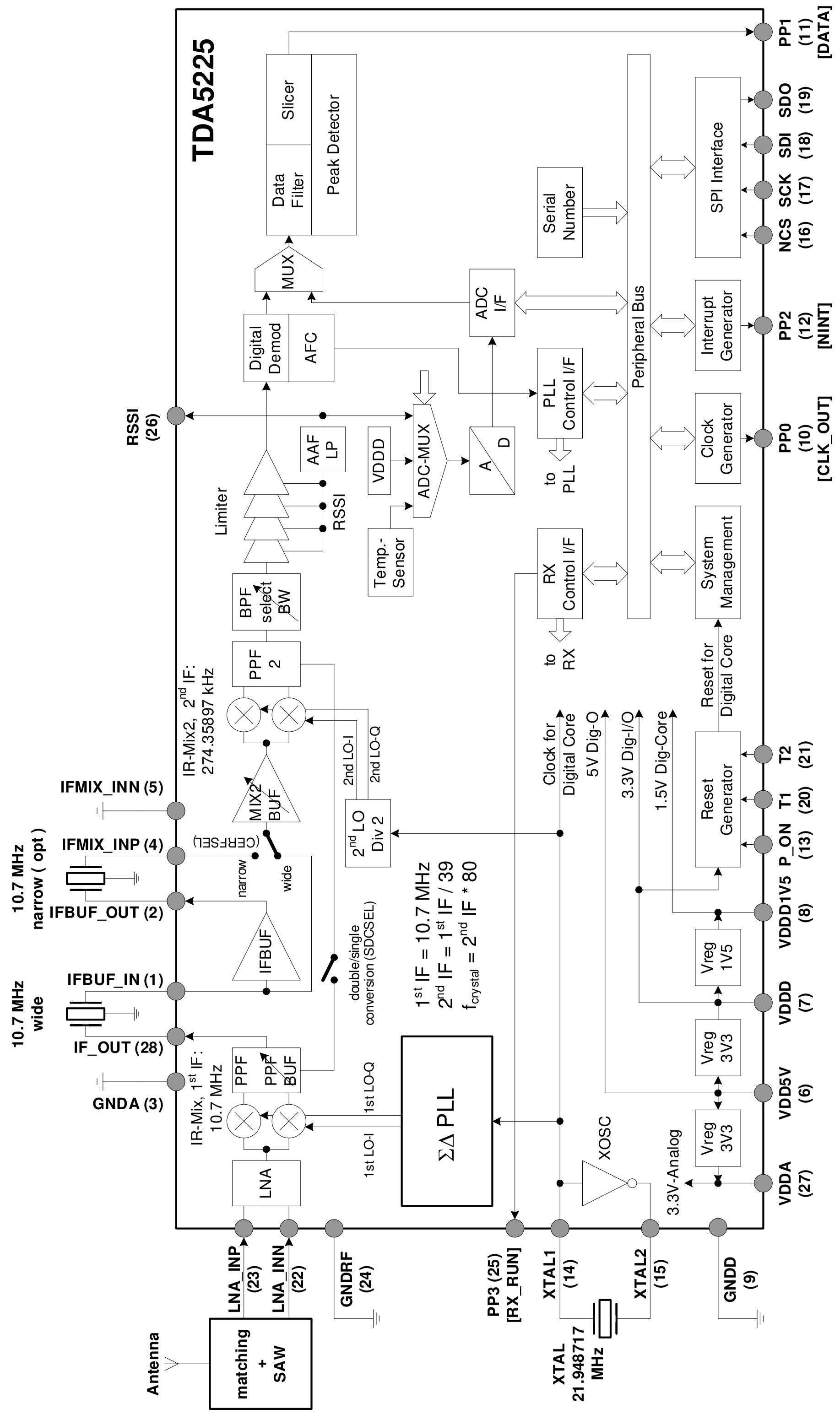


Figure 2 TDA5225 Block Diagram[1)]

1) The function on each PPx port pin can be programmed via SFR (see also **Table 1**). Default values are given in squared brackets in **Figure 2**.

2.4 Functional Block Description

2.4.1 Architecture Overview

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 425-450 MHz, 863-870 MHz, 902-928 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications.

For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

For Multi-Channel systems where even higher channel separation is required, up to two (switchable) external ceramic (CER) filters can be used to improve the selectivity.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution.

The harmonic suppressed limiter output signal feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer.

A digital receiver, which comprises RSSI peak detectors, a matched data filter and a data slicer, decodes the received ASK or FSK data stream. The received data signal is accessible via one of the port pins.

The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2^{nd} local oscillator signal. To accelerate the start up time of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

2.4.2 Block Overview

The TDA5225 is separated into the following main blocks:

- **RF / IF Receiver**
- **Crystal Oscillator and Clock Divider**
- **Sigma-Delta Fractional-N PLL Synthesizer**
- **ASK / FSK Demodulator incl. AFC, AGC and ADC**
- **RSSI Peak Detector**
- **Digital Baseband Receiver**
- **Power Supply Circuitry**
- **System Interface**
- **System Management Unit**

2.4.3 RF/IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located around 10.7 MHz and the second IF frequency around 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two low-side injected I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter (optionally by two, decoupled by a buffer amplifier). For moderate or low cost applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency. The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps. For a frequency offset of -150 kHz to -120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configurable via PPCFG2 register.

The frequency relations are calculated with the following formulas:

$$f_{IF1} = 10.7\text{MHz}$$

$$f_{IF2} = \frac{f_{IF1}}{39}$$

$$f_{crystal} = f_{IF2} \times 80$$

$$f_{LO2} = \frac{f_{crystal}}{2}$$

$$f_{LO1} = f_{crystal} \times NF_{divider}$$

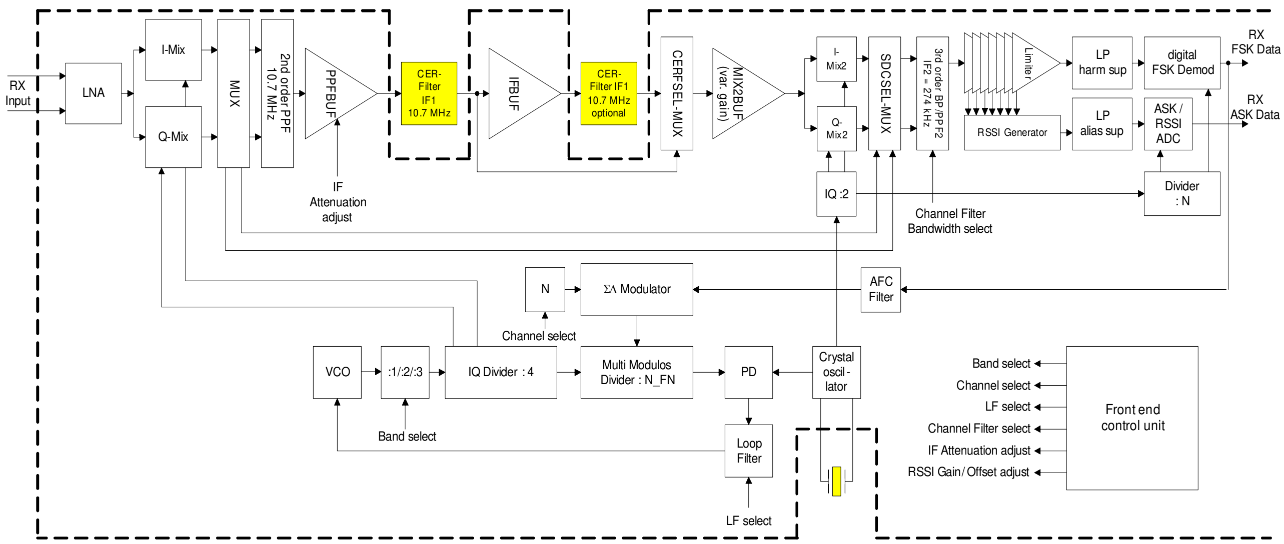


Figure 3 Block Diagram RF Section

The front end of the receiver comprises an LNA, an image reject mixer and a digitally gain controlled buffer amplifier. This buffer amplifier allows the production spread of the on-chip signal strip, of external matching circuitry and RF SAW and ceramic IF filters to be trimmed. The second image reject mixer down converts the first IF to the second IF.

The bandpass filter follows the subsequent formula:

$$f_{center} = \sqrt{f_{corner,\,low} \times f_{corner,\,high}}$$

Therefore asymmetric corner frequencies can be observed. The use of AFC results in more symmetry.

A multi-stage bandpass limiter at a center frequency of 274 kHz completes the receiver chain. The -3dB corner frequencies of the bandpass limiter are typically at 75 kHz and at 520 kHz.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via a programmable anti-aliasing filter this signal is converted to the digital domain by means of a 10-bit ADC.

The limiter output signal is connected to a digital FSK demodulator.

The immunity against strong interference frequencies (so called blockers) is determined by the available filter bandwidth, the filter order and the 3rd order intercept point of the front end stages. For Single-Channel applications with moderate requirements to the selectivity the performance of the on-chip 3rd order bandpass polyphase filter might be sufficient. In this case no external filters are necessary and a single down conversion architecture can be used, which converts the input signal frequency directly to the 2nd IF frequency of 274 kHz.

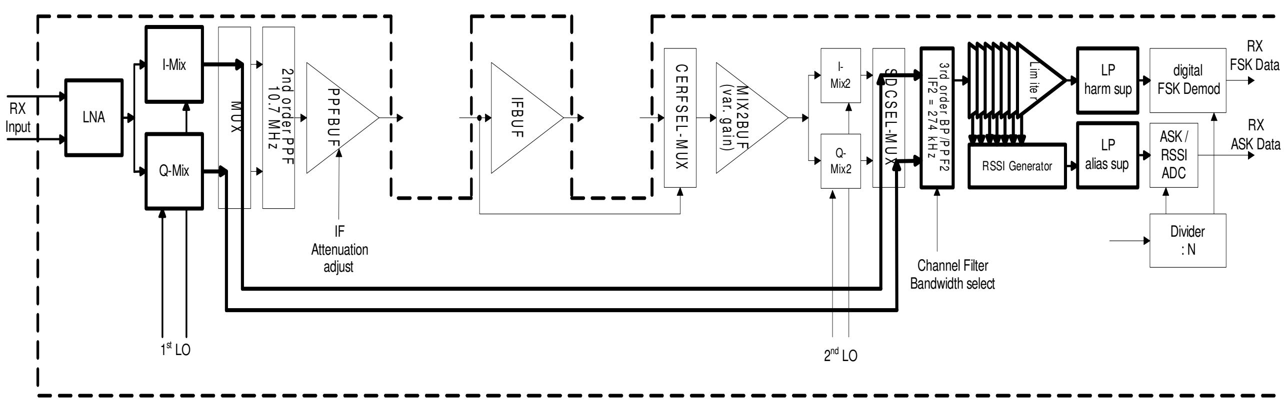


Figure 4 Single Down Conversion (SDC, no external filters required)

For Multi-Channel applications or systems which demand higher selectivity the double down conversion scheme together with one or two external CER filters can be selected. The order of such ceramic filters is in a range of 3, so the selectivity is further improved and a better channel separation is guaranteed.

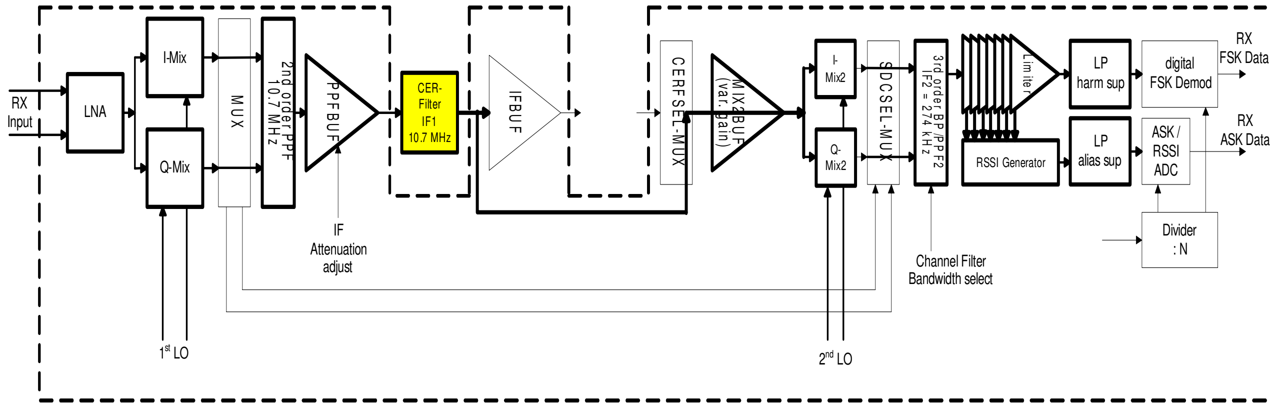


Figure 5 Double Down Conversion (DDC) with one external filter

For applications which demand very high selectivity and/or channel separation even two CER filters may be used. Also in applications where one channel requires a wider bandwidth than the other (e.g. TPMS and RKE) the second filter can be by-passed.

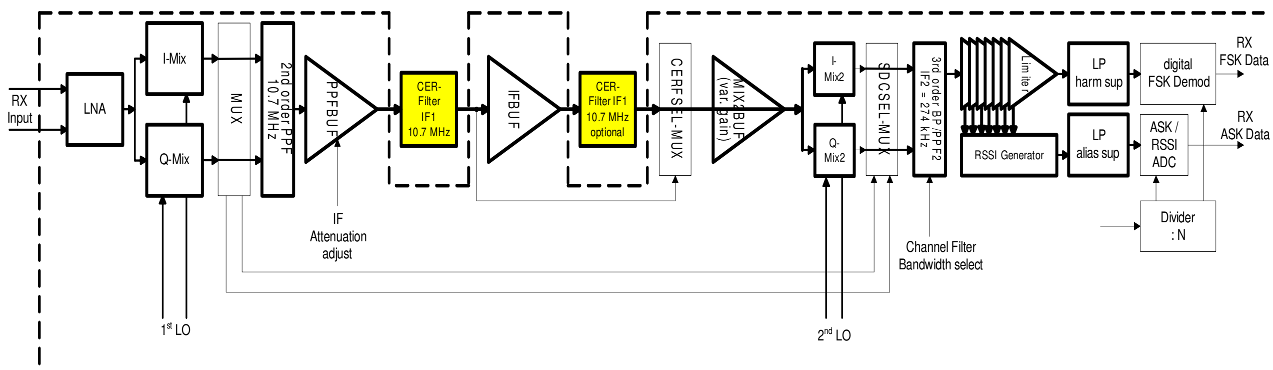


Figure 6 Double Down Conversion (DDC) with two external filters

2.4.4 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator which operates together with the crystal in parallel resonance mode. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly detuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration registers XTALCALx. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the desired value. The SFR control bit XTALHPMS can be used to activate the High Precision Mode also during SLEEP Mode.

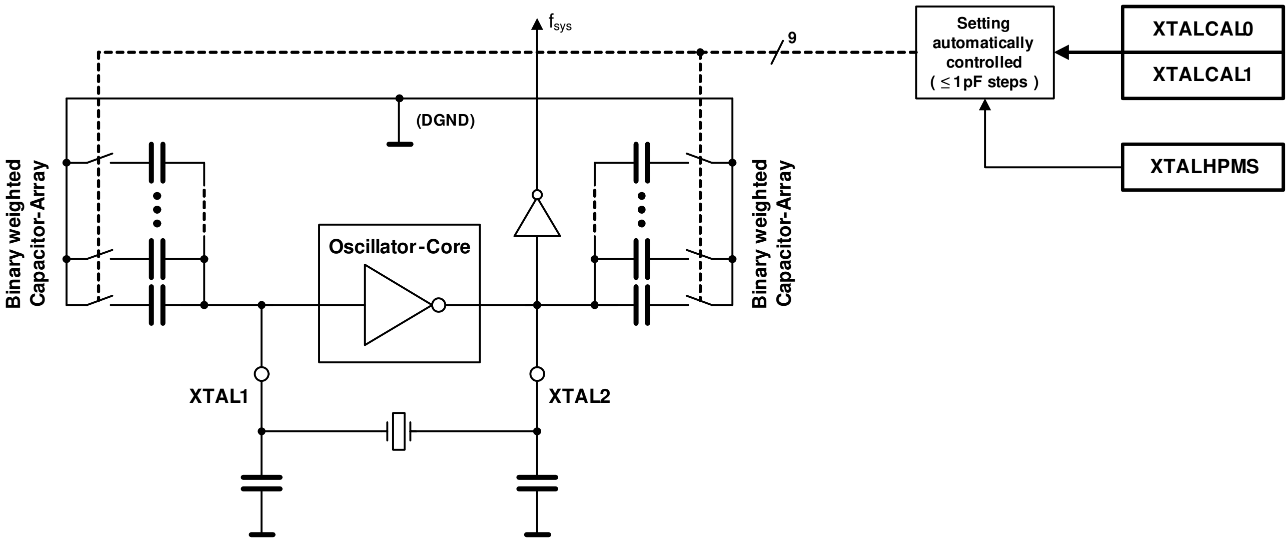


Figure 7 Crystal Oscillator

Recommended Trimming Procedure

• Set the registers XTALCAL0 and XTALCAL1 to the expected nominal values
• Set the TDA5225 to Run Mode Slave
• Wait for 0.5ms minimum
• Trim the oscillator by increasing and decreasing the values of XTALCAL0/1
• Register changes larger than 1 pF are automatically handled by the TDA5225 in 1 pF steps
• After the Oscillator is trimmed, the TDA5225 can be set to SLEEP mode and keeps these values during SLEEP mode
• Add the settings of XTALCAL0/1 to the configuration. It must be set after every power up or brownout!

Using the High Precision Mode

As discussed earlier, the TDA5225 allows the crystal oscillator to be trimmed by the use of internal trim capacitors. It is also possible to use the trim functionality to compensate temperature drift of crystals.
During Run Mode (always when the receiver is active) the capacitors are automatically connected and the oscillator is working in the High Precision Mode.
On entering SLEEP Mode, the capacitors are automatically disconnected to save power.
If the High Precision Mode is also required for SLEEP Mode, the automatic disconnection of trim capacitors can be avoided by setting XTALHPMS to 1 (enable XTAL High Precision Mode during SLEEP Mode).

External Clock Generation Unit

A built in programmable frequency divider can be used to generate an external clock source out of the crystal reference. The 20 bit wide division factor is stored in the registers CLKOUT0, CLKOUT1 and CLKOUT2. The minimum value of the programmable frequency divider is 2. This programmable divider is followed by an additional divider by 2, which generates a 50% duty cycle of the CLK_OUT signal. So the maximum frequency at the CLK_OUT signal is the crystal frequency divided by 4. The minimum CLK_OUT frequency is the crystal frequency divided by 2^{21}.

To save power, this programmable clock signal can be disabled by the SFR control bit CLKOUTEN. In this case the external clock signal is set to low.

The resulting CLK_OUT frequency can be calculated by:

$$f_{CLKOUT} = \frac{f_{sys}}{2 \cdot \mathrm{divisionfactor}}$$

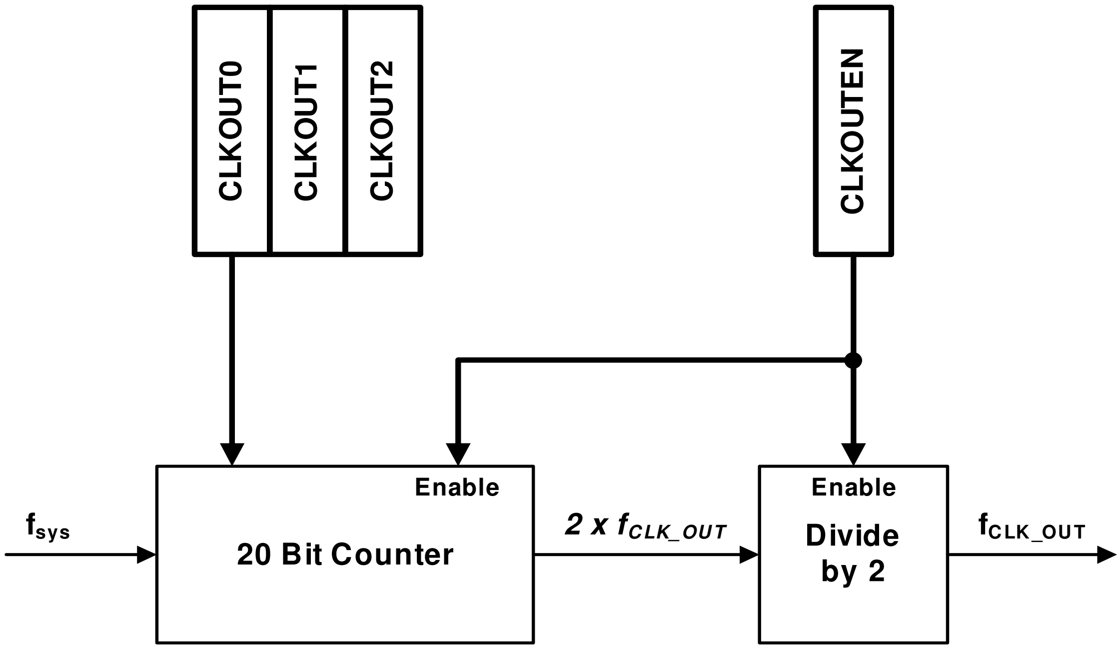


Figure 8 External Clock Generation Unit

The maximum CLK_OUT frequency is limited by the driver capability of the PPx pin and depends on the external load connected to this pin. Please be aware that large loads and/or high clock frequencies at this pin may interfere with the receiver and reduce performance.

After Reset the PPx pin is activated and the division factor is initialized to 11 (equals f_{CLK_OUT} = 998 kHz).

A clock output frequency higher than 1 MHz is not supported.

For high sensitivity applications, the use of the external clock generation unit is not recommended.

2.4.5 Sigma-Delta Fractional-N PLL Block

The Sigma-Delta Fractional-N PLL is fully integrated on chip. The ***V**oltage **C**ontrolled* ***O**scillator* (VCO) with on-chip LC-tank runs at approximately 3.6 GHz and is first divided with a band select divider by 1, 2 or 3 and then with an I/Q-divider by 4 which provides an orthogonal local oscillator signal for the first image reject mixer with the necessary high accuracy.
The multi-modulus divider determines the channel selection and is controlled by a 3rd order Sigma-Delta Modulator (*SDM*). A type IV phase detector, a charge pump with programmable current and an on-chip loop filter closes the phase locked loop.

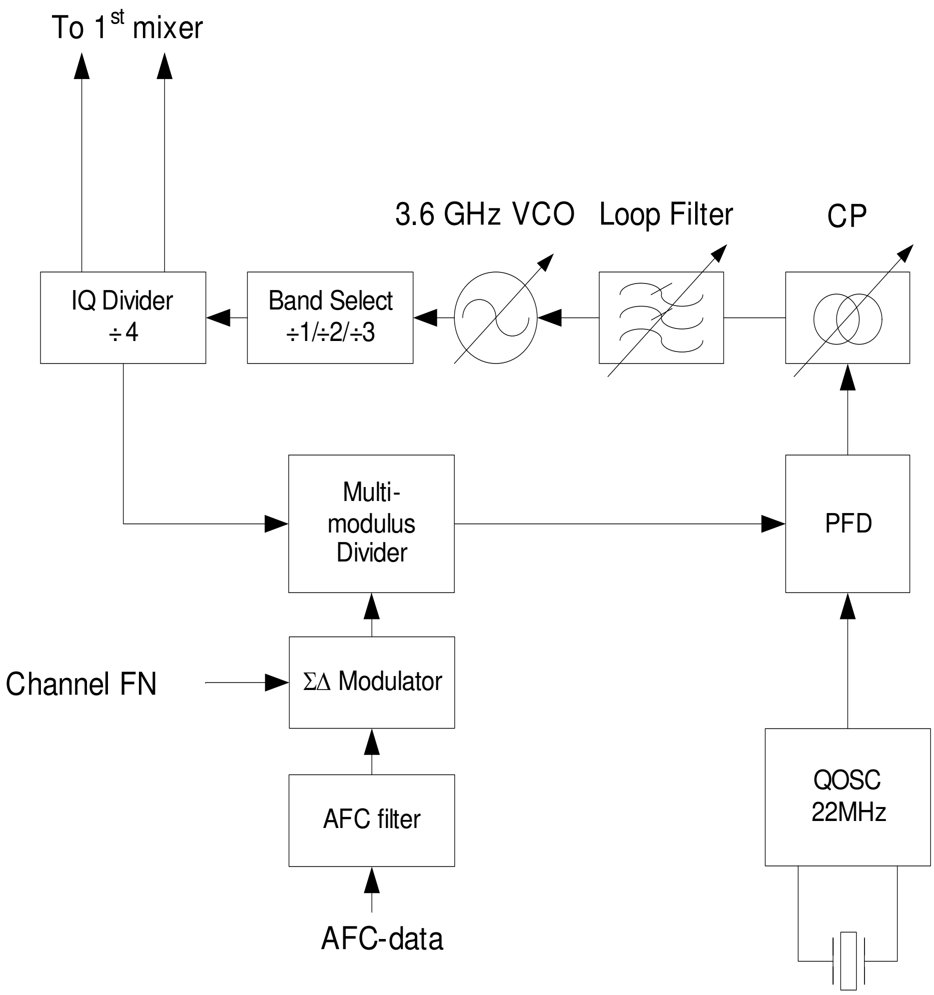


Figure 9 Synthesizer Block Diagram

When defining a Multi-Channel system, the correct selection of channel spacing is extremely important. A general rule is not possible, but following must be considered:
• If an additional SAW filter is used, all channels including their tolerances have to be inside the SAW filter bandwidth.
• The distance between channels must be high enough, that no overlapping can occur. Strong input signals may still appear as recognizable input signal in the neighboring channel because of the limited suppression of IF Filters. Example: a typical 330kHz IF filter has at 10.3 MHz (10.7 MHz - 0.4 MHz) only 30 dB suppression. A -70 dBm input signal appears like a -100 dBm signal, which is inside the receiver sensitivity. In critical cases the use of two IF filters must be considered. See also **Chapter 2.4.3 RF/IF Receiver**.

2.4.5.1 PLL Dividers

The divider chain consists of a band select divider 1/2/3, an I/Q-divider by 4 which provides an orthogonal 1st local oscillator signal for the first image reject mixer with the necessary high accuracy and a multi-modulus divider controlled by the Sigma-Delta Modulator. With the band select divider, the wanted frequency band is selected. Divide by 1 selects the 915 MHz and 868 MHz band, divide by 2 selects the 434 MHz band and divide by 3 selects the 315 MHz band. The ISM band selection is done via bit group BANDSEL in x_PLLINTC1 register.

2.4.5.2 Digital Modulator

The 3rd order ***Sigma-Delta Modulator (SDM)*** has a 22 bit wide input word, however the LSB is always high, and is clocked by the XTAL oscillator. This determines the achievable frequency resolution.

The ***Automatic Frequency Control Unit*** filters the actual frequency offset from the FSK demodulator data and calculates the necessary correction of the divider factor to achieve the nominal IF center frequency.