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TDA5230
TDA5231

Universal Low Power ASK/FSK Single Conversion Multi-Channel Image-Reject Receiver with Digital Baseband Processing

Wireless Control Components

Never stop thinking.

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Page prev. version	Page current version	Subjects (changes since previous revision)
all	**all**	Rework of all chapters Product description enhanced by additional short form information Functional description, explanations added, full SFR information in each chapter Reference: some characteristics added, FSK demodulator BW changed to practical measurement method

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Page prev. version	Page current version	Subjects (changes since previous revision)
	4	IF MUX added in **Chapter 1 Product Description**, **Chapter 2.4.8.1 IF Filter**, and **Dual: AIF0 and BIF0: Conf. A IF Buffer Amplifier Enable**
51	**51**	Explanation for T_{ON} and T_{OFF} from **Chapter 2.4.6.2 Constant On/Off Time** to **Chapter 2.4.6.5 Permanent Wake Up Search** improved
125	**127**	Description Digital I/O pins corrected
134	**135**	Reset Value for register CMC0 corrected
	163	Minimum SPM cycletime (T_{ON} +T_{OFF}) specified
4	**4**	AEC Q100 added
	5	Order information added
all	**all**	Spelling corrections

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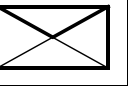


1 Product Description

1.1 Overview

The TDA523x is a family of universal, highly sensitive, low-power single-chip ASK/FSK superheterodyne image-reject-receivers for Manchester-coded data signals in the ISM bands between 302..320 MHz, 433..450 MHz and 865..870 MHz. The chips include fully-integrated digital baseband data processing and produce clean data output via SPI, thus significantly reducing the load on the host processor and standby power consumption.

The TDA523x family of chips offers a high level of integration and needs only few external components for application deployment.

The TDA523x is able to run in several autonomous self-polling and wake-up modes, scanning the received signal for usable data. Interrupts can be initiated based on various criteria, such as the received bit pattern to wake up the host processor. Received data can be scanned for certain message contents (IDs) and is stored in a FIFO data buffer, accessible via the SPI host interface.

The TDA523x is able to scan and receive from different sources with up to two different independent parameter configuration sets. Configurations can differ in modulation ASK/FSK, data rate, wake up criterion, protocol, etc. Additionally, multichannel applications are supported by scanning of up to 3 RF channels in the same band.

The TDA523x is fully programmable to facilitate quick time to market.

1.2 Key Features

- Fully integrated ASK/FSK RF Data Receiver with data FIFO and SPI host interface
- High input sensitivity: e.g. typically -108dBm at 2kbit data rate (see **Specifications**)
- Autonomous wake-up and Self-Polling features allow different modulation for wake-up and data
- Two parallel parameter sets for scanning and receiving from different sources
- Reduces significantly host processing power, system standby power consumption
- Fully integrated Multichannel PLL Synthesizer support up to 17 sub-channels
- Image Reject mixer prevents interferences on mirror frequency
- IF Filter Multiplexer allows IF bandwidth switching
- IF-Limiting Amplifier with RSSI-Output accessible via dedicated pin or register
- Data Framer with versatile Frame Synchronization capability
- Message Contents (ID) scanning
- Unique Serial-Number, accessible via SPI
- Crystal-Oscillator with on chip Fine-Tuning, Clock-Output with configurable Prescaler
- Supply Voltage Range 3.0 V to 3.6 V and 4.5 V to 5.5 V
- Package PG-TSSOP-28-1
- Operating Temperature Range -40 to +105°C
- Qualified according automotive AEC-Q100
- Evaluation boards, reference designs, and free PC configuration and evaluation tools available

1.3 Applications

- Tire Pressure Monitoring Systems
- Remote Keyless Entry Systems
- Remote Control Systems

1.4 Order Information

Type	Ordering Code	Package
TDA5230	Q62705K 791	PG-TSSOP28-1
TDA5231	SP000202847	PG-TSSOP28-1

1.5 Target Application Frequencies for TDA5230 and TDA5231

The TDA523x family of receivers cover a wide range of commonly used receive frequencies within the three major ISM-bands used in TPMS, RKE/PKE and remote control system applications.

The TDA5230 covers operation in the 433..450 MHz and 865..868 MHz ISM bands. The TDA5231 covers complementary operation in the 302..320 MHz ISM-band.

Figure 1 identifies the capabilities of the TDA5230 and TDA5231 within the three different frequency bands.

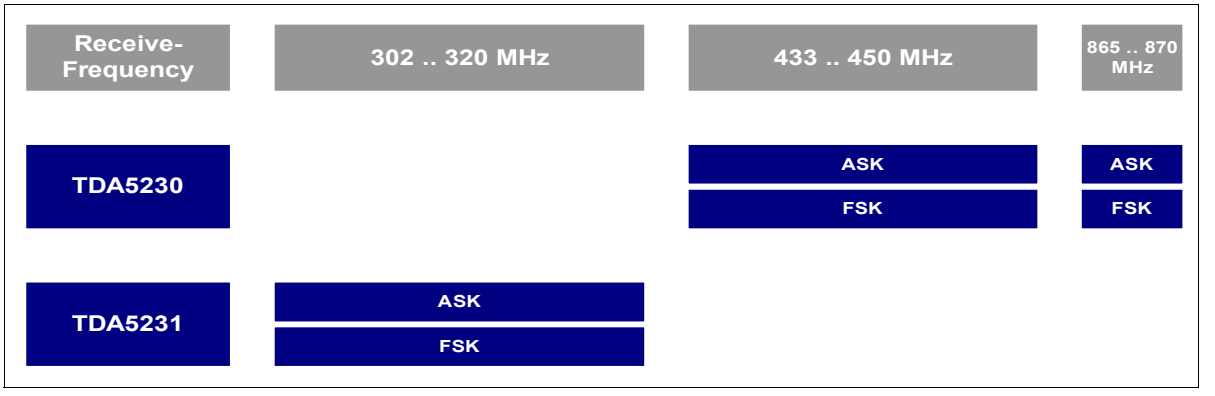


Figure 1 Application Frequencies for TDA5230 and TDA5231

Color underlayed text within this document highlights differences in the operation between the TDA5230 (Lo-Side LO-Injection) and TDA5231 (Hi-Side LO-Injection).

1.6 Major Key-Features of TDA5230 and TDA5231

1.6.1 Typical Application Circuit

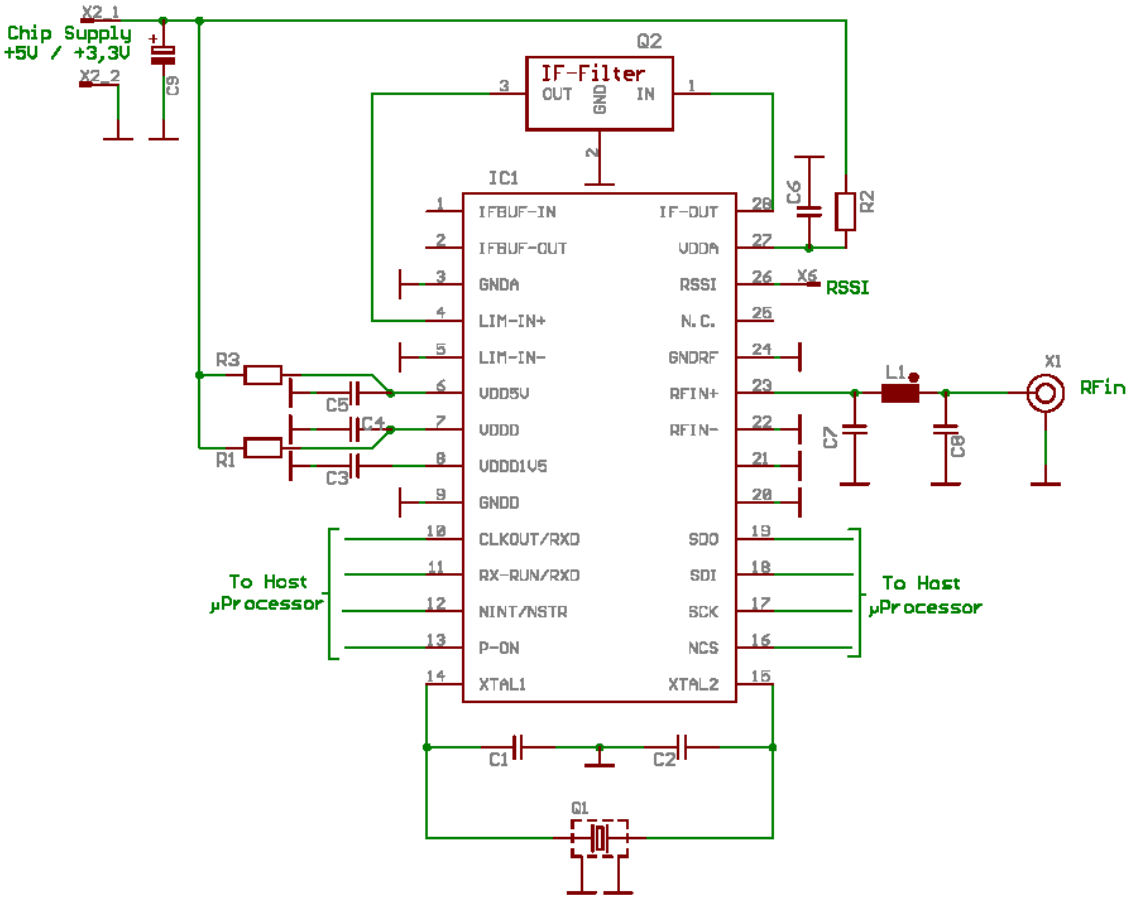


Figure 2 Typical Application Circuit

The TDA523x requires only view external components.

In noise and EMC sensitive applications usage of an input SAW filter plus additional matching circuitry is recommended.

1.6.2 Baseband Processing

TDA523x has integrated all means to process incoming ASK or FSK modulated Manchester-coded bit streams, and convert them into pure data, which can be read out via SPI by the host processor.

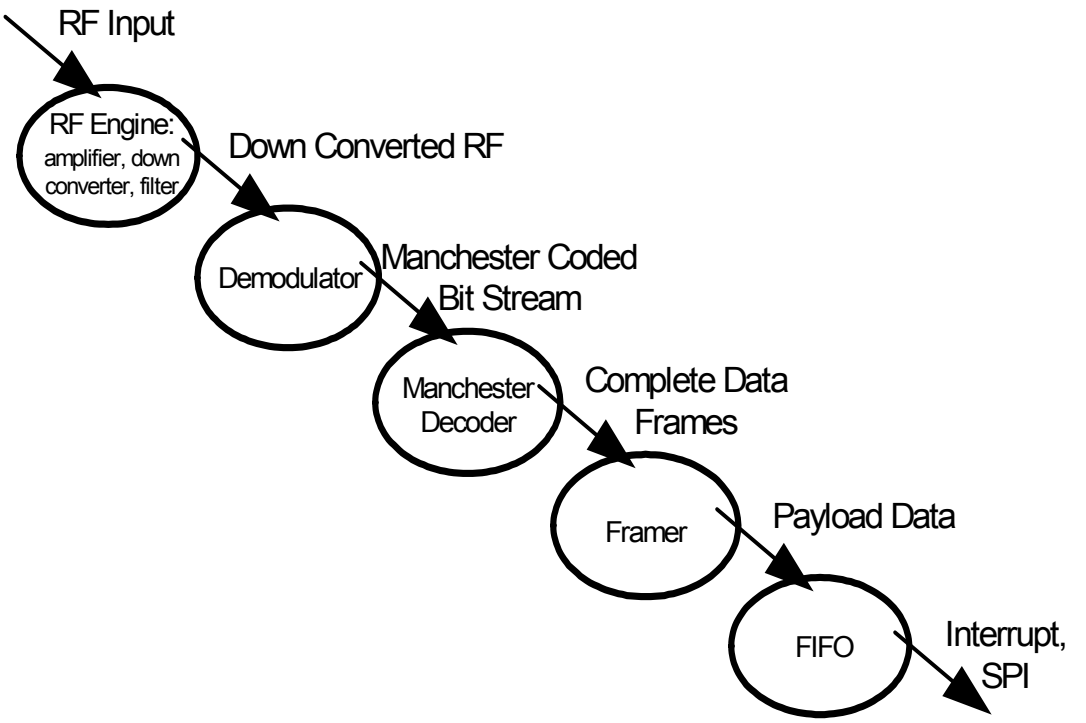


Figure 3 Internal Data Processing Flow

The Manchester-coded bit stream is decoded by the Manchester Decoder into a bit stream containing the wake-up pattern, the TSI (Telegram Start Identifier) and the payload. The Framer separates the payload and stores it in the FIFO. An interrupt is generated and data can be read from the FIFO by the host processor via SPI.

1.6.3 Autonomous Self Polling

The TDA523x offers a fully autonomous Self Polling Mode, in which the RF input signal is scanned for valid data signals base on programmable timing. The host processor is not burdened with this task, so its full processing power is available for other tasks, or the host processor may stay in a power save, or sleep mode. When valid data has been

received, the host processor is alerted by an interrupt, and the data payload is available from the FIFO. Invalid signals are ignored.

The TDA523x offers different programmable scanning modes, and criteria to identify valid wake up patterns, TSIs, and payloads.

Selectable Wake-Up Criteria include detection of a valid data rate, a random Manchester-coded pattern, a chain of equal Manchester-coded bits, or a specific pattern.

Before initiating an interrupt also the TSI must match up to a programmed pattern; optionally the data stream may be scanned for up to 16 bytes of a Message Identifier.

1.6.4 Two Independent Receiver Configuration Sets

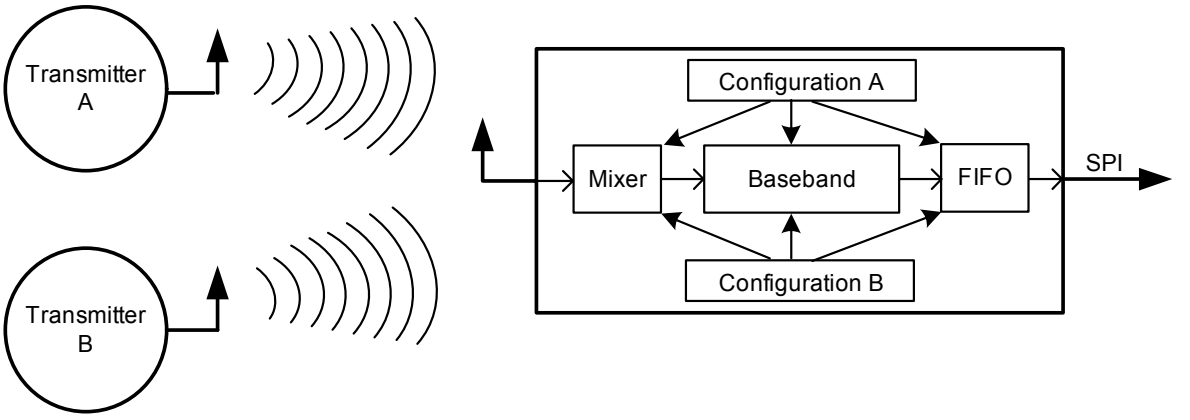


Figure 4 TDA523x Two Independent Receiver Configurations (simplified)

TDA523x has two switchable register sets, allowing scans based on up to two different configurations from different transmitters. Transmissions may differ in sub-channel, modulation, wake-up criterion, data rate, TSI, message identifier, packet length, etc.

In Self Polling Mode configurations are switched autonomously; in Slave Mode, configurations are switched by changing a single register bit.

1.6.5 Multi-Channel PLL Receiver Supports up to 17 Subchannels

TDA523x supports up to 17 subchannels: 1 center channel, 8 channels above, and 8 channels below the center channel frequency. The frequencies for the channels are fixed and depend on the system frequency and the selected band. Additional information is provided in chapter **“RF-PLL Synthesizer” on Page 28**.

In Self Polling Mode up to 3 Channels per Receiver Configuration may be scanned automatically.

1.6.6 Support Software and Evaluation Boards

The TDA523x includes free downloadable support software.

1.6.6.1 The IAF TDA523x Configuration Tool

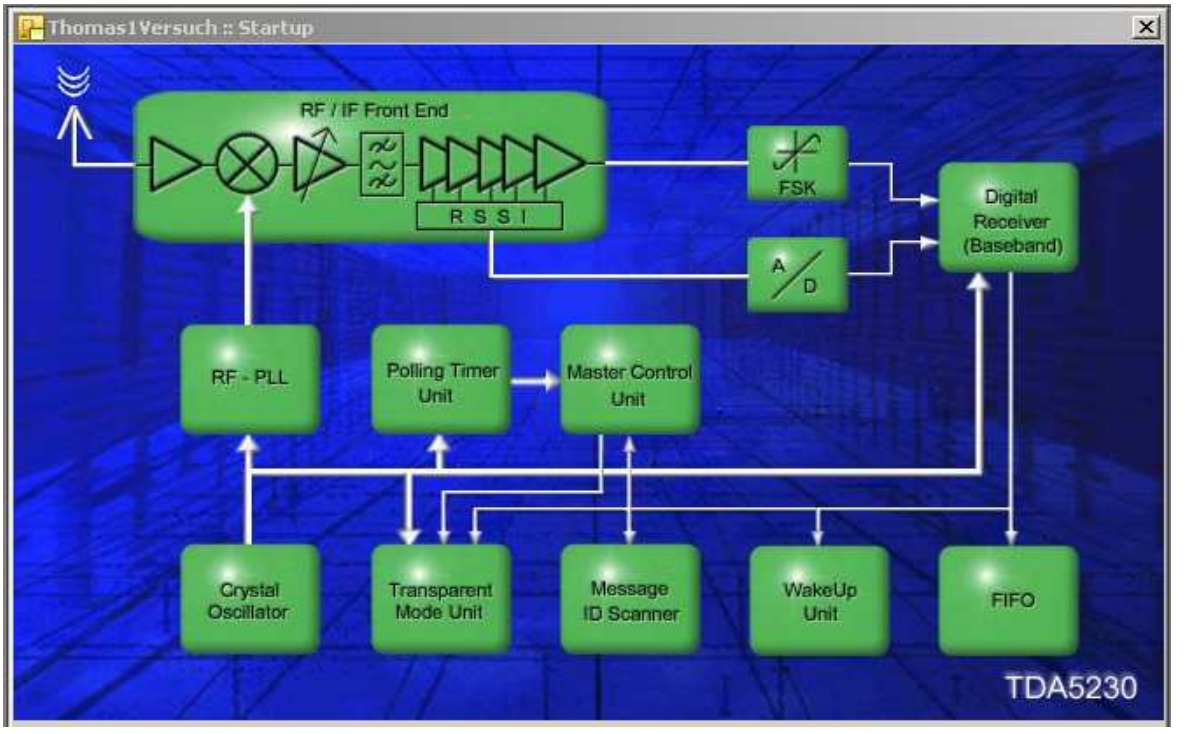


Figure 5 IAF TDA523x Configuration Tool

The IAF TDA523x Configuration Tool offers simple configuration of all register settings. The resulting configuration file may be directly used and downloaded with the TDA523x Explorer or the configuration content may be copied into the target application software.

1.6.6.2 The TDA523x Explorer

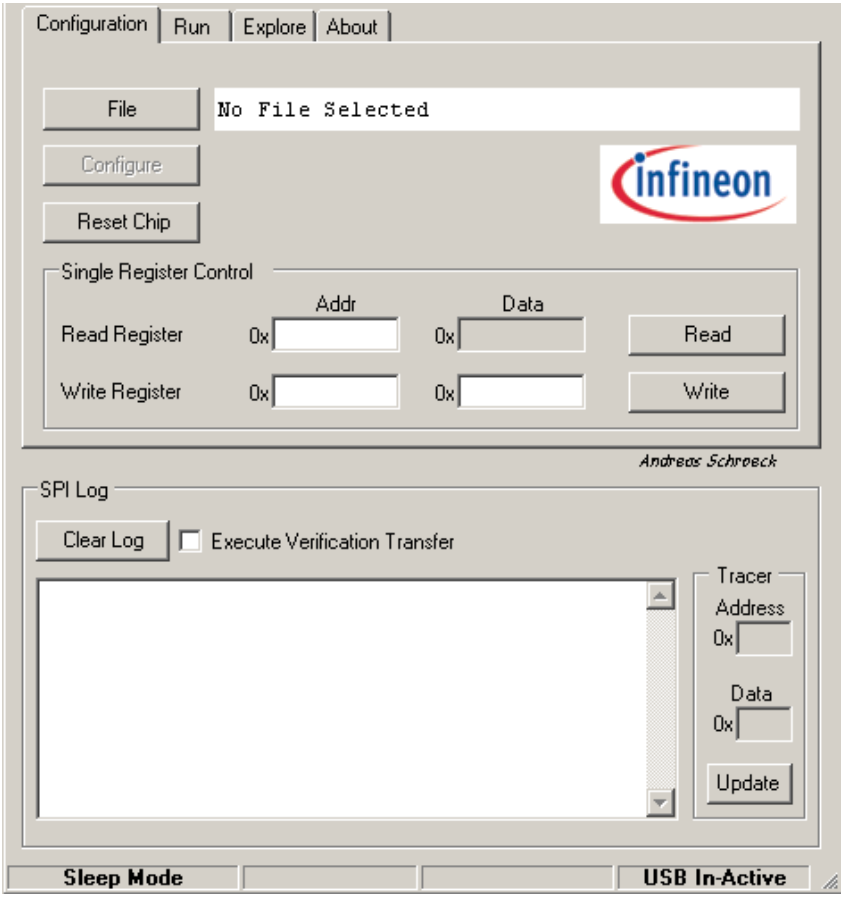


Figure 6 TDA523x Explorer

The TDA523x Explorer works with the TDA523x Evaluation Boards. It allows application solutions to be created and checked via a USB connection from a standard PC. The Explorer allows the user to write registers, read out the data FIFO and related registers.

1.6.6.3 Evaluation Boards

Various Evaluation Boards are available or in development.

All Evaluation Boards have a USB interface to connect to a standard PC and are supported by the TDA523x Explorer.

2 Functional Description

2.1 Pin Configuration

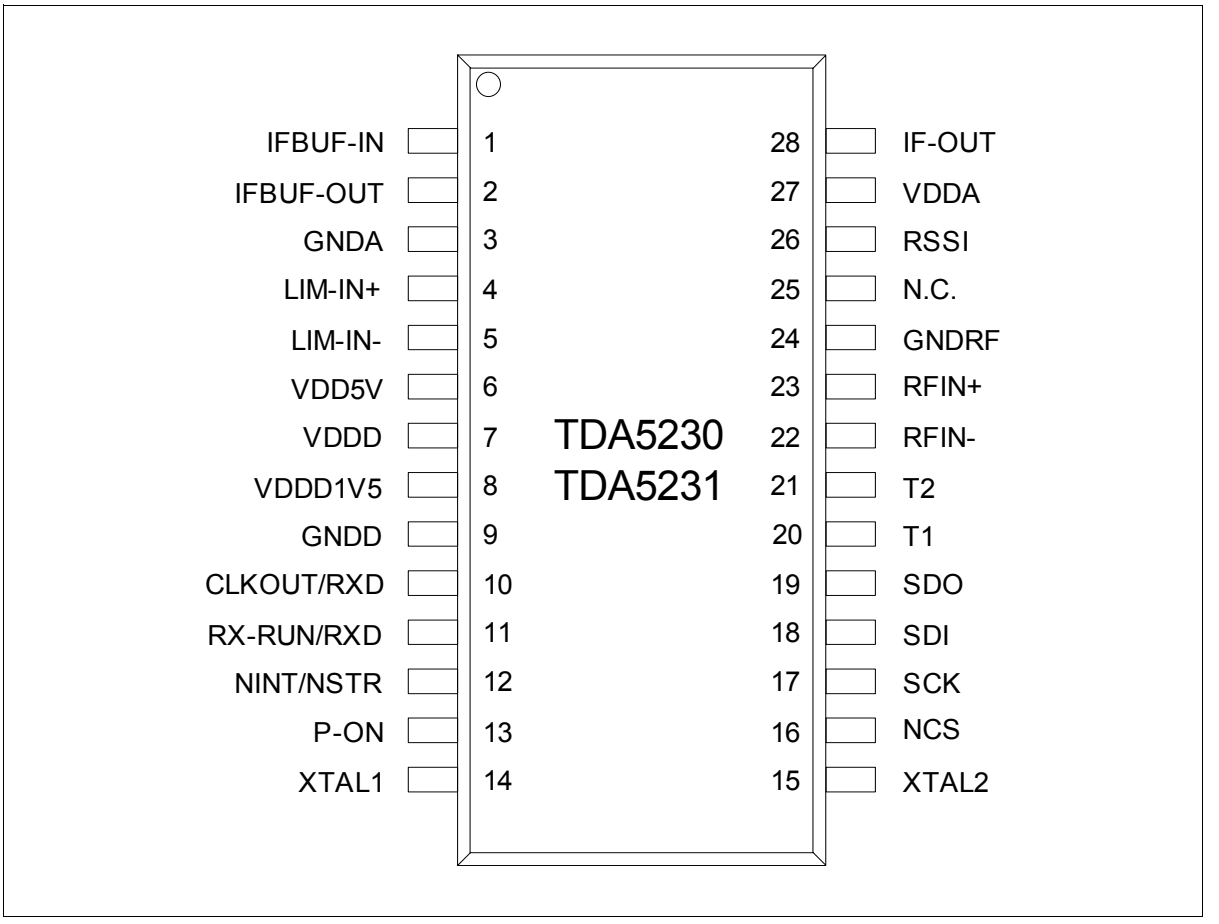
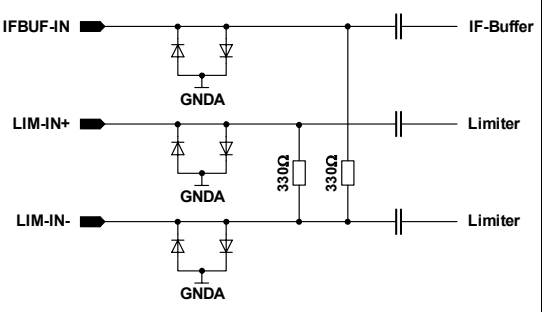
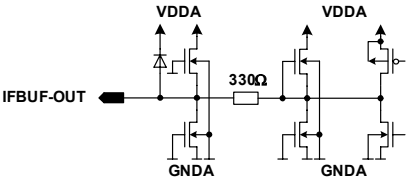
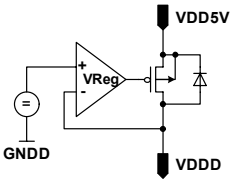
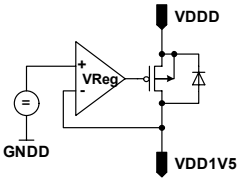
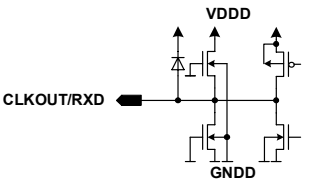
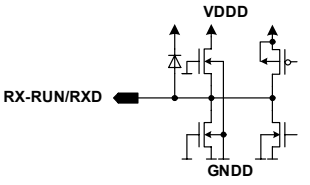
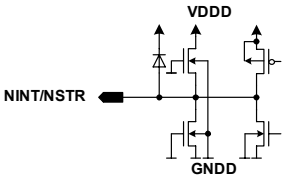
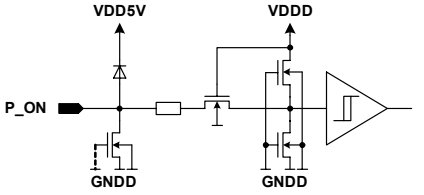
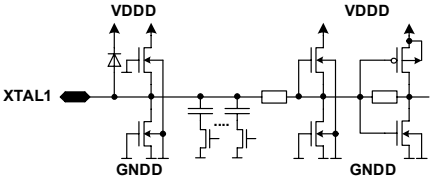
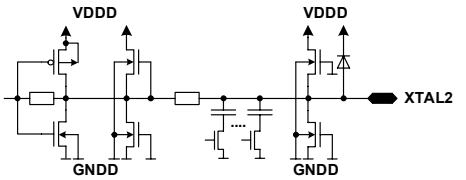


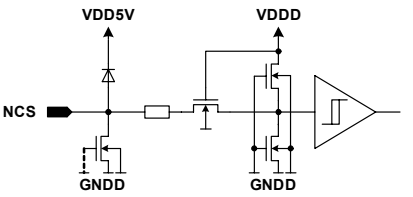
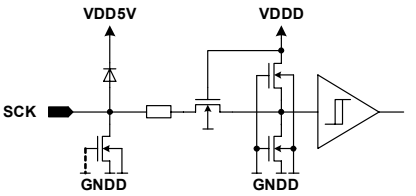
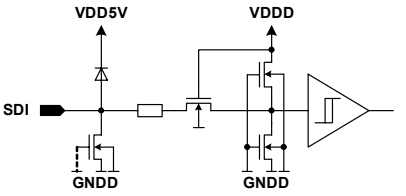
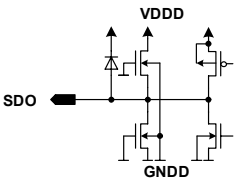
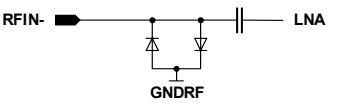
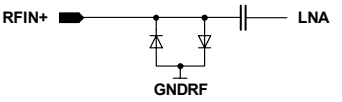
Figure 7 Pin Configuration

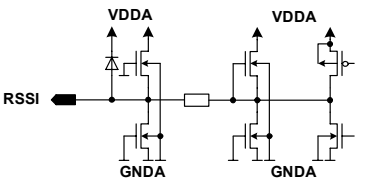
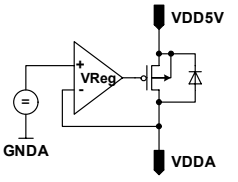
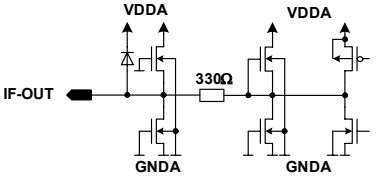
2.2 Pin Definition and Functions

Table 1 Pin Definition and Function

Pin No.	Symbol		Function
1	IFBUF-IN		Input of IF Buffer Amplifier
2	IFBUF-OUT		Output of IF Buffer Amplifier
3	GNDA		Analog Ground
4	LIM-IN+	see schematic of Pin 1	IF Limiter Input
5	LIM-IN-	see schematic of Pin 1	Complementary IF Limiter Input
6	VDD5V		Supply 5 V
7	VDDD		Digital Supply 3.3 V
8	VDDD1V5		Digital Supply 1.5 V
9	GNDD		Digital Ground

Pin No.	Symbol		Function
10	CLKOUT/RXD		Programmable Clock Output and alternative RX Data Output
11	RX-RUN/RXD		Run Mode Output signal and alternative RX Data Output
12	NINT/NSTR		Interrupt Output and alternative RX Data Strobe Output
13	P-ON		Power On
14	XTAL1		Crystal Oscillator
15	XTAL2		Crystal Oscillator

Pin No.	Symbol		Function
16	NCS		SPI Chip Select
17	SCK		SPI Clock
18	SDI		SPI Serial Data Input
19	SDO		SPI Serial Data Output
20	T1		Connect to Digital Ground
21	T2		Connect to RF Ground
22	RFIN-		Complementary LNA Input
23	RFIN+		LNA Input
24	GNDRF		RF Ground
25	N.C.		Do not connect

Pin No.	Symbol		Function
26	RSSI		RSSI Output
27	VDDA		Analog Supply 3.3 V
28	IF-OUT		Mixer IF Output

2.3 Functional Block Diagram

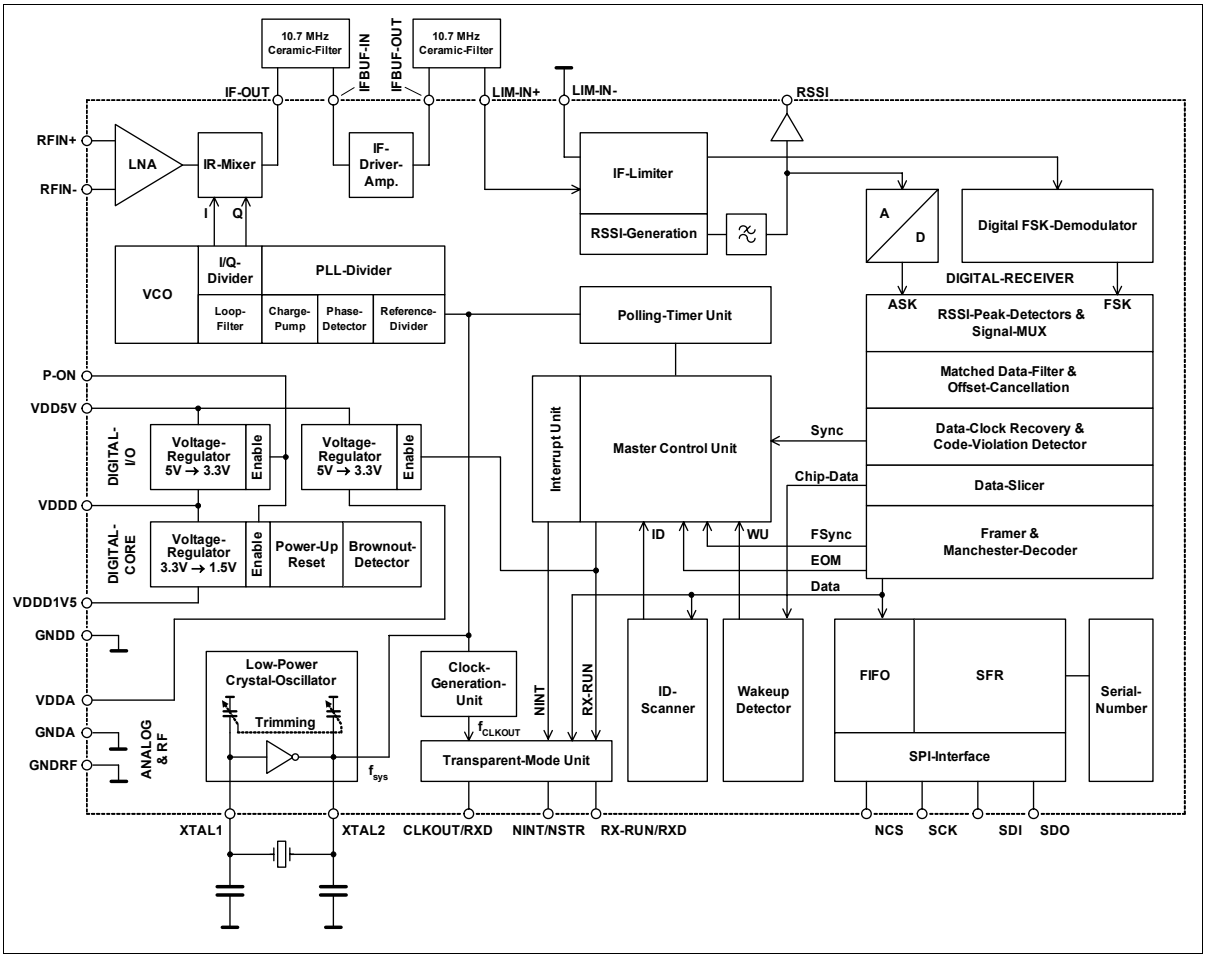


Figure 8 Functional Block Diagram

2.4 Functional Block Description

The RF frontend of the chip contains an LNA followed by an Image Reject Mixer that converts the incoming RF-signal down to IF with adjustable gain from RFIN to IF-OUT. Channel selection is achieved by up to two external ceramic IF filters, which narrow the channel bandwidth. The multistage amplifier performs the limitation of the IF signal and generation of the RSSI signal. The limited IF signal at its output drives the input of the digital FSK Demodulator. The gain and offset of the generated RSSI signal can be digitally adjusted. An A/D converter acts as an interface from the analog RSSI signal path to the Digital Receiver.

The Digital Receiver performs data filtering, offset cancellation and Manchester decoding of the received signals after they are demodulated. The chip also offers a

flexible and configurable frame synchronisation and Message ID scanning feature, supported by special function registers. Received data of an accepted message is stored in a FIFO and can be read out via the SPI interface.

A master control unit (MCU), implemented as a finite state machine and a Polling Timer Unit control all actions of the device and can be configured via Special Function Registers (SFRs). Various self-polling modes can be set up to achieve a maximum of autonomous receiver operation. The Transparent Mode Unit defines the functionality of the pins CLKOUT/RXD, NINT/NSTR and RX-RUN/RXD.

A fully integrated multi-channel PLLdrives the LO ports of the Image-Reject-Mixer. Within a selected operational frequency band multiple channels are accessible by utilizing the same reference crystal-frequency. The reference clock of the PLL and the digital section are provided by a pierce type crystal oscillator that offers on chip fine-tuning to trim out crystal tolerances. A programmable Clock Generation Unit divides the system clock by a programmable ratio and drives the CLKOUT/RXD pin.

On chip voltage regulators generate the required internal supply voltages and allow the IC to be operated at supply voltages between 3 V to 3.6 V and 4.5 V to 5.5 V. The digital supply of the chip is monitored by a brown out detector and is equipped with a built-in reset generator. Every device contains a unique serial number, which can be read out via the SPI Interface.

Special Function Register and Control Bit Symbols

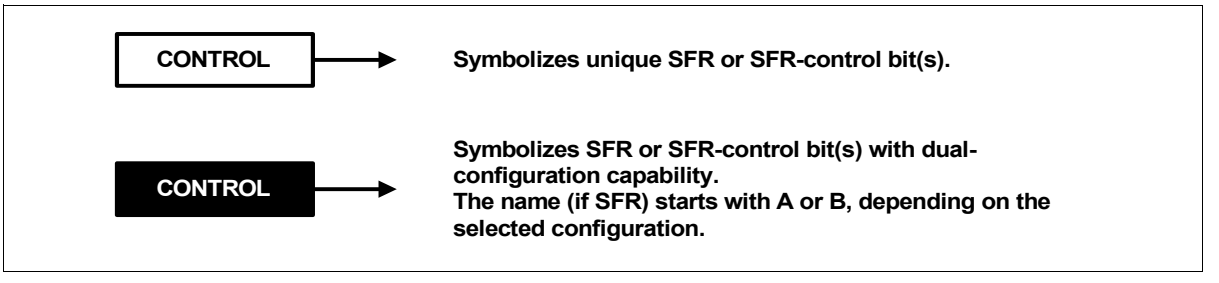


Figure 9 SFR Symbolism

The register names, addresses, and control bits for each function are listed in a table at the end of this section. Functional descriptions of all registers are provided in **Chapter 3 Register Descriptions**.

2.4.1 Power Supply

The chip may be operated within a 5 V or a 3.3 V environment.

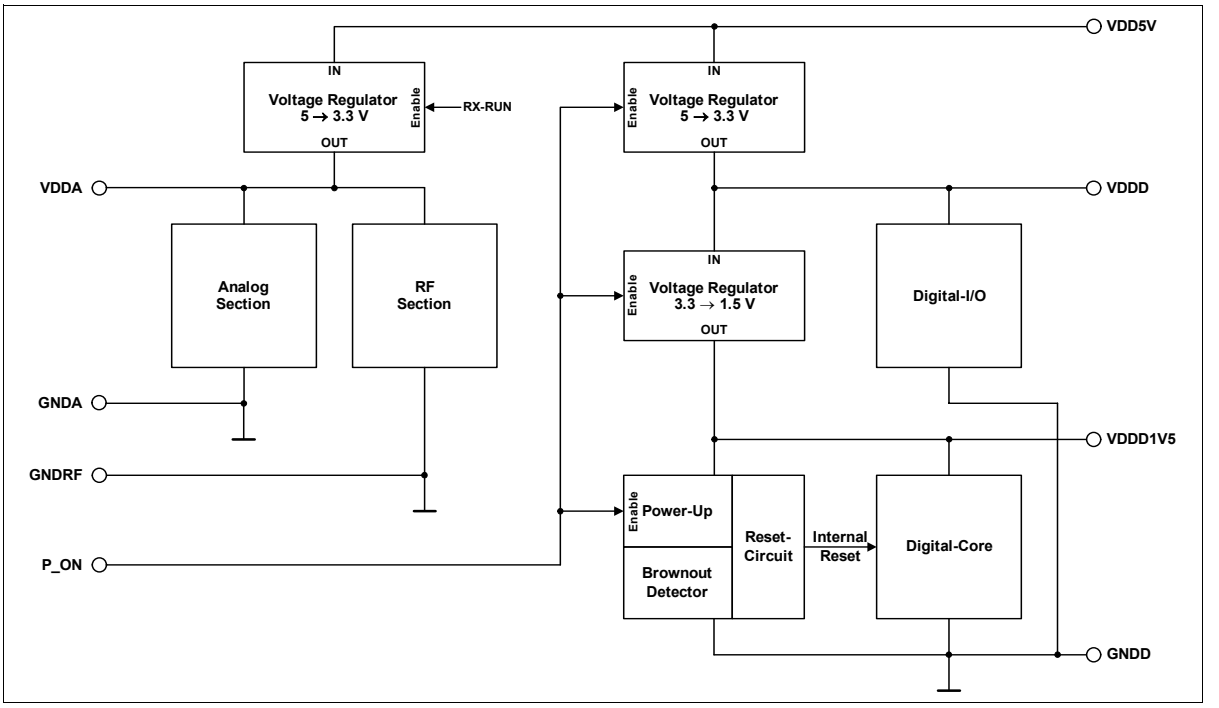


Figure 10 Power Supply

For operation within a 5 V environment, the chip is supplied via the pin VDD5V. In this configuration a 5 to 3.3 V voltage regulator supplies the analog/RF-section (only active in Run Modes) and a second 5 to 3.3 V voltage regulator supplies the digital I/O-pads.

When operating within a 3.3 V environment, the pins VDD5V, VDDA and VDDD must be supplied. The 5 to 3.3 V voltage regulators are inactive in this configuration.

The internal digital core is supplied by an additional 3.3 to 1.5 V regulator.

The regulators for the digital section are controlled by the signal at the P_ON (Power On). A low signal at P_ON disables all regulators and sets the IC into Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF-section is active (RX-RUN = high).

P_ON can be used to initiate a reset. The required negative pulse time t_{P_ON} is specified in **Chapter 4 Specifications**.

To provide data integrity within the digital units, a brown out detector monitors the digital supply and a detected voltage drop of VDDD below approximately 2.45 V initiates a reset.

Figure 11 illustrates a typical power supply application for a 3.3 V and a 5 V environment.

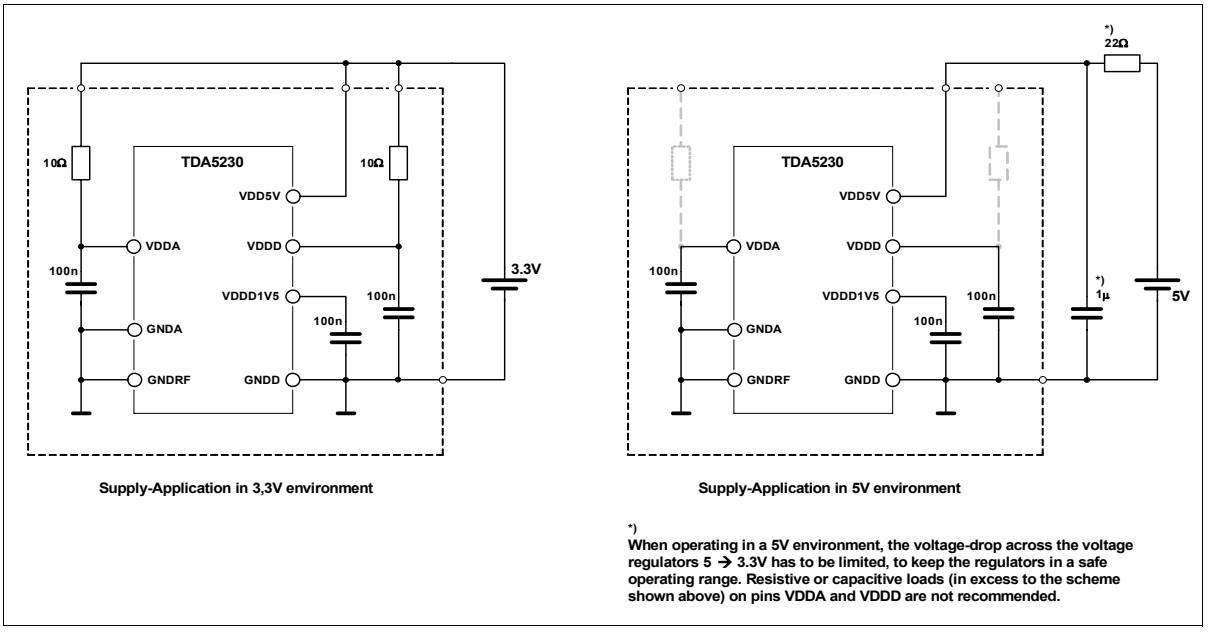


Figure 11 Supply Modes

2.4.1.1 Supply Current

In Sleep Mode, the Master Control Unit switches the crystal oscillator into Low Power Mode (all internal load capacitors are disconnected) to minimize power consumption.

Whenever the chip leaves the Sleep Mode (t_1), the crystal oscillator resumes operation in High Precision Mode and requires $t_{COSCsettle}$ to settle at the trimmed frequency. At t_2 the analog signal path (RF and IF section) and the RF-PLL are activated. At t_3 the chip is ready to receive data. The chip requires $t_{RXstartup}$ from leaving Sleep Mode and until the receiver is ready to receive data.

A transient supply current peak may occur at t_1, depending on the selected trimming capacitance. The average supply current drawn between during $t_{RFstartupdelay}$ is $I_{VDDsleep,high}$.

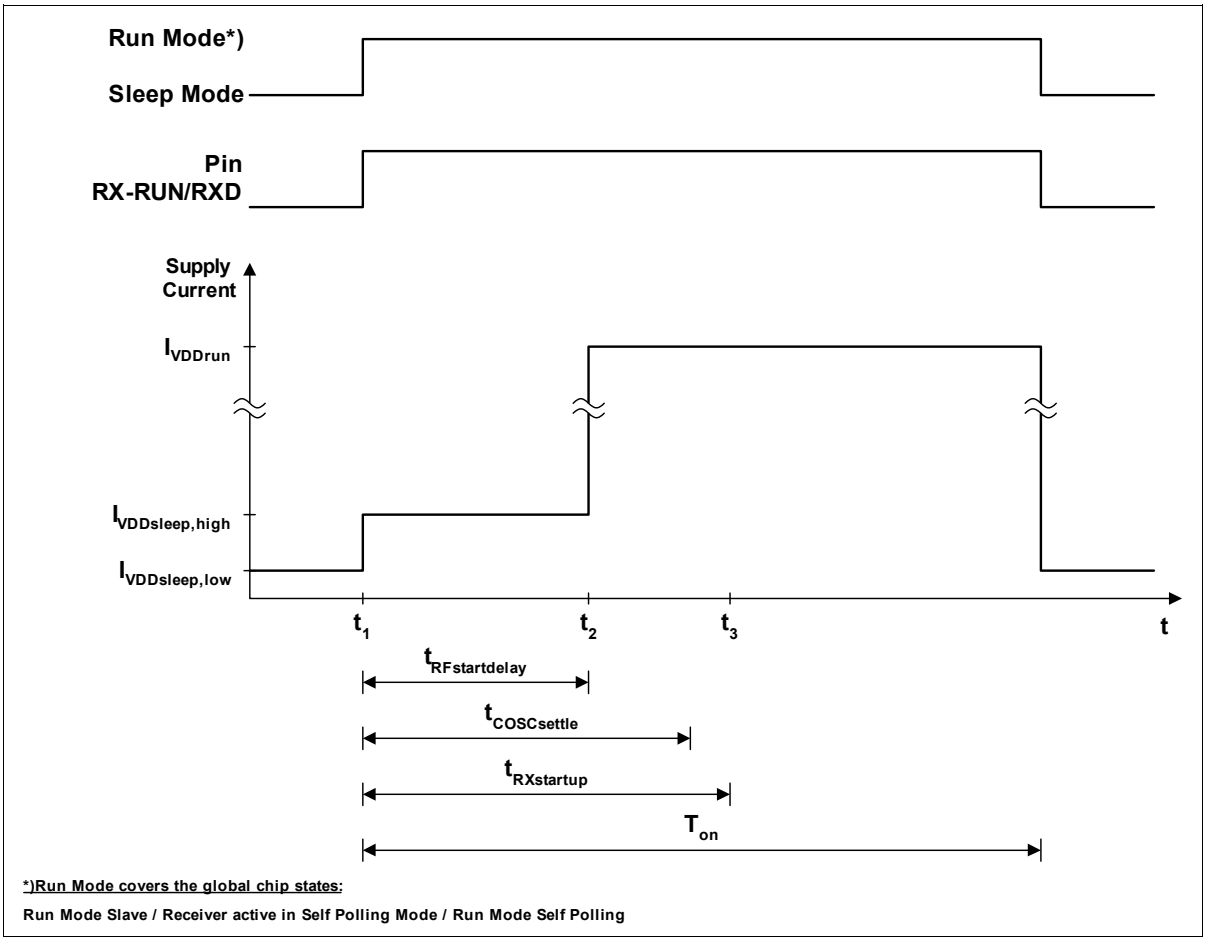


Figure 12 Supply Current Ramp Up/Down

If the IF buffer amplifier or the clock-generation feature (CLKOUT/RXD pin active) is activated, the respective currents must be added.

2.4.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A low at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high at the P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

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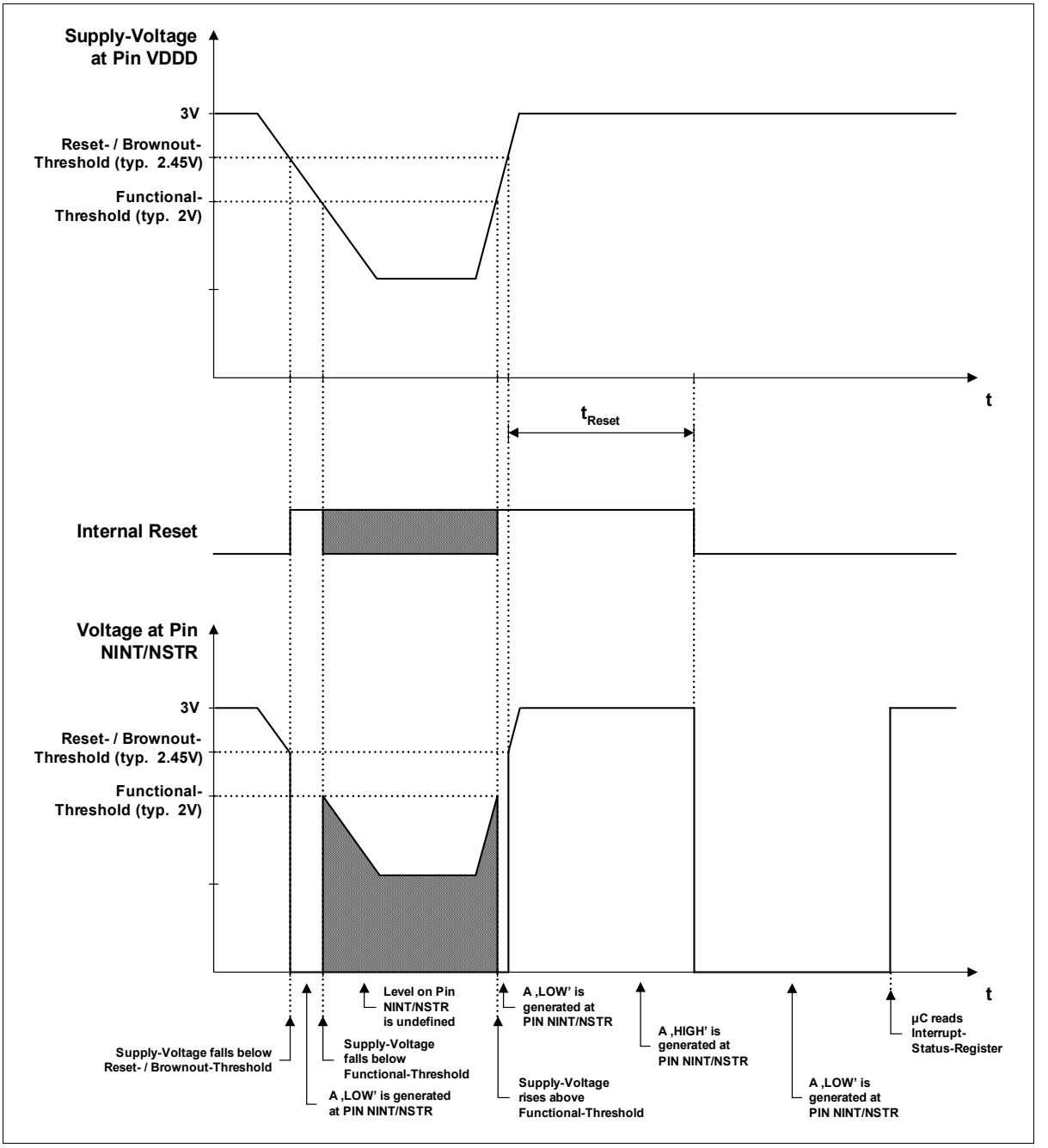

Figure 13 Reset Behavior