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Data Sheet, Version 1.1, 2007-02-26

TDA5252 G2

ASK/FSK 915MHz Wireless Transceiver

Wireless Control Components

Never stop thinking.

Edition 2007-02-26

Published by Infineon Technologies AG,
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Data Sheet, Version 1.1, 2007-02-26

TDA5252 G2

ASK/FSK 915MHz Wireless Transceiver

Wireless Control Components

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Data Sheet

Revision History:	**2007-02-26**	TDA5252 G2
Previous Version: 1.0 as of 2006-12-12		
Page	Subjects (major changes since last revision)	
72	indication of the ESD-integrity values	

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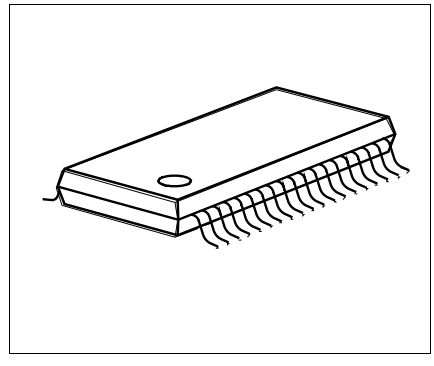
Product Info

General Description



The IC is a low power consumption single chip FSK/ASK Transceiver for half duplex low datarate communication in the 915MHz band. The IC offers a very high level of integration and needs only a few external components. It contains a highly efficient power amplifier, a low noise amplifier (LNA) with AGC, a double balanced mixer, a complex direct conversion stage, I/Q limiters with RSSI generation, an FSK demodulator, a fully integrated VCO and PLL synthesizer, a tuneable crystal oscillator, an onboard data filter, a data comparator (slicer), positive and negative peak detectors, a data rate detection circuit and a 2/3-wire bus interface. Additionally there is a power down feature to save battery power.

Features

- Low supply current (I_s = 9mA typ. receive, I_s = 13mA typ. transmit mode)
- Supply voltage range 2.1 - 5.5V
- Power down mode with very low supply current consumption
- FSK and ASK modulation and demodulation capability
- Fully integrated VCO and PLL synthesizer and loop filter on-chip with on chip crystal oscillator tuning
- I^2C/3-wire µController Interface
- On-chip low pass channel select filter and data filter with tuneable bandwidth
- Data slicer with self-adjusting threshold and 2 peak detectors
- FSK sensitivity < -109dBm, ASK sensitivity < -109dBm
- Transmit power up to +13dBm
- Self-polling logic with ultra fast data rate detection

Application

- Low Bitrate Communication Systems
- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Telemetry Systems
- Electronic Metering
- Home Automation Systems

Type	Ordering Code	Package
TDA5252 G2	SP000057332	PG-TSSOP-38

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1 Product Description

1.1 Overview

The IC is a low power consumption single chip FSK/ASK Transceiver for the ISM frequency band 915MHz. The IC combines a very high level of integration and minimum external part count. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, an FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative data peak detector, a highly efficient power amplifier and a complex digital timing and control unit with I^2C/3-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/ direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip.

The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

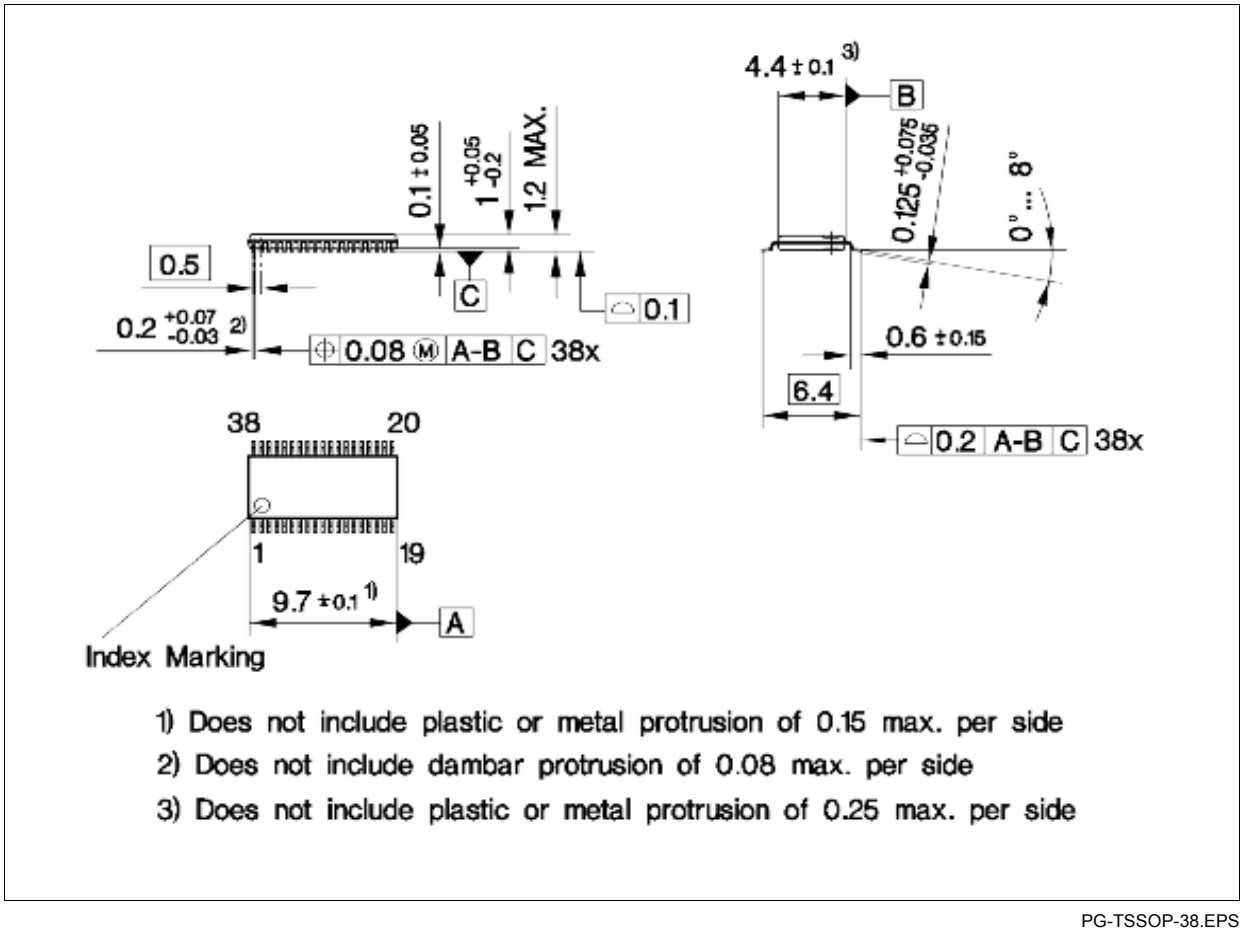
1.2 Features

- Low supply current (I_s = 9 mA typ. receive, I_s = 13mA typ. transmit mode, both at 3 V supply voltage, 25°C)
- Supply voltage range 2.1 V to 5.5 V
- Operating temperature range -40°C to +85°C
- Power down mode with very low supply current consumption
- FSK and ASK modulation and demodulation capability without external circuitry changes, FM demodulation capability
- Fully integrated VCO and PLL synthesizer and loop filter on-chip with on-chip crystal oscillator tuning, therefore no additional external components necessary
- Differential receive signal path completely on-chip, therefore no external filters are necessary
- On-chip low pass channel select and data filter with tuneable bandwith
- Data slicer with self-adjusting threshold and 2 peak detectors
- Self-polling logic with adjustable duty cycle and ultrafast data rate detection and timer mode providing periodical interrupt
- FSK and ASK sensitivity < -109 dBm
- Adjustable LNA gain
- Digital RSSI and Battery Voltage Readout
- Provides Clock Out Pin for external microcontroller
- Transmit power up to +13 dBm in 50Ω load at 5V supply voltage
- I^2C/3-wire microcontroller interface, working at max. 400kbit/s

1.3 Application

- Low Bitrate Communication Systems
- Keyless Entry Systems
- Remote Control Systems
- Alarm Systems
- Telemetry Systems
- Electronic Metering
- Home Automation Systems

1.4 Package Outlines

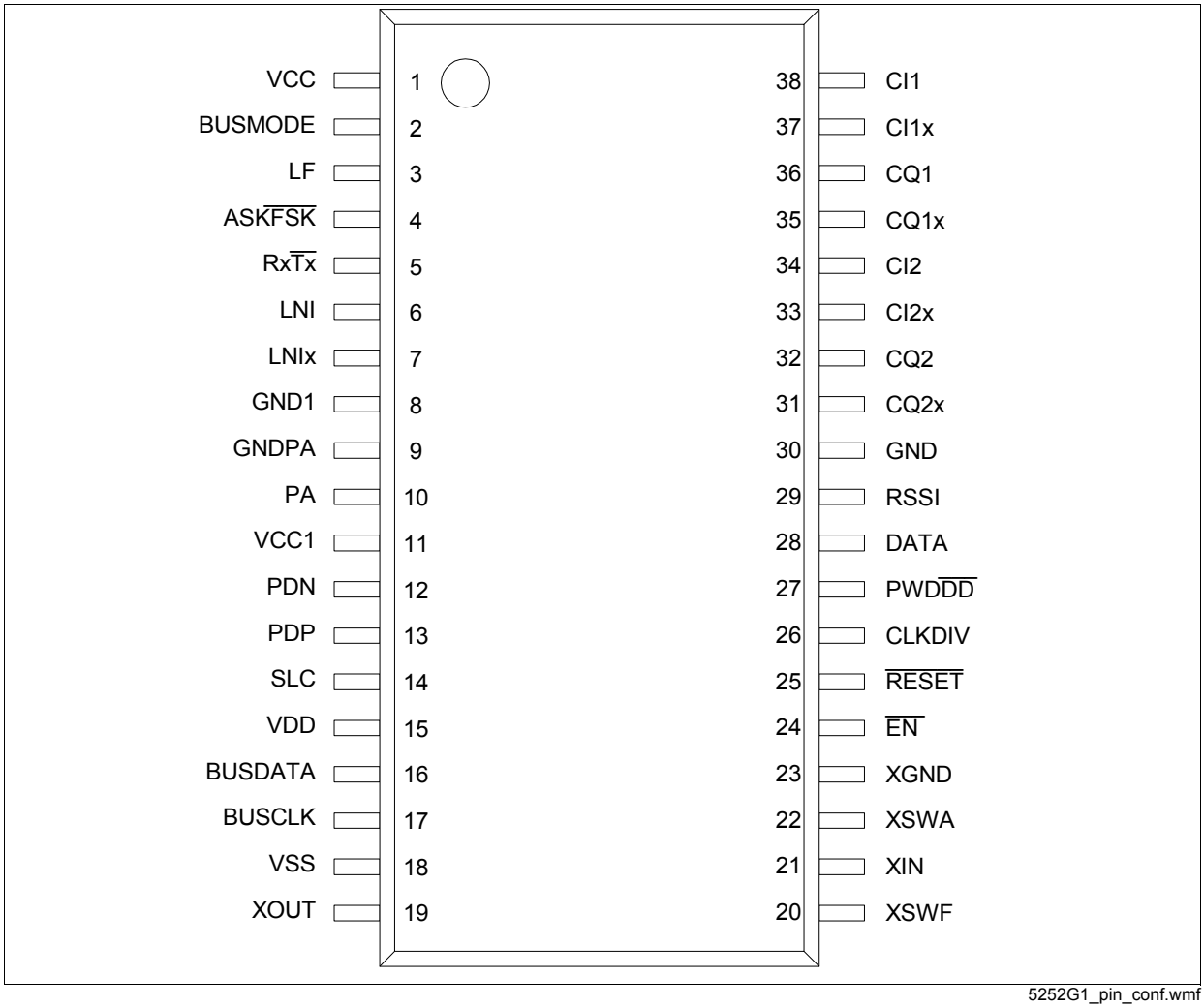


PG-TSSOP-38.EPS

Figure 1-1 PG-TSSOP-38 package outlines

2 Functional Description

2.1 Pin Configuration

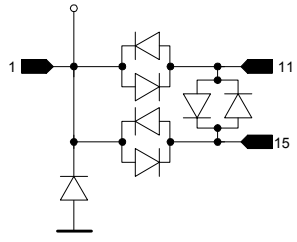
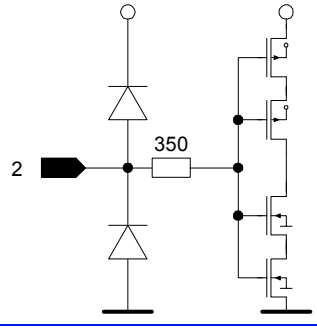
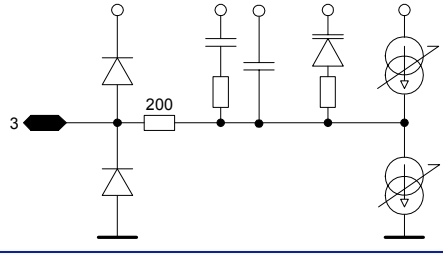
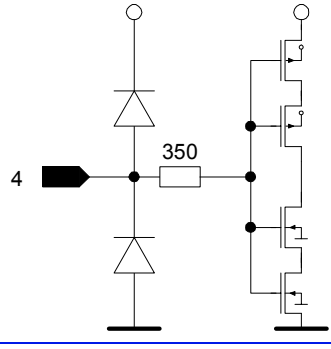


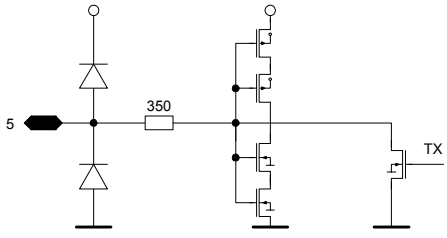
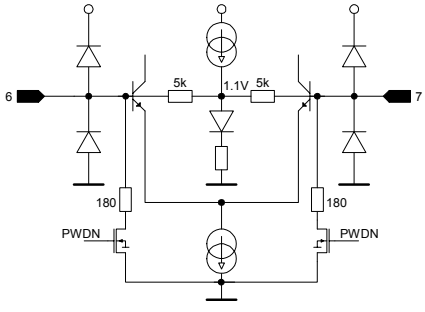
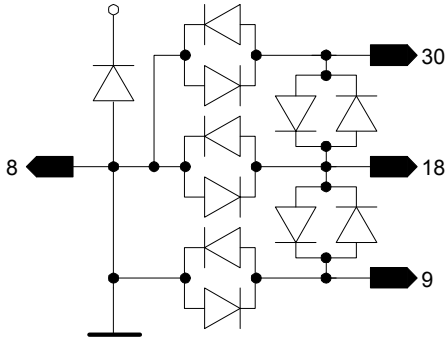
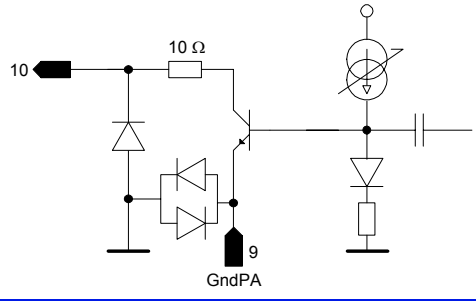
5252G1_pin_conf.wmf

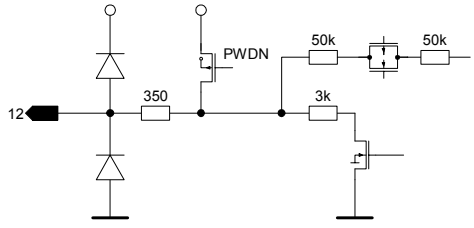
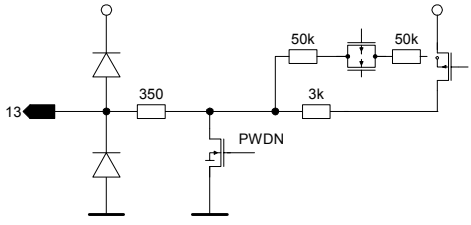
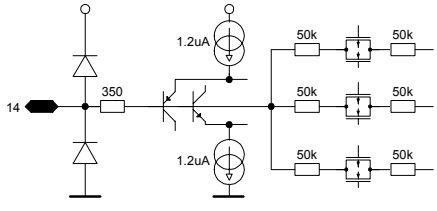
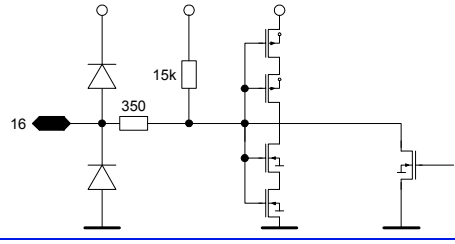
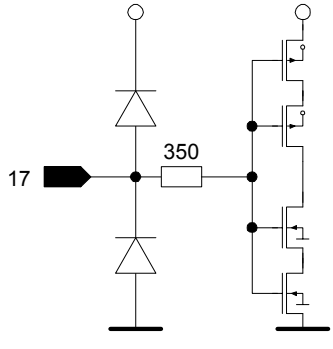
Figure 2-1 Pin Configuration

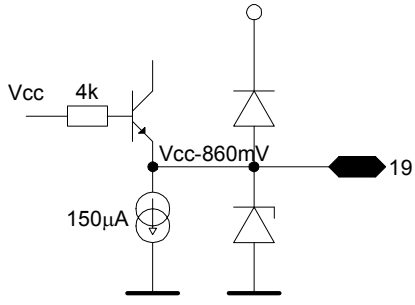
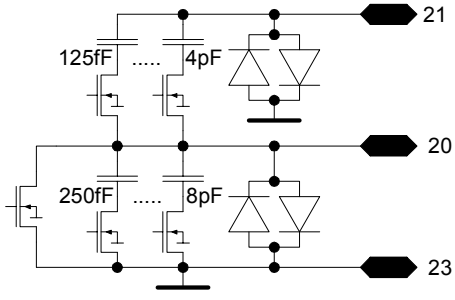
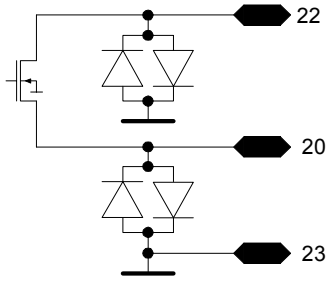
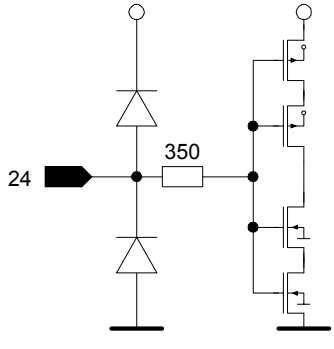
2.2 Pin Definitions and Functions

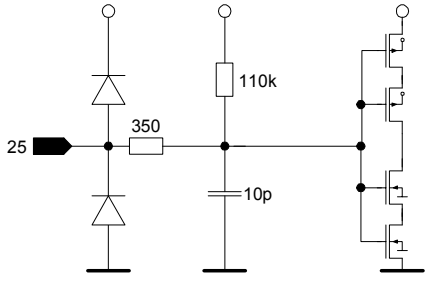
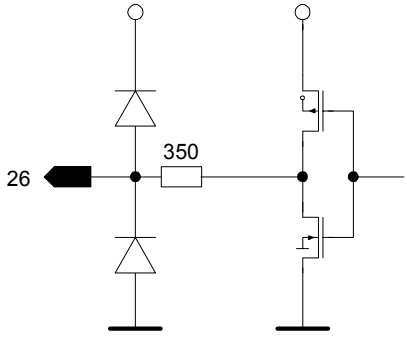
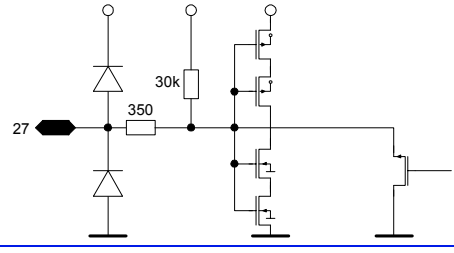
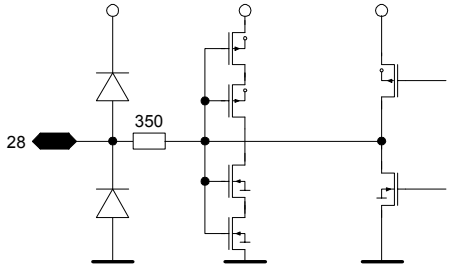
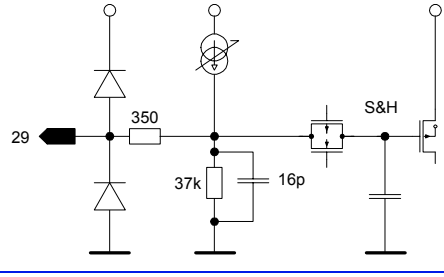
Table 2-1 Pin Definition and Function

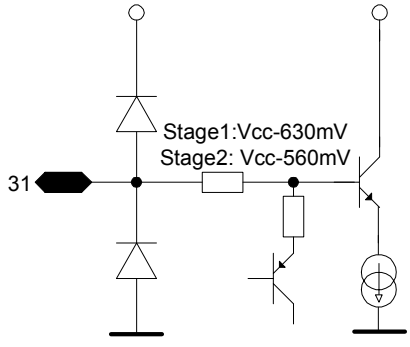
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	VCC		Analog supply (antiparallel diodes between VCC, VCC1, VDD)
2	BUSMODE		Bus mode selection (I²C/3 wire bus mode selection)
3	LF		Loop filter and VCO control voltage
4	ASK$\overline{\text{FSK}}$		ASK/FSK- mode switch input

5	RX$\overline{TX}$		RX/TX-mode switch input/output
6	LNI		RF input to differential Low Noise Amplifier (LNA))
7	LNIX	see Pin 6	Complementary RF input to differential LNA
8	GND1		Ground return for LNA and Power Amplifier (PA) dirver stage
9	GNDPA	see Pin 8	Ground return for PA output stage
10	PA		PA output stage
11	VCC1	see Pin 1	Supply for LNA and PA

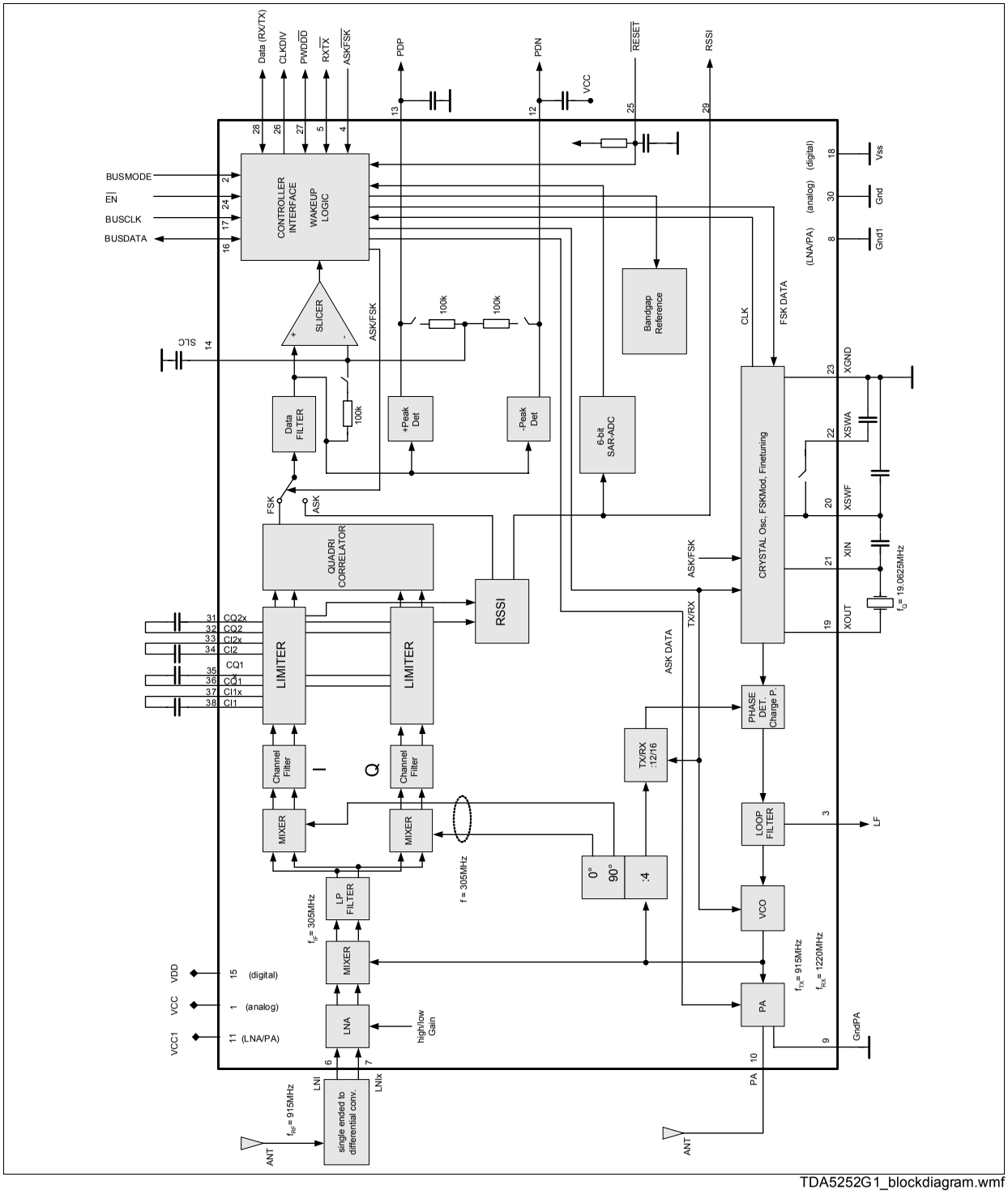
12	PDN		Output of the negative peak detector
13	PDP		Output of the positive peakdetector
14	SLC		Slicer level for the data slicer
15	VDD	see Pin 1	Digital supply
16	BUSDATA		Bus data in/output
17	BUSCLK		Bus clock input
18	VSS	see Pin 8	Ground for digital section

19	XOUT		Crystal oscillator output, can also be used as external reference frequency input.
20	XSWF		FSK modulation switch
21	XIN	see Pin 20	
22	XSWA		ASK modulation/FSK center frequency switch
23	XGND	see Pin 22	Crystal oscillator ground return
24	$\overline{EN}$		3-wire bus enable input

25	$\overline{\text{RESET}}$		Reset of the entire system (to default values), active low
26	CLKDIV		Clock output
27	PWD$\overline{\text{DD}}$		Power Down input (active high), data detect output (active low)
28	DATA		TX Data input, RX data output (RX powerdown: pin 28 @ GND)
29	RSSI		RSSI output

30	GND	see Pin 8	Analog ground
31	CQ2x		Pin for external Capacitor Q-channel, stage 2
32	CQ2	II	Q-channel, stage 2
33	CI2x	II	I-channel, stage 2
34	CI2	II	I-channel, stage 2
35	CQ1x	II	Q-channel, stage 1
36	CQ1	II	Q-channel, stage 1
37	CI1x	II	I-channel, stage 1
38	CI1	II	I-channel, stage 1

2.3 Functional Block Diagram



TDA5252G1_blockdiagram.wmf

Figure 2-2 Main Block Diagram

2.4 Functional Block Description

2.4.1 Power Amplifier (PA)

The power amplifier is operating in C-mode. It can be used in either high or low power mode. In high-power mode the transmit power is approximately +13dBm into 50 Ohm at 5V and +6dBm at 2.1V supply voltage. In low power mode the transmit power is approximately -3dBm at 5V and -30dBm at 2.1V supply voltage using the same matching network. The transmit power is controlled by the **D0**-bit of the **CONFIG** register (subaddress 00H) as shown in the following **Table 2-2**. The default output power mode is high power mode.

Table 2-2 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D0	PA_PWR	0= low TX Power, 1= high TX Power	1

In case of ASK modulation the power amplifier is turned fully on and off by the transmit baseband data, i.e. 100% On-Off-Keying.

2.4.2 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB and symmetrical inputs. It is possible to reduce the gain to 0 dB via logic.

Table 2-3 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D4	LNA_GAIN	0= low Gain, 1= high Gain	1

2.4.3 Downconverter 1st Mixer

The Double Balanced 1st Mixer converts the input frequency (RF) in the range of 915MHz down to the intermediate frequency (IF) at approximately 305MHz. The local oscillator frequency is generated by the PLL synthesizer that is fully implemented on-chip as described in **Section 2.4.5**. This local oscillator operates at approximately 1220MHz in receive mode providing the above mentioned IF frequency of 305MHz. The mixer is followed by a low pass filter with a corner frequency of approximately 350MHz in order to prevent RF and LO signals from appearing in the 305MHz IF signal.

2.4.4 Downconverter 2nd I/Q Mixers

The Low pass filter is followed by 2 mixers (inphase I and quadrature Q) that convert the 305MHz IF signal down to zero-IF. These two mixers are driven by a signal that is generated by dividing the local oscillator signal by 4, thus equalling the IF frequency.

2.4.5 PLL Synthesizer

The Phase Locked Loop synthesizer consists of two VCOs (i.e. transmit and receive VCO), a divider by 4, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCOs are including spiral inductors and varactor diodes. The center frequency of the transmit VCO is 915MHz, the center frequency of the receive VCO is 1220MHz.

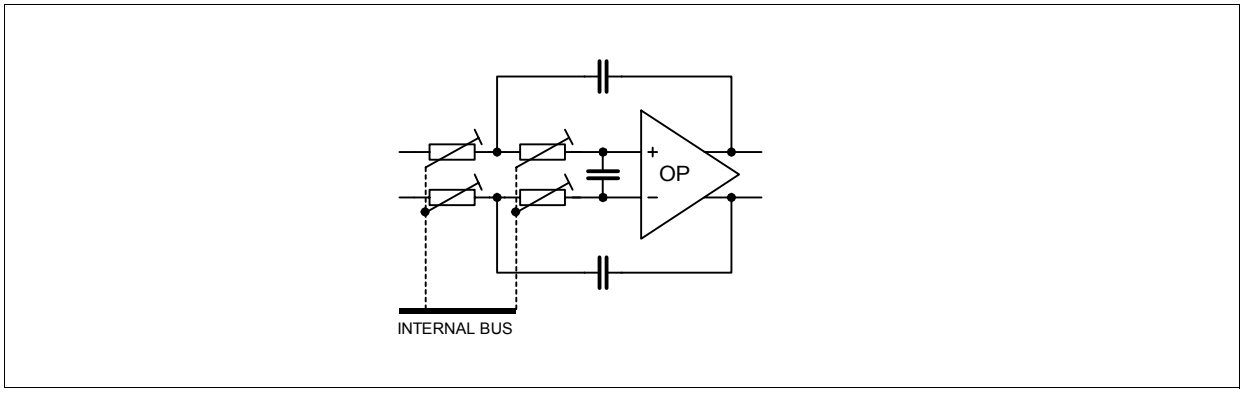
Generally in receive mode the relationship between local oscillator frequency f_{osc}, the receive RF frequency f_{RF} and the IF frequency f_{IF} and thus the frequency that is applied to the I/Q Mixers is given in the following formula:

$$f_{osc} = 4/3\ f_{RF} = 4\ f_{IF} \qquad [2-1]$$

The VCO signal is applied to a divider by 4 which is producing approximately 305MHz signals in quadrature. The overall division ratio of the divider chain following the divider by 4 is 12 in transmit mode and 16 in receive mode as the nominal crystal oscillator frequency is 19.0625MHz. The division ratio is controlled by the **RxTx** pin (pin 5) and the **D10** bit in the **CONFIG** register.

2.4.6 I/Q Filters

The I/Q IF to zero-IF mixers are followed by baseband 6th order low pass filters that are used for RF-channel filtering.



iq_filter.wmf

Figure 2-3 One I/Q Filter stage

The bandwidth of the filters is controlled by the values set in the filter-register. It can be adjusted between 50 and 350kHz in 50kHz steps via the bits D1 to D3 of the **LPF** register (subaddress 03H).

2.4.7 I/Q Limiters

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80dB each in the frequency range of 100Hz up to 350kHz.

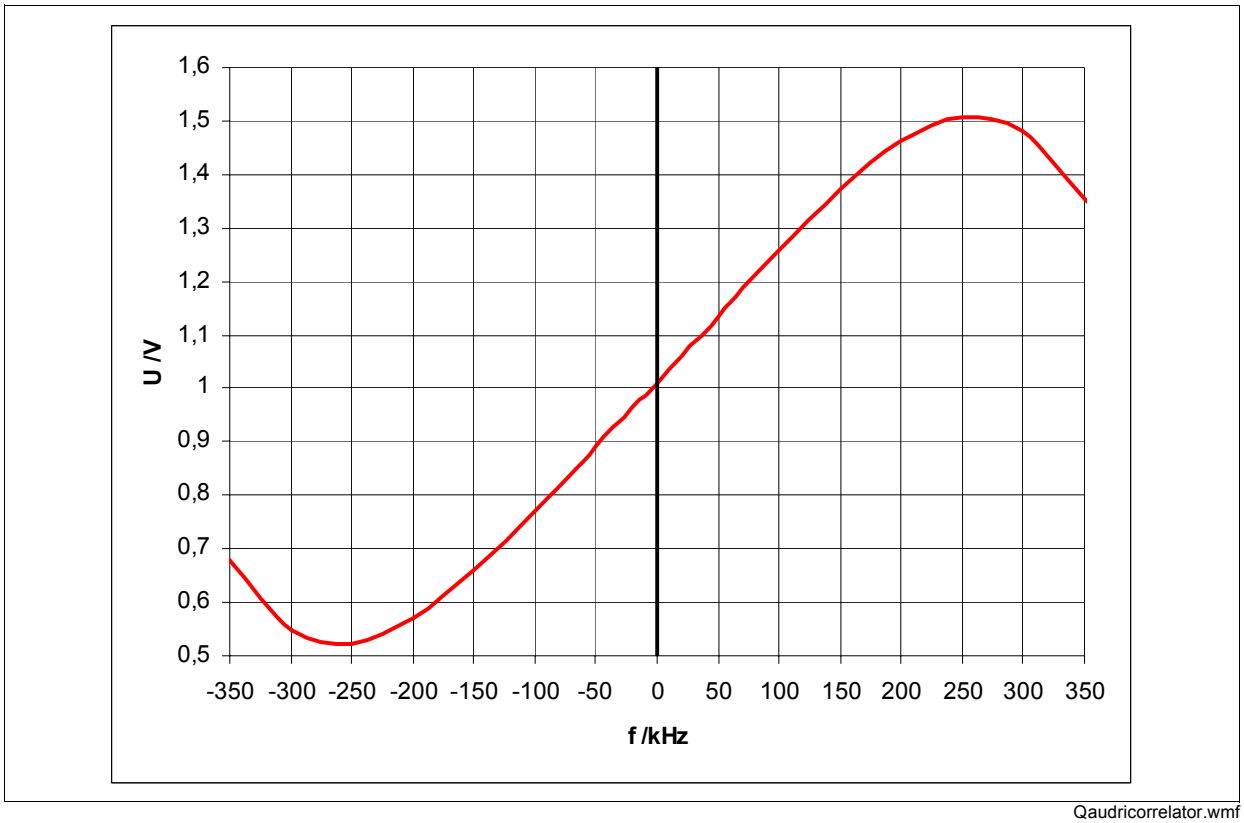
Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

2.4.8 FSK Demodulator

The output differential signals of the I/Q limiters are fed to a quadrature correlator circuit that is used to demodulate frequency shift keyed (FSK) signals. The demodulator gain is 2.4mV/kHz, the maximum frequency deviation is ±300kHz as shown in **Figure 2-4** below.

The demodulated signal is applied to the ASK/FSK mode switch which is connected to the input of the data filter. The switch can be controlled by the **ASKFSK** pin (pin 4) and via the D11 bit in the CONFIG register.

The modulation index *m* must be significantly larger than 2 and the deviation at least larger than 25kHz for correct demodulation of the signal.

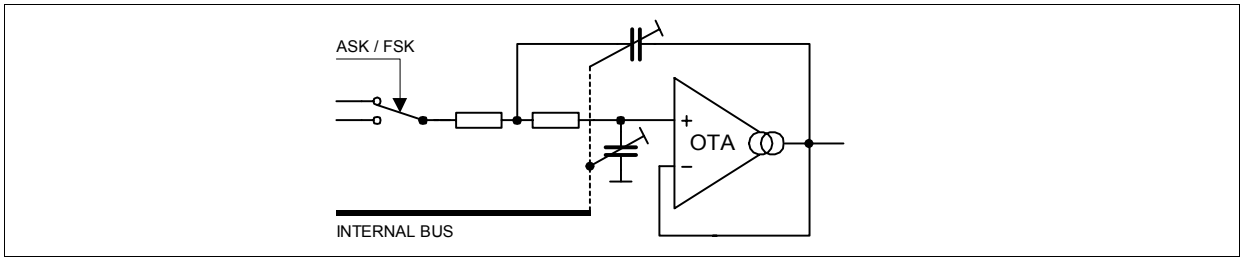


Qaudricorrelator.wmf

Figure 2-4 Typical Quadricorrelator Demodulation Characteristic

2.4.9 Data Filter

The 2-pole data filter has a Sallen-Key architecture and is implemented fully on-chip. The bandwidth can be adjusted between approximately 5kHz and 102kHz via the bits **D4** to **D7** of the **LPF** register (see also Table 2-18).



data_filter.wmf

Figure 2-5 Data Filter architecture

2.4.10 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100kHz. The self-adjusting threshold is generated by a RC-network (LPF) or by use of one or both peak detectors depending on the baseband coding scheme. This can be controlled by the **D15** bit of the **CONFIG** register as shown in the following table.

Table 2-4 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D15	SLICER	0= Lowpass Filter, 1= Peak Detector	0

2.4.11 Peak Detectors

Two separate Peak Detectors are available. They are generating DC voltages in a fast-attack and slow-release manner that are proportional to the positive and negative peak voltages appearing in the data signal. These voltages may be used to generate a threshold voltage for non-Manchester encoded signals, for example. The time-constant of the fast-attack/slow-release action is determined by the RC network with external capacitor.

2.4.12 Crystal Oscillator

The reference oscillator is an NIC oscillator type (Negative Impedance Converter) with a crystal operating in serial resonance. The nominal operating frequency of 19.0625MHz and the frequencies for FSK modulation can be adjusted via 3 external capacitors. Via microcontroller and bus interface the chip-internal capacitors can be used for finetuning of the nominal and the FSK modulation frequencies. This finetuning of the crystal oscillator allows to eliminate frequency errors due to crystal or component tolerances.

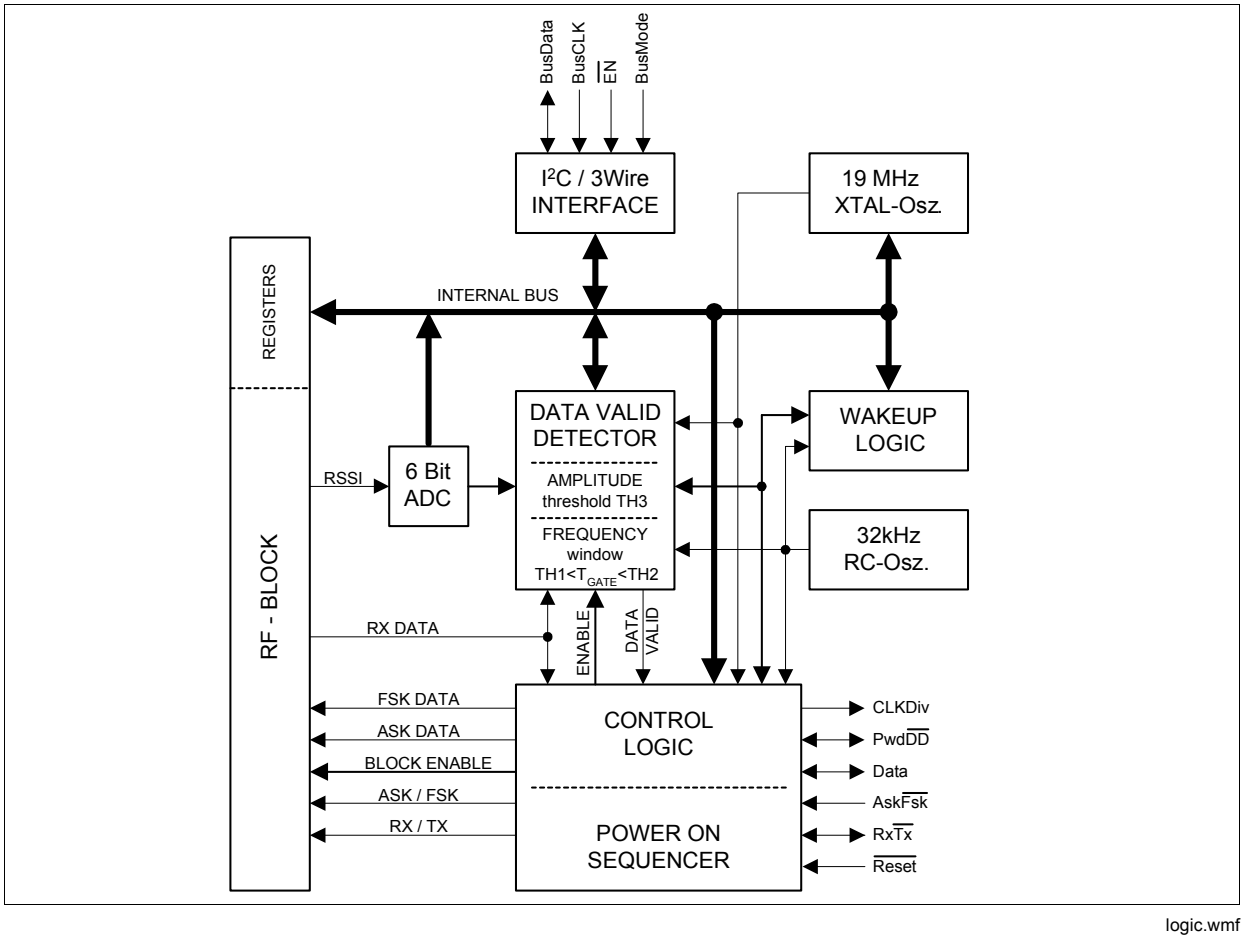
2.4.13 Bandgap Reference Circuitry and Powerdown

A Bandgap Reference Circuit provides a temperature stable 1.2V reference voltage for the device. A power down mode is available to switch off all subcircuits that are controlled by the bidirectional Powerdown&DataDetect **PwdDD** pin (pin 27) as shown in the following table. Power down mode can either be activated by pin 27 or bit D14 in Register 00h. In power down mode also pin 28 (DATA) is affected (see **Section 2.4.17**).

Table 2-5 PwdDD Pin Operating States	
PwdDD	**Operating State**
VDD	Powerdown Mode
Ground/VSS	Device On

2.4.14 Timing and Data Control Unit

The timing and data control unit contains a wake-up logic unit, an I²C/3-wire microcontroller interface, a “data valid” detection unit and a set of configuration registers as shown in the subsequent figure.



logic.wmf

Figure 2-6 Timing and Data Control Unit

The I²C / 3-wire Bus Interface gives an external microcontroller full control over important system parameters at any time.

It is possible to set the device in three different modes: Slave Mode, Self Polling Mode and Timer Mode. This is done by a state machine which is implemented in the WAKEUP LOGIC unit. A detailed description is given in **Section 2.4.16**.

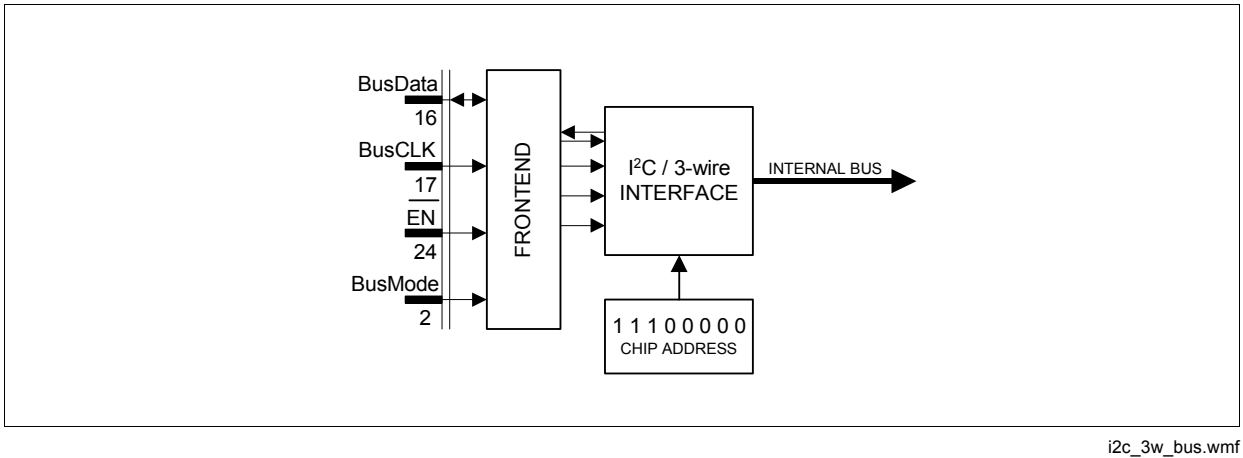
The DATA VALID DETECTOR contains a frequency window counter and an RSSI threshold comparator. The window counter uses the incoming data signal from the data slicer as the gating signal and the crystal oscillator frequency as the timebase to determine the actual datarate. The result is compared with the expected datarate.
The threshold comparator compares the actual RSSI level with the expected RSSI level.
If both conditions are true the **PwdDD** pin is set to LOW in self polling mode as you can see in **Section 2.4.16**. This signal can be used as an interrupt for an external µP. Because the **PwdDD** pin is bidirectional and open drain driven by an internal pull-up resistor it is possible to apply an external LOW thus enabling the device.

2.4.15 Bus Interface and Register Definition

The TDA5252 supports the I^2C bus protocol (2 wire) and a 3-wire bus protocol. Operation is selectable by the **BusMode** pin (pin 2) as shown in the following table. All bus pins (BusData, BusCLK, **EN**, BusMode) have a Schmitt-triggered input stage. The BusData pin is bidirectional where the output is open drain driven by an internal 15kΩ pull up resistor.

Table 2-6 Bus Interface Format

Function	BusMode	EN	BusCLK	BusData
I^2C Mode	Low	High= inactive, Low= active	Clock input	Data in/out
3-wire Mode	High			



i2c_3w_bus.wmf

Figure 2-7 Bus Interface

Note: The Interface is able to access the internal registers at any time, even in POWER DOWN mode. There is no internal clock necessary for Interface operation.

I²C Bus Mode

In this mode the **BusMode** pin (pin 2) = LOW and the **$\overline{\text{EN}}$** pin (pin 24) = LOW.

Data Transition:

Data transition on the pin BusData can only occur when BusCLK is LOW. BusData transitions while BusCLK is HIGH will be interpreted as start or stop condition.

Start Condition (STA):

A start condition is defined by a HIGH to LOW transition of the BusData line while BusCLK is HIGH. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO):

A stop condition is defined by a LOW to HIGH transition of the BusData line while BusCLK is HIGH. This condition terminates the communication between the devices and forces the bus interface into the initial state.

Acknowledge (ACK):

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will set the SDA line to LOW level to indicate it has received the 8 bits of data correctly.

Data Transfer Write Mode:

To start the communication, the bus master must initiate a start condition (STA), followed by the 8bit chip address. The chip address for the TDA5252 is fixed as „1110000“ (MSB at first). The last bit (LSB=A0) of the chip address byte defines the type of operation to be performed:

A0=0, a write operation is selected and A0=1 a read operation is selected.

After this comparison the TDA5252 will generate an ACK and awaits the desired sub address byte (00H...0FH) and data bytes. At the end of the data transition the master has to generate the stop condition (STO).

Data Transfer Read Mode:

To start the communication in the read mode, the bus master must initiate a start condition (STA), followed by the 8 bit chip address (write: A0=0), followed by the sub address to read (80H, 81H), followed by the chip address (read: A0=1). After that procedure the data of the selected register (80H, 81H) is read out. During this time the data line has to be kept in HIGH state and the chip sends out the data. At the end of data transition the master has to generate the stop condition (STO).

Bus Data Format in I²C Mode

Table 2-7 Chip address Organization

MSB							LSB	Function
1	1	1	0	0	0	0	0	Chip Address Write
1	1	1	0	0	0	0	1	Chip Address Read

Table 2-8 I²C Bus Write Mode 8 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN							LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	STO

Table 2-9 I²C Bus Write Mode 16 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN						LSB		
STA	1	1	1	0	0	0	0	**0**	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D15	...	D8	ACK	D7	D6	...	D0	ACK	STO

Table 2-10 I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (READ) 80H, 81H						LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	1	0	0	0	0	**0**	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	STA	1	1	1	0	0	0	0	**1**	ACK

Table 2-10 I²C Bus Read Mode (continued)

MSB	DATA OUT FROM SUB ADDRESS						LSB		
R7	R6	R5	R4	R3	R2	R1	R0	ACK*	STO

* mandatory HIGH

3-wire Bus Mode

In this mode pin 2 (BusMode)= HIGH and Pin 16 (BusData) is in the data input/output pin. Pin 24 ($\overline{EN}$) is used to activate the bus interface to allow the transfer of data to / from the device. When pin 24 ($\overline{EN}$) is inactive (HIGH), data transfer is inhibited.

Data Transition:

Data transition on pin 16 (BusData) can only occur if the clock BusCLK is LOW. To perform a data transfer the interface has to be enabled. This is done by setting the $\overline{EN}$ line to LOW. A serial transfer is done via BusData, BusCLK and $\overline{EN}$. The bit stream needs no chip address.

Data Transfer Write Mode:

To start the communication the $\overline{EN}$ line has to be set to LOW. The desired sub address byte and data bytes have to follow. The subaddress (00H...0FH) determines which of the data bytes are transmitted. At the end of data transition the $\overline{EN}$ must be HIGH.

Data transfer Read Mode:

To start the communication in the read mode, the $\overline{EN}$ line has to be set to LOW followed by the sub address to read (80H, 81H). Afterwards the device is ready to read out data. At the end of data transition $\overline{EN}$ must be HIGH.