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SmartLEWIS™ TRX

TDA5340

High Sensitivity Multi-Channel Transceiver

Data Sheet

Revision 1.2, 13.06.2012

Wireless Sense & Control

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Revision History	
Page or Item	**Subjects (major changes since previous revisions)**
Revision 1.2, 13.06.2012	
Page 62	Package Outline Information added
Revision 1.1, 30.05.2012	
Page 40	Voltage at PA Pin changed to **Peak Voltage at pin RFOUT** with max 10% TX Duty Cycle
Page 40	Inserted maximum **Peak Voltage at pin RFOUT** with TX Duty Cycle above 10%
Page 40	Inserted maximum **DC Voltage at pin RFOUT**
Page 54	Inserted Definition for reception parameters

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Last Trademarks Update 2011-02-24

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1 Product Description

1.1 Overview

The IC is a low power ASK/FSK/GFSK Transceiver for the frequency bands 300-320, 415-495, 863-960 MHz. Bi-phase modulation schemes, like Manchester, bi-phase mark, bi-phase space and differential Manchester as well as NRZ are supported.

The chip offers a high level of integration and needs only a few external components, like a crystal, several blocking capacitors and the necessary matching elements. The IF-filter is integrated but depending on the performance requirements an external ceramic IF-filter can be used. For low cost applications an external passive antenna switch configuration can be used.

The device is qualified according to automotive quality standards and operates between -40 and +110 °C at supply voltage ranges of 3.0-3.6 Volts or 4.5-5.5 Volts.

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer, with high frequency resolution and a crystal oscillator as reference, generates the necessary frequencies for the power amplifier or down conversion mixers. The on-chip temperature sensor may be utilized for temperature drift compensation of the crystal oscillator.

The receiver portion is realized as a double down conversion super-heterodyne / low-IF architecture each with image rejection supplemented by digital signal processing in the baseband. This architecture enables outstanding sensitivity performance in combination with very good blocking performance values.

The transmitter section comprises a class C/E power amplifier with a high efficiency and an output power level of up to 14 dBm. A tuning feature for the output power is possible via several switchable parallel output stages, of course matching to lower power levels is always possible. For higher power applications an external power amplifier can be used and the internal PA serves as a power driver. For ASK modulation a programmable data shaping is provided. With the fractional-N PLL synthesizer and a selectable Gaussian data shaping filter a very accurate and precise FSK modulation is achieved. The transmit data can be either stored in a separate FIFO data buffer or directly provided via the bus interface.

The receiver portion is able to scan autonomuosly for incoming data by using the self polling feature while the host micro controller can stay in power down mode, which reduces the system current consumption significanty.

The digital baseband processing unit together with the high performance downconverter is the key element for the exceptional sensitivity performance of the device which take it close to the theoretical top-performance limits. It comprises signal and noise detectors, matched data filter, clock and data recovery, data slicer and a format decoder. It demodulates the received ASK or FSK data stream and recovers the data clock out of the received data with very fast synchronziation times which can then be either accessed via separate pins or used for further processing like frame synchronization and intermediate storage in the on-chip FIFO.

The RSSI output signal is converted to the digital domain with an ADC. All these signals are accessible via the 4-wire SPI interface bus.

Up to 4 pre-configured telegram formats with different data rates and filter bandwidths can be stored into the device offering independent pre-processing of the received and transmitted data. The downconverter can be also configured to single-conversion mode at moderately reduced selectivity and image rejection performance but at the advantage of saving the external IF filter.

1.2 Key Features

Transceiver

- Multiband / Multichannel (300-320 MHz, 415-495 MHz, 863-960 MHz)
- High receiver sensitivity better than -116 dBm
- Power amplifier with up to 14 dBm output power
- Very Low Current consumption:
  - Receive Mode: 12 mA (typ)
  - Transmit Mode at 10 dBm and 434 MHz: 12 mA (typ)
  - Sleep Mode (XTAL ON): 40 uA (typ)
  - Deep Sleep Mode (XTAL OFF): 7 µA (typ)
  - Power down Mode: 0.9 uA (typ)
- ASK and FSK capability with programmable Gaussian data shaping
- 20 dB programable output power range
- On-chip IF filter with selectable bandwidth (optional an external CER-filter is possible)
- Sigma-delta fractional-N PLL synthesizer with high resolution
- Automatic Frequency Control function (AFC) for offset carrier frequency

Digital Baseband

- Multi protocol handling: Up to 4 parallel parameter sets for autonomous scanning and receiving from different sources
- Integrated data and clock recovery
- Autonomous receive functionality: Frame synchronisation, format decoding, message ID screening
- 288 Bit RX/TX-FIFO for receive and transmit data
- Wake-up generator and polling timer unit
- Ultra-fast wake-up on RSSI
- Supports all bi-phase format schemes and NRZ

General

- Operating temperature range -40 to +110°C
- Supply voltage range 3.0 to 3.6 V or 4.5 to 5.5 V
- Brownout detector
- Integrated 4-wire SPI bus interface
- 32-bit wide Unique ID on chip
- On-chip temperature sensor
- ESD protection +/- 2 kV on all pins (HBM)
- PG-TSSOP-28 package

1.3 Target Applications

- Remote keyless entry (RKE)
- Remote start applications
- Passive Keyless Entry (PKE)
- Security Alarm Systems
- Automatic Meter Reading (AMR) and Infrastructure (AMI)
- Home Automation
- Remote Control
- Sensor Networks
- Short range radio data transmission

1.4 Application Example

The Application examples within this section where optimezed for performance and sytem costs. Of course there exists several steps inbetween which can be realized by the customer to fullfill the application specific needs.

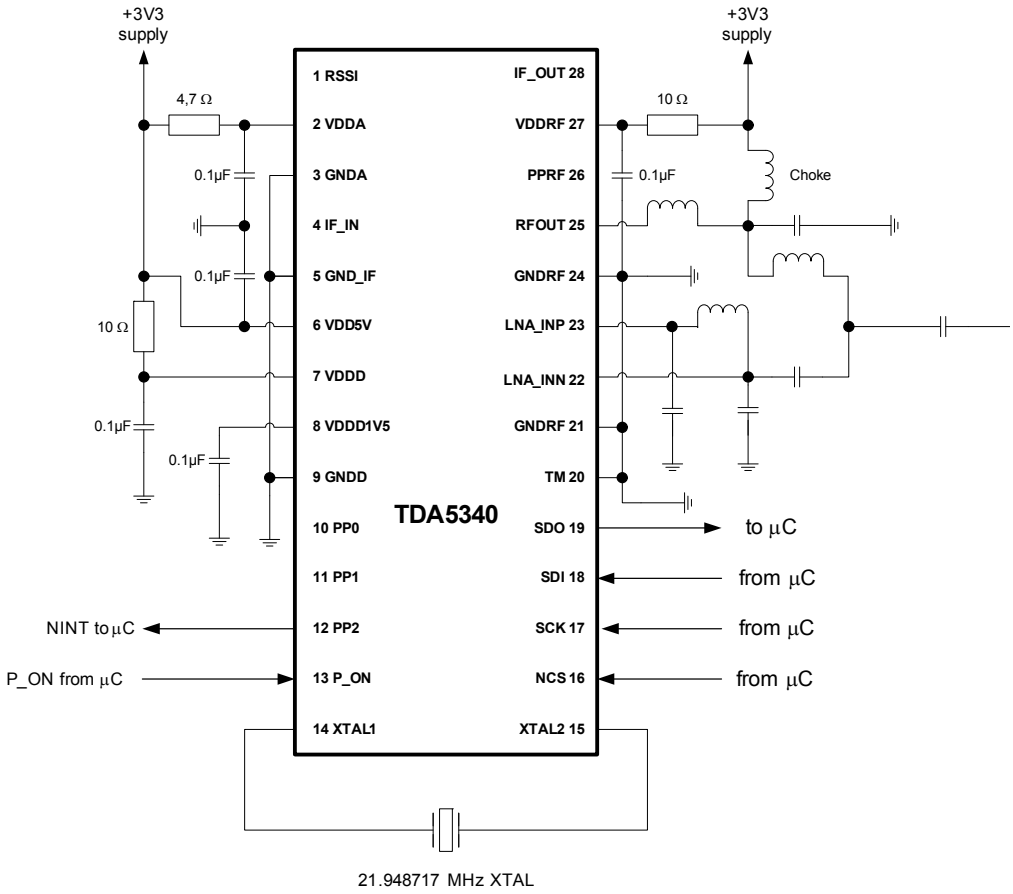


Figure 1 Application Example optimized for System Costs (3V3 Supply)

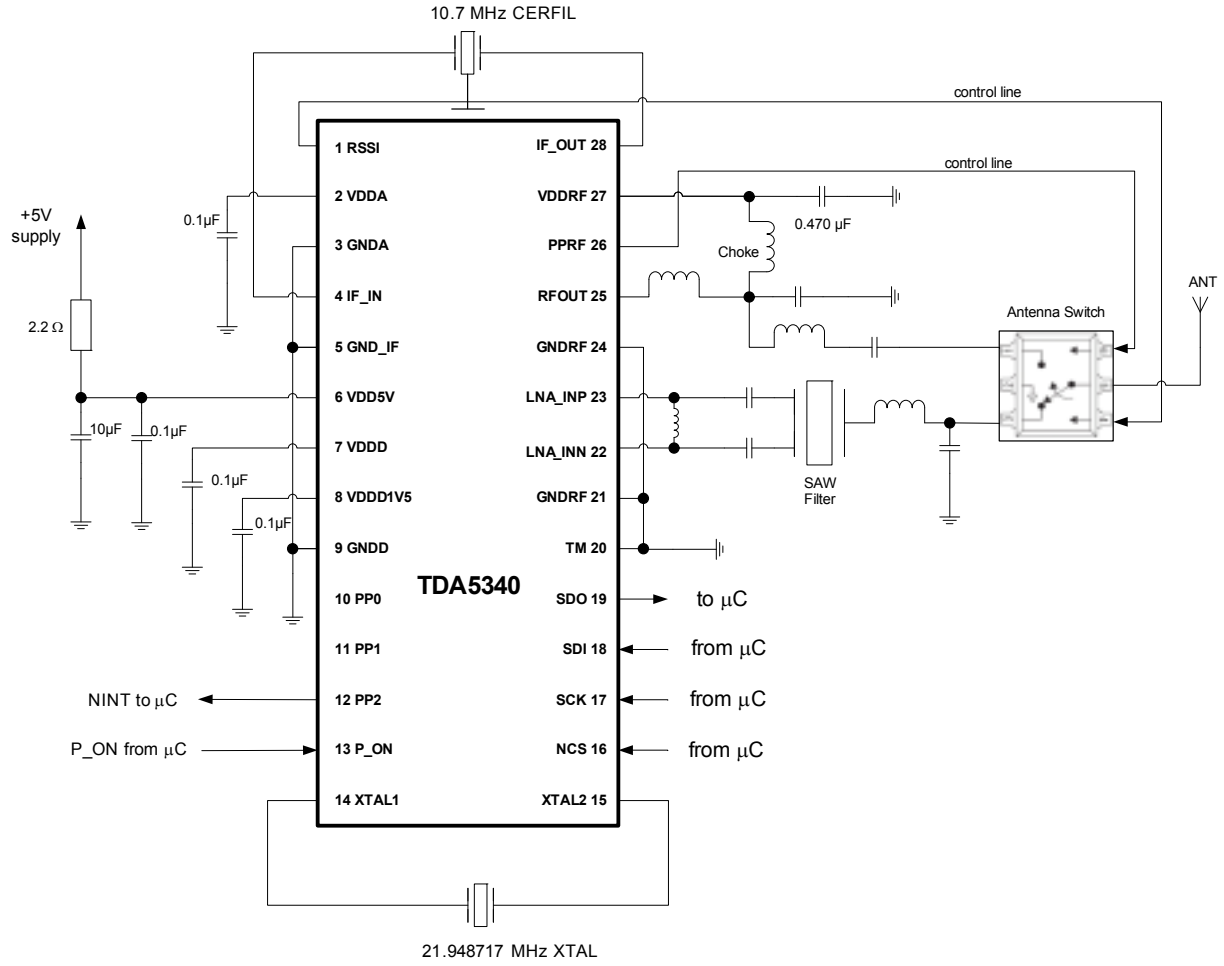


Figure 2 Application Example optimized for RF performance (5V Supply)

2 Functional Overview

2.1 Pin Configuration

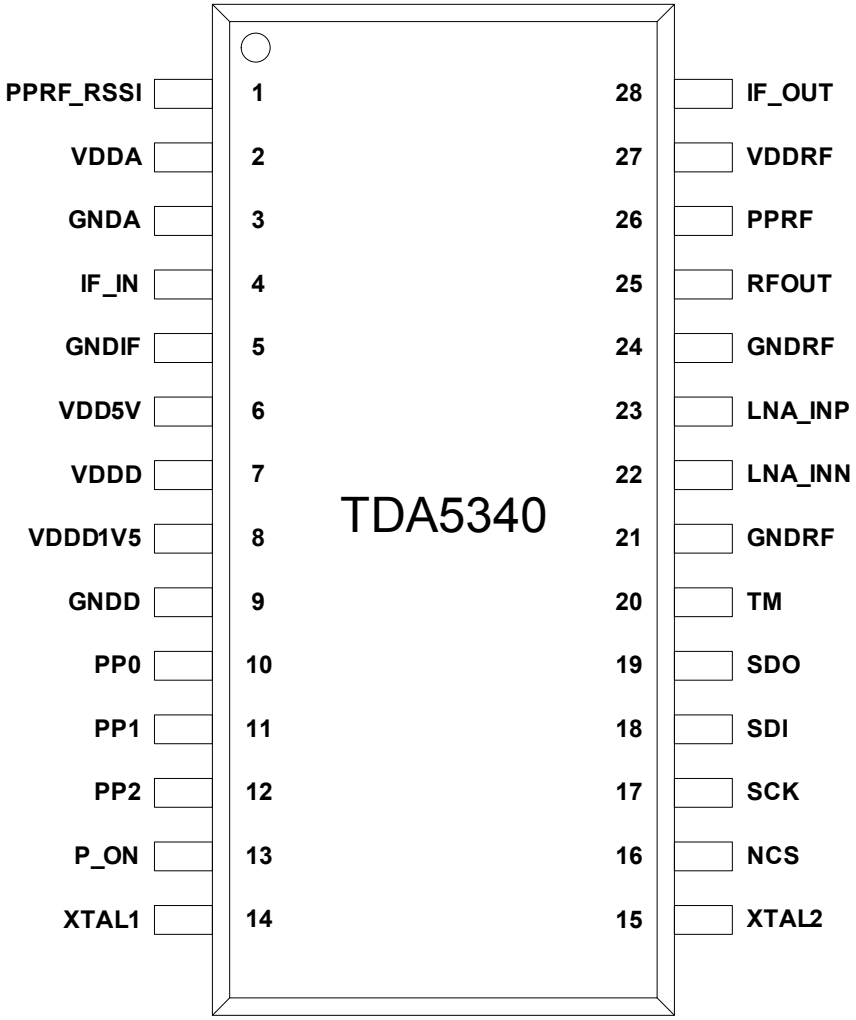


Figure 3 Pin-Out

2.1.1 Pin Definition

Table 1 Pin Definition and Function

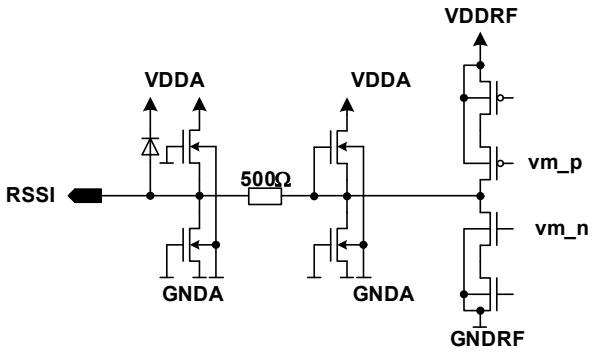
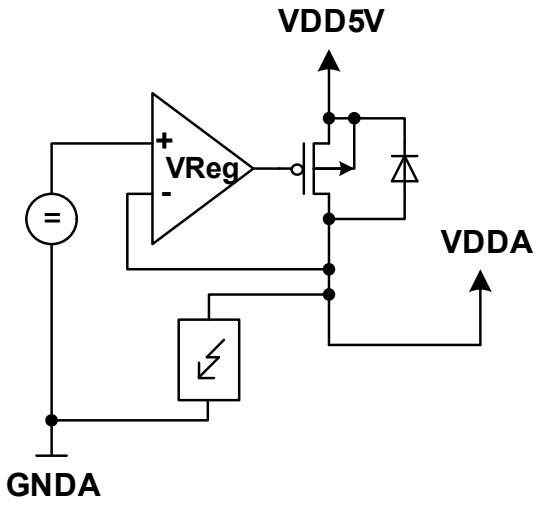
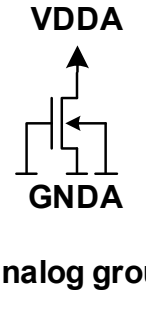
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
1	PPRF_RSSI		Analog output Digital output with weak driver capability, always in 3V domain CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
2	VDDA		Analog input Analog supply
3	GNDA		Analog Ground

Table 1 Pin Definition and Function

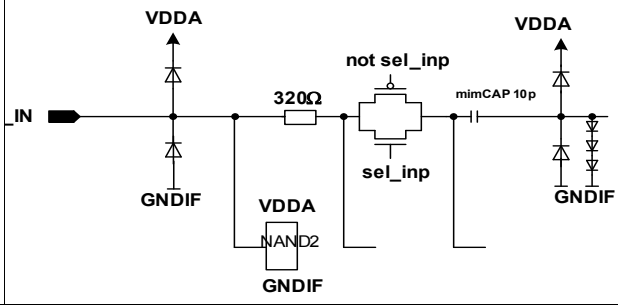
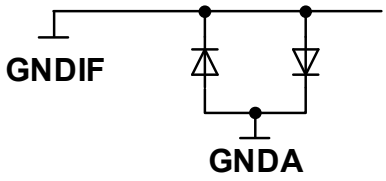
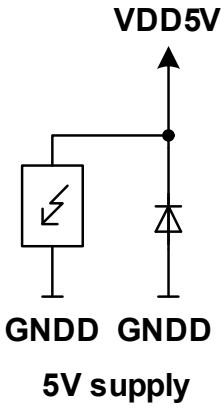
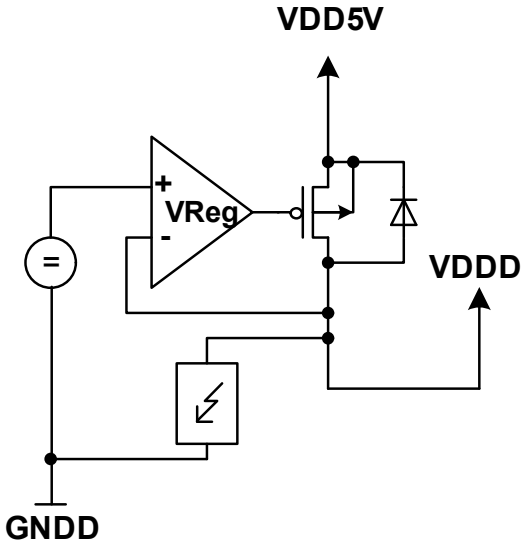
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
4	IF_IN		Analog input IF mixer input
5	GND_IF		Analog Ground
6	VDD5V		Analog input 5 Volt supply input
7	VDDD		Analog input digital supply input

Table 1 Pin Definition and Function

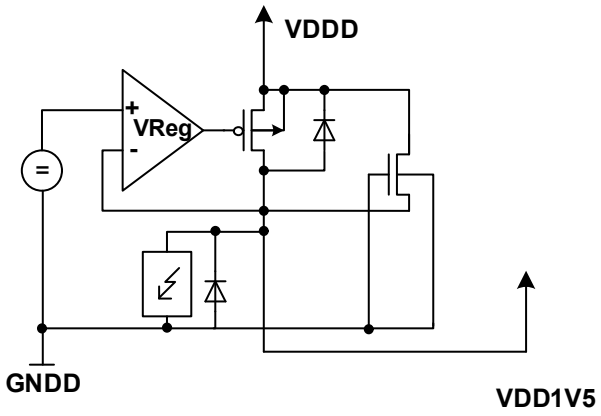
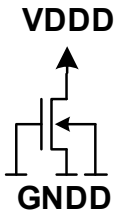
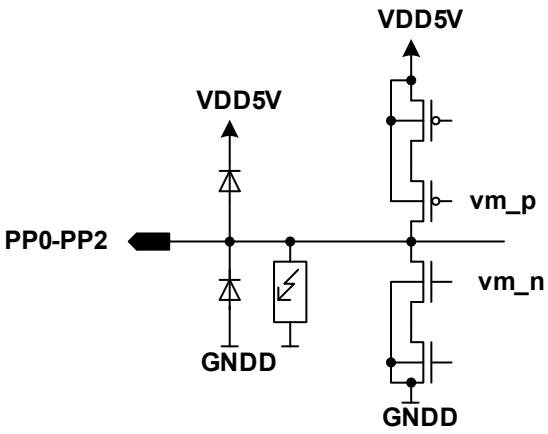
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
8	VDDD1V5		Analog output 1.5V regulator
9	GNDD		Digital ground
10	PP0		Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: CLK_OUT
11	PP1	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: DATA

Table 1 Pin Definition and Function

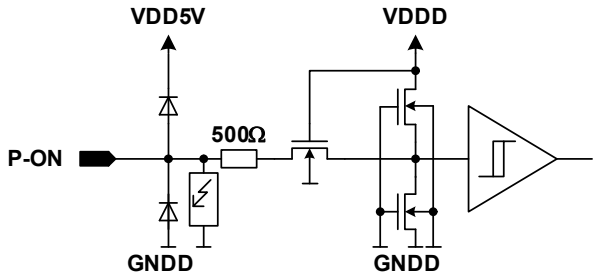
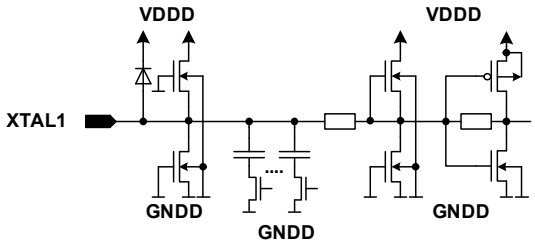
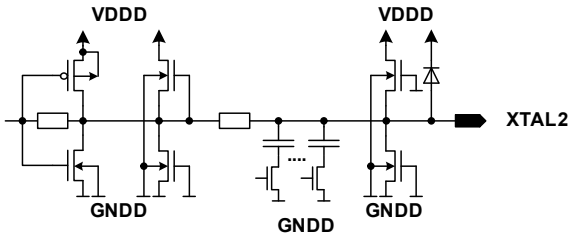
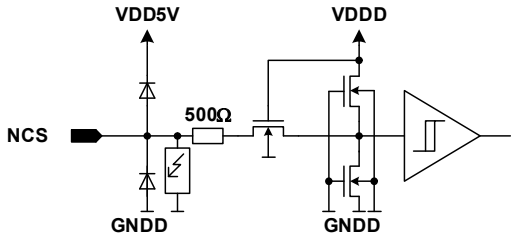
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
12	PP2	same as PP0	Digital output CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: NINT
13	P_ON		Digital input power-on reset
14	XTAL1		Analog input crystal oscillator input
15	XTAL2		Analog output crystal oscillator output
16	NCS		Digital input SPI Not Chip select

Table 1 Pin Definition and Function

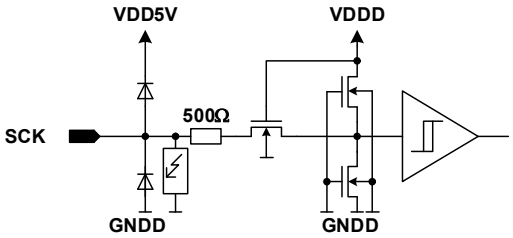
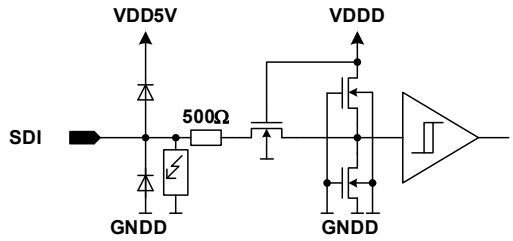
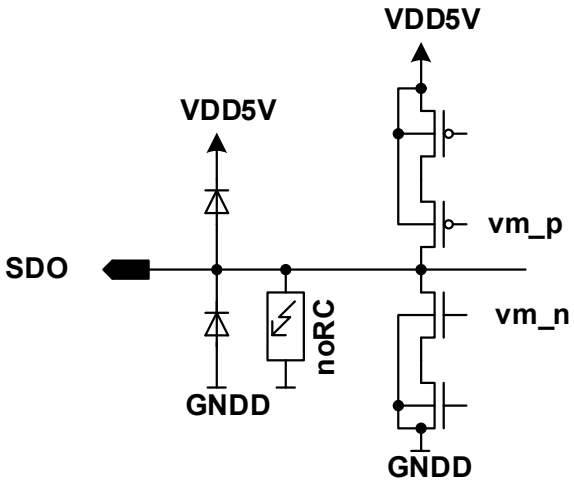
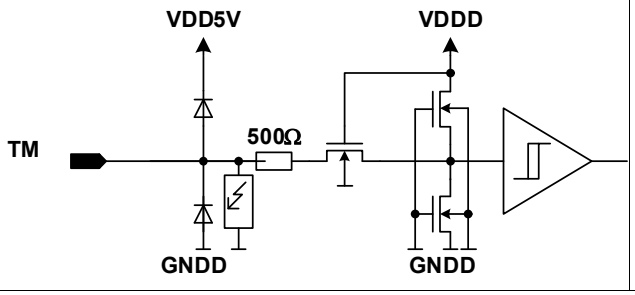
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
17	SCK		Digital input SPI clock
18	SDI		Digital input SPI data in
19	SDO		Digital output SPI data out
20	TM		Digital input connect to digital ground

Table 1 Pin Definition and Function

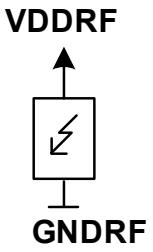
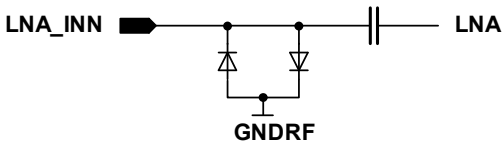
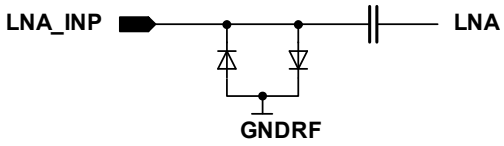
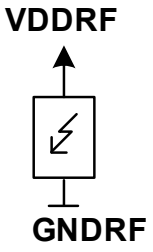
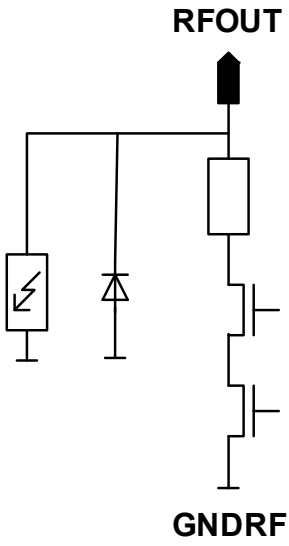
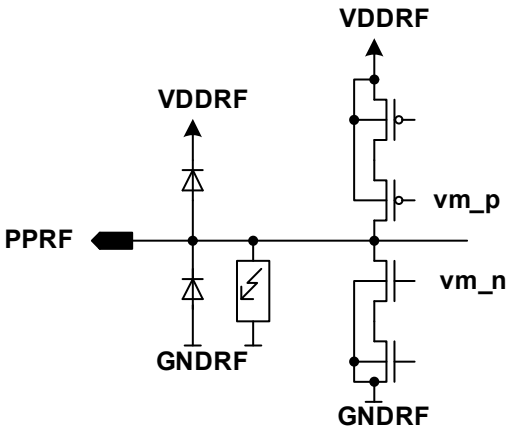
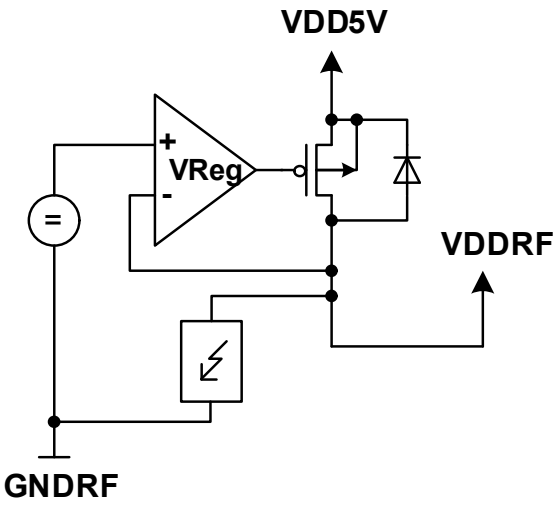
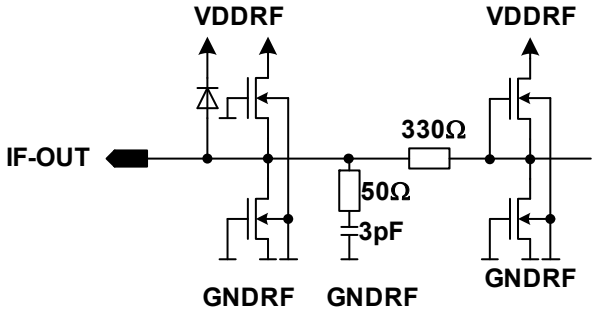
Pin Nr	Pad Name	Equivalent I/O Schematic	Function
21	GNDRF		Analog ground
22	LNA_INN		Analog input - RF input
23	LNA_INP		Analog input +RF input
24	GNDRF		Analog ground
25	RFOUT		Analog output power amplifier output

Table 1 Pin Definition and Function

Pin Nr	Pad Name	Equivalent I/O Schematic	Function
26	PPRF		Digital output always in 3V domain CLK_OUT, RX_RUN, NINT, ANT_EXTSW1, ANT_EXTSW1, DATA, DATA_MATCHFIL, CH_DATA, CH_STR, RXD, RXSTR, TXSTR and TRISTATE are programmable via SFR default: TRISTATE
27	VDDRF		Analog input RF supply
28	IF_OUT		Analog output Mixer output

2.2 Functional Block Diagram

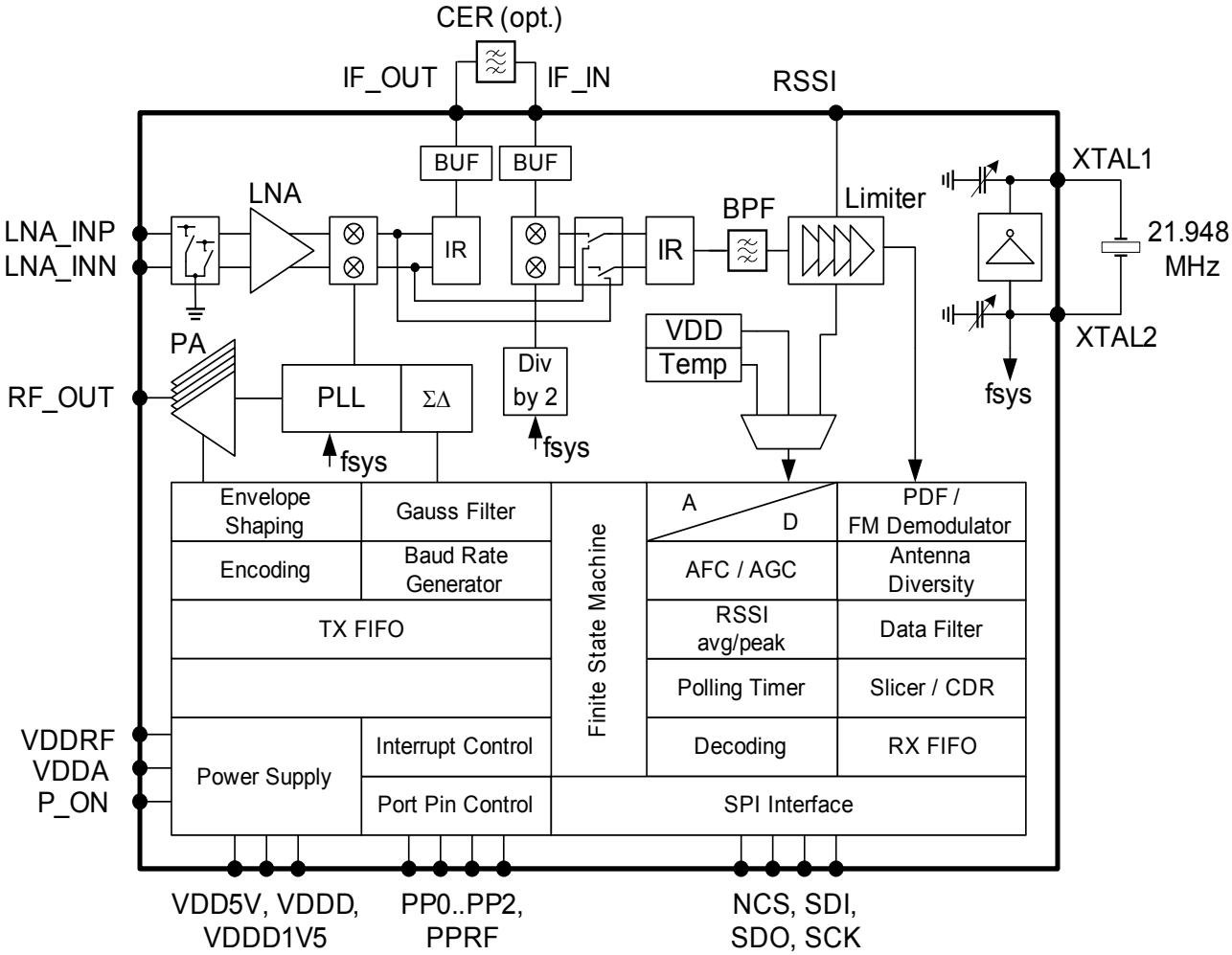


Figure 4 TDA5340 Block Diagram

2.3 Architecture Overview

A fully integrated Sigma-Delta Fractional-N PLL Synthesizer covers the frequency bands 300-320 MHz, 415-495 MHz, 860-960 MHz with a high frequency resolution, using only one VCO running at around 3.6 GHz. This makes the IC most suitable for Multi-Band/Multi-Channel applications. For Multi-Channel applications a very good channel separation is essential. To achieve the necessary high sensitivity and selectivity a double down conversion super-heterodyne architecture is used. The first IF frequency is located at 10.7 MHz and the second IF frequency at 274 kHz. For both IF frequencies an adjustment-free image frequency rejection feature is realized. In the second IF domain the filtering is done with an on-chip third order bandpass polyphase filter. A multi-stage bandpass limiter completes the RF/IF path of the receiver. For Single-Channel applications with relaxed requirements to selectivity, a single down conversion low-IF scheme can be selected.

A highly efficient Class C/E Power amplifier with an output level of +14dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for highest system power savings. The data can be either shifted out of a on-chip transmit FIFO or directly provided on an input pin.

An RSSI generator delivers a DC signal proportional to the applied input power and is also used as an ASK demodulator. Via an anti-aliasing filter this signal feeds an ADC with 10 bits resolution. The limiter output signal

feeds a digital FSK demodulator. This block demodulates the FSK data and delivers an AFC signal which controls the divider factor of the PLL synthesizer. A digital receiver, which comprises RSSI peak detectors, a matched data filter, a clock and data recovery, a data slicer, a frame synchronization and a data FIFO, decodes the received ASK or FSK data stream. The recovered data and clock signals are accessible via 2 separate pins. The FIFO data buffer is accessible via the SPI bus interface.The crystal oscillator serves as the reference frequency for the PLL phase detector, the clock signal of the Sigma-Delta modulator and divided by two as the 2nd local oscillator signal. To accelerate the start up of the crystal oscillator two modes are selectable: a Low Power Mode (with lower precision) and a High Precision Mode.

2.4 Block Overview

The TDA5340 is separated into the following main blocks:

- RF / IF Receiver
- Power Amplifier
- Crystal Oscillator and Clock Divider
- Sigma-Delta Fractional-N PLL Synthesizer
- ASK / FSK Demodulator incl. AFC and AGC
- RSSI Peak Detector
- Digital Baseband Receiver
- Digital Baseband Transmitter
- Power Supply Circuitry
- System Interface
- System Management Unit

2.5 Operating Modes

The transceiver has three different power saving modes, two receive modes and a transmit mode. The different operating modes are used to adjust the transceiver functionality to the needs of the application. Depending on the used communication protocols the appropriate power saving mode can be selected. In the table below all different modes are listed and corresponding to the modes the active blocks and current consumptions are shown.

Table 2 Operating Modes

Operating Mode	Transceiver Blocks								typ. Current Consumption
	Dig. Vreg	Ana. Vreg	XTAL	SFR	SPI	PLL	PA	RX	
Power Down	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	0.9 µA
Deep Sleep	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	7 µA
Sleep	ON	OFF	ON[1)]	ON	ON	OFF	OFF	OFF	40 µA[2)]
Sleep ADC enabled	ON	ON	ON[1)]	ON	ON	OFF	OFF	OFF	1 mA
Transmit Ready	ON	ON	ON	ON	ON	ON	OFF	OFF	5.8 mA
Transmit Idle	ON	ON	ON	ON	ON	OFF	OFF	OFF	<3 mA
Transmit	ON	ON	ON	ON	ON	ON	ON	OFF	12.5 mA[3)]
Receive	ON	ON	ON	ON	ON	ON	OFF	ON	11 mA[4)]

1) selectable between XTAL in high or low precision mode
2) XTAL in low precision mode
3) 10dBm Output power at 434MHz
4) single down conversion Mode (no external CER Filter used)

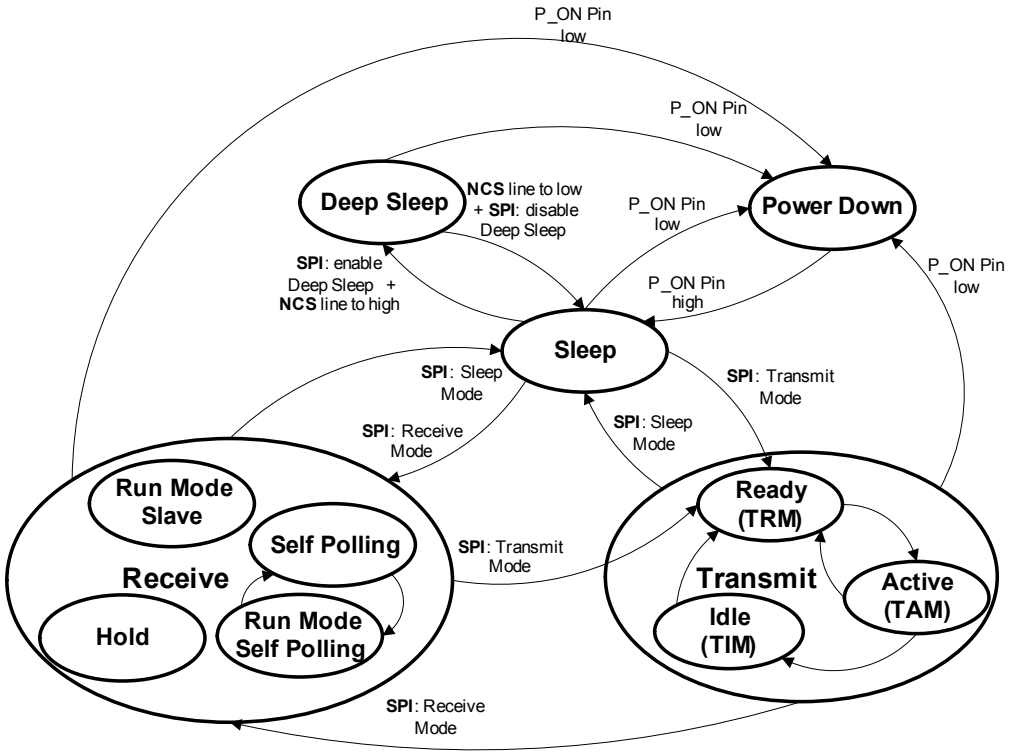


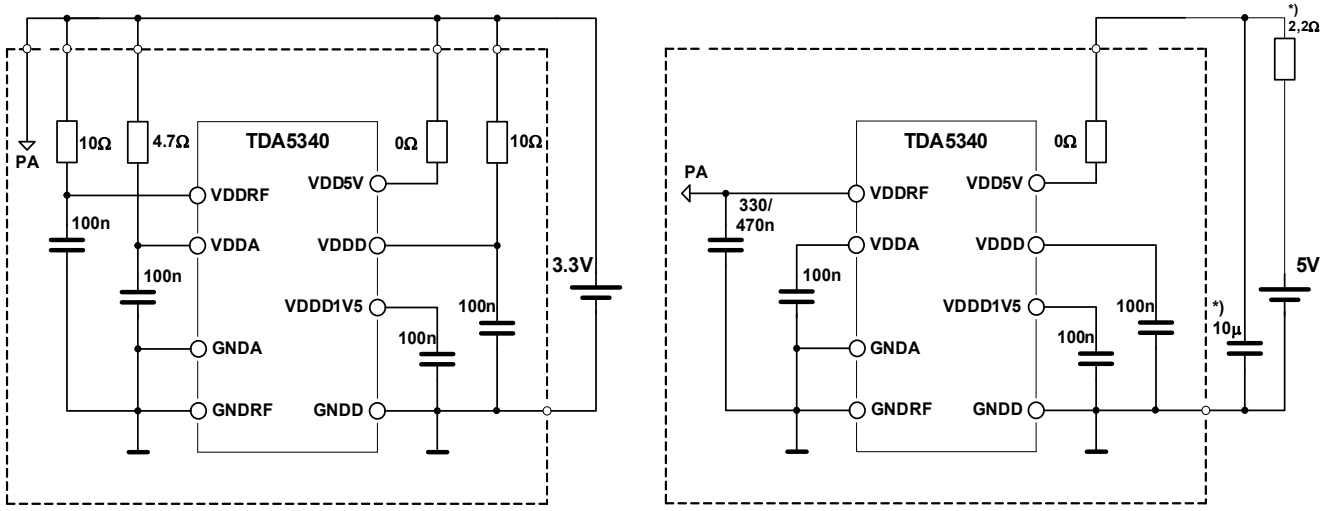
Figure 5 Main State Diagram

2.6 Block Description

2.6.1 Power Supply Circuitry

The chip may be operated within a 5 Volts or a 3.3 Volts environment.

For operation within a 5 Volts environment (supply voltage range 1), the chip is supplied via the VDD5V pin. In this configuration the digital I/O pads are supplied via VDD5V and a 5 V to 3.3 V voltage regulator supplies the analog/RF section (only active in Run Modes). When operating within a 3.3 Volts environment (supply voltage range 2), the VDD5V, VDDA, VDDD and VDDRF pins must be supplied. The 5 V to 3.3 V voltage regulators are inactive in this configuration.The internal digital core is supplied by an additional 3.3 V to 1.5 V regulator.The regulators for the digital section are controlled by the signal at P_ON (Power On) pin. A low signal at P_ON disables all regulators and set the IC in Power Down Mode. A low to high transition at P_ON enables the regulators for the digital section and initiates a power on reset. The regulator for the analog section is controlled by the Master Control Unit and is active only when the RF section is active.To provide data integrity within the digital units, a brownout detector monitors the digital supply. In case a voltage drop of VDDD below approximately 2.45 V is detected a RESET will be initiated. A typical power supply application for a 3.3 Volts and a 5 Volts environment is shown in the figure below.



Supply-Application in 3.3V environment

Supply-Application in 5V environment

*)
When operating in a 5V environment, the voltage-drop across the voltage regulators 5 → 3.3V has to be limited, to keep the regulators in a safe operating range. Resistive or capacitive loads (in excess to the scheme shown above) on pins VDDA and VDDD are not recommended.

Figure 6 3.3 Volts and 5 Volts Applications

2.6.2 Chip Reset

Power down and power on are controlled by the P_ON pin. A LOW at this pin keeps the IC in Power Down Mode. All voltage regulators and the internal biasing are switched off. A high transition at P_ON pin activates the appropriate voltage regulators and the internal biasing of the chip. A power up reset is generated at the same time.

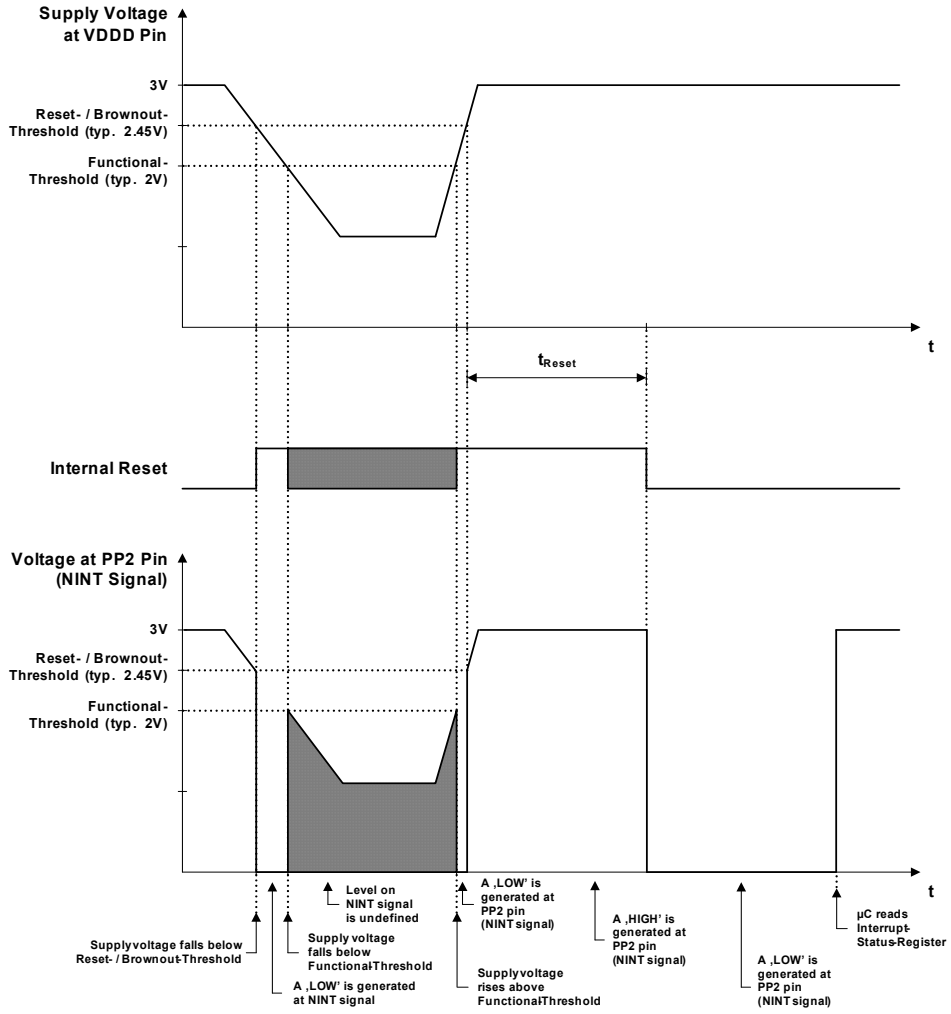


Figure 7 Reset Behavior

A second source that can trigger a reset is a brownout event. Whenever the integrated brownout detector measures a voltage drop below the brownout threshold on the digital supply, the integrity of the stored data and configuration can no longer be guaranteed; thus a reset is generated. While the supply voltage stays between the brownout and the functional threshold of the chip, the NINT signal is forced to low. When the supply voltage drops below the functional threshold, the levels of all digital output pins are undefined. When the supply voltage raises above the brownout threshold, the IC generates a high pulse at NINT and remains in the reset state for the duration of the reset time. When the IC leaves the reset state, the Interrupt Status registers are set to 0xFF and the NINT signal is forced to low. Now, the IC starts operation in the SLEEP Mode, ready to receive commands via the SPI interface. The NINT signal will go high, when one of the Interrupt Status registers is read for the first time.

2.6.3 RF / IF Receiver

The receiver path uses a double down conversion super-heterodyne/low-IF architecture, where the first IF frequency is located at 10.7 MHz and the second IF frequency at 274 kHz. For the first IF frequency an adjustment-free image frequency rejection is realized by means of two I/Q-mixers followed by a second order passive polyphase filter centered at 10.7 MHz (PPF). The I/Q-oscillator signals for the first down conversion are delivered from the PLL synthesizer. The frequency selection in the first IF domain is done by an external CER filter. For moderate or low performance applications, this ceramic filter can be substituted by a simple LC Pi-filter or completely by-passed using the receiver as a single down conversion low-IF scheme with 274 kHz IF frequency.

The down conversion to the second IF frequency is done by means of two high-side injected I/Q-mixers together with an on-chip third order bandpass polyphase filter (PPF2 + BPF). The I/Q-oscillator signals for the second down conversion are directly derived by division of two from the crystal oscillator frequency. The bandwidth of the bandpass filter (BPF) can be selected from 50 kHz to 300 kHz in 5 steps. For a frequency offset of 150 kHz to 120 kHz, the AFC (Automatic Frequency Control) function is mandatory. Activated AFC option might require a longer preamble sequence in the receive data stream.

The receiver enable signal (RX_RUN) can be offered at each of the port pins to control external components. Whenever the receiver is active, the RX_RUN output signal is active. Active high or active low is configurable via PPCFG2 register.

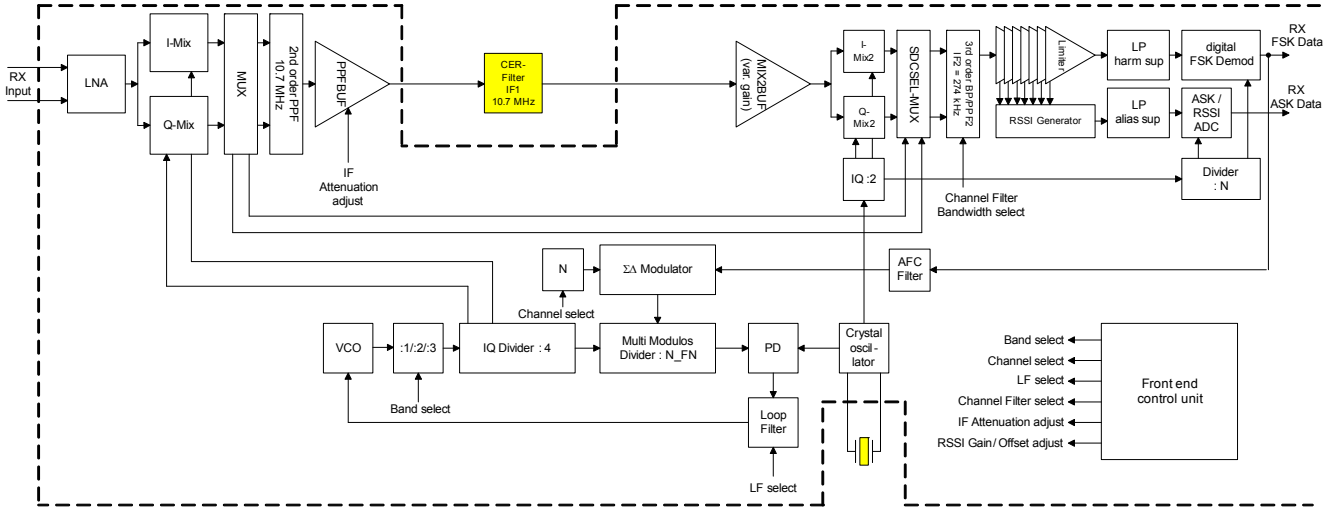


Figure 8 Block Diagram RF Receiver Section

2.6.4 Transmitter

A highly efficient Class C/E Power amplifier with output levels of +14 dBm combined with a Gaussian Filter for GFSK and amplitude ramping functions for shaped ASK is implemented. A high resolution power adjustment can be done to trim the output power for highest system power savings. The data can be either shifted out of a on-chip transmit FIFO or directly provided on an input pin.

2.6.5 Crystal Oscillator and Clock Divider

The crystal oscillator is a Pierce type oscillator. An automatic amplitude regulation circuitry allows the oscillator to operate with minimum current consumption. In SLEEP Mode, where the current consumption should be as low as possible, the load capacitor must be small and the frequency is slightly detuned, therefore all internal trim capacitors are disconnected. The internal capacitors are controlled by the crystal oscillator calibration registers XTALCALx. With a binary weighted capacitor array the necessary load capacitor can be selected.

Whenever a XTALCALx register value is updated, the selected trim capacitors are automatically connected to the crystal so that the frequency is precise at the specified value. Step size is 1 pF. The SFR control bit XTALHPMS can be used to activate the High Precision Mode also during SLEEP Mode.