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TDA6650TT; TDA6651TT

5 V mixer/oscillator and low noise PLL synthesizer for hybrid terrestrial tuner (digital and analog)

Rev. 05 — 10 January 2007 | Product data sheet

1. General description

The TDA6650TT; TDA6651TT is a programmable 3-band mixer/oscillator and low phase noise PLL synthesizer intended for pure 3-band tuner concepts applied to hybrid (digital and analog) or digital only terrestrial and cable TV reception.

Table 1. Different versions are available depending on the target application[1]

Application	Type version
hybrid (analog and digital)	TDA6650TT/C3
	TDA6651TT/C3
digital only	TDA6650TT/C3/S2
	TDA6651TT/C3/S2
	TDA6651TT/C3/S3

[1] See Table 22 "Characteristics" for differences between TDA6651TT/C3/S2 and TDA6651TT/C3/S3.

The device includes three double balanced mixers for low, mid and high bands, three oscillators for the corresponding bands, a switchable IF amplifier, a wideband AGC detector and a low noise PLL synthesizer. The frequencies of the three bands are shown in Table 2. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling and to improve the adjacent channel rejection.

Table 2. Recommended band limits in MHz

Band	RF input		Oscillator	
	Min	Max	Min	Max
PAL and DVB-T tuners for hybrid application[1]				
Low	44.25	157.25	83.15	196.15
Mid	157.25	443.25	196.15	482.15
High	443.25	863.25	482.15	902.15
DVB-T tuners for digital only application[2]				
Low	47.00	160.00	83.15	196.15
Mid	160.00	446.00	196.15	482.15
High	446.00	866.00	482.15	902.15

[1] RF input frequency is the frequency of the corresponding picture carrier for analog standard.

[2] RF input frequency is the frequency of the center of DVB-T channel.

The IF amplifier is switchable in order to drive both symmetrical and asymmetrical outputs. When it is used as an asymmetrical amplifier, the IFOUTB pin needs to be connected to the supply voltage V_{CCA}.

founded by Philips

Five open-drain PMOS ports are included on the IC. Two of them, BS1 and BS2, are also dedicated to the selection of the low, mid and high bands. PMOS port BS5 pin is shared with the ADC.

The AGC detector provides a control that can be used in a tuner to set the gain of the RF stage. Six AGC take-over points are available by software. Two programmable AGC time constants are available for search tuning and normal tuner operation.

The local oscillator signal is fed to the fractional-N divider. The divided frequency is compared to the comparison frequency into the fast phase detector which drives the charge pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the 33 V tuning voltage without the need to add an external transistor.

The comparison frequency is obtained from an on-chip crystal oscillator. The crystal frequency can be output to the XTOUT pin to drive the clock input of a digital demodulation IC.

Control data is entered via the I^2C-bus; six serial bytes are required to address the device, select the Local Oscillator (LO) frequency, select the step frequency, program the output ports and set the charge pump current or select the ALBC mode, enable or disable the crystal output buffer, select the AGC take-over point and time constant and/or select a specific test mode. A status byte concerning the AGC level detector and the ADC voltage can be read out on the SDA line during a read operation. During a read operation, the loop ‘in-lock’ flag, the power-on reset flag and the automatic loop bandwidth control flag are read.

The device has 4 programmable addresses. Each address can be selected by applying a specific voltage to pin AS, enabling the use of multiple devices in the same system.

The I^2C-bus is fast mode compatible, except for the timing as described in the functional description and is compatible with 5 V, 3.3 V and 2.5 V microcontrollers depending on the voltage applied to pin BVS.

2. Features

- Single-chip 5 V mixer/oscillator and low phase noise PLL synthesizer for TV and VCR tuners, dedicated to hybrid (digital and analog) as well as pure digital applications (DVB-T)
- Five possible step frequencies to cope with different digital terrestrial TV and analog TV standards
- Eight charge pump currents between 40 μA and 600 μA to reach the optimum phase noise performance over the bands
- Automatic Loop Bandwidth Control (ALBC) sets the optimum phase noise performance for DVB-T channels
- I^2C-bus protocol compatible with 2.5 V, 3.3 V and 5 V microcontrollers:
  - Address + 5 data bytes transmission (I^2C-bus write mode)
  - Address + 1 status byte (I^2C-bus read mode)
  - Four independent I^2C-bus addresses.
- Five PMOS open-drain ports with 15 mA source capability for band switching and general purpose; one of these ports is combined with a 5-step ADC
- Wideband AGC detector for internal tuner AGC:

  - Six programmable take-over points
  - Two programmable time constants
  - AGC flag.
- In-lock flag
- Crystal frequency output buffer
- 33 V tuning voltage output
- Fractional-N programmable divider
- Balanced mixers with a common emitter input for the low band and for the mid band (each single input)
- Balanced mixer with a common base input for the high band (balanced input)
- 2-pin asymmetrical oscillator for the low band
- 2-pin symmetrical oscillator for the mid band
- 4-pin symmetrical oscillator for the high band
- Switched concept IF amplifier with both asymmetrical and symmetrical outputs to drive low impedance or SAW filters i.e. 500 Ω / 40 pF.

3. Applications

For all applications, the recommendations given in the latest application note *AN10544* must be used.

3.1 Application summary

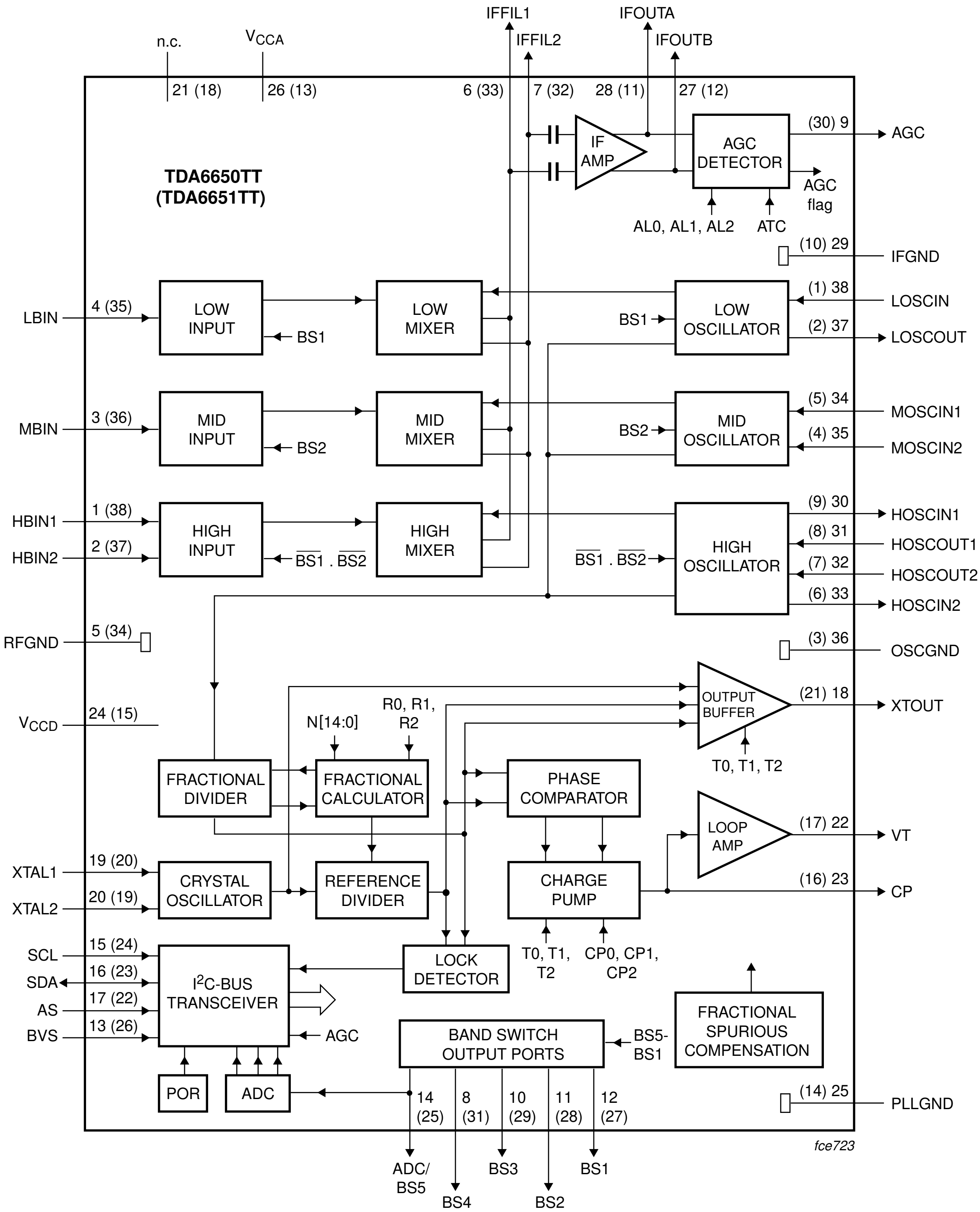
- Digital and analog terrestrial tuners (OFDM, PAL, etc.)
- Cable tuners (QAM)
- Digital TV sets
- Digital set-top boxes.

4. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
TDA6650TT/C3	TSSOP38	plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm	SOT510-1
TDA6650TT/C3/S2			
TDA6651TT/C3			
TDA6651TT/C3/S2			
TDA6651TT/C3/S3			

5. Block diagram



The pin numbers in parenthesis represent the TDA6651TT.

Fig 1. Block diagram

6. Pinning information

6.1 Pin description

Table 4. Pin description

Symbol	Pin		Description
	TDA6650TT	TDA6651TT	
HBIN1	1	38	high band RF input 1
HBIN2	2	37	high band RF input 2
MBIN	3	36	mid band RF input
LBIN	4	35	low band RF input
RFGND	5	34	RF ground
IFFIL1	6	33	IF filter output 1
IFFIL2	7	32	IF filter output 2
BS4	8	31	PMOS open-drain output port 4 for general purpose
AGC	9	30	AGC output
BS3	10	29	PMOS open-drain output port 3 for general purpose
BS2	11	28	PMOS open-drain output port 2 to select the mid band
BS1	12	27	PMOS open-drain output port 1 to select the low band
BVS	13	26	bus voltage selection input
ADC/BS5	14	25	ADC input or PMOS open-drain output port 5 for general purpose
SCL	15	24	I^2C-bus serial clock input
SDA	16	23	I^2C-bus serial data input and output
AS	17	22	I^2C-bus address selection input
XTOUT	18	21	crystal frequency buffer output
XTAL1	19	20	crystal oscillator input 1
XTAL2	20	19	crystal oscillator input 2
n.c	21	18	not connected
VT	22	17	tuning voltage output
CP	23	16	charge pump output
V_{CCD}	24	15	supply voltage for the PLL part
PLLGND	25	14	PLL ground
V_{CCA}	26	13	supply voltage for the analog part
IFOUTB	27	12	IF output B for symmetrical amplifier and asymmetrical IF amplifier switch input
IFOUTA	28	11	IF output A
IFGND	29	10	IF ground
HOSCIN1	30	9	high band oscillator input 1
HOSCOUT1	31	8	high band oscillator output 1
HOSCOUT2	32	7	high band oscillator output 2
HOSCIN2	33	6	high band oscillator input 2

Table 4. Pin description *...continued*

Symbol	Pin		Description
	TDA6650TT	TDA6651TT	
MOSCIN1	34	5	mid band oscillator input 1
MOSCIN2	35	4	mid band oscillator input 2
OSCGND	36	3	oscillators ground
LOSCOUT	37	2	low band oscillator output
LOSCIN	38	1	low band oscillator input

6.2 Pinning

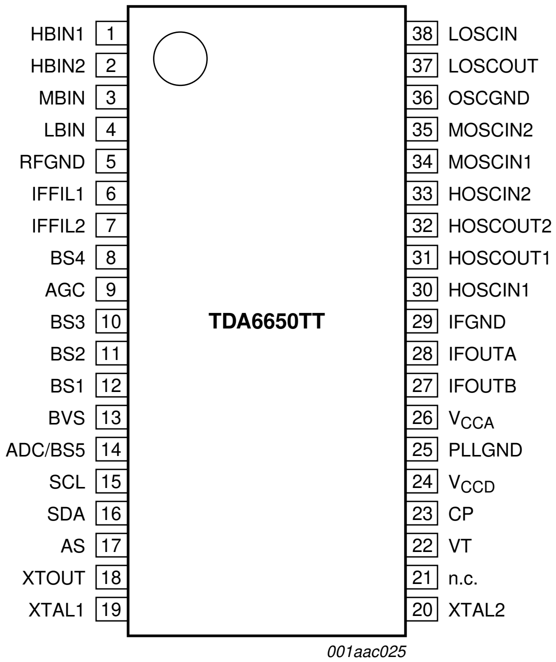


Fig 2. Pin configuration TDA6650TT

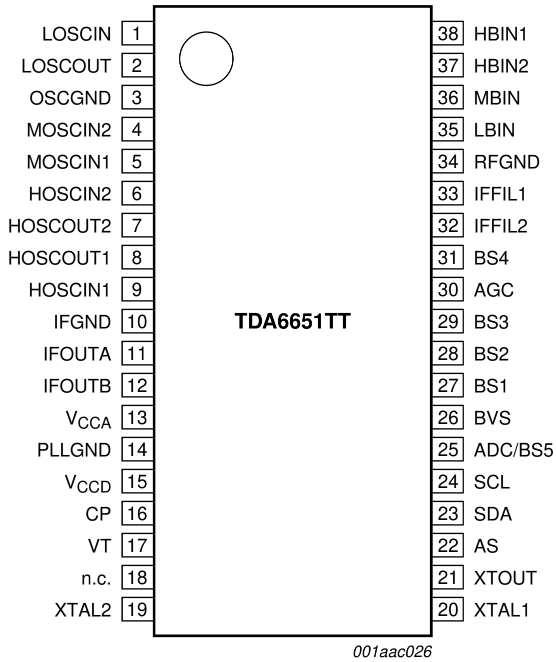


Fig 3. Pin configuration TDA6651TT

7. Functional description

7.1 Mixer, Oscillator and PLL (MOPLL) functions

Bit BS1 enables the BS1 port, the low band mixer and the low band oscillator. Bit BS2 enables the BS2 port, the mid band mixer and the mid band oscillator. When both BS1 and BS2 bits are logic 0, the high band mixer and the high band oscillator are enabled.

The oscillator signal is applied to the fractional-N programmable divider. The divided signal f_{div} is fed to the phase comparator where it is compared in both phase and frequency with the comparison frequency f_{comp}. This frequency is derived from the signal present on the crystal oscillator f_{xtal} and divided in the reference divider. There is a fractional calculator on the chip that generates the data for the fractional divider as well as the reference divider ratio, depending on the step frequency selected. The crystal oscillator requires a 4 MHz crystal in series with an 18 pF capacitor between pins XTAL1 and XTAL2.

The output of the phase comparator drives the charge pump and the loop amplifier section. This amplifier has an on-chip high voltage drive transistor. Pin CP is the output of the charge pump, and pin VT is the pin to drive the tuning voltage to the varicap diodes of the oscillators and the tracking filters. The loop filter has to be connected between pins CP and VT. The spurious signals introduced by the fractional divider are automatically compensated by the spurious compensation block.

It is possible to drive the clock input of a digital demodulation IC from pin XTOUT with the 4 MHz signal from the crystal oscillator. This output is also used to output $\frac{1}{2}f_{div}$ and f_{comp} signals in a specific test mode (see Table 9). It is possible to switch off this output, which is recommended when it is not used.

For test and alignment purposes, it is also possible to release the tuning voltage output by selecting the sinking mode (see Table 9), and by applying an external voltage on pin VT.

In addition to the BS1 and BS2 output ports that are used for the band selection, there are three general purpose ports BS3, BS4 and BS5. All five ports are PMOS open-drain type, each with 15 mA drive capability. The connection for port BS5 and the ADC input is combined on one pin. It is not possible to use the ADC if port BS5 is used.

The AGC detector compares the level at the IF amplifier output to a reference level which is selected from 6 different levels via the I^{2}C-bus. The time constant of the AGC can be selected via the I^{2}C-bus to cope with normal operation as well as with search operation.

When the output level on pin AGC is higher than the threshold V_{RMH}, then bit AGC = 1. When the output level on pin AGC is lower than the threshold V_{RML}, then bit AGC = 0. Between these two thresholds, bit AGC is not defined. The status of the AGC bit can be read via the I^{2}C-bus according to the read mode as described in Table 15.

7.2 I^{2}C-bus voltage

The I^{2}C-bus lines SCL and SDA can be connected to an I^{2}C-bus system tied to 2.5 V, 3.3 V or 5 V. The choice of the bus input threshold voltages is made with pin BVS that can be left open-circuit, connected to the supply voltage or to ground (see Table 5).

Table 5. I^{2}C-bus voltage selection

Pin BVS connection	Bus voltage	Logic level	
		LOW	HIGH
To ground	2.5 V	0 V to 0.75 V	1.75 V to 5.5 V
Open-circuit	3.3 V	0 V to 1.0 V	2.3 V to 5.5 V
To V_{CC}	5 V	0 V to 1.5 V	3.0 V to 5.5 V

7.3 Phase noise, I^{2}C-bus traffic and crosstalk

While the TDA6650TT; TDA6651TT is dedicated for hybrid terrestrial applications, the low noise PLL will clean up the noise spectrum of the VCOs close to the carrier to reach noise levels at 1 kHz offset from the carrier compatible with e.g. DVB-T reception.

Linked to this noise improvement, some disturbances may become visible while they were not visible because they were hidden into the noise in analog dedicated applications and circuits.

This is especially true for disturbances coming from the I²C-bus traffic, whatever this traffic is intended for the MOPLL or for another slave on the bus.

To avoid this I²C-bus crosstalk and be able to have a clean noise spectrum, it is necessary to use a bus gate that enables the signal on the bus to drive the MOPLL only when the communication is intended for the tuner part (such a kind of I²C-bus gate is included into the NXP terrestrial channel decoders), and to avoid unnecessary repeated sending of the same information.

8. I²C-bus protocol

The TDA6650TT; TDA6651TT is controlled via the two-wire I²C-bus. For programming, there is one device address (7 bits) and the R/$\overline{W}$ bit for selecting read or write mode. To be able to have more than one MOPLL in an I²C-bus system, one of four possible addresses is selected depending on the voltage applied to address selection pin AS (see Table 8).

The TDA6650TT; TDA6651TT fulfils the fast mode I²C-bus, according to the NXP I²C-bus specification, except for the timing as described in Figure 4. The I²C-bus interface is designed in such a way that the pins SCL and SDA can be connected to 5 V, 3.3 V or to 2.5 V pulled-up I²C-bus lines, depending on the voltage applied to pin BVS (see Table 5).

8.1 Write mode; R/$\overline{W}$ = 0

After the address transmission (first byte), data bytes can be sent to the device (see Table 6). Five data bytes are needed to fully program the TDA6650TT; TDA6651TT. The I²C-bus transceiver has an auto-increment facility that permits programming the device within one single transmission (address + 5 data bytes).

The TDA6650TT; TDA6651TT can also be partly programmed on the condition that the first data byte following the address is byte 2 (divider byte 1) or byte 4 (control byte 1). The first bit of the first data byte transmitted indicates whether byte 2 (first bit = 0) or byte 4 (first bit = 1) will follow. Until an I²C-bus STOP condition is sent by the controller, additional data bytes can be entered without the need to re-address the device. The fractional calculator is updated only at the end of the transmission (STOP condition). Each control byte is loaded after the 8th clock pulse of the corresponding control byte. Main divider data are valid only if no new I²C-bus transmission is started (START condition) during the computation period of 50 μs.

Both DB1 and DB2 need to be sent to change the main divider ratio. If the value of the ratio selection bits R2, R1 and R0 are changed, the bytes DB1 and DB2 have to be sent in the same transmission.

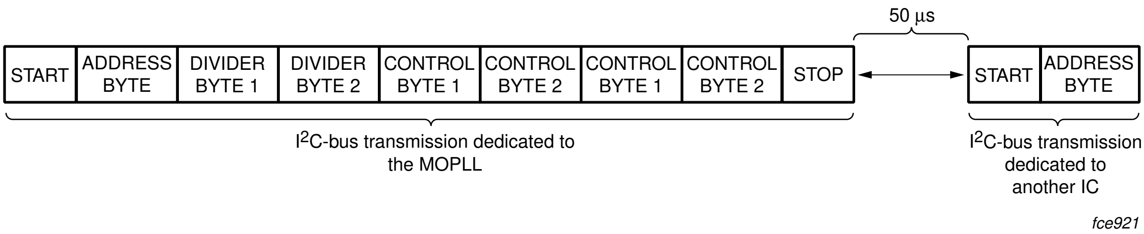


Fig 4. Example of I²C-bus transmission frame

Table 6. I²C-bus write data format

Name	Byte	Bit								Ack
		MSB[1]							**LSB**	
Address byte	1	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1 (DB1)	2	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	3	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1 (CB1); see Table 7	4	1	T/A = 1	T2	T1	T0	R2	R1	R0	A
		1	T/A = 0	0	0	ATC	AL2	AL1	AL0	A
Control byte 2 (CB2)	5	CP2	CP1	CP0	BS5	BS4	BS3	BS2	BS1	A

[1] MSB is transmitted first.

Table 7. Description of write data format bits

Bit	Description
A	acknowledge
MA1 and MA0	programmable address bits; see Table 8
R/$\overline{W}$	logic 0 for write mode
N14 to N0	programmable LO frequency; $N = N14 \times 2^{14} + N13 \times 2^{13} + N12 \times 2^{12} + ... + N1 \times 2^{1} + N0$
T/A	test/AGC bit
	T/A = 0: the next 6 bits sent are AGC settings
	T/A = 1: the next 6 bits sent are test and reference divider ratio settings
T2, T1 and T0	test bits; see Table 9
R2, R1 and R0	reference divider ratio and programmable frequency step; see Table 10
ATC	AGC current setting and time constant; capacitor on pin AGC = 150 nF
	ATC = 0: AGC current = 220 nA; AGC time constant = 2 s
	ATC = 1: AGC current = 9 µA; AGC time constant = 50 ms
AL2, AL1 and AL0	AGC take-over point bits; see Table 11
CP2, CP1 and CP0	charge pump current; see Table 12
BS5, BS4, BS3, BS2 and BS1	PMOS ports control bits
	BSn = 0: corresponding port is off, high-impedance state (status at power-on reset)
	BSn = 1: corresponding port is on; $V_O = V_{CC} - V_{DS(sat)}$

8.1.1 I²C-bus address selection

The device address contains programmable address bits MA1 and MA0, which offer the possibility of having up to four MOPLL ICs in one system. Table 8 gives the relationship between the voltage applied to the AS input and the MA1 and MA0 bits.

Table 8. Address selection

Voltage applied to pin AS	MA1	MA0
0 V to $0.1V_{CC}$	0	0
$0.2V_{CC}$ to $0.3V_{CC}$ or open-circuit	0	1
$0.4V_{CC}$ to $0.6V_{CC}$	1	0
$0.9V_{CC}$ to V_{CC}	1	1

8.1.2 XTOUT output buffer and mode setting

The crystal frequency can be sent to pin XTOUT and used in the application, for example to drive the clock input of a digital demodulator, saving a quartz crystal in the bill of material. To output f_{xtal}, it is necessary to set T[2:0] to 001. If the output signal on this pin is not used, it is recommended to disable it, by setting T[2:0] to 000. This pin is also used to output $\frac{1}{2}f_{div}$ and f_{comp} in a test mode. At power-on, the XTOUT output buffer is set to on, supplying the f_{xtal} signal. The relation between the signal on pin XTOUT and the setting of the T[2:0] bits is given in Table 9.

Table 9. XTOUT buffer status and test modes

T2	T1	T0	Pin XTOUT	Mode
0	0	0	disabled	normal mode with XTOUT buffer off
0	0	1	f_{xtal} (4 MHz)	normal mode with XTOUT buffer on
0	1	0	$\frac{1}{2}f_{div}$	charge pump off
0	1	1	f_{xtal} (4 MHz)	switch ALBC on or off[1]
1	0	0	f_{comp}	test mode
1	0	1	$\frac{1}{2}f_{div}$	test mode
1	1	0	f_{xtal} (4 MHz)	charge pump sinking current[2]
1	1	1	disabled	charge pump sourcing current

[1] Automatic Loop Bandwidth Control (ALBC) is disabled at power-on reset. After power-on reset this feature is enabled by setting T[2:0] = 011. To disable again the ALBC, set T[2:0] = 011 again. This test mode acts like a toggle switch, which means each time it is set the status of the ALBC changes. To toggle the ALBC, two consecutive Control byte 1s (CB1), should be sent: one byte with T[2:0] = 011 indicating that ALBC will be switched on or off and one byte programming the test mode to be selected (see Table 30, example of I²C-bus sequence).

[2] This is the default mode at power-on reset. This mode disables the tuning voltage.

8.1.3 Step frequency setting

The step frequency is set by three bits, giving five steps to cope with different application requirements.

The reference divider ratio is automatically set depending on bits R2, R1 and R0. The phase detector works at either 4 MHz, 2 MHz or 1 MHz.

Table 10 shows the step frequencies and corresponding reference divider ratios. When the value of bits R2, R1 and R0 are changed, it is necessary to re-send the data bytes DB1 and DB2.

Table 10. Reference divider ratio select bits

R2	R1	R0	Reference divider ratio	Frequency comparison	Frequency step
0	0	0	2	2 MHz	62.5 kHz
0	0	1	1	4 MHz	142.86 kHz
0	1	0	1	4 MHz	166.67 kHz
0	1	1	4	1 MHz	50 kHz
1	0	0	1	4 MHz	125 kHz
1	0	1	-	-	reserved
1	1	0	-	-	reserved
1	1	1	-	-	reserved

8.1.4 AGC detector setting

The AGC take-over point can be selected out of 6 levels according to Table 11.

Table 11. AGC programming

AL2	AL1	AL0		Typical take-over point level
0	0	0	[1]	124 dBμV (p-p)
0	0	1	[1]	121 dBμV (p-p)
0	1	0	[1]	118 dBμV (p-p)
0	1	1	[2]	115 dBμV (p-p)
1	0	0	[2]	112 dBμV (p-p)
1	0	1	[2]	109 dBμV (p-p)
1	1	0	[3]	I_{AGC} = 0 A
1	1	1	[4]	V_{AGC} = 3.5 V

[1] This take-over point is available for both symmetrical and asymmetrical modes.

[2] This take-over point is available for asymmetrical mode only.

[3] The AGC current sources are disabled. The AGC output goes into a high-impedance state and an external AGC source can be connected in parallel and will not be influenced.

[4] The AGC detector is disabled and I_{AGC} = 9 μA.

8.1.5 Charge pump current setting

The charge pump current can be chosen from 8 values depending on the value of bits CP2, CP1 and CP0 bits; see Table 12. The programming of the CP bits are not taken into account when ALBC mode is in use.

Table 12. Charge pump current

CP2	CP1	CP0	Charge pump current number	Typical current (absolute value in μA)
0	0	0	1	38
0	0	1	2	54
0	1	0	3	83
0	1	1	4	122
1	0	0	5	163

Table 12. Charge pump current...*continued*

CP2	CP1	CP0	Charge pump current number	Typical current (absolute value in μA)
1	0	1	6	254
1	1	0	7	400
1	1	1	8	580

8.1.6 Automatic Loop Bandwidth Control (ALBC)

In a PLL controlled VCO in which the PLL reduces phase noise close to the carrier, there is an optimum loop bandwidth corresponding to the minimum integrated phase jitter. This loop bandwidth depends on different parameters like the VCO slope, the loop filter components, the dividing ratio and the gain of the phase detector and charge pump.

In order to reach the best phase noise performance it is necessary, especially in a wideband system like a digital tuner, to set the charge pump current to different values depending on the band and frequency used. This is to cope with the variations of the different parameters that set the bandwidth. The selection can be done in the application and requires for each frequency to program not only the divider ratios, but also the band and the best charge pump current.

The TDA6650TT; TDA6651TT includes the ALBC feature that automatically sets the band and the charge pump current, provided the IC is used in the DVB-T standard application shown in Figure 27 and 28. This feature is activated by setting bits T[2:0] = 011 after power-on reset. This feature is disabled when the same bits are set again. When ALBC is activated, the output ports BS1, BS2 and BS3 are not programmed by the corresponding BS bits, but are set according to Table 13 and 14. When ALBC is active, bit ALBC = 1. Table 14 summarizes the programming of the band selection and the charge pump current when ALBC is active.

Table 13. ALBC settings

Bit				Band selected	Charge pump current	Port		
ALBC	BS3	BS2	BS1			BS3	BS2	BS1
0	X	0	0	high	see Table 14	follows bit BS3	off	off
0	X	0	1	low	see Table 14	follows bit BS3	off	on
0	X	1	0	mid	see Table 14	follows bit BS3	on	off
0	X	1	1	forbidden				
1	X	X	X	depends on LO program, shown in Table 14				

Table 14. ALBC band selection and charge current setting

LO frequency	Band	Charge pump current number
80 MHz to 92 MHz	low	2
92 MHz to 144 MHz	low	3
144 MHz to 156 MHz	low	4
156 MHz to 176 MHz	low	5
176 MHz to 184 MHz	low	6

Table 14. ALBC band selection and charge current setting*…continued*

LO frequency	Band	Charge pump current number
184 MHz to 196 MHz	low	7
196 MHz to 224 MHz	mid	2
224 MHz to 296 MHz	mid	3
296 MHz to 380 MHz	mid	4
380 MHz to 404 MHz	mid	5
404 MHz to 448 MHz	mid	6
448 MHz to 472 MHz	mid	7
472 MHz to 484 MHz	mid	8
484 MHz to 604 MHz	high	4
604 MHz to 676 MHz	high	5
676 MHz to 752 MHz	high	6
752 MHz to 868 MHz	high	7
868 MHz to 904 MHz	high	8

8.2 Read mode; $R/\overline{W}$ = 1

Data can be read from the device by setting the $R/\overline{W}$ bit to 1 (see Table 15). After the device address has been recognized, the device generates an acknowledge pulse and the first data byte (status byte) is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL clock signal.

A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge). End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.

Table 15. I²C-bus read data format

Name	Byte	Bit								ACK
		MSB[1]							LSB	
Address byte	1	1	1	0	0	0	MA1	MA0	$R/\overline{W}$ = 1	A
Status byte	2	POR	FL	ALBC	1	AGC	A2	A1	A0	-

[1] MSB is transmitted first.

Table 16. Description of read data format bits

Bit	Description
A	acknowledge bit
POR	power-on reset flag
	POR = 0, normal operation
	POR = 1, power-on reset
FL	in-lock flag
	FL = 0, not locked
	FL = 1, the PLL is locked

Table 16. Description of read data format bits *…continued*

Bit	Description
ALBC	automatic loop bandwidth control flag
	ALBC = 0, no automatic loop bandwidth control
	ALBC = 1, automatic loop bandwidth control selected
AGC	internal AGC flag
	AGC = 0 when internal AGC is active ($V_{AGC} < V_{RML}$)
	AGC = 1 when internal AGC is not active ($V_{AGC} > V_{RMH}$)
A2, A1, A0	digital outputs of the 5-level ADC; see Table 17

Table 17. ADC levels

Voltage applied to pin ADC[1]	A2	A1	A0
$0.6V_{CC}$ to V_{CC}	1	0	0
$0.45V_{CC}$ to $0.6V_{CC}$	0	1	1
$0.3V_{CC}$ to $0.45V_{CC}$	0	1	0
$0.15V_{CC}$ to $0.3V_{CC}$	0	0	1
0 V to $0.15V_{CC}$	0	0	0

[1] Accuracy is $\pm0.03V_{CC}$. Bit BS5 must be set to logic 0 to disable the BS5 output port. The BS5 output port uses the same pin as the ADC and can not be used when the ADC is in use.

8.3 Status at power-on reset

At power on or when the supply voltage drops below approximately 2.85 V (at T_{amb} = 25 °C), internal registers are set according to Table 18.

At power on, the charge pump current is set to 580 μA, the test bits T[2:0] are set to 110 which means that the charge pump is sinking current, the tuning voltage output is disabled and the ALBC function is disabled. The XTOUT buffer is on, driving the 4 MHz signal from the crystal oscillator and all the ports are off. As a consequence, the high band is selected by default.

Table 18. Default setting at power-on reset

Name	Byte	Bit[1]							
		MSB							LSB
Address byte	1	1	1	0	0	0	MA1	MA0	X
Divider byte 1 (DB1)	2	0	N14 = X	N13 = X	N12 = X	N11 = X	N10 = X	N9 = X	N8 = X
Divider byte 2 (DB2)	3	N7 = X	N6 = X	N5 = X	N4 = X	N3 = X	N2 = X	N1 = X	N0 = X
Control byte 1 (CB1)	4	1	T/A = X[2]	T2 = 1	T1 = 1	T0 = 0	R2 = X	R1 = X	R0 = X
		1	T/A = X[3]	0	0	ATC = 0	AL2 = 0	AL1 = 1	AL0 = 0
Control byte 2 (CB2)	5	CP2 = 1	CP1 = 1	CP0 = 1	BS5 = 0	BS4 = 0	BS3 = 0	BS2 = 0	BS1 = 0

[1] X means that this bit is not set or reset at power-on reset.

[2] The next six bits are written, when bit T/A = 1 in a write sequence.

[3] The next six bits are written, when bit T/A = 0 in a write sequence.

9. Internal circuitry

Table 19. Internal pin configuration

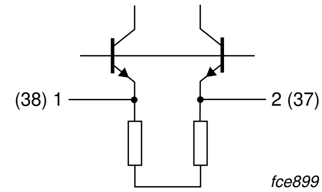
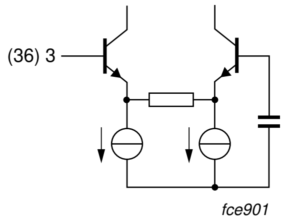
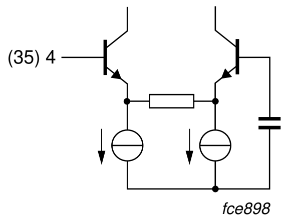
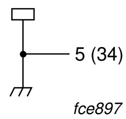
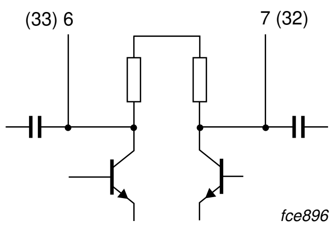
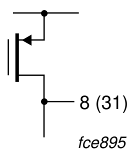
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650TT	TDA6651TT	Low	Mid	High	
HBIN1	1	38	n.a.	n.a	1.0 V	
HBIN2	2	37	n.a.	n.a	1.0 V	
MBIN	3	36	n.a.	1.8 V	n.a.	
LBIN	4	35	1.8 V	n.a.	n.a	
RFGND	5	34	-	-	-	
IFFIL1	6	33	3.7 V	3.7 V	3.7 V	
IFFIL2	7	32	3.7 V	3.7 V	3.7 V	
BS4	8	31	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	

Table 19. Internal pin configuration...*continued*

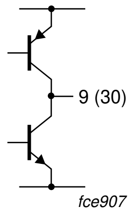
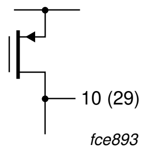
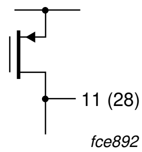
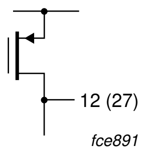
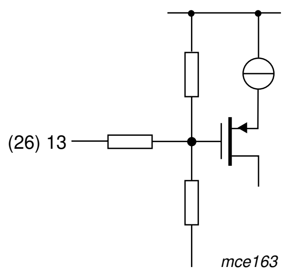
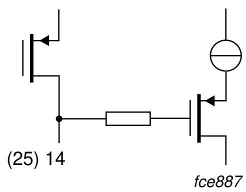
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650TT	TDA6651TT	Low	Mid	High	
AGC	9	30	0 V or 3.5 V	0 V or 3.5 V	0 V or 3.5 V	
BS3	10	29	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	high-Z or $V_{CC} - V_{DS}$	
BS2	11	28	high-Z	$V_{CC} - V_{DS}$	high-Z	
BS1	12	27	$V_{CC} - V_{DS}$	high-Z	high-Z	
BVS	13	26	2.5 V	2.5 V	2.5 V	
ADC/BS5	14	25	V_{CEsat} or high-Z	V_{CEsat} or high-Z	V_{CEsat} or high-Z	

Table 19. Internal pin configuration*...continued*

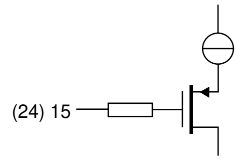
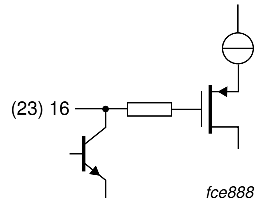
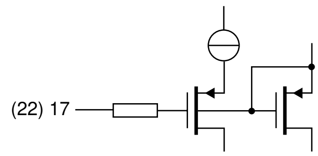
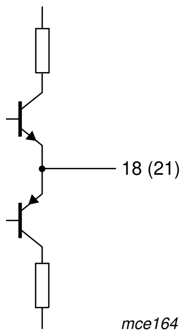
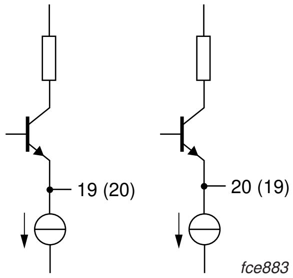
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650TT	TDA6651TT	Low	Mid	High	
SCL	15	24	high-Z	high-Z	high-Z	
SDA	16	23	high-Z	high-Z	high-Z	
AS	17	22	1.25 V	1.25 V	1.25 V	
XTOUT	18	21	3.45 V	3.45 V	3.45 V	
XTAL1	19	20	2.2 V	2.2 V	2.2 V	
XTAL2	20	19	2.2 V	2.2 V	2.2 V	
n.c.	21	18	n.a.			not connected

Table 19. Internal pin configuration *…continued*

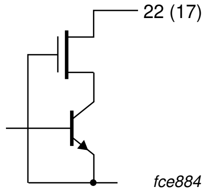
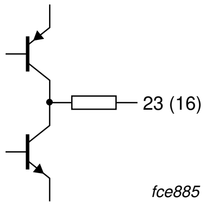
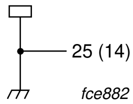
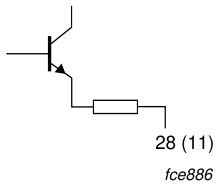
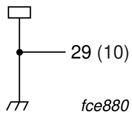
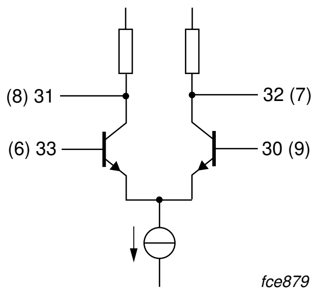
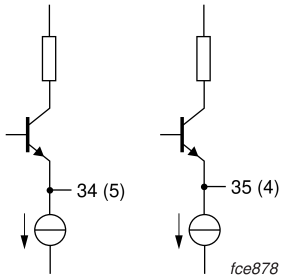
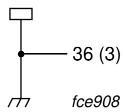
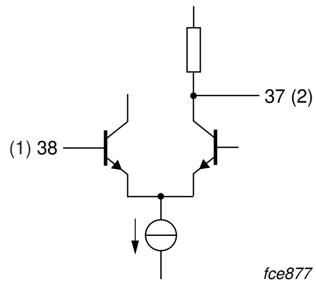
Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650TT	TDA6651TT	Low	Mid	High	
VT	22	17	V_{VT}	V_{VT}	V_{VT}	
CP	23	16	1.8 V	1.8 V	1.8 V	
V_{CCD}	24	15	5 V	5 V	5 V	
PLLGND	25	14	-	-	-	
V_{CCA}	26	13	5 V	5 V	5 V	
IFOUTB	27	12	2.1 V	2.1 V	2.1 V	
IFOUTA	28	11	2.1 V	2.1 V	2.1 V	
IFGND	29	10	-	-	-	
HOSCIN1	30	9	2.2 V	2.2 V	1.8 V	
HOSCOUT1	31	8	5 V	5 V	2.5 V	
HOSCOUT2	32	7	5 V	5 V	2.5 V	
HOSCIN2	33	6	2.2 V	2.2 V	1.8 V	

Table 19. Internal pin configuration *...continued*

Symbol	Pin		Average DC voltage versus band selection			Description[1]
	TDA6650TT	TDA6651TT	Low	Mid	High	
MOSCIN1	34	5	2.3 V	1.3 V	2.3 V	
MOSCIN2	35	4	2.3 V	1.3 V	2.3 V	
OSCGND	36	3	-	-	-	
LOSCOUT	37	2	1.7 V	1.4 V	1.4 V	
LOSCIN	38	1	2.9 V	3.5 V	3.5 V	

[1] The pin numbers in parenthesis refer to the TDA6651TT.

10. Limiting values

Table 20. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Positive currents are entering the IC and negative currents are going out of the IC; all voltages are referenced to ground [1].

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCA}	analog supply voltage		–0.3	+6	V
V_{CCD}	digital supply voltage		–0.3	+6	V
V_{VT}	tuning voltage output		–0.3	+35	V
V_{SDA}	serial data input and output voltage		–0.3	+6	V
I_{SDA}	serial data output current	during acknowledge	0	10	mA
V_{SCL}	serial clock input voltage		–0.3	+6	V
V_{AS}	address selection input voltage		–0.3	+6	V

Table 20. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Positive currents are entering the IC and negative currents are going out of the IC; all voltages are referenced to ground [1].

Symbol	Parameter	Conditions		Min	Max	Unit
V_n	voltage on all other inputs, outputs and combined inputs and outputs, except grounds	4.5 V < V_{CC} < 5.5 V		−0.3	V_{CC} + 0.3	V
I_{BSn}	PMOS port output current	corresponding port on; open-drain		−20	0	mA
$I_{BS(tot)}$	sum of all PMOS port output currents	open-drain		−50	0	mA
$t_{sc(max)}$	maximum short-circuit time	each pin to V_{CC} or to ground		-	10	s
T_{stg}	storage temperature			−40	+150	°C
T_{amb}	ambient temperature		[2]	−20	$T_{amb(max)}$	°C
T_j	junction temperature			-	150	°C

[1] Maximum ratings cannot be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings cannot be accumulated.

[2] The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the printed-circuit board. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. An estimation of the junction temperature can be obtained through measurement of the temperature of the top center of the package ($T_{package}$). The temperature difference junction to case (ΔT_{j-c}) is estimated at about 13 °C on the demo board (PCB 827-3). The junction temperature: $T_j = T_{package} + \Delta T_{j-c}$.

11. Thermal characteristics

Table 21. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1][2][3]		
	TDA6650TT			82	K/W
	TDA6651TT			74	K/W

[1] Measured in free air as defined by JEDEC standard JESD51-2.

[2] These values are given for information only. The thermal resistance depends strongly on the nature and design of the printed-circuit board used in the application.The thermal resistance given corresponds to the value that can be measured on a multilayer printed-circuit board (4 layers) as defined by JEDEC standard.

[3] The junction temperature influences strongly the reliability of an IC. The printed-circuit board used in the application contributes in a large part to the overall thermal characteristic. It must therefore be insured that the junction temperature of the IC never exceeds $T_{j(max)}$ = 150 °C at the maximum ambient temperature.

12. Characteristics

Table 22. Characteristics

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage			4.5	5.0	5.5	V
I_{CC}	supply current	PMOS ports off		80	96	115	mA
		one PMOS port on: sourcing 15 mA		96	112	131	mA
		two PMOS ports on: one port sourcing 15 mA and one other port sourcing 5 mA		101	117	136	mA
General functions							
V_{POR}	power-on reset supply voltage	power-on reset active if $V_{CC} < V_{POR}$		-	2.85	3.5	V
Δf_{lock}	frequency range the PLL is able to synthesize			64	-	1024	MHz
Crystal oscillator[1]							
f_{xtal}	crystal frequency			-	4.0	-	MHz
$\lvert Z_{xtal} \rvert$	input impedance (absolute value)	f_{xtal} = 4 MHz; V_{CC} = 4.5 V to 5.5 V; T_{amb} = −20 °C to + $T_{amb(max)}$, see Section 10		350	430	-	Ω
P_{xtal}	crystal drive level	f_{xtal} = 4 MHz	[2]	-	70	-	µW
PMOS ports: pins BS1, BS2, BS3, BS4 and BS5							
$I_{LO(off)}$	output leakage current in off state	V_{CC} = 5.5 V; V_{BS} = 0 V		−10	-	-	µA
$V_{DS(sat)}$	output saturation voltage	only corresponding buffer is on, sourcing 15 mA; $V_{DS(sat)} = V_{CC} - V_{BS}$		-	0.2	0.4	V
ADC input: pin ADC							
V_i	ADC input voltage	see Table 17		0	-	5.5	V
I_{IH}	HIGH-level input current	$V_{ADC} = V_{CC}$		-	-	10	µA
I_{IL}	LOW-level input current	V_{ADC} = 0 V		−10	-	-	µA
Address selection input: pin AS							
I_{IH}	HIGH-level input current	V_{AS} = 5.5 V		-	-	10	µA
I_{IL}	LOW-level input current	V_{AS} = 0 V		−10	-	-	µA
Bus voltage selection input: pin BVS							
I_{IH}	HIGH-level input current	V_{BVS} = 5.5 V		-	-	100	µA
I_{IL}	LOW-level input current	V_{BVS} = 0 V		−100	-	-	µA
Buffered output: pin XTOUT							
$V_{o(p-p)}$	square wave AC output voltage (peak-to peak value)		[3]	-	400	-	mV
Z_o	output impedance			-	175	-	Ω

Table 22. Characteristics…*continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I^2C-bus							
Inputs: pins SCL and SDA							
f_{clk}	clock frequency	frequency on SCL		-	-	400	kHz
V_{IL}	LOW-level input voltage	V_{BVS} = 0 V		0	-	0.75	V
		V_{BVS} = 2.5 V or open-circuit		0	-	1.0	V
		V_{BVS} = 5 V		0	-	1.5	V
V_{IH}	HIGH-level input voltage	V_{BVS} = 0 V		1.75	-	5.5	V
		V_{BVS} = 2.5 V or open-circuit		2.3	-	5.5	V
		V_{BVS} = 5 V		3.0	-	5.5	V
I_{IH}	HIGH-level input current	V_{CC} = 0 V; V_{BUS} = 5.5 V		-	-	10	µA
		V_{CC} = 5.5 V; V_{BUS} = 5.5 V		-	-	10	µA
I_{IL}	LOW-level input current	V_{CC} = 0 V; V_{BUS} = 1.5 V		-	-	10	µA
		V_{CC} = 5.5 V; V_{BUS} = 0 V		–10	-	-	µA
Output: pin SDA							
I_{LH}	leakage current	V_{SDA} = 5.5 V		-	-	10	µA
$V_{O(ack)}$	output voltage during acknowledge	I_{SDA} = 3 mA		-	-	0.4	V
Charge pump output: pin CP							
$\|I_o\|$	output current (absolute value)	see Table 12		-	-	-	µA
$I_{L(off)}$	off-state leakage current	charge pump off (T[2:0] = 010)		–15	0	+15	nA
Tuning voltage output: pin VT							
$I_{L(off)}$	leakage current when switched-off	tuning supply voltage = 33 V		-	-	10	µA
$V_{o(cl)}$	output voltage when the loop is closed	tuning supply voltage = 33 V; R_L = 15 kΩ		0.3	-	32.7	V
Noise performance							
$J_{\phi(rms)}$	phase jitter (RMS value)	integrated between 1 kHz and 1 MHz offset from the carrier					
		digital only application: TDA6650TT/C3/S2; TDA6651TT/C3/S2; TDA6651TT/C3/S3		-	0.5	-	deg
		hybrid application: TDA6650TT/C3; TDA6651TT/C3		-	0.6	-	deg
Low band mixer, including IF amplifier							
f_{RF}	RF frequency	picture carrier for digital only application: TDA6650TT/C3/S2; TDA6651TT/C3/S2; TDA6651TT/C3/S3	[4]	47.00	-	160.00	MHz
		picture carrier for hybrid application: TDA6650TT/C3; TDA6651TT/C3	[4]	43.25	-	157.25	MHz

Table 22. Characteristics*…continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_v	voltage gain	asymmetrical IF output; R_L = 75 Ω; see Figure 14					
		f_{RF} = 44.25 MHz		21	24	27	dB
		f_{RF} = 157.25 MHz		21	24	27	dB
		symmetrical IF output; R_L = 1.25 kΩ; see Figure 15					
		f_{RF} = 44.25 MHz		25	28	31	dB
		f_{RF} = 157.25 MHz		25	28	31	dB
NF	noise figure	see Figure 16 and 17					
		f_{RF} = 50 MHz		-	8.0	10.0	dB
		f_{RF} = 150 MHz		-	8.0	10.0	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 18	[5]				
		f_{RF} = 44.25 MHz		107	110	-	dBμV
		f_{RF} = 157.25 MHz		107	110	-	dBμV
		symmetrical application; see Figure 19	[5]				
		f_{RF} = 44.25 MHz		117	120	-	dBμV
		f_{RF} = 157.25 MHz		117	120	-	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	90	-	dBμV
INT_{SO2}	channel SO2 beat	hybrid application: TDA6650TT/C3; TDA6651TT/C3; V_{RFpix} = 80 dBμV	[6]	57	60	-	dBc
$V_{i(lock)}$	input level without lock-out	see Figure 25	[7]	-	-	120	dBμV
G_i	input conductance	f_{RF} = 44.25 MHz; see Figure 5		-	0.13	-	mS
		f_{RF} = 157.25 MHz; see Figure 5		-	0.11	-	mS
C_i	input capacitance	f_{RF} = 44.25 MHz to 157.25 MHz; see Figure 5		-	1.36	-	pF
Mid band mixer, including IF amplifier							
f_{RF}	RF frequency	picture carrier for digital only application: TDA6650TT/C3/S2; TDA6651TT/C3/S2; TDA6651TT/C3/S3	[4]	160.00	-	446.00	MHz
		picture carrier for hybrid application: TDA6650TT/C3; TDA6651TT/C3	[4]	157.25	-	443.25	MHz

Table 22. Characteristics...*continued*

$V_{CCA} = V_{CCD} = 5$ V; $T_{amb} = 25$ °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Figure 14					
		f_{RF} = 157.25 MHz		21	24	27	dB
		f_{RF} = 443.25 MHz		21	24	27	dB
		symmetrical IF output; load = 1.25 kΩ; see Figure 15					
		f_{RF} = 157.25 MHz		25	28	31	dB
		f_{RF} = 443.25 MHz		25	28	31	dB
NF	noise figure	see Figure 16 and 17					
		f_{RF} = 150 MHz		-	8.0	10.0	dB
		f_{RF} = 300 MHz		-	9.0	11.0	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 18	[5]				
		f_{RF} = 157.25 MHz		107	110	-	dBμV
		f_{RF} = 443.25 MHz		107	110	-	dBμV
		symmetrical application; see Figure 19	[5]				
		f_{RF} = 157.25 MHz		117	120	-	dBμV
		f_{RF} = 443.25 MHz		117	120	-	dBμV
$V_{f(N+5)-1}$	(N + 5) – 1 MHz pulling	$f_{RF(wanted)}$ = 443.25 MHz; f_{osc} = 482.15 MHz; $f_{RF(unwanted)}$ = 482.25 MHz	[8]	-	80	-	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	89	-	dBμV
$V_{i(lock)}$	input level without lock-out	see Figure 25	[7]	-	-	120	dBμV
G_i	input conductance	see Figure 6		-	0.3	-	mS
C_i	input capacitance	see Figure 6		-	1.1	-	pF
High band mixer, including IF amplifier							
f_{RF}	RF frequency	picture carrier for digital only application: TDA6650TT/C3/S2; TDA6651TT/C3/S2; TDA6651TT/C3/S3	[4]	446.00	-	866.00	MHz
		picture carrier for hybrid application: TDA6650TT/C3; TDA6651TT/C3	[4]	443.25	-	863.25	MHz
G_v	voltage gain	asymmetrical IF output; load = 75 Ω; see Figure 20					
		f_{RF} = 443.25 MHz		31.5	34.5	37.5	dB
		f_{RF} = 863.25 MHz		31.5	34.5	37.5	dB
		symmetrical IF output; load = 1.25 kΩ; see Figure 21					
		f_{RF} = 443.25 MHz		35.5	38.5	41.5	dB
		f_{RF} = 863.25 MHz		35.5	38.5	41.5	dB

Table 22. Characteristics...*continued*

V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C; values are given for an asymmetrical IF output loaded with a 75 Ω load or with a symmetrical IF output loaded with 1.25 kΩ; positive currents are entering the IC and negative currents are going out of the IC; the performances of the circuits are measured in the measurement circuits Figure 27 and 28 for digital application or in the measurement circuits Figure 29 and 30 for hybrid application; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
NF	noise figure, not corrected for image	see Figure 22					
		f_{RF} = 443.25 MHz		-	6.0	8.0	dB
		f_{RF} = 863.25 MHz		-	7.0	9.0	dB
V_o	output voltage causing 1 % cross modulation in channel	asymmetrical application; see Figure 23	[5]				
		f_{RF} = 443.25 MHz		107	110	-	dBμV
		f_{RF} = 863.25 MHz		107	110	-	dBμV
		symmetrical application; see Figure 24	[5]				
		f_{RF} = 443.25 MHz		117	120	-	dBμV
		f_{RF} = 863.25 MHz		117	120	-	dBμV
$V_{i(lock)}$	input level without lock-out	see Figure 26	[7]	-	-	120	dBμV
$V_{f(N+5)-1}$	(N + 5) – 1 MHz pulling	$f_{RF(wanted)}$ = 815.25 MHz; f_{osc} = 854.15 MHz; $f_{RF(unwanted)}$ = 854.25 MHz	[8]	-	80	-	dBμV
V_i	input voltage causing 750 Hz frequency deviation pulling in channel	asymmetrical IF output		-	79	-	dBμV
Z_i	input impedance (R_S + jL_Sω)	f_{RF} = 443.25 MHz; see Figure 7					
		R_S		-	35	-	Ω
		L_S		-	8	-	nH
		f_{RF} = 863.25 MHz; see Figure 7					
		R_S		-	36	-	Ω
		L_S		-	8	-	nH
Low band oscillator							
f_{osc}	oscillator frequency		[9]	83.15	-	196.15	MHz
$\Delta f_{osc(V)}$	oscillator frequency shift with supply voltage		[10]	-	110	-	kHz
$\Delta f_{osc(T)}$	oscillator frequency drift with temperature	ΔT = 25 °C; V_{CC} = 5 V with compensation	[11]	-	900	-	kHz
$\Phi_{osc(dig)}$	phase noise, carrier to sideband noise in digital application	TDA6650TT/C3/S2; TDA6651TT/C3/S2; TDA6651TT/C3/S3					
		±1 kHz frequency offset; f_{comp} = 4 MHz; see Figure 8, 27 and 28		82	95	-	dBc/Hz
		±10 kHz frequency offset; worst case in the frequency range; see Figure 9, 27 and 28		87	100	-	dBc/Hz
		±100 kHz frequency offset; worst case in the frequency range; see Figure 10, 27 and 28		104	110	-	dBc/Hz
		±1.4 MHz frequency offset; worst case in the frequency range; see Figure 27 and 28		-	117	-	dBc/Hz