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Data Sheet, V 1.0, May 2007

TDA7200

ASK/FSK Single Conversion Receiver

Version 1.0

Wireless Control Components

Never stop thinking.

Edition 2007-05-02

Published by Infineon Technologies AG,
Am Campeon 1-12,
85579 Neubiberg, Germany

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Revision History:	**2007-05-02**	V 1.0
Previous Version:	none	

Page	Subjects (major changes since last revision)

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Table of Contents **Page**

1 Product Description

1.1 Overview

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the frequency band 400 to 440 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, an advanced data comparator (slicer) with selection between two threshold modes and a peak detector. Additionally there is a power down feature to save current and extend battery life, and two selectable alternatives of generating the data slicer threshold.

1.2 Features

- Low supply current (Is = 5.7 mA typ. in FSK mode, Is = 5.0 mA typ. in ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (50nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -106 dBm over specified temperature range (-20 to +70°C)
- FSK sensitivity better than -100 dBm over specified temperature range (-20 to +70°C)
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with selection between two threshold modes (see **Section 2.4.8**)

1.3 Application

- Remote Control Systems
- Alarm Systems
- Low Bitrate Communication Systems

Table 1 Order Information

Type	Ordering Code	Package
TDA7200	SP000296473	PG-TSSOP-28

2 Functional Description

2.1 Pin Configuration

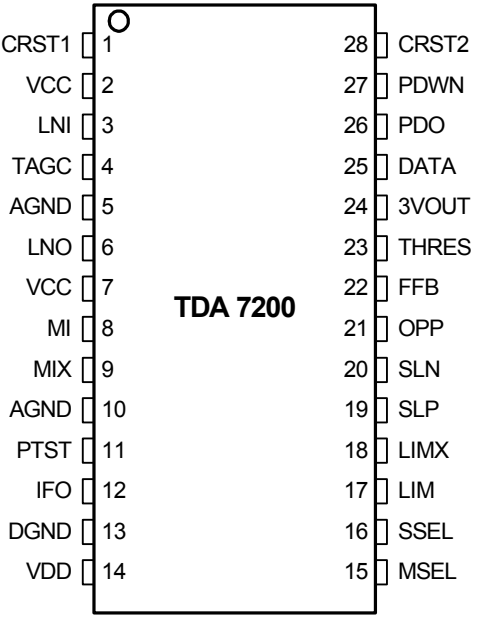
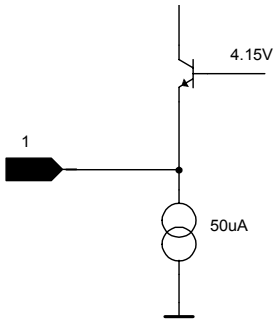
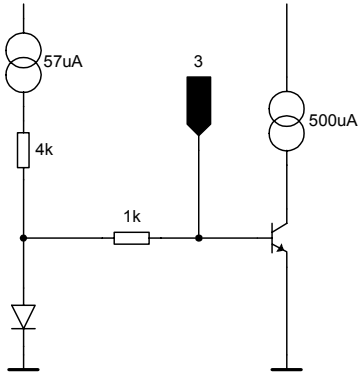
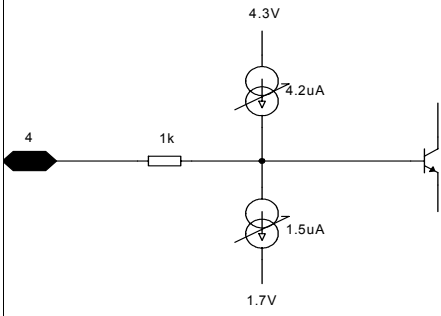
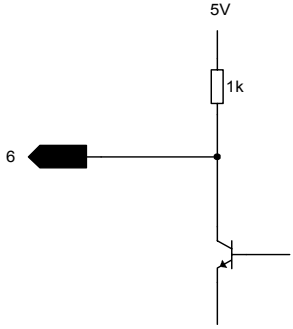


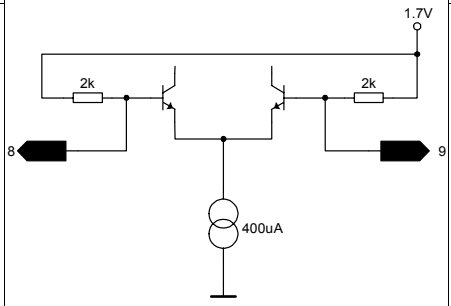
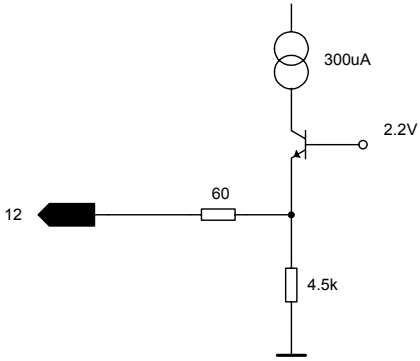
Figure 1 Pin Configuration

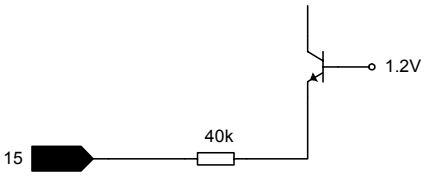
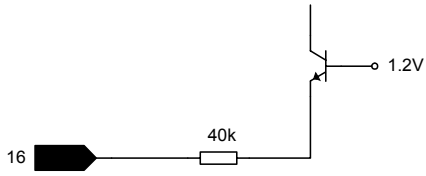
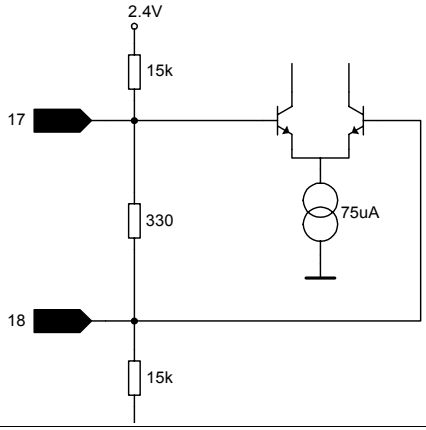
2.2 Pin Definition and Functions

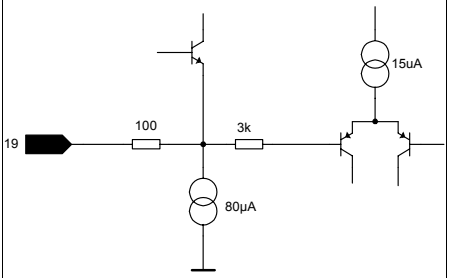
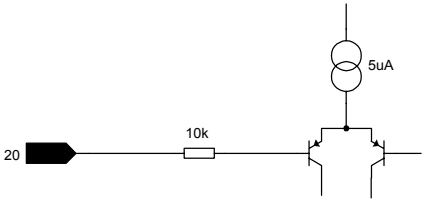
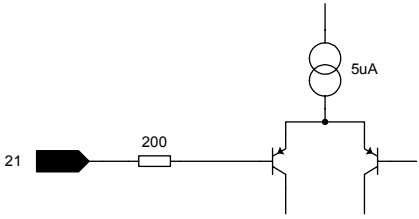
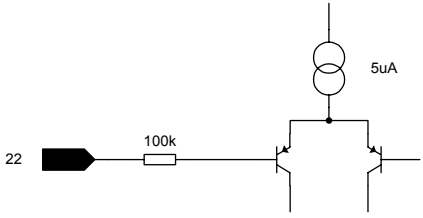
Table 2 Pin Defintion and Function

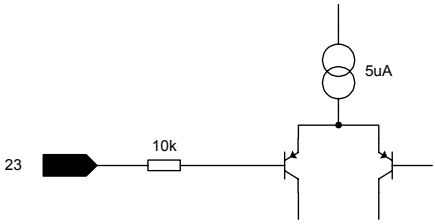
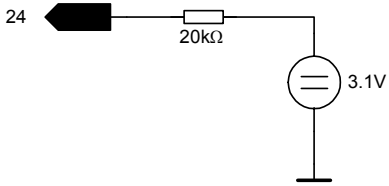
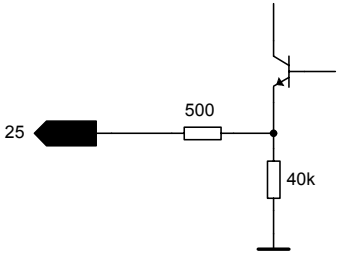
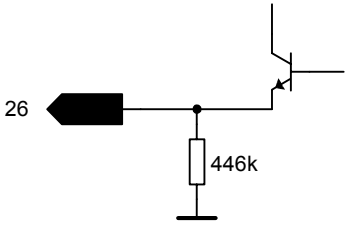
Pin No.	Symbol	Equivalent I/O Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

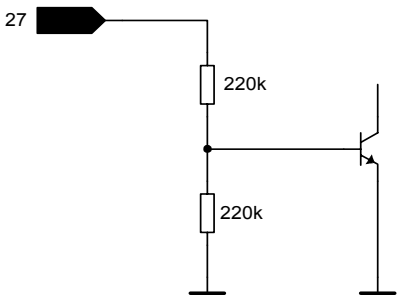
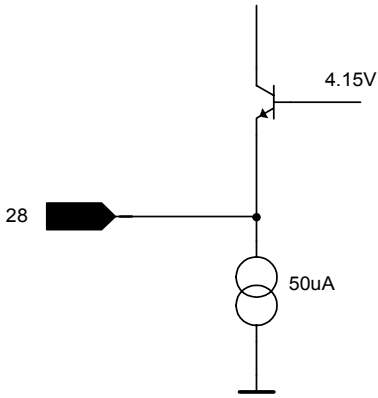
Pin No.	Symbol	Equivalent I/O Schematic	Function
4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply

Pin No.	Symbol	Equivalent I/O Schematic	Function
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	PTST		has to be left open
12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuity)

Pin No.	Symbol	Equivalent I/O Schematic	Function
15	MSEL		ASK/FSK Modulation Format Sector
16	SSEL		Data Slicer Reference Level Sector
17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input

Pin No.	Symbol	Equivalent I/O Schematic	Function
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input
21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin

Pin No.	Symbol	Equivalent I/O Schematic	Function
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output
25	DATA		Data Output
26	PDO		Peak Detector Output

Pin No.	Symbol	Equivalent I/O Schematic	Function
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

2.3 Functional Block Diagram

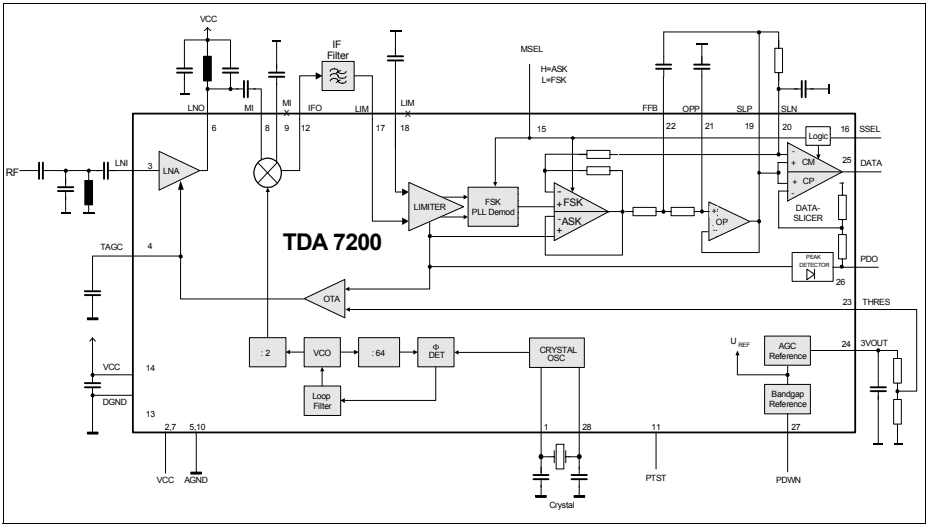


Figure 2 Block Diagram

2.4 Functional Block Description

2.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 3dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in **Section 3.1**. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in **Section 3.1**.

2.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 400-440MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 21dB by utilising either high- or low-side injection of the local oscillator signal. In case the mixer is interfaced only single-ended, the unused mixer input has to be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 20MHz in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

2.4.3 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The frequency range of the VCO guaranteed over production spread and the specified temperature range is 820 to 860MHz. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer. The VCO signal is divided by two before it is fed to the Mixer. Depending on whether high- or low-side injection of the local oscillator is used, the receiving frequency range is 400 to 420MHz and 420 to 440MHz - see also **Section 3.4**.

2.4.4 Crystal Oscillator

The calculation of the value of the necessary crystal load capacitance is shown in **Section 3.3**, the crystal frequency calculation is explained in **Section 3.4**.

2.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80 dB that has a bandpass-characteristic centred around 10.7 MHz. It has a typical input impedance of 330 Ω to allow for easy interfacing to a 10.7 MHz ceramic IF filter. The limiter circuit also acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in **Figure 4**. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry. The RSSI output is applied to the modulation format switch, to the Peak Detector input and to the AGC circuitry.

In order to demodulate ASK signals the MSEL pin has to be in its ‘High‘-state as described in the next chapter.

2.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7 MHz center frequency VCO. The demodulator gain is typically 200µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch described in more detail below. This signal is representing the demodulated signal with low frequencies applied to the demodulator demodulated to logic zero and high frequencies demodulated to logic ones. However this is only valid in case the local oscillator is low-side injected to the mixer which is applicable to receive frequencies above 420MHz. In case of receive frequencies below 420MHz high frequencies are demodulated as logical zeroes due to a sign inversion in the downconversion mixing process as the L0 is high-side injected to the mixer. See also **Section 3.4**.

The modulation format switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL** pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits. The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in **Section 3.6**.

Table 3 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The demodulator circuit is switched off in case of reception of ASK signals.

2.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in **Section 3.2**.

2.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of up to 100kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for subsequent circuits. A self-adjusting slicer-threshold on pin 20 its generated by a RC-term. In ASK-mode alternatively a scaled value of the voltage at the PDO-output (approx. 87%) can be used as the slicer-threshold as shown in **Table 4**. The data slicer threshold generation alternatives are described in more detail in **Section 3.5**.

Table 4 SSEL Pin Operating States

SSEL	MSEL	Selected Slicing Level (SL)
X	Low	external SL on Pin 20 (RC-term, e.g.)
High	High	external SL on Pin 20 (RC-term, e.g.)
Low	High	87% of PDO-output (approx.)

2.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. A capacitor is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

2.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the PWDN pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 50nA.

Table 5 PDWN Pin Operating States

PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

3 Applications

3.1 Application Circuit

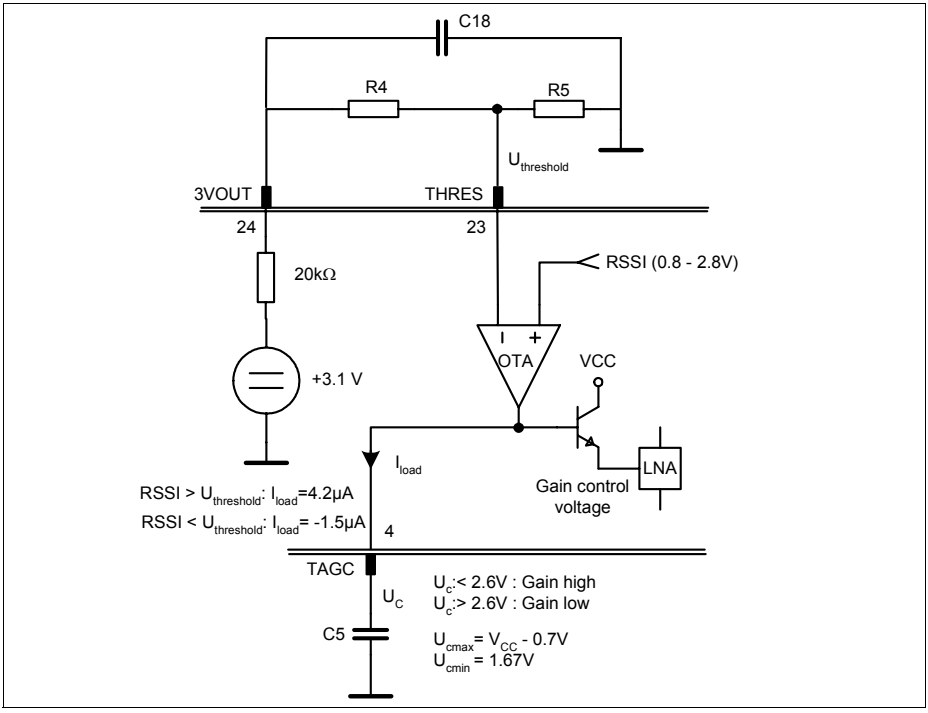


Figure 3 LNA Automatic Gain Control Circuity

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin
(Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the

AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

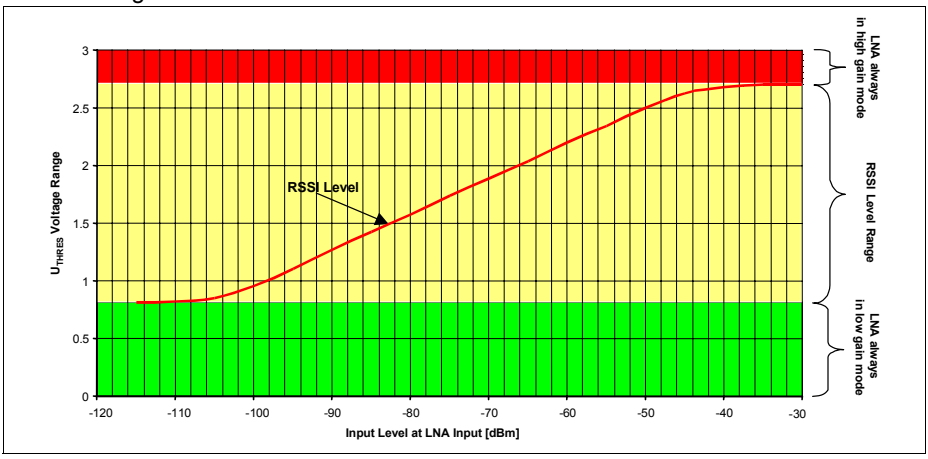


Figure 4 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1)] and a threshold voltage of 1.8V

Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation **THRES** has to be connected to GND.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1) note the 20kΩ resistor in series with the 3.1V internal voltage source

3.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1)].

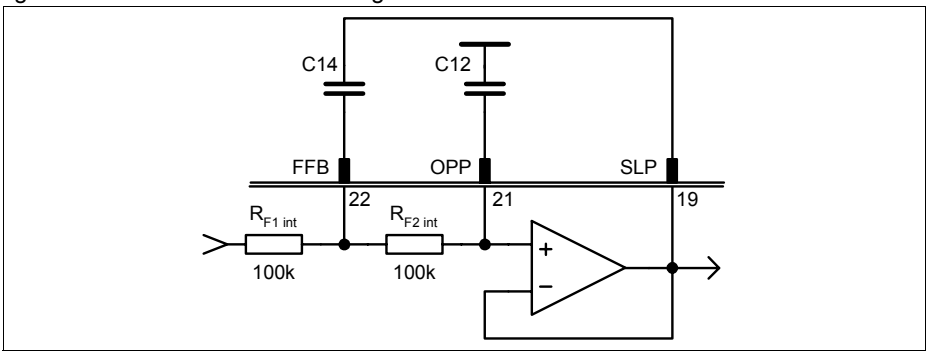


Figure 5 Data Filter Design

with $R_{F1int}=R_{F2int}=R$

$$C14=\frac{2Q\sqrt{b}}{R2\pi f_{3dB}} \quad C12=\frac{\sqrt{b}}{4QR\pi f_{3dB}}$$

with

$$Q=\frac{\sqrt{b}}{a}$$

Q is the qualify factor of the poles where, in case of a Bessel filter a=1.3617, b=0.618 and thus Q=0.577

and in case of a Butter worth filter a=1.414, b=1
and thus Q=0.71

Example: Butter worth filter with f_{3dB}=5kHz and R=100kΩ:
C14=450pF, C12=225pF

1) taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

3.3 Crystal Load Capacitance Calculation

The value of the capacitor necessary to achieve that the crystal oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in **Section 4.1.3** and by the crystal specifications given by the crystal manufacturer.

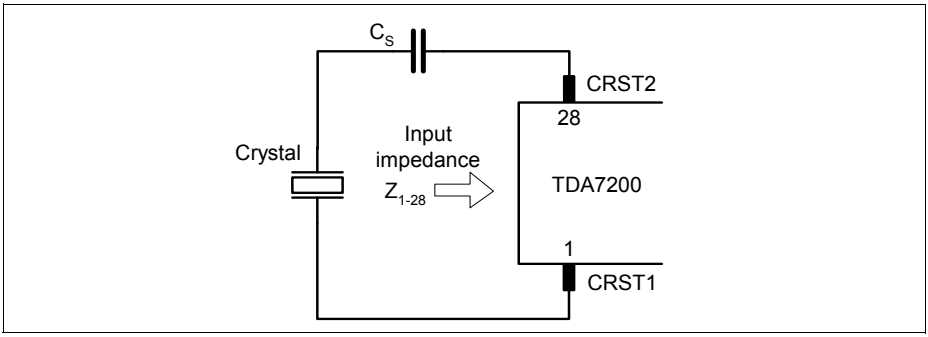


Figure 6 Determination of Series Capacitance Vale for the Quartz Oscillator

The required series capacitor for a crystal with specified load capacitance C_L can be calculated as

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L}$$

C_L is the nominal load capacitance specified by the crystal manufacturer.

Example:

13.4 MHz: C_L = 12 pF X_L=1010 Ω C_S = 5.9 pF

This value may be obtained by putting two capacitors in series to the crystal, such as 22pF and 8.2pF for 13.4MHz.

But please note that the calculated C_S-value includes all parasitic.

3.4 Crystal Frequency Calculation

As described in **Section 2.4.3** the operating range of the on-chip VCO is wide enough to guarantee a receive frequency range between 400 and 440MHz. The VCO signal is divided by 2 before applied to the mixer. This local oscillator signal can be used to downconvert the RF signals both with high- or low-side injection at the mixer. High-side

injection of the local oscillator has to be used for receive frequencies between 400 and 420MHz. In this case the local oscillator frequency is calculated by adding the IF frequency (10.7 MHz) to the RF frequency. Thus the higher frequency of a FSK-modulated signal is demodulated as a logical zero (low).

Low-side injection has to be used for receive frequencies above 420 MHz. The local oscillator frequency is calculated by subtracting the IF frequency (10.7 MHz) from the RF frequency then. In this case no sign-inversion occurs and the higher frequency of a FSK-modulated signal is demodulated as a logical one (high). The overall division ratio in the PLL is 32.

Therefore the crystal frequency may be calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{32}$$

with f_{RF} receive frequency

f_{LO} local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)

f_{QU} quartz crystal oscillator frequency

32 ratio of local oscillator (PLL) frequency and crystal frequency.

This yields the following example:

$$f_{QU} = \frac{434.2MHz - 10.7MHz}{32} = 13.234375\ MHz$$

3.5 Data Slicer Threshold Generation

The threshold of the data slicer can be generated using an external R-C integrator as shown in **Figure 7**.

The time constant T_A of this circuit including also the internal resistors R_{F3int} and R_{F4int} (see **Figure 9**) has to be significantly larger than the longest period of no signal change T_L within the data sequence.

In order to keep distortion low, the minimum value for R is 20kΩ.

T_A has to be calculated as

$$T_A = \frac{R1 \cdot (R_{F3\text{int}} + R_{F4\text{int}})}{R1 + R_{F3\text{int}} + R_{F4\text{int}}} \cdot C13 \quad = R1 II (R_{F3\text{int}} + R_{F4\text{int}}) \cdot C13 \qquad ...for\ ASK$$

and

$$T_A = \frac{R1 \cdot R_{F4\text{int}}}{R1 + R_{F3\text{int}} + R_{F4\text{int}}} \cdot C13 \quad = \frac{R1 II (R_{F3\text{int}} + R_{F4\text{int}})}{v} \cdot C13 \qquad ...for\ FSK$$

R1, $R_{F3\ int}$, $R_{F4\ int}$ and C13 see also **Figure 7** and **Figure 9**

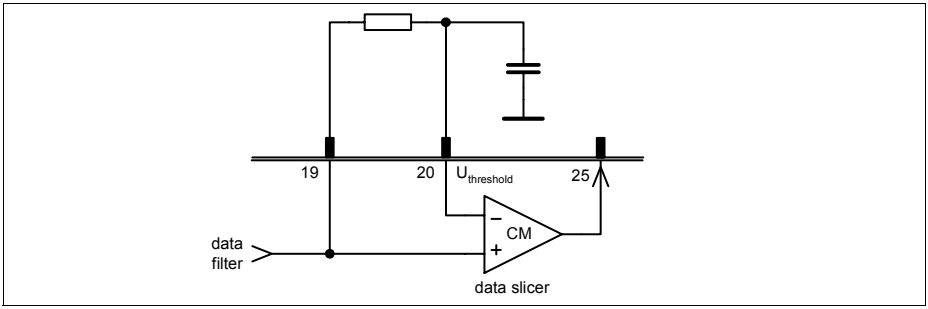


Figure 7 Data Slicer Threshold Generation with External R-C Integrator

In case of ASK operation another possibility for threshold generation is to use the peak detector in connection with an internal resistive divider and one capacitor as shown in **Figure 8**. For selecting the peak detector as reference for the slicing level a logic low as to be applied on the SSEL pin.

In case of MSEL is high (or open), which means that ASK-Mode is selected, a logic low on the SSEL pin yields a logic high on the AND-output and thus the peak-detector is selected (see **Figure 9**).

In case of FSK the MSEL-pin and furthermore the one input of the AND-gate is low, so the peak detector can not be selected.

The capacitor value is depending on the coding scheme and the protocol used.

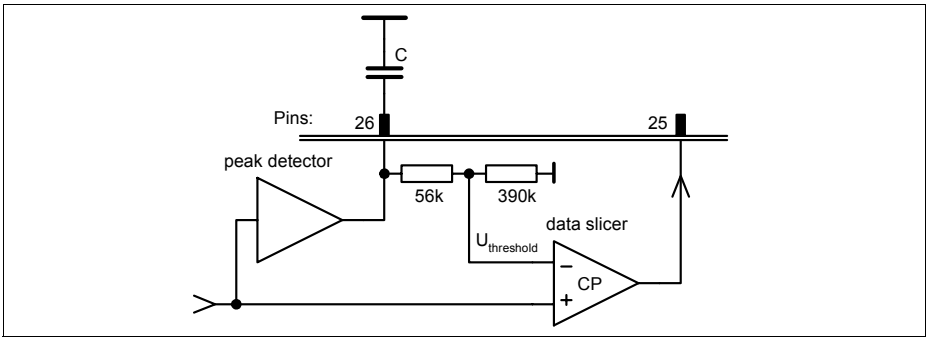


Figure 8 Data Slicer Threshold Generation Utilising the Peak Detector

3.6 ASK/FSK-Data Path Functional Description

The TDA7200 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier.

In ASK-mode alternatively to the voltage at Pin 20 (SLN) a value of approx. 87% of the peak-detector output-voltage at Pin 26 (PDO) can be used as the slicer-reference level.

The slicing reference level is generated by an internal voltage divider (R_{T1int}, R_{T2int}), which is applied on the peak detector output.

The selection between these modes is controlled by Pin 16 (SSEL), as described in **Section 3.5**.

This is shown in **Figure 9**.