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TDA7255V

ASK/FSK 434 MHz Wireless Transceiver

Data Sheet

Revision 1.1, 2010-11-10

Wireless Sense & Control

Edition 2010-11-10

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2010-11-10	
	Just minor changes

Table of Contents

1 Product Description

1.1 Overview

The TDA7255V is an ASK/FSK single-channel transceiver for 433 - 435 MHz frequency band in a tiny VQFN-40 package. Due to the very high level of integration the device requires only a few external components. The extreme low current consumption in receive, transmit and especially in power down mode and the wide supply voltage range make TDA7255V the ideal choice for small, battery driven applications.

The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, a FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative data peak detector, a highly efficient power amplifier and a complex digital timing and control unit with I^2C/3-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip.

The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

1.2 Features

- FSK and ASK modulation and demodulation capability without external circuitry changes, FM demodulation capability
- Frequency range: 433 to 435 MHz
- Sensitivity FSK typically -115 dBm at 4 kbit/s data rate
- Sensitivity ASK typically -112 dBm at 4 kbit/s data rate
- Transmit power up to +13 dBm
- Low supply current (I_s = 9 mA typ. in receive mode, I_s = 13,5 mA typ. in transmit mode (both at 3 V supply voltage, 25°C)
- Very low supply current in power down mode (5 nA typ.)
- Supply voltage range: 2.1 V to 5.5 V
- Data rates up to 100 kbit/s Manchester encoded
- Fully integrated PLL synthesizer including VCO and loop filter on-chip with on-chip crystal oscillator tuning
- Differential receive signal path completely on-chip, therefore no external filters are necessary
- On-chip low pass channel select and data filter with tuneable bandwidth
- Data slicer with self-adjusting threshold and 2 peak detectors
- Self-polling logic with adjustable duty cycle and ultrafast data rate detection and timer mode providing periodical interrupt
- Adjustable LNA gain
- Digital RSSI and battery voltage readout
- Clock Out Pin for external microcontroller
- I^2C/3-wire microcontroller interface, working at max. 400 kbit/s
- Operating temperature range -40°C to +85°C
- 5.5 x 6.5 mm small VQFN-40 package

1.3 Application

The TDA7255V is targeted specifically at highly size-sensitive industrial and consumer applications such as small home automation or security and alarm systems.

Main applications:

- Bi-directional remote control systems
- Home automation systems
- Lighting control
- Security and alarm systems
- Industrial control
- Remote keyless entry systems
- Low bit-rate communication systems

1.4 Ordering Information

Type	Ordering Code	Package
TDA7255V	SP000698114	PG-VQFN-40-8

1.5 Package Outlines

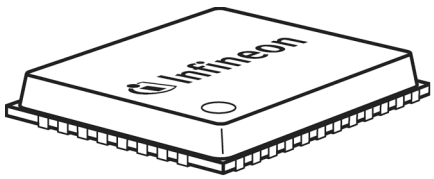


Figure 1 Package PG-VQFN-40-8

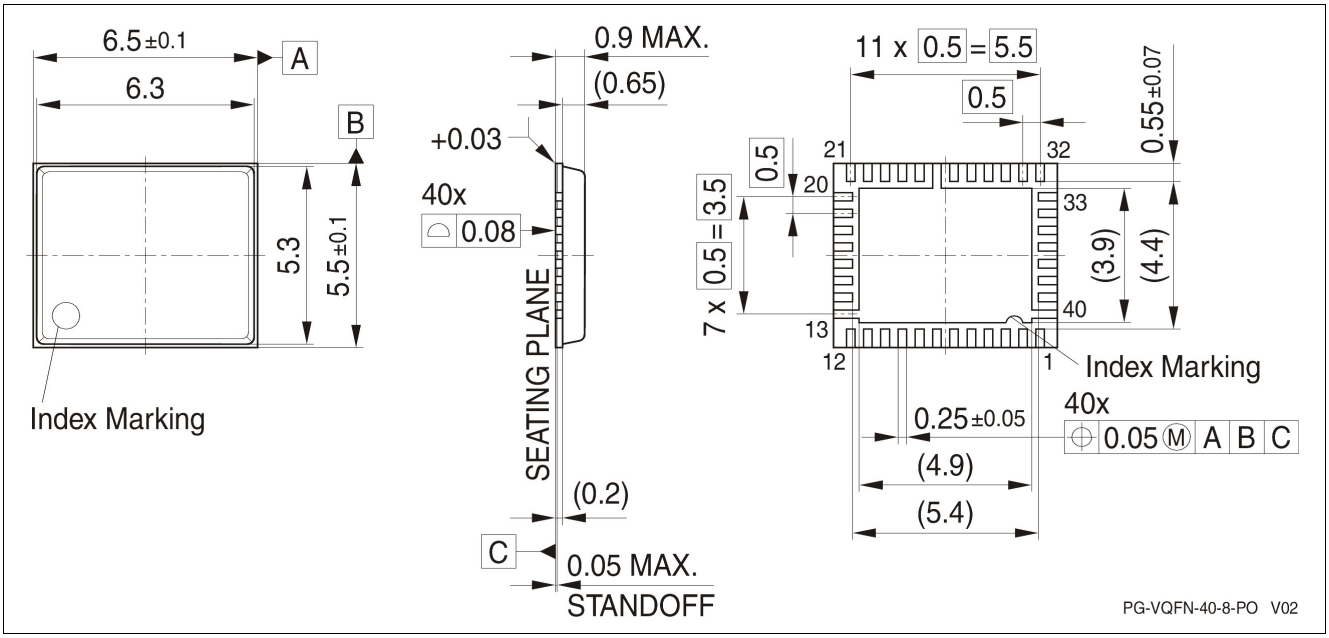


Figure 2 PG-VQFN-40-8 Package Outlines

2 Functional Description

2.1 Pin Configuration

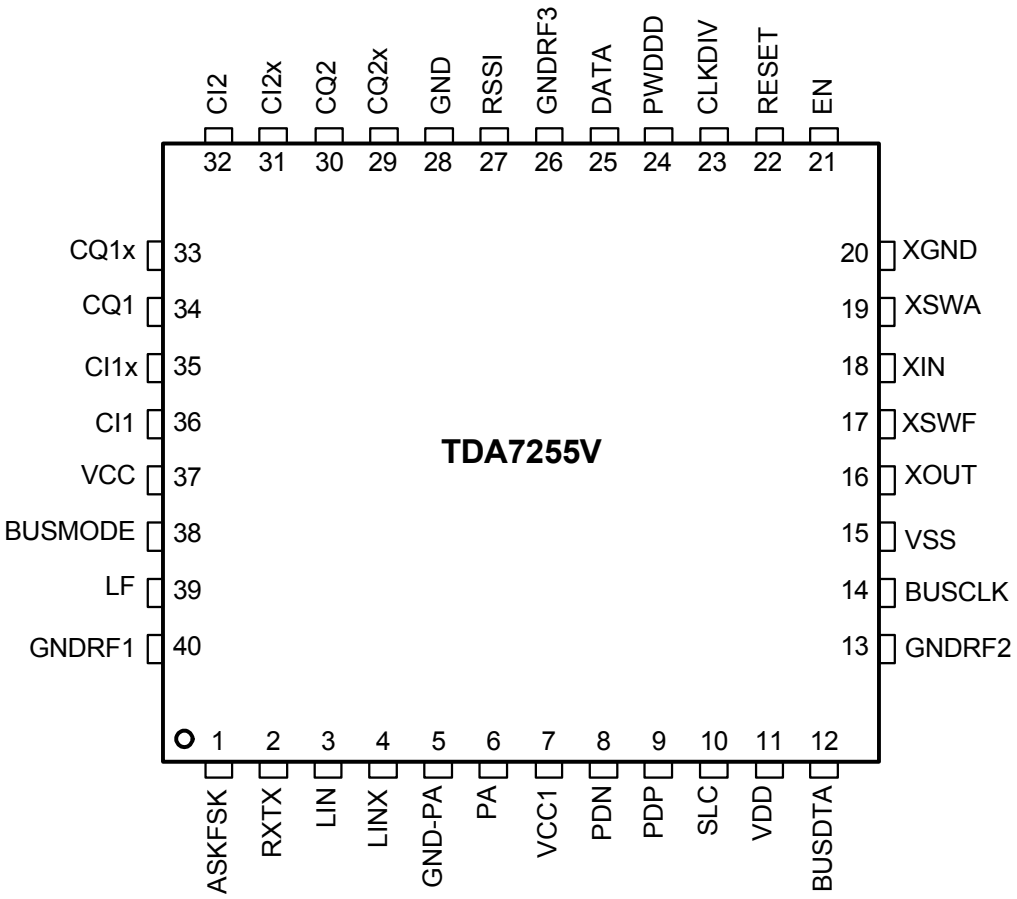


Figure 3 Pin Configuration TDA7255V

2.2 Pin Definitions and Functions

Table 1 Pin Definition and Function

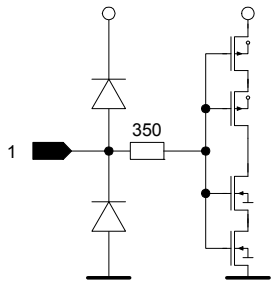
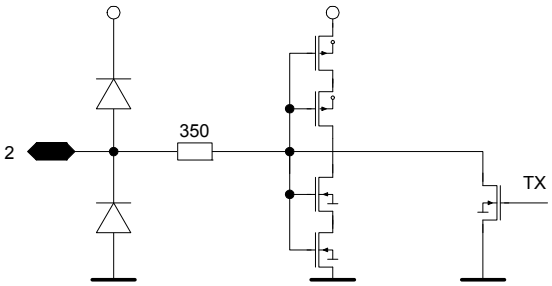
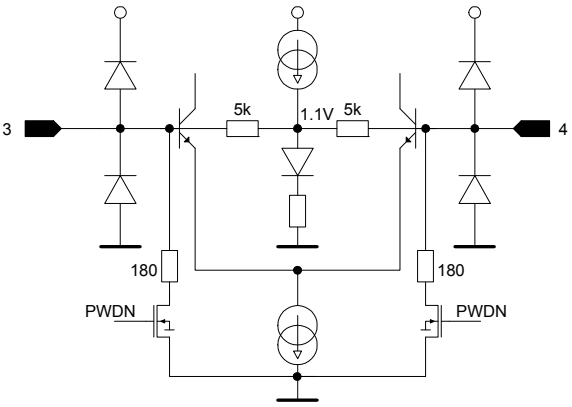
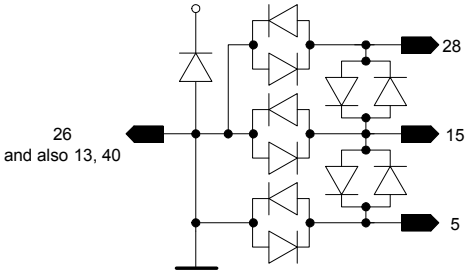
Ball No.	Name	Pin Type	Buffer Type	Function
1	ASKFSK			ASK/FSK-Mode Switch Input High = ASK Low = FSK
2	RXTX			RX/TX-Mode Switch Input/Output High = RX Low = TX
3	LNI			RF Input to Differential Low Noise Amplifier (LNA)
4	LNIX		See Pin 3	Complementary RF Input to Differential LNA
5	GND-PA			Ground Return for Power Amplifier (PA) Driver Stage

Table 1 Pin Definition and Function (cont'd)

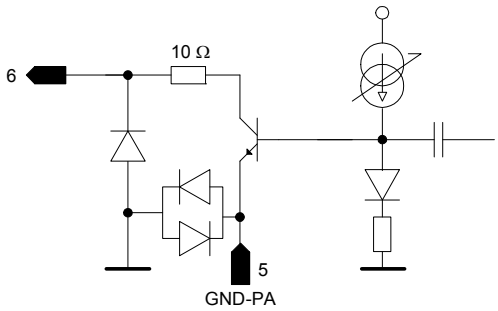
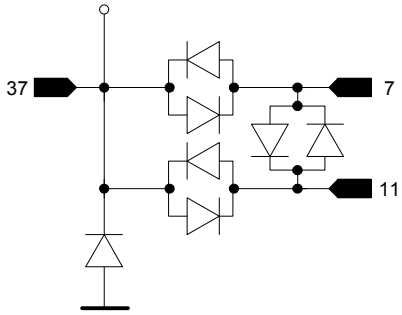
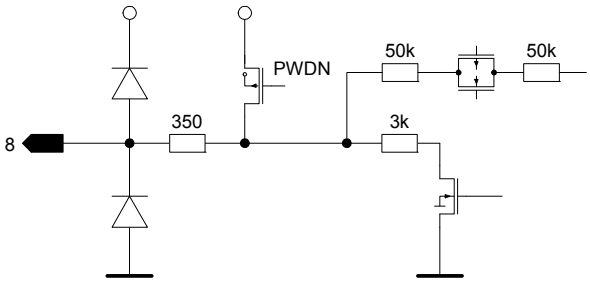
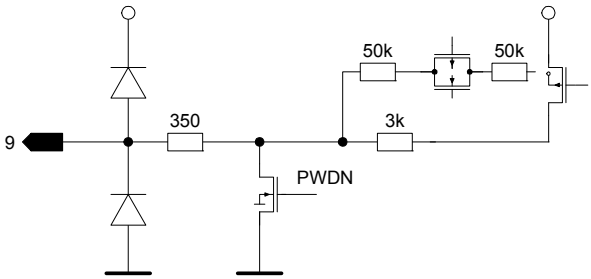
Ball No.	Name	Pin Type	Buffer Type	Function
6	PA			PA Output Stage
7	VCC1			Supply for LNA and PA
8	PDN			Output of the Negative Peak Detector
9	PDP			Output of the Positive Peak Detector

Table 1 Pin Definition and Function (cont'd)

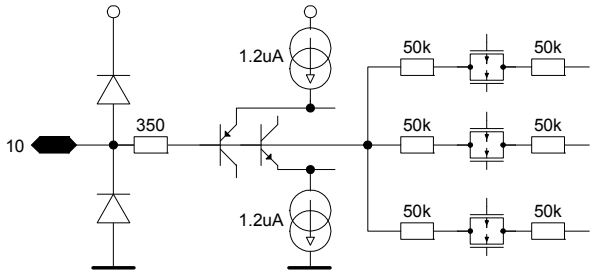
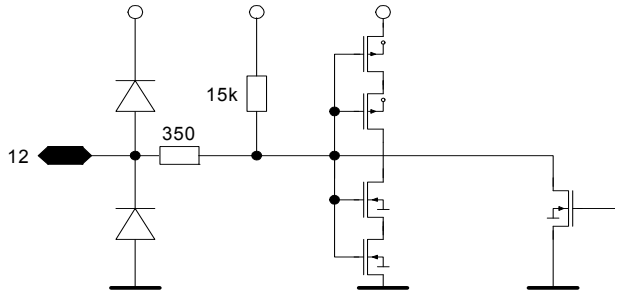
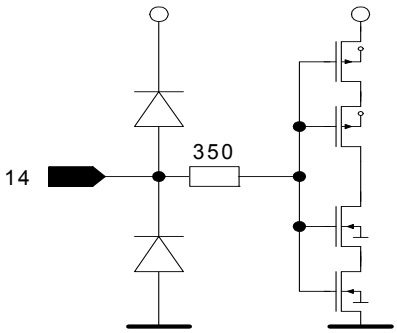
Ball No.	Name	Pin Type	Buffer Type	Function
10	SLC			Slicer Level for the Data Slicer
11	VDD		See Pin 7	Digital Supply A 10 Ω serial resistor in the VDD supply line is strongly recommended; see also **Chapter 4.4**
12	BUSDTA			Bus Data In/Output
13	GNDRF2		See Pin 5	Ground Return for RF Except PA
14	BUSCLK			Bus Clock Input
15	VSS		See Pin 5	Ground for Digital Section

Table 1 Pin Definition and Function (cont'd)

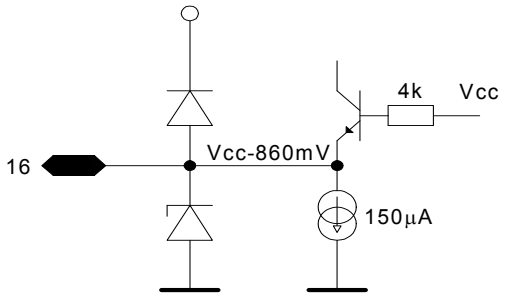
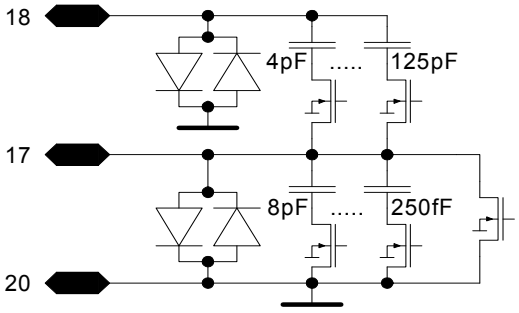
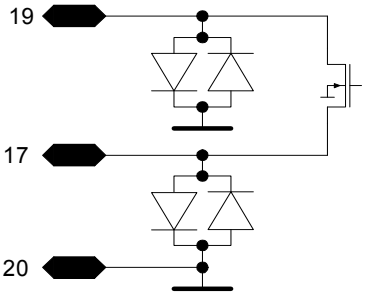
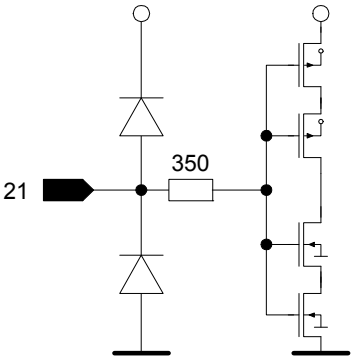
Ball No.	Name	Pin Type	Buffer Type	Function
16	XOUT			Crystal Oscillator Output Can also be used as external reference frequency input
17	XSWF			FSK Modulation Switch
18	XIN		See Pin 17	Ground for Digital Section
19	XSWA			ASK Modulation/FSK Center Frequency Switch
20	XGND		See Pin 19	Crystal Oscillator Ground Return
21	EN			3-Wire Bus Enable Input, Active Low

Table 1 Pin Definition and Function (cont'd)

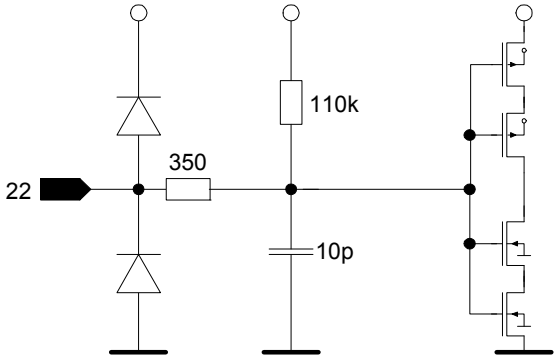
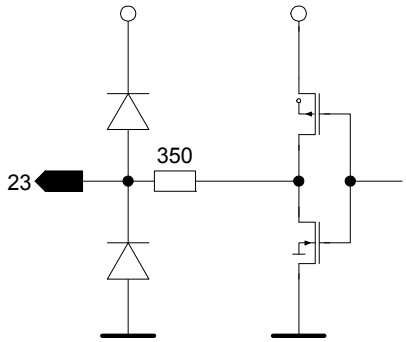
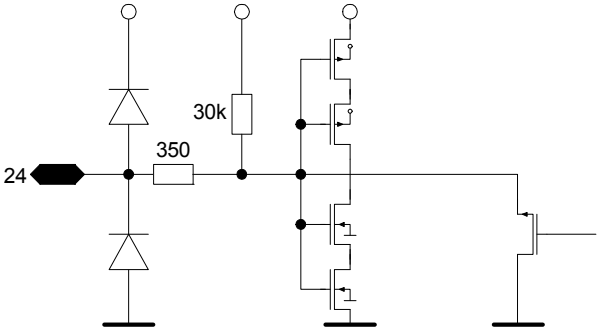
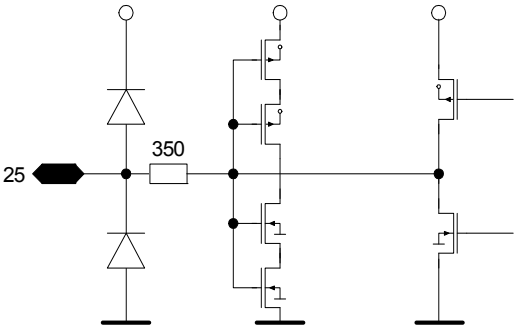
Ball No.	Name	Pin Type	Buffer Type	Function
22	RESET			Reset of the Entire System (to Default Values) Active Low
23	CLKDIV			Clock Output
24	PWDDD			Power Down Input (Active High), Data Detect Output (Active Low)
25	DATA			TX Data Input, RX Data Output (RX Powerdown: Pin 25 @ GND)
26	GNDRF3		See Pin 5	Ground Return for RF except PA

Table 1 Pin Definition and Function (cont'd)

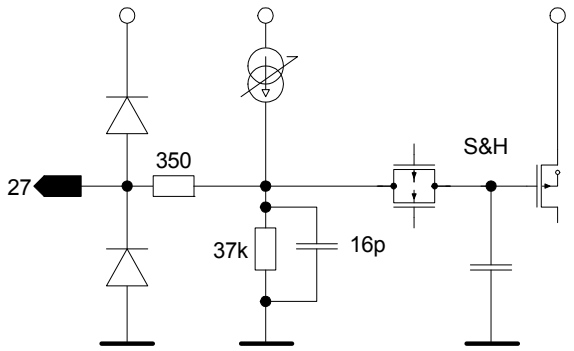
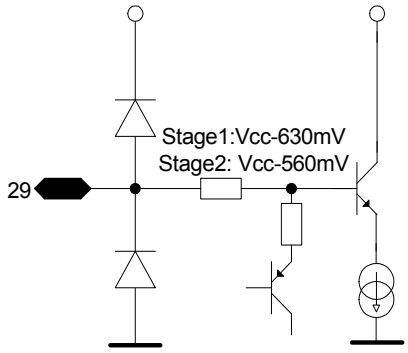
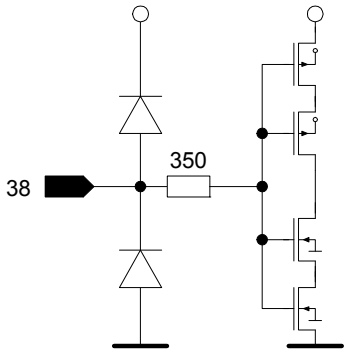
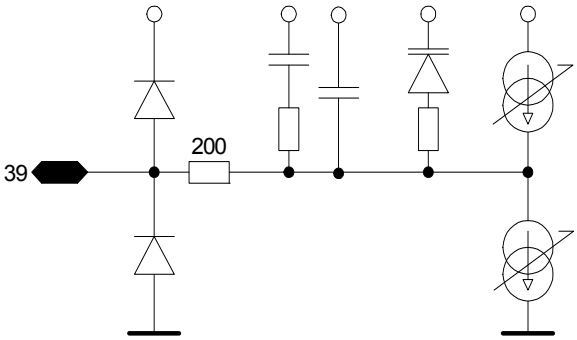
Ball No.	Name	Pin Type	Buffer Type	Function
27	RSSI			RSSI Output
28	GND		See Pin 5	Analog Ground
29	CQ2x			Pin for External Capacitor Q-channel, stage 2
30	CQ2		See Pin 29	Pin for External Capacitor Q-channel, stage 2
31	CI2x		See Pin 29	Pin for External Capacitor I-channel, stage 2
32	CI2		See Pin 29	Pin for External Capacitor I-channel, stage 2
33	CQ1x		See Pin 29	Pin for External Capacitor Q-channel, stage 1
34	CQ1		See Pin 29	Pin for External Capacitor Q-channel, stage 1
35	CI1x		See Pin 29	Pin for External Capacitor I-channel, stage 1
36	CI1		See Pin 29	Pin for External Capacitor I-channel, stage 1
37	VCC		See Pin 7	Analog Supply Antiparallel diodes between VCC, VCC1, VDD

Table 1 Pin Definition and Function (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
38	BUSMODE			Bus Mode Selection I^2C/3 wire bus mode selection
39	LF			Loop Filter and VCO Control Voltage
40	GNDRF1		See Pin 5	Ground Return for LNA

2.3 Functional Block Diagram

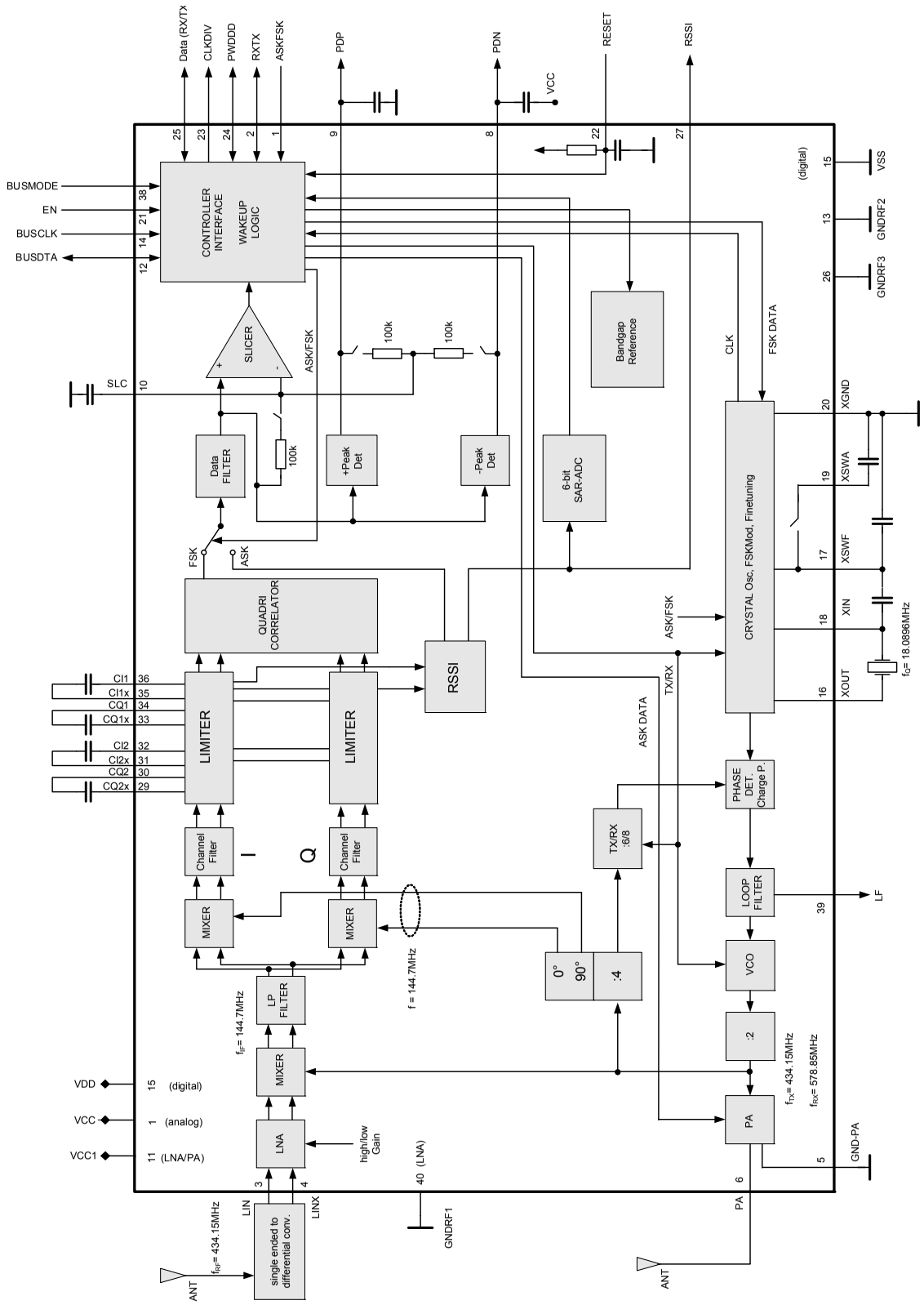


Figure 4 Main Block Diagram

2.4 Functional Block Description

2.4.1 Power Amplifier (PA)

The power amplifier is operating in C-mode. It can be used in either high or low power mode. In high-power mode the transmit power is approximately +13 dBm into 50 Ω at 5 V and +6 dBm at 2.1 V supply voltage. In low power mode the transmit power is approximately +11 dBm at 5 V and -32 dBm at 2.1 V supply voltage using the same matching network. The transmit power is controlled by the D0-bit of the CONFIG register (sub-address 00H) as shown in the following **Table 2**. The default output power mode is high power mode.

Table 2 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D0	PA_PWR	0 = Low TX Power, 1 = High TX Power	1

In case of ASK modulation the power amplifier is turned fully on and off by the transmit baseband data, i.e. 100% On-Off-Keying.

2.4.2 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20 dB and symmetrical inputs. It is possible to reduce the gain to 0 dB via logic.

Table 3 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D4	LNA_GAIN	0 = Low Gain, 1 = High Gain	1

2.4.3 Downconverter 1st Mixer

The Double Balanced 1st Mixer converts the input frequency (RF) in the range of 434-435 MHz down to the intermediate frequency (IF) at approximately 144 MHz. The local oscillator frequency is generated by the PLL synthesizer that is fully implemented on-chip as described in **Chapter 2.4.5**. This local oscillator operates at approximately 578 MHz in receive mode providing the above mentioned IF frequency of 144 MHz. The mixer is followed by a low pass filter with a corner frequency of approximately 175 MHz in order to prevent RF and LO signals from appearing in the 144 MHz IF signal.

2.4.4 Downconverter 2nd I/Q Mixers

The Low pass filter is followed by 2 mixers (inphase I and quadrature Q) that convert the 144 MHz IF signal down to zero-IF. These two mixers are driven by a signal that is generated by dividing the local oscillator signal by 4, thus equalling the IF frequency.

2.4.5 PLL Synthesizer

The Phase Locked Loop synthesizer consists of two VCOs (i.e. transmit and receive VCO), a divider by 4, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCOs are including spiral inductors and varactor diodes. The center frequency of the transmit VCO is 868 MHz, the center frequency of the receive VCO is 1156 MHz.

Generally in receive mode the relationship between local oscillator frequency f_{osc}, the receive RF frequency f f_{RF} and the IF frequency f f_{IF} and thus the frequency that is applied to the I/Q Mixers is given in the following formula:

$$\frac{f_{osc}}{2} = 4/3\, f_{RF} = 4\, f_{IF} \tag{1}$$

The VCO signal is applied to a divider by 2 and afterwards by 4 which is producing approximately 144 MHz signals in quadrature. The overall division ratio of the divider chain following the divider by 2 and 4 is 6 in transmit mode and 8 in receive mode as the nominal crystal oscillator frequency is 18.083 MHz. The division ratio is controlled by the RxTx pin (pin 2) and the D10 bit in the CONFIG register.

2.4.6 I/Q Filters

The I/Q IF to zero-IF mixers are followed by baseband 6th order low pass filters that are used for RF-channel filtering.

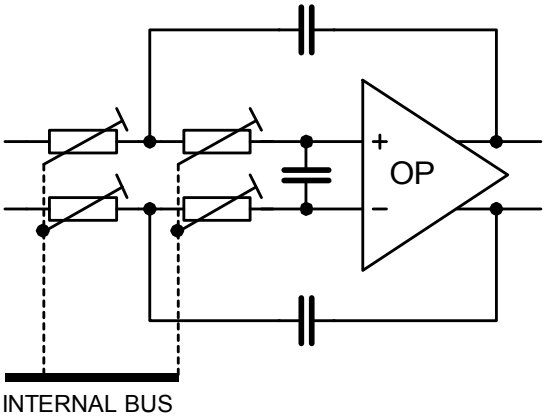


Figure 5 One I/Q Filter Stage

The bandwidth of the filters is controlled by the values set in the filter-register. It can be adjusted between 50 and 350 kHz in 50 kHz steps via the bits D1 to D3 of the LPF register (sub-address 03H).

2.4.7 I/Q Limiters

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80 dB each in the frequency range of 100 Hz up to 350 kHz. Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

2.4.8 FSK Demodulator

The output differential signals of the I/Q limiters are fed to a quadrature correlator circuit that is used to demodulate frequency shift keyed (FSK) signals. The demodulator gain is 2.4 mV/kHz, the maximum frequency deviation is ±300 kHz as shown in **Figure 6** below.

The demodulated signal is applied to the ASK/FSK mode switch which is connected to the input of the data filter. The switch can be controlled by the ASKFSK pin (pin 1) and via the D11 bit in the CONFIG register.

The modulation index m must be significantly larger than 2 and the deviation at least larger than 25 kHz for correct demodulation of the signal.

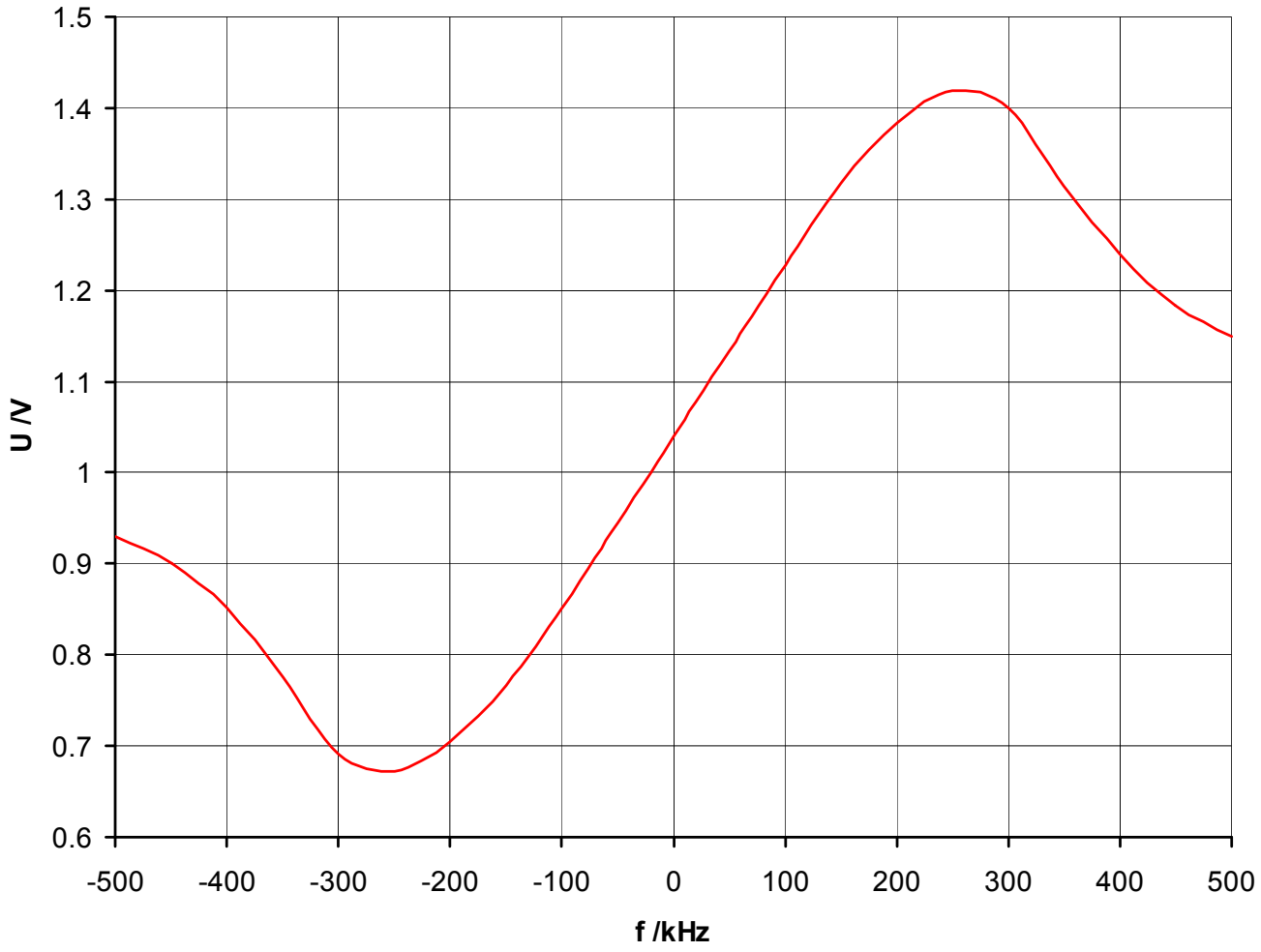


Figure 6 Quadricorrelator Demodulation Characteristic

2.4.9 Data Filter

The 2-pole data filter has a Sallen-Key architecture and is implemented fully on-chip. The bandwidth can be adjusted between approximately 5 kHz and 102 kHz via the bits D4 to D7 of the LPF register as shown in **Table 29**.

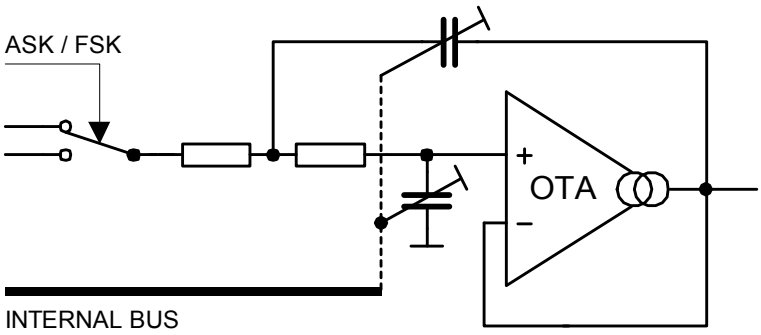


Figure 7 Data Filter Architecture

2.4.10 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. The self-adjusting threshold is generated by a RC-network (LPF) or by use of one or both peak detectors depending on the baseband coding scheme as described in **Chapter 3.6**. This can be controlled by the D15 bit of the CONFIG register as shown in the following table.

Table 4 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D15	SLICER	0 = Lowpass Filter, 1 = Peak Detector	0

2.4.11 Peak Detectors

Two separate Peak Detectors are available. They are generating DC voltages in a fast-attack and slow-release manner that are proportional to the positive and negative peak voltages appearing in the data signal. These voltages may be used to generate a threshold voltage for non-Manchester encoded signals, for example. The time-constant of the fast-attack/slow-release action is determined by the RC network with external capacitor.

2.4.12 Crystal Oscillator

The reference oscillator is an NIC oscillator type (Negative Impedance Converter) with a crystal operating in serial resonance. The nominal operating frequency of 18.089583 MHz and the frequencies for FSK modulation can be adjusted via 3 external capacitors. Via microcontroller and bus interface the chip-internal capacitors can be used for fine-tuning of the nominal and the FSK modulation frequencies. This fine-tuning of the crystal oscillator allows to eliminate frequency errors due to crystal or component tolerances.

2.4.13 Bandgap Reference Circuitry and Powerdown

A Bandgap Reference Circuit provides a temperature stable 1.2 V reference voltage for the device. A power down mode is available to switch off all subcircuits that are controlled by the bidirectional Powerdown & DataDetect PWDDD pin (pin 24) as shown in the following table. Power down mode can either be activated by pin 24 or bit D14 in Register 00h. In power down mode also pin 25 (DATA) is affected (see **Chapter 2.4.18**).

Table 5 PWDDD Pin Operating States

PWDDD	Operating State
VDD	Powerdown Mode
Ground/VSS	Device On

2.4.14 Timing and Data Control Unit

The timing and data control unit contains a wake-up logic unit, an I²C/3-wire microcontroller interface, a “data valid” detection unit and a set of configuration registers as shown in the subsequent figure.

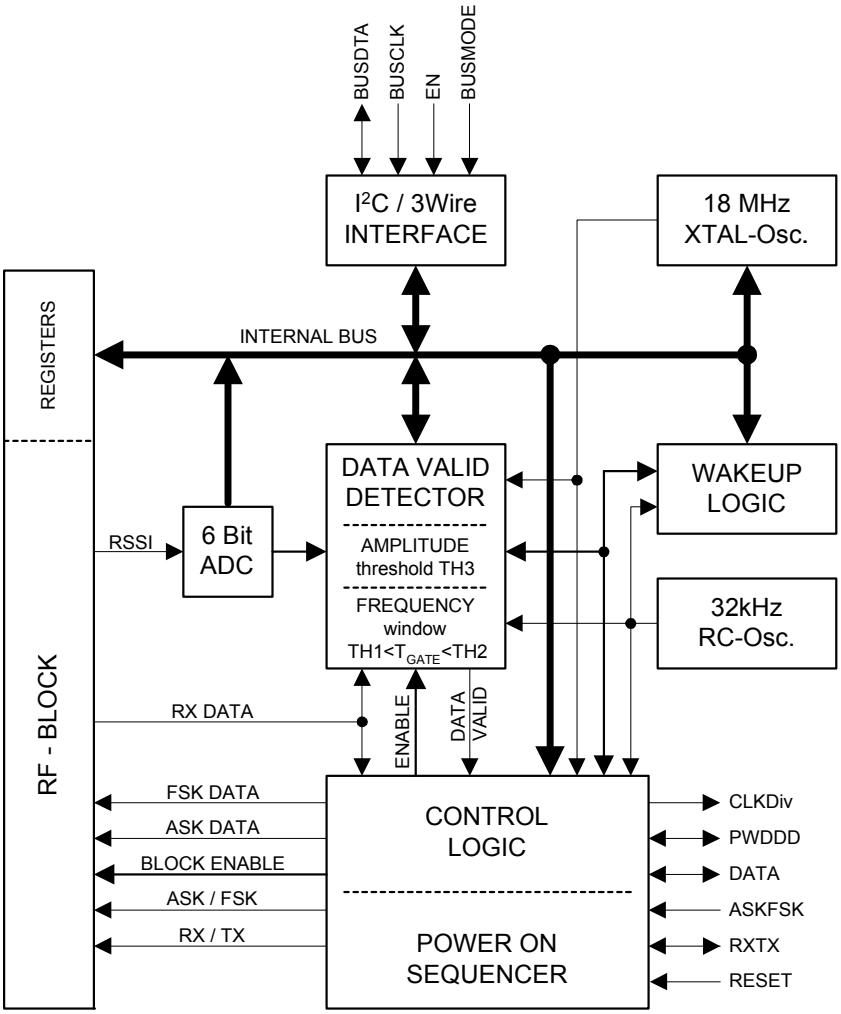


Figure 8 Timing and Data Control Unit

The I²C/3-wire Bus Interface gives an external microcontroller full control over important system parameters at any time.

It is possible to set the device in three different modes: Slave Mode, Self Polling Mode and Timer Mode. This is done by a state machine which is implemented in the WAKEUP LOGIC unit. A detailed description is given in **Chapter 2.4.17**.

The DATA VALID DETECTOR contains a frequency window counter and an RSSI threshold comparator. The window counter uses the incoming data signal from the data slicer as the gating signal and the crystal oscillator frequency as the time base to determine the actual data rate. The result is compared with the expected data rate.

The threshold comparator compares the actual RSSI level with the expected RSSI level.

If both conditions are true the PWDDD pin is set to LOW in self polling mode as you can see in **Chapter 2.4.17**. This signal can be used as an interrupt for an external μP. Because the PWDDD pin is bidirectional and open drain driven by an internal pull-up resistor it is possible to apply an external LOW thus enabling the device.

2.4.15 Bus Interface and Register Definition

The TDA7255V supports the I²C bus protocol (2 wire) and a 3-wire bus protocol. Operation is selectable by the BUSMODE pin (pin 38) as shown in the following table. All bus pins (BUSDTA, BUSCLK, EN, BUSMODE) have a Schmitt-triggered input stage. The BUSDTA pin is bidirectional where the output is open drain driven by an internal 15 kΩ pull up resistor.

Table 6 Bus Interface Format

Function	BUSMODE	EN	BUSCLK	BUSDTA
I²C Mode	Low	High = inactive, Low = active	Clock input	Data in/out
3-wire Mode	High			

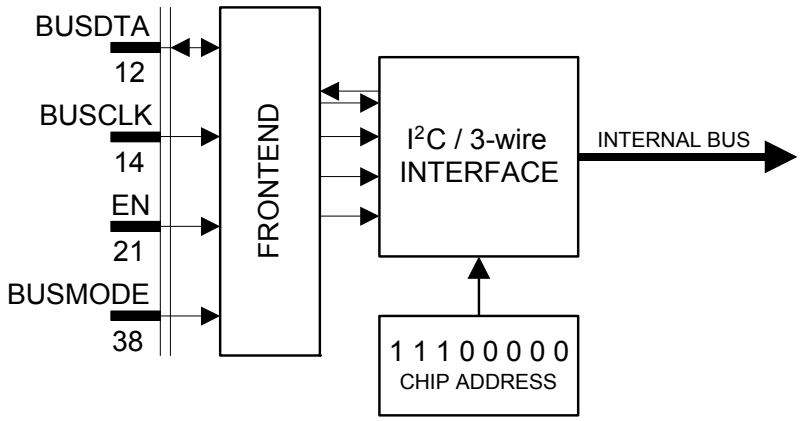


Figure 9 Bus Interface

Note: The interface is able to access the internal registers at any time, even in POWER DOWN mode. There is no internal clock necessary for Interface operation.

2.4.15.1 I²C Bus Mode

In this mode the BUSMODE pin (pin 38) = LOW and the EN pin (pin 21) = LOW.

Data Transition

Data transition on the pin BUSDTA can only occur when BUSCLK is LOW. BUSDTA transitions while BUSCLK is HIGH will be interpreted as start or stop condition.

Start Condition (STA)

A start condition is defined by a HIGH to LOW transition of the BUSDTA line while BUSCLK is HIGH. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO)

A stop condition is defined by a LOW to HIGH transition of the BUSDTA line while BUSCLK is HIGH. This condition terminates the communication between the devices and forces the bus interface into the initial state.

Acknowledge (ACK)

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will set the SDA line to LOW level to indicate it has received the 8 bits of data correctly.

Data Transfer Write Mode

To start the communication, the bus master must initiate a start condition (STA), followed by the 8 bit chip address. The chip address for the TDA7255V is fixed as „1110000“ (MSB at first). The last bit (LSB = A0) of the chip address byte defines the type of operation to be performed:

A0 = 0, a write operation is selected and A0 = 1 a read operation is selected.

After this comparison the TDA7255V will generate an ACK and awaits the desired sub address byte (00H...0FH) and data bytes. At the end of the data transition the master has to generate the stop condition (STO).

Data Transfer Read Mode

To start the communication in the read mode, the bus master must initiate a start condition (STA), followed by the 8 bit chip address (write: A0 = 0), followed by the sub address to read (80H, 81H), followed by the chip address (read: A0 = 1). After that procedure the data of the selected register (80H, 81H) is read out. During this time the data line has to be kept in HIGH state and the chip sends out the data. At the end of data transition the master has to generate the stop condition (STO).

2.4.15.2 Bus Data Format in I²C Mode

Table 7 Chip Address Organization

MSB							LSB	Function
1	1	1	0	0	0	0	0	Chip Address Write
1	1	1	0	0	0	0	1	Chip Address Read

Table 8 I²C Bus Write Mode 8 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN						LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	STO

Table 9 I²C Bus Write Mode 16 Bit

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH						LSB		MSB	DATA IN						LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D15	...	D8	ACK	D7	D6	...	D0	ACK	STO

Table 10 I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (READ) 80H, 81H						LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	STA	1	1	1	0	0	0	0	1	ACK

Table 11 I²C Bus Read Mode (continued)

MSB	DATA OUT FROM SUB ADDRESS						LSB		
R7	R6	R5	R4	R3	R2	R1	R0	ACK[1)]	STO

1) Mandatory HIGH

2.4.15.3 3-Wire Bus Mode

In this mode pin 38 (BUSMODE) = HIGH and Pin 12 (BUSDTA) is in the data input/output pin. Pin 21 (EN) is used to activate the bus interface to allow the transfer of data to / from the device. When pin 21 (EN) is inactive (HIGH), data transfer is inhibited.

Data Transition

Data transition on pin 12 (BUSDTA) can only occur if the clock BUSCLK is LOW. To perform a data transfer the interface has to be enabled. This is done by setting the EN line to LOW. A serial transfer is done via BUSDTA, BUSCLK and EN. The bit stream needs no chip address.

Data Transfer Write Mode

To start the communication the EN line has to be set to LOW. The desired sub address byte and data bytes have to follow. The sub-address (00H...0FH) determines which of the data bytes are transmitted. At the end of data transition the EN must be HIGH.

Data Transfer Read Mode

To start the communication in the read mode, the EN line has to be set to LOW followed by the sub address to read (80H, 81H). Afterwards the device is ready to read out data. At the end of data transition EN must be HIGH.

2.4.15.4 Bus Data Format 3-Wire Bus Mode

Table 12 3-Wire Bus Write Mode

MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH,0FH						LSB	MSB	DATA IN X...0 (X = 7 or 15)						LSB
S7	S6	S5	S4	S3	S2	S1	S0	DX	...	D5	D4	D3	D2	D1	D0

Table 13 3-Wire Bus Read Mode

MSB	SUB ADDRESS (READ) 80H, 81H						LSB	MSB	DATA OUT FROM SUB ADDRESS						LSB
S7	S6	S5	S4	S3	S2	S1	S0	R7	R6	R5	R4	R3	R2	R1	R0