Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

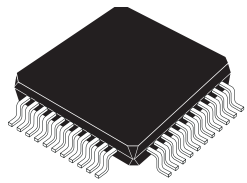
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

TDA7407

Advanced car signal processor

Features

- Fully integrated signal processor optimized for car radio applications
- Fully programmable by i^2c bus
- Includes audioprocessor, stereo decoder with noise blanker and multipath detector
- Softmute function
- Programmable roll-off compensation
- No external components



LQFP44

Description

The TDA7407 is the newcomer of the CSP family introduced by TDA7460/61. It uses the same innovative concepts and design technologies allowing fully software programmability through I^2C bus and overall cost optimisation for the system designer.

The device includes a three band audioprocessor with configurable inputs, and absence of external components for filter settings, a last generation stereo decoder with multipath detector, and a sophisticated stereo blend and noise cancellation circuitry. Strength points of the CSP approach are flexibility and overall cost/room saving in the application, combined with high performances.

Order codes

Part number	Package	Packing
TDA7407	LQFP44	Tray
TDA7407TR	LQFP44	Tape and reel

Contents

List of tables

List of figures

1 Block diagram and pin connections

Figure 1. Block diagram

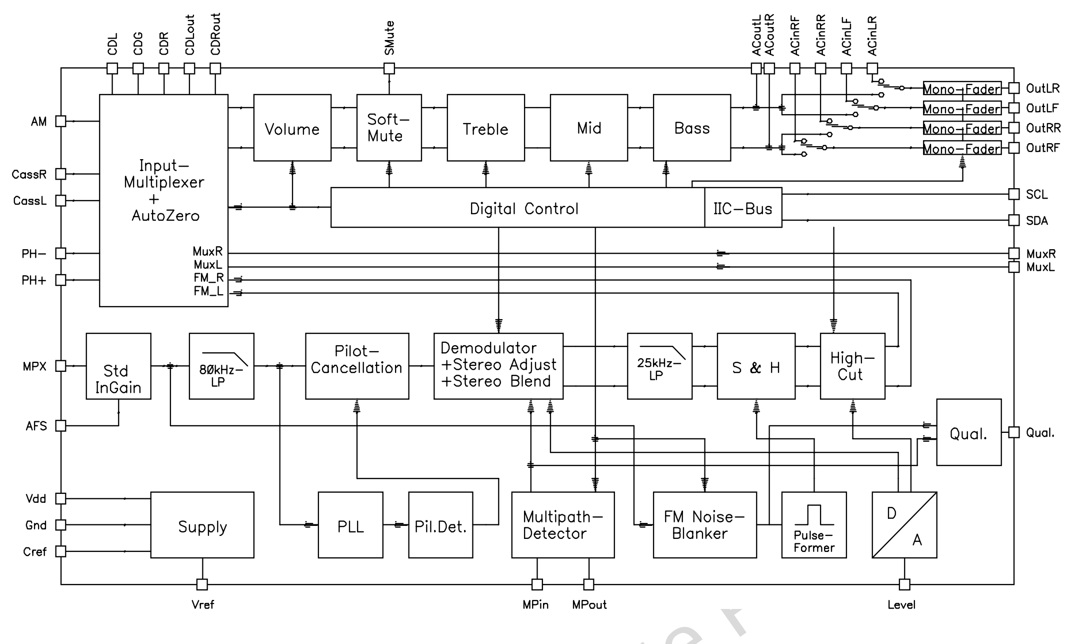


Figure 2. Pin connections (top view)

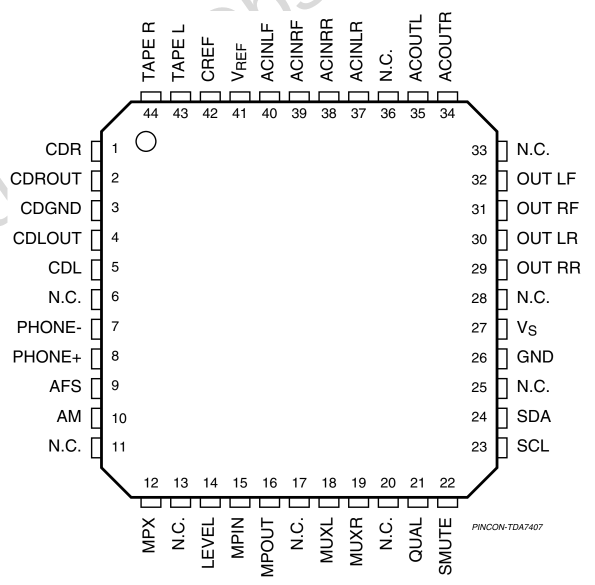


Table 1. Pin Description

N.	Name	Function	Type
1	CDR	CD right channel input	I
2	CDROUT	CD output right channel	O
3	CDGND	CD input common ground	I
4	CDLOUT	CD output left channel	O
5	CDL	CD input left channel	I
6	nc		-
7	PH -	Differential phone input -	I
8	PH +	Differential phone input +	I
9	AFS	AFS drive	I
10	AM	AM input	I
11	nc		-
12	MPX	FM stereo decoder input	I
13	nc		-
14	LEVEL	Level input stereo decoder	I
15	MPIN	Multipath input	I
16	MPOUT	Multipath output	O
17	nc		-
18	MUXL	Multiplexer output left channel	O
19	MUXR	Multiplexer output right channel	O
20	nc		-
21	QUAL	Stereo decoder quality output	O
22	SMUTE	Soft mute drive	I
23	SCL	I^2C clock line	I
24	SDA	I^2C data line	I/O
25	nc		-
26	GND	Supply ground	S
27	VS	Supply voltage	S
28	nc		-
29	OUTRR	Right rear speaker output	O
30	OUTLR	Left rear speaker output	O
31	OUTRF	Right front spaeaker output	O
32	OUTLF	Left front speaker output	O
33	nc		-
34	ACOUTR	Pre-speaker AC output right channel	O
35	ACOUTL	Pre-speaker AC output left channel	O

Table 1. Pin Description (continued)

N.	Name	Function	Type
36	nc		-
37	ACINLR	Pre-speaker input left rear channel	I
38	ACINRR	Pre-speaker input right rear channel	I
39	ACINRF	Pre-speaker input right front channel	I
40	ACINLF	Pre-speaker input left front channel	I
41	VREF	Reference voltage output	O
42	CREF	Reference capacitor pin	S
43	TAPEL	Tape input left	I
44	TAPER	Tape input right	I

Pin type legend: I = Input ; O = Output; I/O = Input/Output; S = Supply; nc = not connected

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature range	-40 to 85	°C
T_{stg}	Operating storage temperature range	-55 to 150	°C

Table 3. Supply

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		7.5	9	10	V
I_S	Supply current	V_S = 9V	30	35	40	mA
SVRR	Ripple rejection @ 1KHz	Audioprocessor (all filters flat)	50	60		dB
		Stereo decoder + audioprocessor	45	55		dB

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\text{-}j\ pins}$	Thermal resistance junction to pins (max)	85	°C/W

1.1 ESD

All pins are protected against ESD according to the MIL883 standard.

2 Audio processor part

2.1 List of features

2.1.1 Input multiplexer

- Quasi differential CD and cassette stereo input
- AM mono input
- Phone differential input
- Multiplexer signal after In-Gain available at separate pins

2.1.2 Volume control

- 1dB attenuator
- Max. gain 15dB
- Max. attenuation 79dB

2.1.3 Bass control

- 2^{nd} order frequency response
- Q-factor programmable in 4 steps
- Center frequency programmable in 4(5) steps
- DC gain programmable
- ±15 x 1dB steps

2.1.4 Mid control

- 2^{nd} order frequency response
- Q-factor programmable in 2 steps
- Center frequency programmable in 4 steps
- ±15 x 1dB steps

2.1.5 Treble control

- 2^{nd} order frequency response
- Center frequency programmable in 4 steps
- ±15 x 1dB steps

2.1.6 Speaker control

- 4 independent speaker controls in 1dB steps
- max gain 15dB
- max. attenuation 79dB

2.1.7 Mute functions

- Direct mute
- Digitally controlled softmute with 4 programmable mute time.

2.2 Electrical characteristics

Table 5. Audio processor electrical characteristics
(V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	all inputs except phone	70	100	130	KΩ
V_{CL}	Clipping level		2.2	2.6		V_{RMS}
S_{IN}	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. input gain		13	15	17	dB
G_{STEP}	Step resolution		0.5	1	1.5	dB
V_{DC}	DC steps	Adjacent gain step	-5	0.5	5	mV
		GMIN to GMAX	-10	5	10	mV
Differential CD stereo input						
R_{in}	Input resistance	Differential	70	100	130	KΩ
		Common mode	70	100	130	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1V_{RMS} @ 1KHz	45	70		dB
		V_{CM} = 1V_{RMS} @ 10KHz	45	60		dB
e_N	Output noise @ speaker outputs	20Hz to 20KHz flat; all stages 0dB		6	15	mV
Differential phone input						
R_{in}	Input resistance	Differential	40	56		KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1V_{RMS} @ 1KHz	40	70		dB
		V_{CM} = 1V_{RMS} @ 10KHz	40	60		dB
Volume control						
G_{MAX}	Max gain		13	15	17	dB
A_{MAX}	Max attenuation		70	79		dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -60 to 20dB	-4	0	3	dB
E_T	Tracking error				2	dB

Table 5. Audio processor electrical characteristics (continued)
(V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DC}	DC steps	Adjacent attenuation steps		0.1	3	mV
		From 0dB to GMIN		0.5	5	mV
Soft mute/AFS						
A_{MUTE}	Mute attenuation		80	100		dB
T_D	Delay time	T1		0.48		ms
		T2		0.96		ms
		T3		40.4		ms
		T4		324		ms
$V_{TH\ low}$	Low threshold for SM-/AFS- Pin(1)				1	V
$V_{TH\ high}$	High threshold for SM-/AFS-Pin		2.5			V
R_{PD}	Internal pull-up resistor			45		KΩ
Bass control						
C_{RANGE}	Control range		±13	±15	±17	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_C	Center frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100 (150) (2)	110	Hz
Q_{BASS}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	1	dB
		DC = on	3.5	4.4	5.5	dB
MID control						
C_{RANGE}	Control range		±13	±15	±17	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_C	Center frequency	f_{C1}	450	500	550	Hz
		f_{C2}	0.9	1	1.1	kHz
		f_{C3}	1.35	1.5	1.65	kHz
		f_{C4}	1.8	2	2.2	kHz

Table 5. Audio processor electrical characteristics (continued)
(V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Q_{MID}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.8	2	2.2	
Treble control						
C_{RANGE}	Control range		±13	±15	±17	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_C	Center frequency	f_{C1}	8	10	12	KHz
		f_{C2}	10	12.5	15	KHz
		f_{C3}	12	15	18	KHz
		f_{C4}	14	17.5	21	KHz

1. The SM pin is active low (mute = 0)
2. See note in programming section

3 Stereo decoder part

Table 6. Stereo decoder electrical characteristics
(V_S = 9V; de-emphasis time constant = 50µs, V_{MPX} = 500mV (75KHz deviation), fm= 1KHz, Gv = 6dB. T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{in}	MPX input level	G_v = 3.5dB		0.5	1.25	V_{RMS}
R_{in}	Input resistance		70	100	130	KΩ
G_{MIN}	Min. input gain		1.5	3.5	4.5	dB
GMAX	Max. input gain		8.5	11	12.5	dB
GSTEP	Step resolution		1.75	2.5	3.25	dB
SVRR	Supply voltage ripple rejection	Vripple = 100mV; f = 1KHz	35	60		dB
α	Max. channel separation		30	50		dB
THD	Total harmonic distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus noise to noise ratio	A-weighted, S = $2V_{RMS}$	80	91		dB
Mono / stereo switch						
V_{PTHST1}	Pilot threshold voltage	for Stereo, PTH = 1	10	15	25	mV
V_{PTHST0}	Pilot threshold voltage	for Stereo, PTH = 0	15	25	35	mV
V_{PTHMO1}	Pilot threshold voltage	for Mono, PTH = 1	7	12	17	mV
V_{PTHMO0}	Pilot threshold voltage	for Mono, PTH = 1	10	19	25	mV
PLL						
Δf/f	Capture range		0.5			%
De-emphasis and highcut						
t_{HC50}	De-emphasis time constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCH}	25	50	75	µs
t_{HC75}	De-emphasis time constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCH}	50	75	100	µs
t_{HC50}	Highcut time constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCL}	100	150	200	µs
t_{HC75}	Highcut time constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCL}	150	225	300	µs
Stereo blend and highcut control						
REF5V	Internal reference voltage		4.7	5	5.3	V
T_{CREF5V}	Temperature coefficient			3300		ppm
L_{Gmin}	Min. LEVEL gain		-1	0	1	dB
L_{Gmax}	Max. LEVEL gain		8	10	12	dB

Table 6. Stereo decoder electrical characteristics (continued)
(V_S = 9V; de-emphasis time constant = 50µs, V_{MPX} = 500mV (75KHz deviation), fm= 1KHz, Gv = 6dB. T_{amb} = 25°C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
L_{Gstep}	LEVEL gain step resolution		0.3	0.67	1	dB
$VSBL_{min}$	Min. voltage for mono		25	29	33	%REF5V
$VSBL_{max}$	Min. voltage for mono		54	58	62	%REF5V
$VSBL_{step}$	Step resolution		2.2	4.2	6.2	%REF5V
$VHCH_{min}$	Min. voltage for NO highcut		38	42	46	%REF5V
$VHCH_{max}$	Min. voltage for NO highcut		62	66	70	%REF5V
$VHCH_{step}$	Step resolution		5	8.4	12	%REF5V
$VHCL_{min}$	Min. voltage for full highcut		12	17	22	%VHCH
$VHCL_{max}$	Max. voltage for full highcut		28	33	38	%VHCH
$VHCL_{step}$	Step resolution		2.2	4.2	6.2	%VHCH
Carrier and harmonic suppression at the output						
$\alpha19$	Pilot signal f = 19KHz		40	50		dB
$\alpha38$	Subcarrier f = 38KHz				75	dB
$\alpha57$	Subcarrier f = 57KHz				62	dB
$\alpha76$	Subcarrier f = 76KHz				90	dB
Intermodulation (Note 1)						
$\alpha2$	f_{mod} = 10KHz, f_{spur} = 1KHz				65	dB
$\alpha3$	f_{mod} = 13KHz, f_{spur} = 1KHz				75	dB
Traffic Ratio (Note 2)						
$\alpha57$	Signal f = 57KHz				70	dB
SCA - Subsidiary communications authorization (note 3)						
$\alpha67$	Signal f = 67KHz				75	dB
ACI - Adjacent channel interference (note 4)						
$\alpha114$	Signal f = 114KHz				95	dB
$\alpha190$	Signal f = 190KHz				84	dB

3.1 Notes to the characteristics:

1. Intermodulation suppression:

$$\alpha 2 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz)}};\ f_s = (2 \times 10kHz) - 19kHz$$

$$\alpha 3 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz)}};\ f_s = (3 \times 13kHz) - 38kHz$$

measured with: 91% pilot signal; fm = 10kHz or 13kHz.

2. Traffic radio (V.F.) suppression: measured with: 91% stereo signal; 9% pilot signal; fm = 1kHz; 5% subcarrier (f = 57kHz, fm = 23Hz AM, m = 60%)

$$\alpha 57(V.W > F.) = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz \pm 23kHz)}}$$

3. SCA (Subsidiary Communications Authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1kHz; 10% SCA - subcarrier (fs = 67kHz, unmodulated).

$$\alpha 67 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at9kHz)}};\ F_s = (2 \times 38kHz) - 67kHz$$

4. ACI (Adjacent Channel Interference):

$$\alpha 114 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at4kHz)}};\ F_s = 110kHz - (3 \times 38kHz)$$

$$\alpha 114 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at4kHz)}};\ F_s = 186kHz - (5 \times 38kHz)$$

measured with: 90% mono signal; 9% pilot signal; fm =1kHz; 1% spurious signal (fs = 110kHz or 186kHz, unmodulated).

4 Noise blanker part

- internal 2nd order 140kHz high pass filter
- programmable trigger threshold
- trigger threshold dependent on high frequency noise with programmable gain
- additional circuits for deviation and fieldstrength dependent trigger adjustment
- very low offset current during hold time due to opamps wMOS inputs
- four selectable pulse suppression times
- programmable noise rectifier charge/discharge current

Table 7. Noise blanker electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger threshold (1) (2)	meas. with V_{PEAK} = 0.9V	NBT = 111	(10)	30	(10)	mV_{OP}
			NBT = 110	(10)	35	(10)	mV_{OP}
			NBT = 101	(10)	40	(10)	mV_{OP}
			NBT = 100	(10)	45	(10)	mV_{OP}
			NBT = 011	(10)	50	(10)	mV_{OP}
			NBT = 010	(10)	55	(10)	mV_{OP}
			NBT = 001	(10)	60	(10)	mV_{OP}
			NBT = 000	(10)	65	(10)	mV_{OP}
$V_{TRNOISE}$	Noise controlled trigger threshold (3)	meas. with V_{PEAK} = 1.5V	NCT = 00	(10)	260	(10)	mV_{OP}
			NCT = 01	(10)	220	(10)	mV_{OP}
			NCT = 10	(10)	180	(10)	mV_{OP}
			NCT = 11	(10)	140	(10)	mV_{OP}
V_{RECT}	Rectifier voltage	V_{MPX} = 0mV	NRD (7) = 00	0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 200mV; f = 150KHz		2.2	2.5	2.9	V
$V_{RECT\ DEV}$	Deviation dependent rectifier voltage (4)	means. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	V_{OP}
			OVD = 10	0.9	1.2	1.5	V_{OP}
			OVD = 01	1.7	2.0	2.3	V_{OP}
			OVD = 00	2.5	2.8	3.1	V_{OP}
$V_{RECT\ FS}$	Fieldstrength controlled rectifier voltage (5)	means. with V_{MPX} = 0mV V_{LEVEL} << V_{SBL} (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	0.9	1.4	1.5	V
			FSC = 01	1.7	1.9	2.3	V
			FSC = 00	2.1	2.4	3.1	V

Table 7. Noise blanker electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
T_S	Suppression pulse duration (6)	Signal HOLDN in testmode	BLT = 00	TBD	38	TBD	µs
			BLT = 10	TBD	32	TBD	µs
			BLT = 01	TBD	25.5	TBD	µs
			BLT = 00	TBD	22	TBD	µs
$V_{RECTADJ}$	Noise rectifier discharge adjustment (7)	Signal PEAK in testmode	NRD = 00 (5)	(10)	0.3	(10)	V/ms
			NRD = 01 (5)	(10)	0.8	(10)	V/ms
			NRD = 10 (5)	(10)	1.3	(10)	V/ms
			NRD = 11 (5)	(10)	2.0	(10)	V/ms
SR_{PEAK}	Noise rectifier charge	Signal PEAK in testmode	PCH = 0 (8)	(10)	10	(10)	mV/µs
			PCH = 1 (8)	(10)	20	(10)	mV/µs
V_{ADJMP}	Noise rectifier adjustment through multipath (9)	Signal PEAK in testmode	MPNB = 00 (9)	(10)	0.3	(10)	V/ms
			MPNB = 01 (9)	(10)	0.5	(10)	V/ms
			MPNB = 10 (9)	(10)	0.7	(10)	V/ms
			MPNB = 11 (9)	(10)	0.9	(10)	V/ms

1. All Thresholds are measured using a pulse with TR =2ms, THIGH = 2ms and TF = 10ms. The repetition rate must not increase the PEAK voltage
2. NBT represents the Noiseblanker Byte bits D2, D0 for the noise blanker trigger threshold
3. NAT represents the Noiseblanker Byte bit pair D4, D3 for the noise controlled triggeradjustment
4. OVD represents the Noiseblanker Byte bit pair D7, D6 for the over deviation detector
5. FSC represents the Fieldstrength Byte bit pair D1, D0 for the fieldstrength control
6. BLT represents the Speaker RR Byte bit pair D7, D6 for the blanktime adjustment
7. NRD represents the Configuration Byte bit pair D1, D0 for the noise rectifier discharge adjustment
8. PCH represents the Stereo decoder Byte bit D5 for the noise rectifier charge current adjustment
9. MPNB represents the HighCut Byte bit D7 and the Fieldstrength Byte D7 for the noise rectifier multipath adjustment
10. By design / characterization functionally guaranteed through dedicated test mode structure

Figure 3. Vn timing diagram

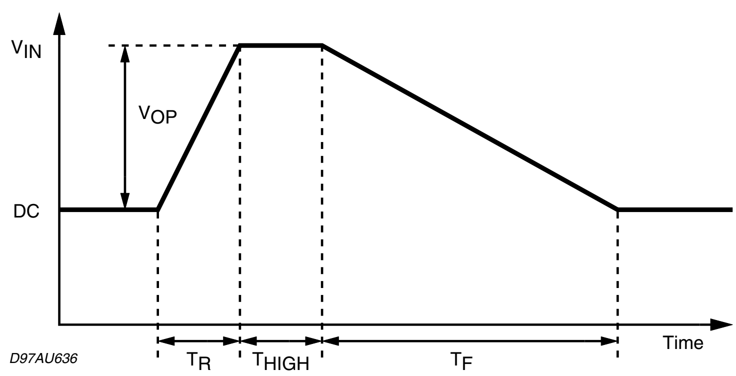


Figure 4. Trigger threshold vs. V_{PEAK}

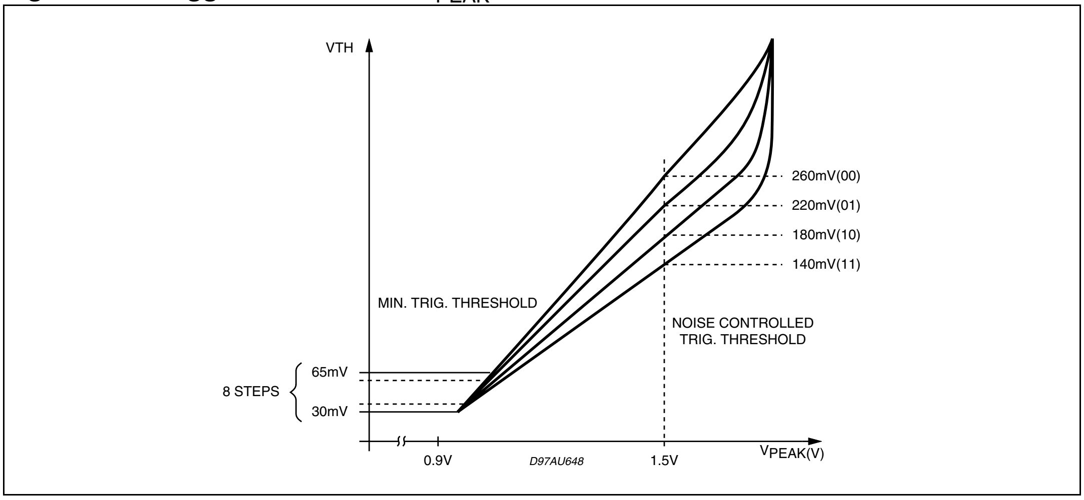


Figure 5. Deviation controlled trigger adjustment

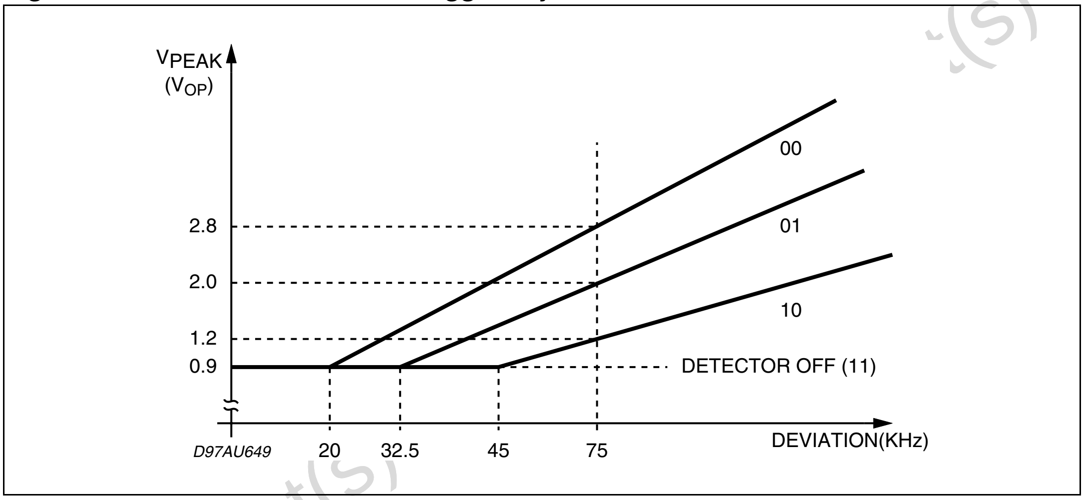
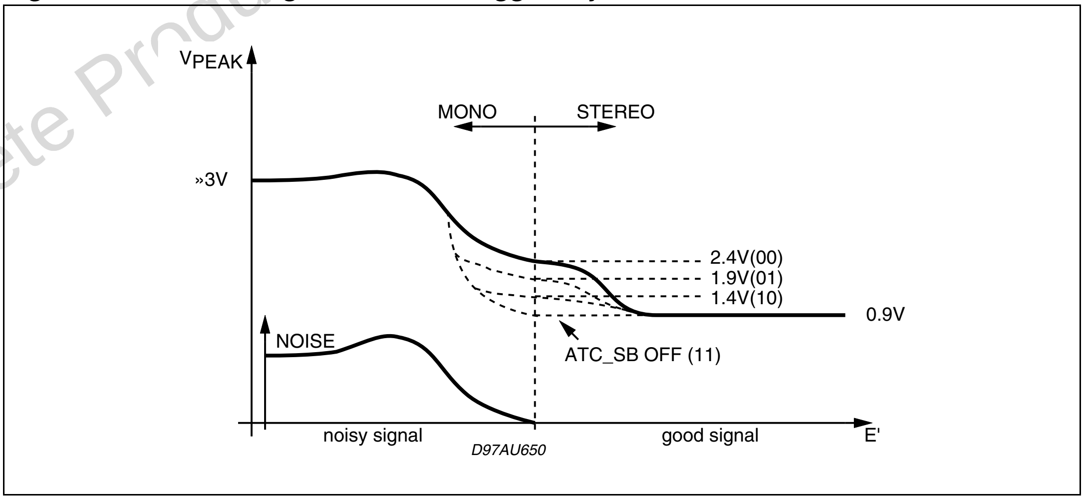


Figure 6. Fieldstrength controlled trigger adjustment



5 Multipath detector

- Internal 19kHz band pass filter
- Programmable band pass and rectifier gain
- two pin solution fully independent usable for external programming
- selectable internal influence on Stereoblend

Table 8. **Multipath electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CMP}	Center frequency of multipath-bandpass	stereo decoder locked on pilot tone		19		KHz
G_{BPMP}	Bandpass gain	bits D_2, D_1 configuration byte = 00		6		dB
		bits D_2, D_1 configuration byte = 10		12		dB
		bits D_2, D_1 configuration byte = 01		16		dB
		bits D_2, D_1 configuration byte = 11		18		dB
G_{RECTMP}	Rectifier gain	bits D_7, D_6 configuration byte = 00		7.6		dB
		bits D_7, D_6 configuration byte = 01		4.6		dB
		bits D_7, D_6 configuration byte = 10		0		dB
		bits D_7, D_6 configuration byte = 11		off		dB
I_{CHMP}	Rectifier charge current	bit D_5 configuration byte = 0		0.5		µA
		bit D_5 configuration byte = 1		1.0		µA
I_{DISMP}	Rectifier discharge current		0.5	1	1.5	mA

Table 9. **Quality detector**

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
A	Multipath Influence factor	Addr. 12 / Bit 5+6	00		0.7		dB
			01		0.85		dB
			10		1.00		dB
			11		1.15		dB
B	Noise influence factor	Addr. 16 / Bit 1+2	00		15		dB
			01		12		dB
			10		9		dB
			11		6		dB

5.1 Description of the audioprocessor part

5.1.1 Input multiplexer

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereo decoder input.

5.1.2 Input stages

Most of the input stages have remained the same as in preceeding ST audioprocessors with the exception of the CD inputs (see *Figure 7*). In the meantime there are some CD players on the market having a significant high source impedance which strongly affects the common mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common mode rejection even with those CD players.

The output of the CD stage is permanently available of the CD out-pins

5.1.3 AutoZero

In order to reduce the number of pins, there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid that effect a special offset cancellation stage called AutoZero is implemented.
This stage is located before the volume block to eliminate all offsets generated by the stereo decoder, the input stage and the In-Gain (please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not cancelled).

Auto-zeroing is started every time the DATA-BYTE 0 is selected and takes a time of max. 0.3ms. To avoid audible clicks the audioprocessor is muted before the volume stage during this time.

5.1.4 AutoZero remain

In some cases, for example if the µP is executing a refresh cycle of the I^2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7407 could be switched in the "Auto Zero Remain mode" (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

5.1.5 Multiplexer output

The output signal of the input multiplexer is available at separate pins (please see the block diagram). This signal represents the input signal amplifier by the In-Gain stage and is also going into the mixer stage.

5.1.6 Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^2C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions.

Figure 7. Input stages

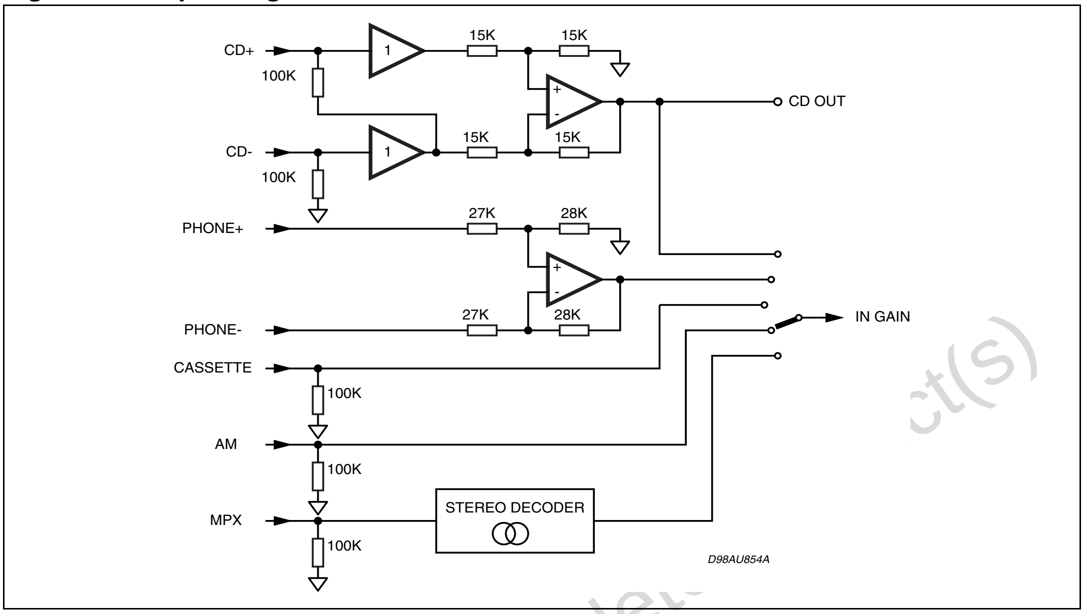
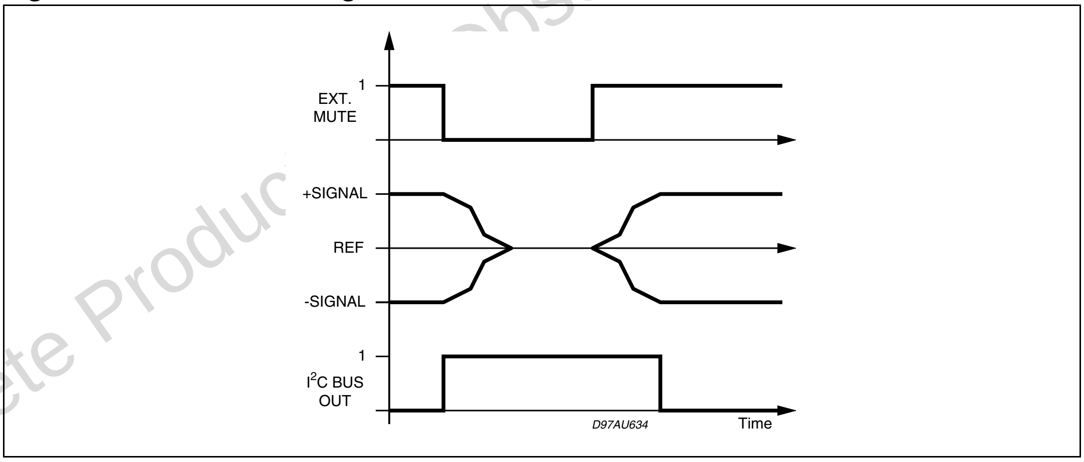


Figure 8. Softmute timing



Note: Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

5.1.7 BASS

There are four parameters programmable in the bass stage: (see figs *9*, *10*, *11*, *12*):

5.1.8 Attenuation (80Hz)

Figure 9 shows the attenuation as a function of frequency at a center frequency of 80Hz.

5.1.9 Center frequency (60, 70, 80, 100Hz)

Figure 10 shows the four possible center frequencies 60,70,80 and 100Hz.

5.1.10 Quality factors (1, 1.25, 1.5, 2)

Figure 11 shows the four possible quality factors 1, 1.25, 1.5 and 2.

5.1.11 DC mode

In this mode the DC gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25%, which can be used to reach alternative center frequencies or quality factors. (see *Figure 12*)

5.1.12 MID

There are 3 parameters programmable in the mid stage (see figures *13*, *14* and *15*)

5.1.13 Attenuation (1kHz)

Figure 13 shows the attenuation as a function of frequency at a center frequency of 1kHz.

5.1.14 Center frequency (500, 1k, 1.5k, 2k Hz)

Figure 14 shows the four possible center frequencies 500Hz, 1kHz, 1.5kHz and 2kHz.

5.1.15 Quality factor (2 at 1kHz)

Figure 15 shows the two possible quality factors 1 and 2 at a center frequency of 1kHz.

5.1.16 Treble

There are two parameters programmable in the treble stage (see figures *16*, and *17*):

5.1.17 Attenuation (17.5kHz)

Figure 16 shows the attenuation as a function of frequency at a center frequency of 17.5KHz.

5.1.18 Center frequency (10, 12.5, 15, 17.5kHz)

Figure 17 shows the four possible Center Frequency (10, 12.5, 15 and 17.5kHz).

5.1.19 AC coupling

In some applications additional signal manipulations are desired, for example surround sound or more band equalizing. For this purpose AC Coupling is placed before the speaker attenuators, which can be activated or internally shorted by Bit7 in the Bass/Treble configuration byte. In short condition the input signal of the speaker attenuator is available at

AC Outputs and the AC Input could be used as additional stereo inputs. The input impedance of the AC Inputs is always 50KΩ.

5.1.20 Speaker Attenuator

The speaker attenuators have exactely the same structure and range like the volume stage.

Figure 9. Bass control @ fc = 80Hz, Q = 1

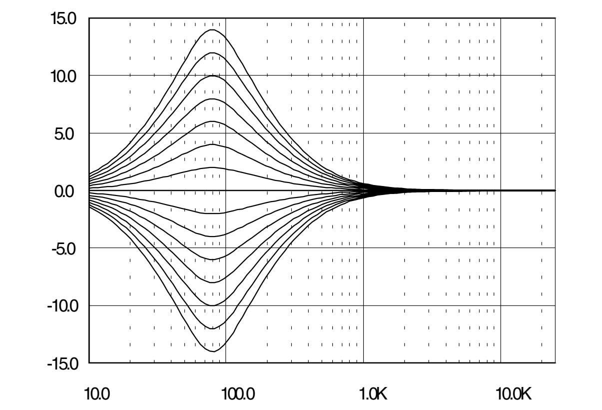


Figure 10. Bass center @ Gain = 14dB, Q =1

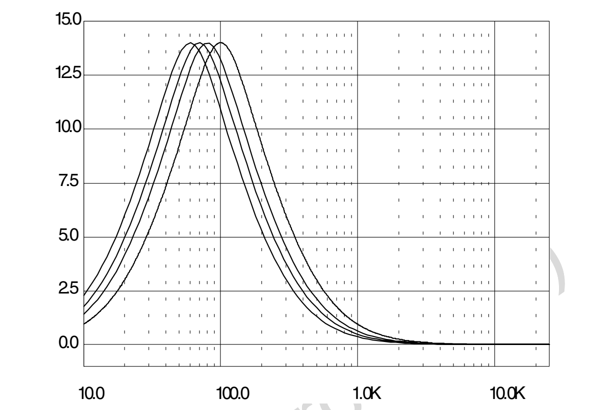


Figure 11. Bass quality factors @ Gain =14dB, fc = 80Hz

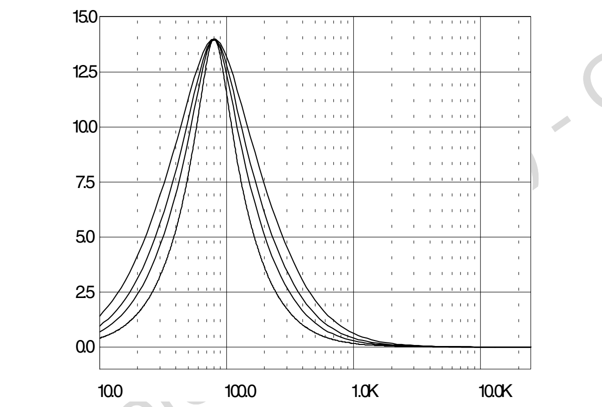
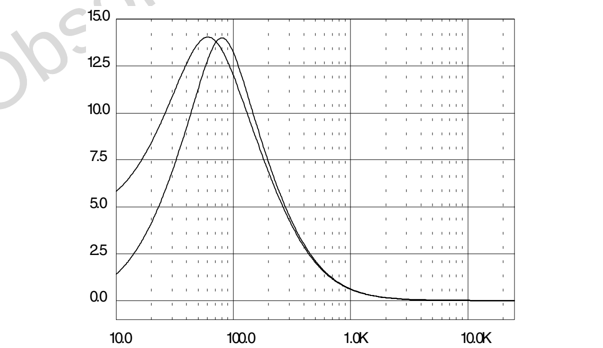


Figure 12. Bass normal and DC mode @ Gain = 14dB, fc = 80Hz



Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100Hz.

Figure 13. Mid control @ fc=1kHz, Q=1

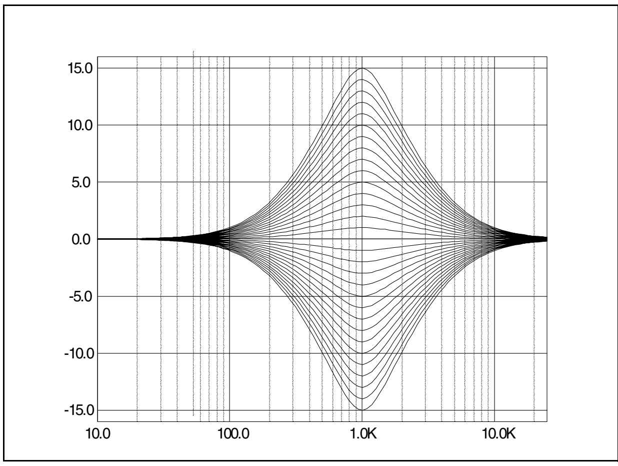


Figure 14. Mid center frequency @ Gain=14dB, Q1

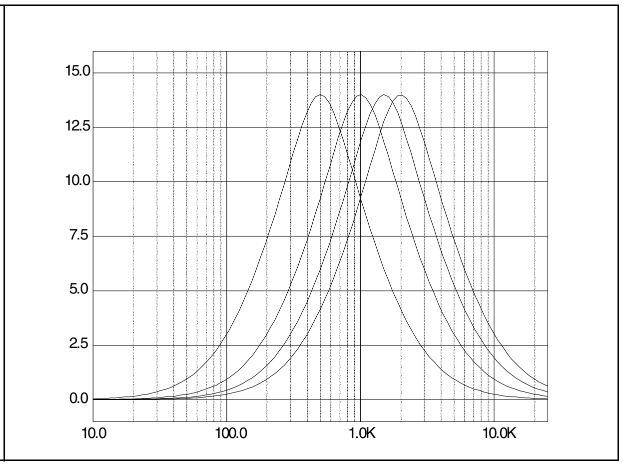


Figure 15. Mid Q factor @ fc=1kHz, Gain=14dB

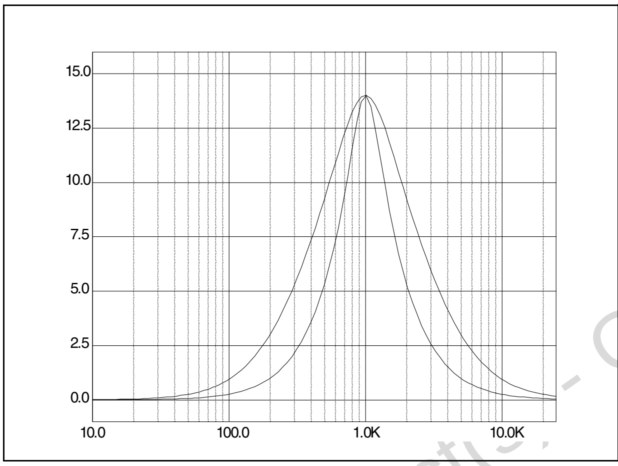


Figure 16. Treble control @ fc = 17.5KHz

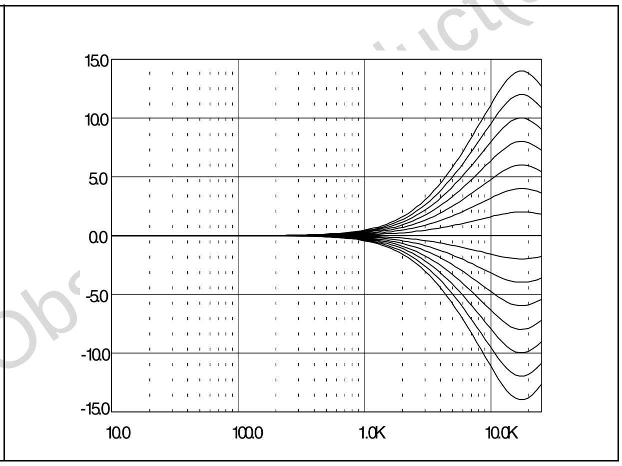


Figure 17. Treble center frequencies@ Gain = 14dB