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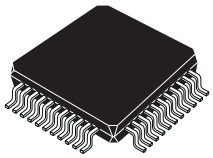
TDA7411

ADVANCED CAR SIGNAL PROCESSOR

- FULLY INTEGRATED SIGNAL PROCESSOR OPTIMIZED FOR CAR RADIO APPLICATIONS
- FULY PROGRAMMABLE BY I^2C BUS
- INCLUDES AUDIOPROCESSOR, STEREO-DECODER WITH NOISE BLAMKER AND MULTIPATH DETECTOR
- SOFTMUTE FUNCTION
- PROGRAMMABLE ROLL-OFF COMPENSATION
- NO EXTERNAL COMPONENTS



TQFP44
ORDERING NUMBER: TDA7411

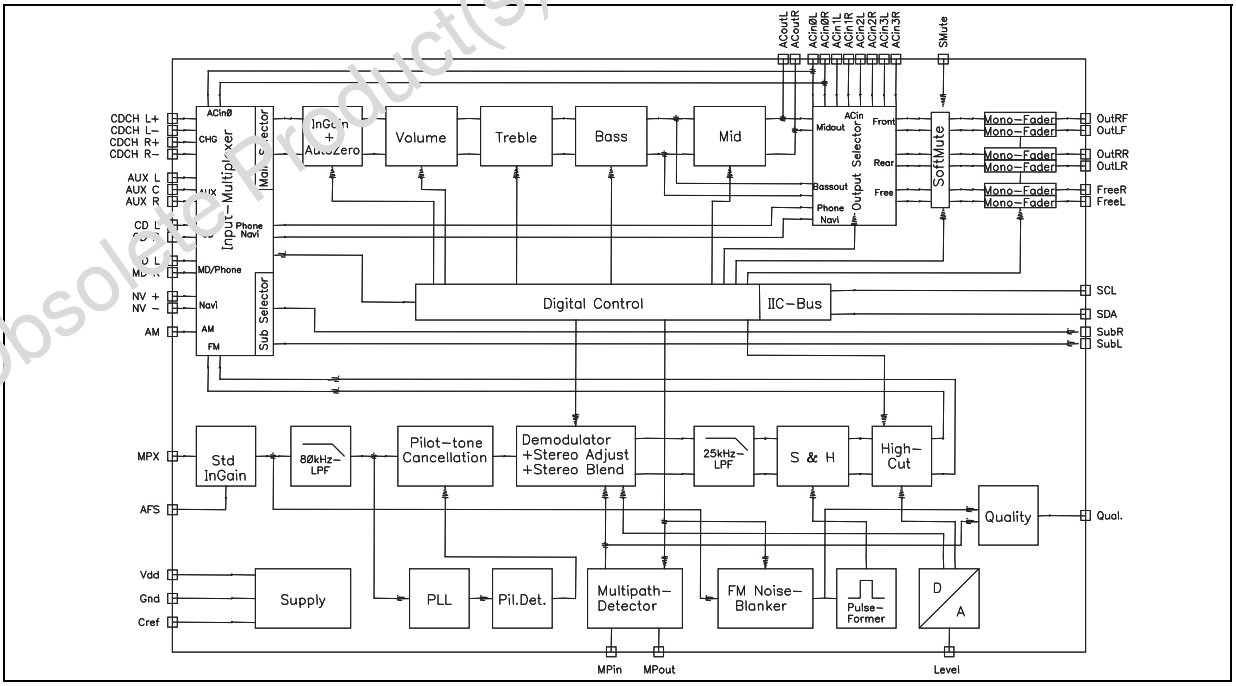
DESCRIPTION

The TDA7411 is the successor of the TDA7407 in the CSP family introduced by the TDA7460/61. It uses the same innovative concepts and design technologies allowing fully software programmability through I^2C bus and overall cost optimization for the system designer.

The device includes a three band audio processor with extended configurable input and output stages and absence of external components for filter settings, a last generation stereo decoder with multi path detector and a sophisticated stereo blend, high cut control and noise cancellation circuitry.

Strength points of the CSP approach are flexibility and overall cost/room saving in the application, combined with high performances.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature Range	-40 to 85	°C
T_{stg}	Operating Storage Temperature Range	-55 to 150	°C

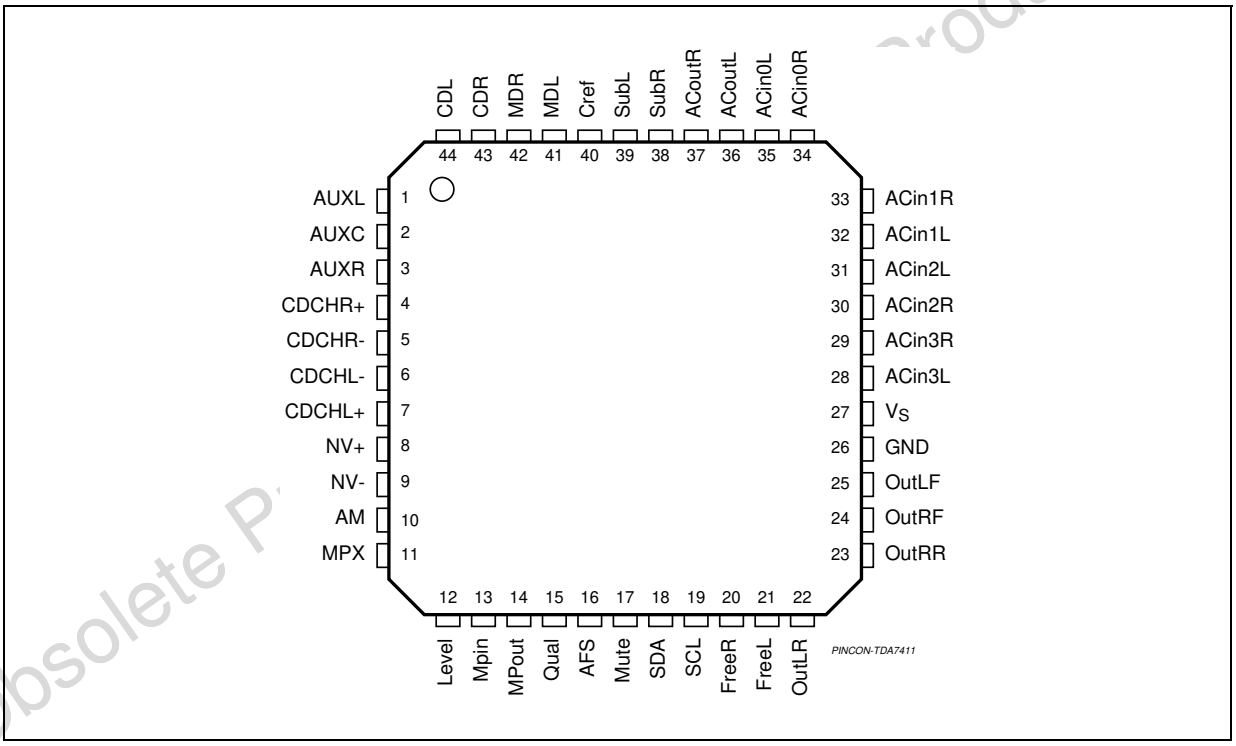
SUPPLY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		7.5	8	10	V
I_S	Supply Current	V_S = 9V		45		mA
SVRR	Ripple Rejection @ 1KHz	Audioprocessor (all filters flat)		60		dB
		Stereodecoder + Audioprocessor		55		dB

ESD

All pins are protected against ESD according to the MIL883 standard.

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\text{-}j\ pins}$	Thermal Resistance Junction to pins	Max	85	°C/W

PIN DESCRIPTION

Nr.	Name	Function	Type
1	**AUXL**	Quasi Differential Input Left	I
2	**AUXC**	Quasi Differential Input Common	I
3	**AUXR**	Quasi Differential Input Right	I
4	**CDCHR+**	Full Differential Input Right Plus	I
5	**CDCHR-**	Full Differential Input Right Minus (not used in quasi differential mode)	I
6	**CDCHL-**	Full Differential Input Left Minus (CDCHCom in Qdiff mode)	I
7	**CDCHL+**	Full Differential Input Left Plus	I
8	**NV+**	Mono Differential Input Plus	I
9	**NV-**	Mono Differential Input Minus	I
10	**AM**	AM Input	I
11	**MPX**	FM Stereo Decoder Input	I
12	**Level**	Level Input Stereo Decoder	I
13	**MPin**	Multi Path Input	I
14	**MPout**	Multi Path Output	O
15	**Qual**	Stereo Decoder Quality Output	O
16	**AFS**	Alternative Frequency Search Drive	I
17	**Mute**	Soft Mute Drive	I
18	**SDA**	I^2C Data Line	I/O
19	**SCL**	I^2C Clock Line	I
20	**FreeR**	Free Right Speaker Output	O
21	**FreeL**	Free Left Speaker Output	O
22	**OutLR**	Rear Left Speaker Output	O
23	**OutRR**	Rear Right Speaker Output	O
24	**OutRF**	Front Right Speaker Output	O
25	**OutLF**	Front Left Speaker Output	O
26	**GND**	Supply Ground	S
27	**VS**	Supply Voltage	S
28	**ACin3L**	Pre-speaker Input Three Left	I
29	**ACin3R**	Pre-speaker Input Three Right	I
30	**ACin2R**	Pre-speaker Input Two Right	I
31	**ACin2L**	Pre-speaker Input Two Left	I
32	**ACin1L**	Pre-speaker Input Three Left	I
33	**ACin1R**	Pre-speaker Input Three Right	I
34	**ACin0R**	Pre-speaker Input Zero Right	I
35	**ACin0L**	Pre-speaker Input Zero Left	I
36	**ACoutL**	Pre-speaker Output Left	O
37	**ACoutR**	Pre-speaker Output Right	O
38	**SubR**	Sub Channel Selector Output Right	O
39	**SubL**	Sub Channel Selector Output Left	O
40	**Cref**	Reference Capacitor Pin	O
41	**MDL**	Mini Disk Input Left	I
42	**MDR**	Mini Disk Input Right	I
43	**CDR**	Compact Disk Input Right (Test mode Output)	I
44	**CDL**	Compact Disk Input Left	I

Pin type legenda: I = Input ; O = Output; I/O = Input/Output; S = Supply; nc = not connected.

AUDIO PROCESSOR PART

Input Multiplexer

– full differential stereo input configurable as quasi-differential input
– quasi differential auxiliary stereo input
– mini disk stereo input configurable as mono differential input
– compact disk stereo input
– mono differential navigation input
– AM mono input
– second multiplexer for sub channel output

Volume control

– 1dB attenuator
– Max. gain 15dB
– Max. attenuation 79dB

Bass Control

– 2^{nd} order frequency response
– Center frequency programmable in 4(5) steps
– DC gain programmable
– ±15 x 1dB steps

Mid Control

– 2^{nd} order frequency response
– Center frequency programmable in 4 steps
– Q-factor programmable in 2 steps
– ±15 x 1dB steps

Treble Control

– 2^{nd} order frequency response
– Center frequency programmable in 4 steps
– ±15 x 1dB steps

Speaker Control

– 6 independent speaker controls in 1dB steps
– max. gain 15dB
– max. attenuation 79dB
– implemented soft mute capability
– speaker input multiplexer

Mute Functions

– independent direct fast mute controlled by I^2C interface
– independent soft mute for Front L/R, Rear and Free controlled by I^2C interface
– digitally controlled soft mute with 4 programmable mute-times
– pin controlled soft mute
soft mute monitor function @ Mute pin

ELECTRICAL CHARACTERISTICS

(V_S = 8V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SELECTOR						
R_{in}	Input Resistance	all inputs except Phone	70	100	130	KΩ
V_{CL}	Clipping Level	THD < 0.3%	1.6	1.7		V_{RMS}
S_{IN}	Input Separation		80	100		dB
$G_{IN\ MIN}$	Min. Input Gain		-0.5	0	0.5	dB
$G_{IN\ MAX}$	Max. Input Gain		14	15	16	dB
G_{STEP}	Step Resolution		0.5	1	1.5	dB
V_{DC}	DC Steps	Adjacent Gain Step	-5	0.5	5	mV
		G_{MIN} to G_{MAX}	-10	5	10	mV
FULL AND QUASI DIFFERENTIAL STEREO INPUT						
R_{in}	Input Resistance (see Figure 1)	Differential	70	100	130	KΩ
		Common Mode	70	100	130	KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1V_{RMS} @ 1KHz	45	70		dB
		V_{CM} = 1V_{RMS} @ 10KHz	45	60		dB
e_N	Output Noise @ Speaker Outputs	20Hz to 20KHz flat; all stages 0dB		9	15	μV
MONO DIFFERENTIAL INPUT (NV and MD in differential mode)						
R_{in}	Input Resistance	Differential	40	56		KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1V_{RMS} @ 1KHz	40	70		dB
		V_{CM} = 1V_{RMS} @ 10KHz	40	60		dB
VOLUME CONTROL						
G_{MAX}	Max Gain		14	15	16	dB
A_{MAX}	Max Attenuation		74	79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	G = -20 to +20dB	-1.25	0	+1.25	dB
		G = -60 to +20dB	-4	0	+3	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV
		From 0dB to GMIN		0.5	5	mV
SOFT MUTE/AFS						
A_{MUTE}	Mute Attenuation		80	100		dB
T_D	Delay Time	T1		0.24		ms
		T2		0.48		ms
		T3		10.1		ms
		T4		20.2		ms
$V_{TH\ low}$	Low Threshold for Mute/AFS-Pin[1]				1	V
$V_{TH\ high}$	High Threshold for SM -Pin			1.8		V
$V_{TH\ high}$	High Threshold for AFS -Pin			2.4		V
V_{SMon}	Monitor Voltage for SMon			2.4		V
R_{PD}	Internal Pull-up Resistor			100		KΩ
BASS CONTROL						
C_{RANGE}	Control Range		±13	±15	±17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB

ELECTRICAL CHARACTERISTICS (continued)
(V_S = 8V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_C	Center Frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100 (150)(2)	110	Hz
Q_{BASS}	Quality Factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
DC_{GAIN}	Bass-DC-Gain	DC = off	-1	0	1	dB
		DC = on	3.5	4.4	5.5	dB
MID CONTROL						
C_{RANGE}	Control Range		±13	±15	±17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
f_C	Center Frequency	f_{C1}	450	500	550	Hz
		f_{C2}	0.9	1	1.1	kHz
		f_{C3}	1.35	1.5	1.65	kHz
		f_{C4}	1.8	2	2.2	kHz
Q_{BASS}	Quality Factor	Q_1	0.9	1	1.1	
		Q_2	1.8	2	2.2	
TREBLE CONTROL						
G_{MAX}	Control Range		±13	±15	±17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
f_C	Center Frequency	f_{C1}	8	10	12	KHz
		f_{C2}	10	12.5	15	KHz
		f_{C3}	12	15	18	KHz
		f_{C4}	14	17.5	21	KHz
SPEAKER ATTENUATORS						
R_{in}	Impedance @ACin0,2,3		35	50	65	kΩ
R_{in}	Impedance @ACin1	R_{in1}	35	50	65	kΩ
		R_{in2}	28	40	52	kΩ
		R_{in3}	21	30	39	kΩ
G_{MAX}	Max. Gain		13	15	17	dB
A_{MAX}	Max. Attenuation		-74	-79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
A_{MUTE}	Output Mute Attenuation		80	90		dB
E_E	Attenuation Set Error				±2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps	-5	0.1	5	mV
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	1.6	1.8		V_{RMS}
R_L	Output Load Resistance		2			kΩ
C_L	Output Load Capacitance				10	nF

ELECTRICAL CHARACTERISTICS (continued)
(V_S = 8V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{OUT}	Output Impedance			30	120	Ω
V_{DC}	DC Voltage Level		3.8	4	4.2	V
GENERAL						
e_{NO}	Output Noise	BW = 20Hz - 20kHz				
		output muted		3	10	µV
		all gains = 0dB		6.5	15	µV
				6.5		µV
S/N	Signal to Noise Ratio	all gains = 0dB;flat; V_O = $2V_{RMS}$	102	110		dB
		bass, treble at +12dB; a-weighted; V_O = $2.6V_{RMS}$	96	100		dB
d	Distortion	all stages 0dB; Mono Diff Inputs, Vout = $0.75V_{RMS}$; All other inputs, V_{out} = $1V_{RMS}$		0.04	0.1	%
		V_{OUT}=$1V_{RMS}$; Bass & Treble = 12dB		0.05	0.15	%
S_C	Channel Separation L/R		80	100		dB
E_T	Total Tracking Error	A_V = 0 to -20dB	-1	0	1	dB
		A_V = -20 to -60dB	-2	0	2	dB
V_{POR}	Internal POR Voltage			3		V
BUS INPUTS						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	V_O = 1.6mA			0.4	V

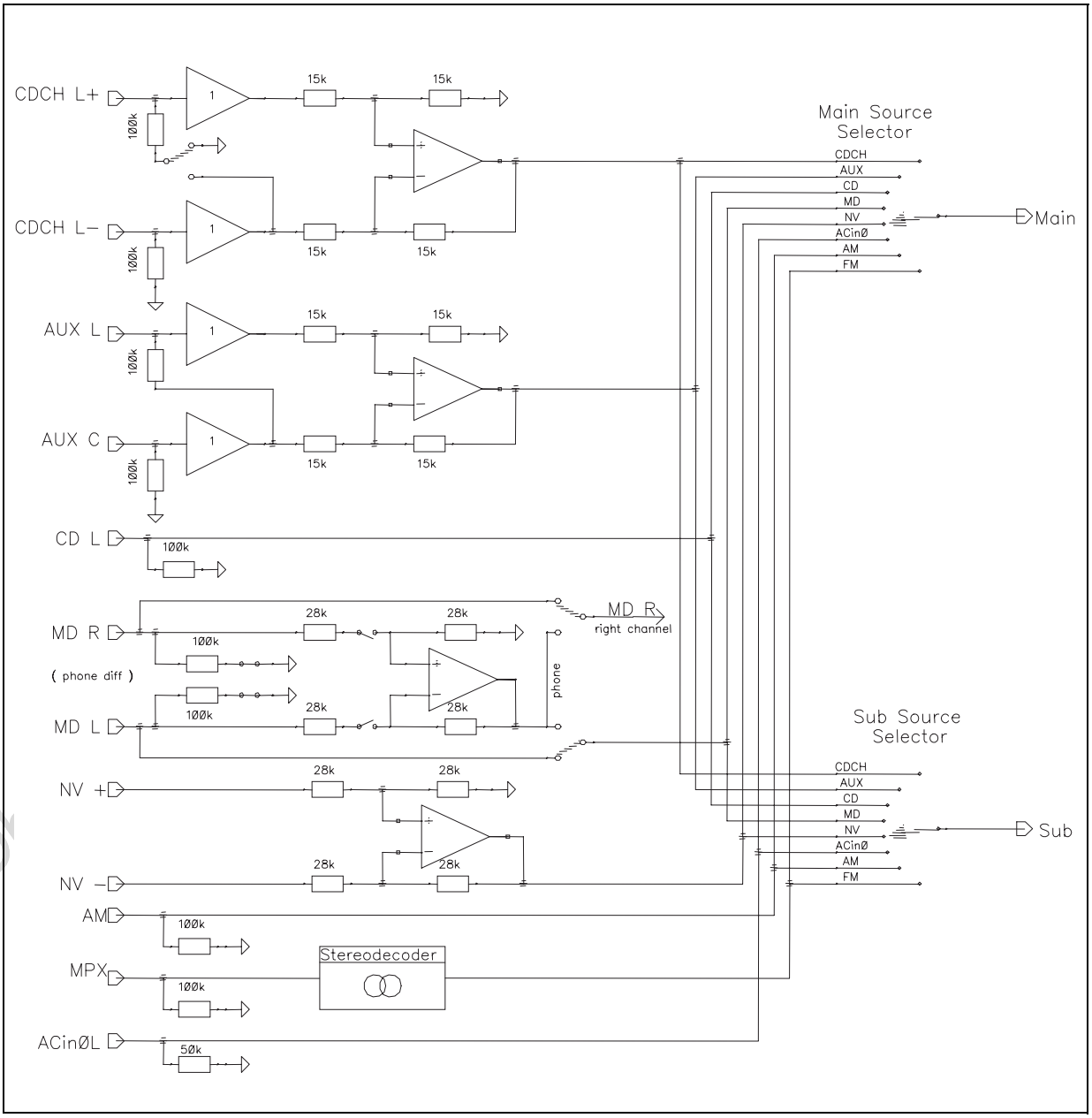
1) The SM and AFS pin are active low (Mute = 0)
2) See description of Audio processor Part section 1.8.

DESCRIPTION OF THE AUDIOPROCESSOR PART

Input Multiplexer

– CDCH full differential input configurable as quasi-differential input
– auxiliary quasi-differential input
– CD stereo
– MD stereo configurable as mono-differential phone input
– mono-differential NV input
– AM mono
– and stereo decoder input.

Figure 1. Input Selectors TDA7411

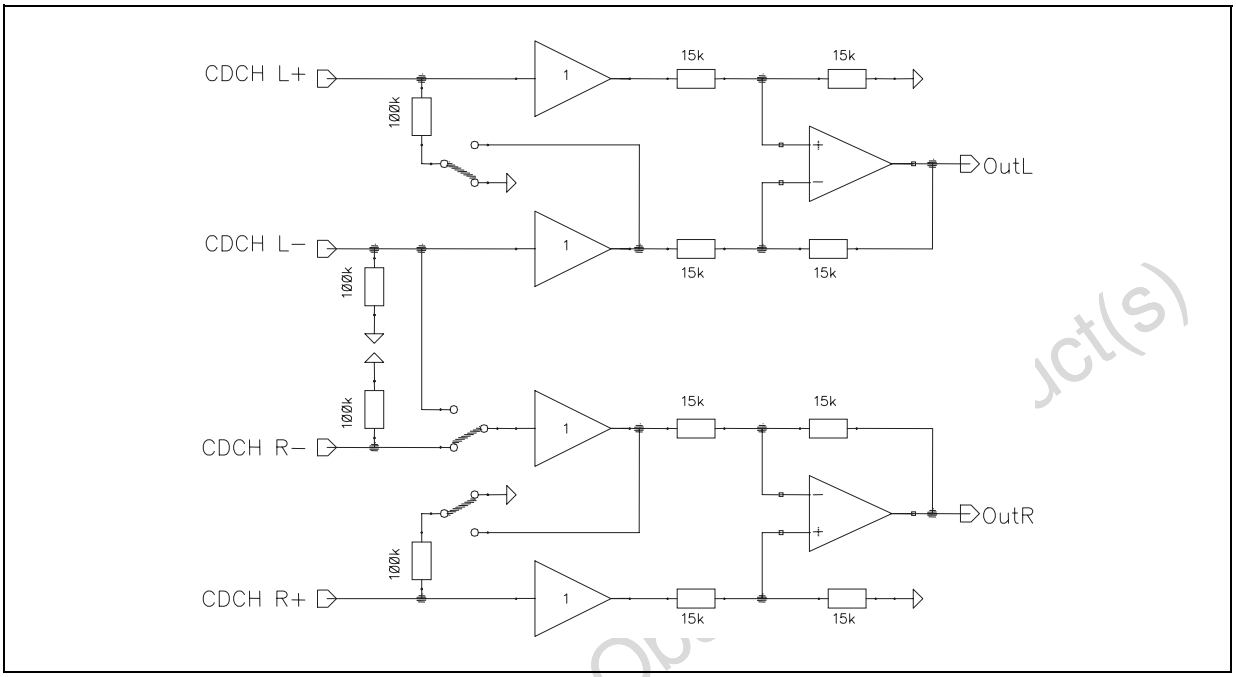


Input stages

In the basic configuration one full differential, one quasi-differential, two single ended stereo, one mono-differential and two tuner (AM and MPX) inputs are available. In addition the ac coupling input Acin0 can be used as single ended input for the input multiplexer.

The full-differential input can be switched into quasi-differential mode (see Fig. 2) and the MD single ended input can be used as mono-differential input (see Fig.1).

Figure 2. Full differential input



AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain-stage would be transferred or even amplified to the output. To avoid that effect a special Offset-cancellation-stage called AutoZero is implemented. This stage is located after the In-Gain-stage to eliminate all offsets generated by the stereo decoder, the Input-Stages and the In-Gain (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the DATA-BYTE 0 is selected and takes a time of max. 0.3ms. To avoid audible clicks the audio processor is muted before the tone control stage during this time.

AutoZero-Remain

In some cases, for example if the µP is executing a refresh cycle of the IIC-Bus-programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7411 could be switched in the **AutoZero-Remain-Mode** (Bit 6 of the sub address byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment-value remains.

Sub Channel Multiplexer

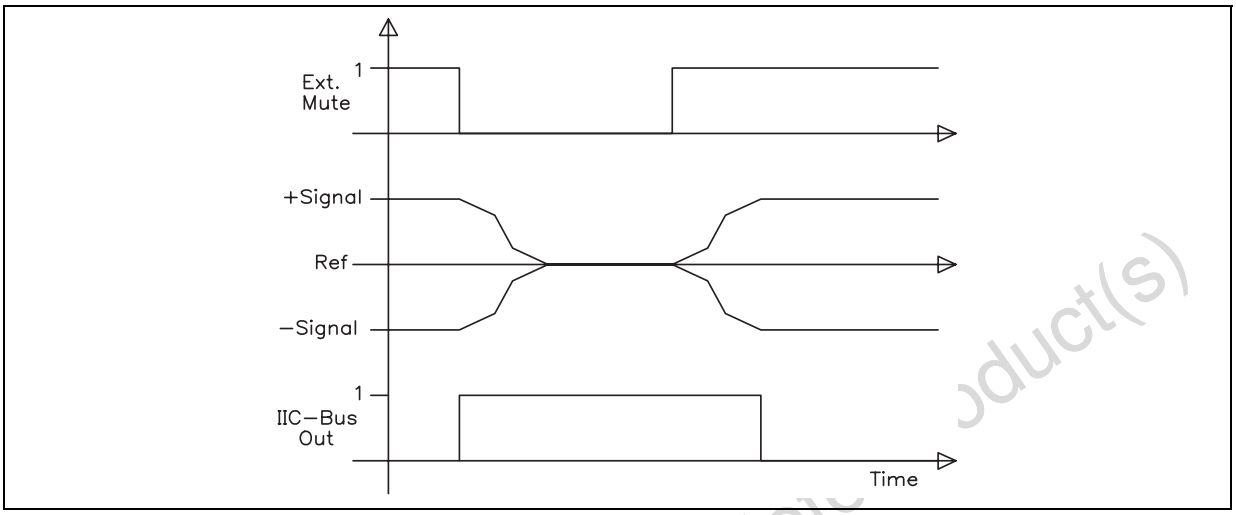
All input stages are available as source in the sub channel multiplexer. The selected source is buffered and available at the pins SubR, SubL.

Mute Capability of Audio Processor

The main channel and the sub channel of the TDA7411 can be muted after the Source selectors. This mute (no soft mute!) must be started by I^2C bus.

The digitally controlled SoftMute stages are placed in the speaker and allow muting/demuting of the signal with an I^2C-bus programmable slope. The mute process can either be activated by the SoftMute pin or by the I^2C-bus. The slope is realized in a special S-shaped curve to mute slowly in the critical regions (see Figure 3).

Figure 3. Soft mute-Timing



Note: Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal.

Using the IIC bus control the soft mute can be activated independently for FrontL, FrontR, Rear and Free. For timing purposes the Bit 3 of the I2C-bus output register is set to 1 as soon as the soft mute of any speaker is started until the end of demuting of all speakers. The Mute pin is able to work as monitor for the same signal. The standard function of the pin is not influenced by the monitor function.

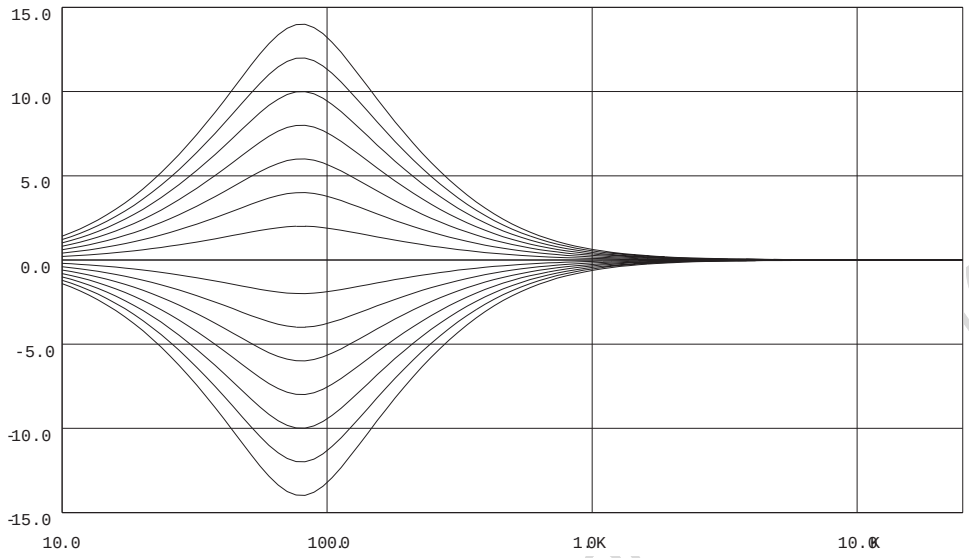
Bass

There are four parameters programmable in the bass stage:

Attenuation

Figure 4 shows the attenuation as a function of frequency at a center frequency of 80Hz.

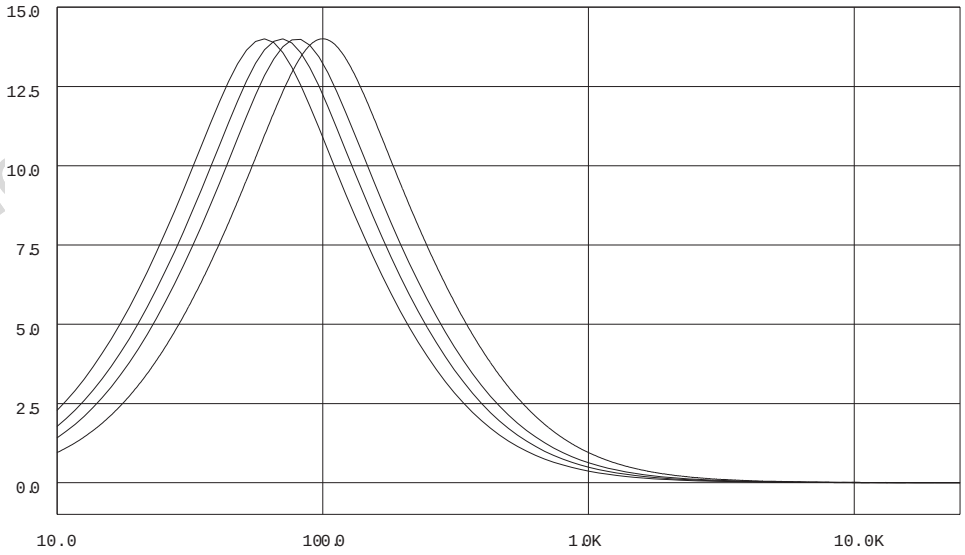
Figure 4. Bass Control @ f_C = 80Hz, Q = 1



Center Frequency

Figure 5 shows the four possible center frequencies 60, 70, 80 and 100Hz.

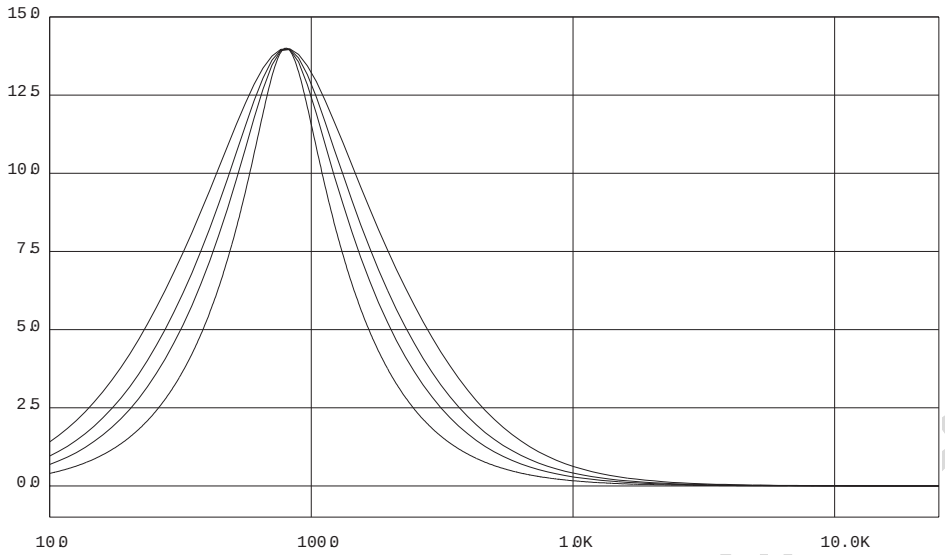
Figure 5.



Quality Factors

Figure 6 shows the four possible quality factors 1, 1.25, 1.5 and 2.

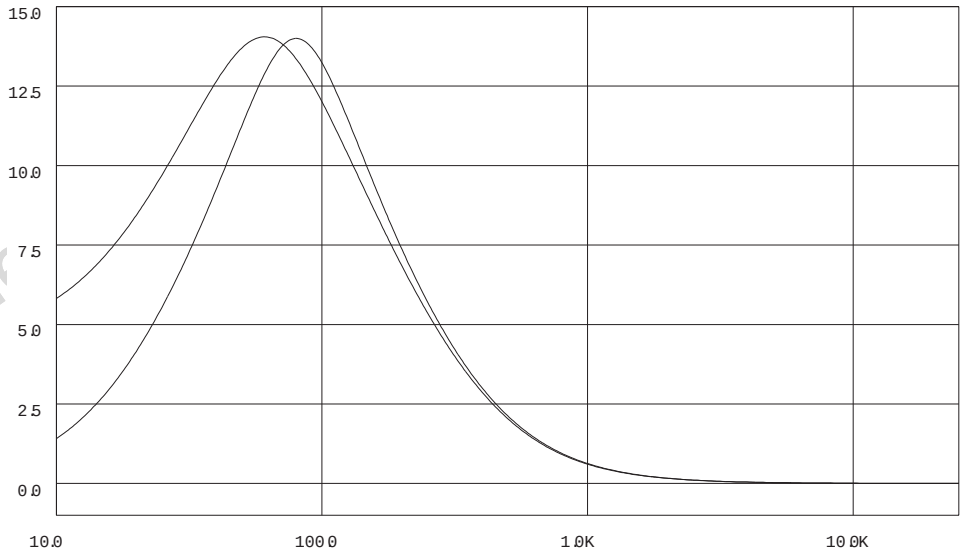
Figure 6. Bass Quality factors @ Gain = 14dB, f_C = 80Hz



DC Mode

In this mode the DC-gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25%, which can be used to reach alternative center frequencies or quality factors.

Figure 7. Bass normal and DC Mode @ Gain = 14dB, f_C = 80Hz



Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100Hz.

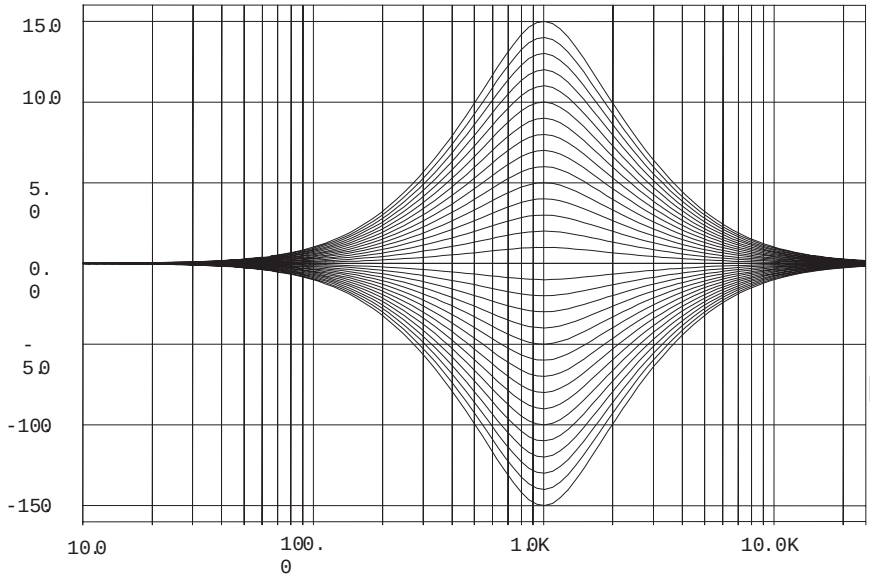
MID

There are 3 parameters programmable in the mid stage:

Attenuation

Figure 8 shows the attenuation as a function of frequency at a center frequency of 1kHz.

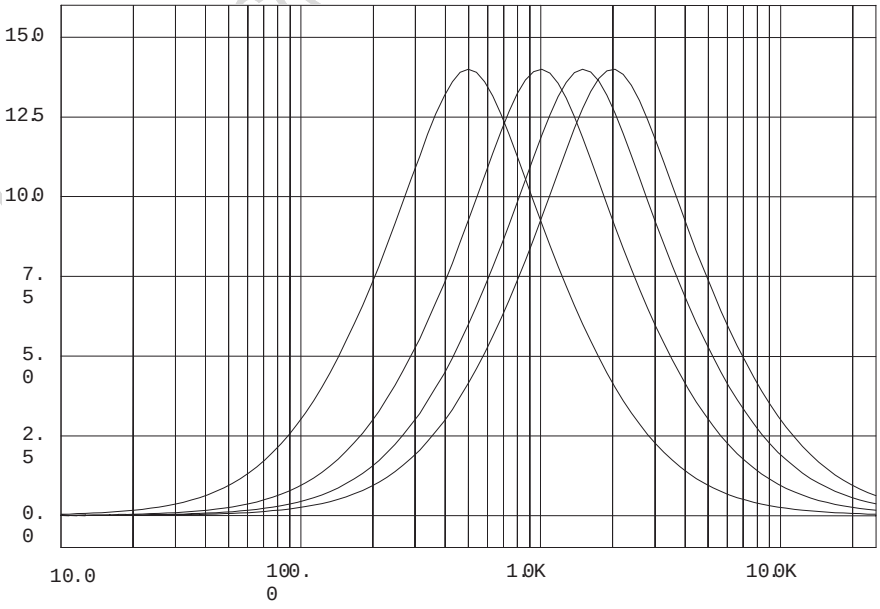
Figure 8. Mid Control @ f_C = 1kHz, Q = 1



Center Frequency

Figure 9 shows the four possible center frequencies 500Hz, 1kHz, 1.5kHz and 2kHz.

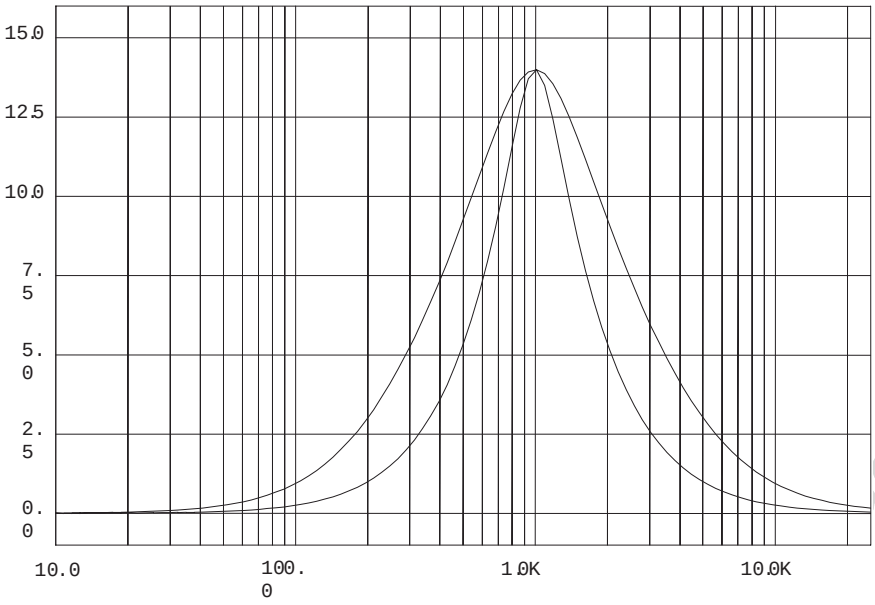
Figure 9.



Quality Factor

Figure 10 shows the two possible quality factors 1 and 2 at a center frequency of 1kHz.

Figure 10. Mid Q-factor @ f_C = 1kHz, Gain=14dB



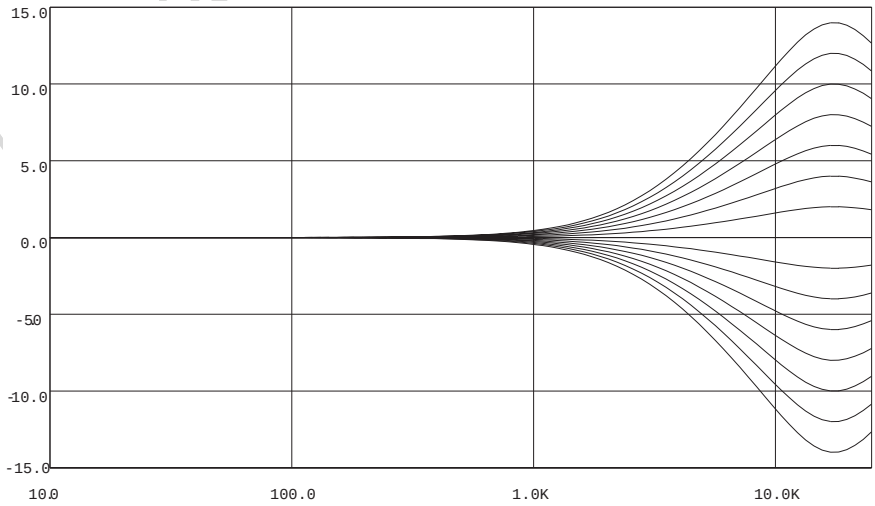
TREBLE

There are two parameters programmable in the treble stage:

Attenuation

Figure 11 shows the attenuation as a function of frequency at a center frequency of 17.5kHz.

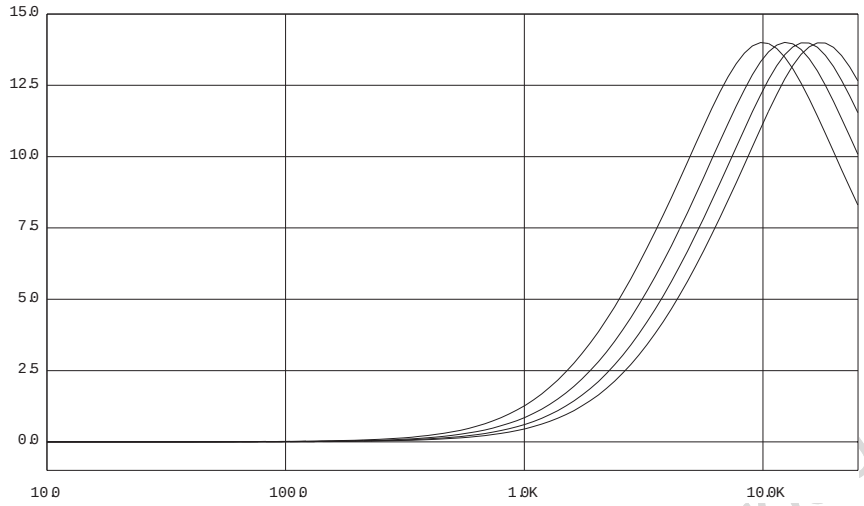
Figure 11. Treble Control @ f_C = 17.5kHz



Center Frequency

Figure 12 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5kHz.

Figure 12. Treble Center Frequencies @ Gain = 14dB



Speaker Coupling

In some applications additional signal manipulations are desired, for example surround-sound or more-band-equalizing. For this purpose an AC-Coupling with four different AC-Coupling inputs is placed before the speaker-attenuators.

The input-impedance of the AC-Inputs is always 50kΩ with exception of AC input ACin1, which has programmable input impedance. For ACin3 exists an internal mixing stage and an internal mono low pass filter, which is available as input only for the speaker FreeL/R.

There are two possibilities for internal DC Coupling:

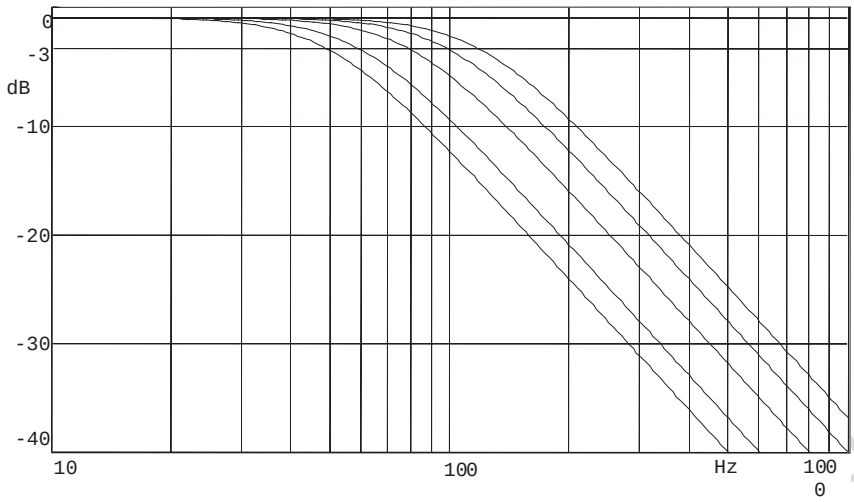
- main channel after the bass filter
- main channel after the middle filter (same as at ACout pin)

The I^2C bus programming tables shows the possible speaker sources.

Low Pass Filter

Figure 13 shows the five possible corner frequencies of the low pass filter:

Figure 13. Low Pass Corner Frequencies



Anti-Radiation-Filter

An Anti-Radiation-Filter is implemented to suppress the radiation at the SC-clock-frequency and its harmonics. This radiation is only present if the stereo decoder is selected and/or SC-Filters are active (<>0dB). If not, the filter can be switched off in order to optimize the noise-performance.

Speaker Attenuator

The speaker-attenuators have exactly the same control range like the Volume-stage. Every stereo speaker stage has an implemented independently I^2C controlled and Mute pin controlled SoftMute stage (see section mute capability of AP).

STEREODECODER PART

Features:

– no external components necessary
– PLL with adjustment free, fully integrated VCO
– automatic pilot dependent MONO/STEREO switching
– very high suppression of intermodulation and interference
– programmable Roll-Off compensation
– dedicated RDS-Soft mute
– High cut- and Stereo blend-characteristics programmable in a wide range
– internal Noise blanker with several threshold controls
– alternative frequency search function
– Multipath-detector with programmable internal/external influence
– I^2C-bus control of all necessary functions

.

ELECTRICAL CHARACTERISTICS

(V_S = 8V; deemphasis time constant = 50µs,V_{MPX} = 500mV(75KHz deviation), fm= 1KHz, Gv = 6dB, T_{amb} = 27°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{in}	MPX Input Level	G_v = 3.5dB		0.5	1.25	V_{RMS}
R_{in}	Input Resistance		70	100	130	KΩ
G_{MIN}	Min. Input Gain		1.5	3.5	4.5	dB
GMAX	Max. Input Gain		8.5	11	12.5	dB
GSTEP	Step Resolution		1.75	2.5	3.25	dB
SVRR	Supply Voltage Ripple Rejection	Vripple = 100mV; f = 1KHz	35	60		dB
α	Max. channel Separation		30	50		dB
THD	Total Harmonic Distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus Noise to Noise Ratio	A-weighted, S = $2V_{RMS}$	80	91		dB
MONO/STEREO-SWITCH						
V_{PTHST1}	Pilot Threshold Voltage	for Stereo, PTH = 1	10	15	25	mV
V_{PTHST0}	Pilot Threshold Voltage	for Stereo, PTH = 0	15	25	35	mV
V_{PTHMO1}	Pilot Threshold Voltage	for Mono, PTH = 1	7	12	17	mV
V_{PTHMO0}	Pilot Threshold Voltage	for Mono, PTH = 1	10	19	25	mV
PLL						
Δf/f	Capture Range		0.5			%
DEEMPHASIS and HIGHCUT						
t_{HC50}	Deemphasis Time Constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCH}	25	50	75	µs
t_{HC75}	Deemphasis Time Constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCH}	50	75	100	µs
t_{HC50}	Highcut Time Constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCL}	100	150	200	µs
t_{HC75}	Highcut Time Constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCL}	150	225	300	µs

ELECTRICAL CHARACTERISTICS (continued)
(V_S = 8V; deemphasis time constant = 50µs,V_{MPX} = 500mV(75KHz deviation), fm= 1KHz, Gv = 6dB, T_{amb} = 27°C; unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
STEREOBLEND-and HIGHCUT-CONTROL						
REF5V	Internal Reference Voltage		4.7	5	5.3	V
T_{CREF5V}	Temperature Coefficient			3300		ppm
L_{Gmin}	Min. LEVEL Gain		-1	0	1	dB
L_{Gmax}	Max. LEVEL Gain		8	10	12	dB
L_{Gstep}	LEVEL Gain Step Resolution		0.3	0.67	1	dB
$VSBL_{min}$	Min. Voltage for Mono		25	29	33	%REF5V
$VSBL_{max}$	Min. Voltage for Mono		54	58	62	%REF5V
$VSBL_{step}$	Step Resolution		2.2	4.2	6.2	%REF5V
$VHCH_{min}$	Min. Voltage for NO Highcut		38	42	46	%REF5V
$VHCH_{max}$	Min. Voltage for NO Highcut		62	66	70	%REF5V
$VHCH_{step}$	Step Resolution		5	8.4	12	%REF5V
$VHCL_{min}$	Min. Voltage for FULL Highcut		12	17	22	%VHCH
$VHCL_{max}$	Max. Voltage for FULL Highcut		28	33	38	%VHCH
$VHCL_{step}$	Step Resolution		2.2	4.2	6.2	%VHCH
Carrier and harmonic suppression at the output						
α19	Pilot Signal f = 19KHz		40	50		dB
α38	Subcarrier f = 38KHz				75	dB
α57	Subcarrier f = 57KHz				62	dB
α76	Subcarrier f = 76KHz				90	dB
Intermodulation (Note 1)						
α2	f_{mod} = 10KHz, f_{spur} = 1KHz				65	dB
α3	f_{mod} = 13KHz, f_{spur} = 1KHz				75	dB
Traffic Ratio (Note 2)						
α57	Signal f = 57KHz				70	dB
SCA - Subsidiary Communications Authoorization (Note 3)						
α67	Signal f = 67KHz				75	dB
ACI - Adjacent Channel Interference (Note 4)						
α114	Signal f = 114KHz				95	dB
α190	Signal f = 190KHz				84	dB

Notes to the characteristics:

1. Intermodulation Suppression:

$$\alpha 2 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz)}} ; f_s = (2 \times 10kHz) - 19kHz$$

$$\alpha 3 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz)}} ; f_s = (3 \times 13kHz) - 38kHz$$

measured with: 91% pilot signal; fm = 10kHz or 13kHz.

2. Traffic Radio (V.F.) Suppression: measured with: 91% stereo signal; 9% pilot signal; fm=1kHz; 5% sub-

carrier (f = 57kHz, fm = 23Hz AM, m = 60%)

$$\alpha 57(V.W > F.) = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at1kHz \pm 23kHz)}}$$

3. SCA (Subsidiary Communications Authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1kHz; 10%SCA - subcarrier (fs = 67kHz, unmodulated).

$$\alpha 67 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at9kHz)}} ; F_s = (2 \times 38kHz) - 67kHz$$

4. ACI (Adjacent Channel Interference):

$$\alpha 114 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at4kHz)}} ; F_s = 110kHz - (3 \times 38kHz)$$

$$\alpha 114 = \frac{V_{O(signal)(at1kHz)}}{V_{O(spurious)(at4kHz)}} ; F_s = 186kHz - (5 \times 38kHz)$$

measured with: 90% mono signal; 9% pilot signal; fm =1kHz; 1% spurious signal(fs = 110kHz or 186kHz, unmodulated).

NOISE BLANKER PART

Features:

– internal 2nd order 140kHz high-pass filter
– programmable trigger threshold
– trigger threshold dependent on high frequency noise with programmable gain
– additional circuits for deviation- and fieldstrength-dependent trigger adjustment
– very low offset current during hold time due to opamps with MOS inputs
– 4 selectable pulse suppression times
– programmable noise rectifier charge/discharge current

ELECTRICAL CHARACTERISTICS (continued)

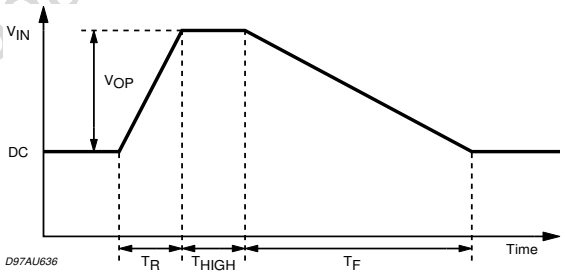
Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger Threshold [0) 1)]	meas. with V_{PEAK} = 0.9V	NBT = 111	(c)	30	(c)	mV_{OP}
			NBT = 110	(c)	35	(c)	mV_{OP}
			NBT = 101	(c)	40	(c)	mV_{OP}
			NBT = 100	(c)	45	(c)	mV_{OP}
			NBT = 011	(c)	50	(c)	mV_{OP}
			NBT = 010	(c)	55	(c)	mV_{OP}
			NBT = 001	(c)	60	(c)	mV_{OP}
			NBT = 000	(c)	65	(c)	mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger Threshold [2)]	meas. with V_{PEAK} = 1.5V	NCT = 00	(c)	260	(c)	mV_{OP}
			NCT = 01	(c)	220	(c)	mV_{OP}
			NCT = 10	(c)	180	(c)	mV_{OP}
			NCT = 11	(c)	140	(c)	mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV	NRD [6)] = 00	0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 200mV; f = 150KHz			3.5		V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
$V_{RECT\ DEV}$	deviation dependent rectifier Voltage 3)	means. with V_{MPX} = 500mV (75KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	V_{OP}
			OVD = 10	0.9	1.2	1.5	V_{OP}
			OVD = 01	1.7	2.0	2.3	V_{OP}
			OVD = 00	2.5	2.8	3.1	V_{OP}
$V_{RECT\ FS}$	Fieldstrength Controlled Rectifier Voltage 4)	means. with V_{MPX} = 0mV $V_{LEVEL} << V_{SBL}$ (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	0.9	1.4	1.5	V
			FSC = 01	1.7	1.9	2.3	V
			FSC = 00	2.1	2.4	3.1	V
T_S	Suppression Pulse Duration 5)	Signal HOLDNin Testmode	BLT = 00		38		µs
			BLT = 10		32		µs
			BLT = 01		25.5		µs
			BLT = 00		22		µs
$V_{RECTADJ}$	Noise Rectifier discharge adjustment 6)	Signal PEAK in Testmode	NRD = 00 6)	(c)	0.3	(c)	V/ms
			NRD = 01 6)	(c)	0.8	(c)	V/ms
			NRD = 10 6)	(c)	1.3	(c)	V/ms
			NRD = 11 6)	(c)	2.0	(c)	V/ms
SR_{PEAK}	Noise Rectifier Charge	Signal PEAK in Testmode	PCH = 0 7)	(c)	10	(c)	mV/µs
			PCH = 1 7)	(c)	20	(c)	mV/µs
V_{ADJMP}	Noise Rectifier adjustment through Multipath 8)	Signal PEAK in Testmode	MPNB = 00 8)	(c)	0.3	(c)	V/ms
			MPNB = 01 8)	(c)	0.5	(c)	V/ms
			MPNB = 10 8)	(c)	0.7	(c)	V/ms
			MPNB = 11 8)	(c)	0.9	(c)	V/ms

(c) = by design/characterization functionally guaranteed through dedicated test mode structure
0) All Thresholds are measured using a pulse with TR =2µs, TH_{IGH} = 2µs and T_F = 10µs. The repetition rate must not increase the PEAK voltage.

Figure 14. Timing



1) NBT represents the Noiseblanker Byte bits D_2, D_0 for the noise blanker trigger threshold
2) NAT represents the Noiseblanker Byte bit pair D_4, D_3 for the noise controlled triggeradjustment
3) OVD represents the Noiseblanker Byte bit pair D_7, D_6 for the over deviation detector
4) FSC represents the Fieldstrength Byte bit pair D_1, D_0 for the fieldstrength control
5) BLT represents the Speaker RR Byte bit pair D_7, D_6 for the blanktime adjustment
6) NRD represents the Configuration-Byte bit pair D_1, D_0 for the noise rectifier discharge-adjustment
7) PCH represents the Stereodecoder-Byte bit D_5 for the noise rectifier charge-current adjustment
8) MPNB represents the HighCut-Byte bit D_7 and the Fieldstrength-Byte D_7 for the noise rectifier multipath adjustment

Figure 15. Trigger Threshold vs. V_{PEAK}

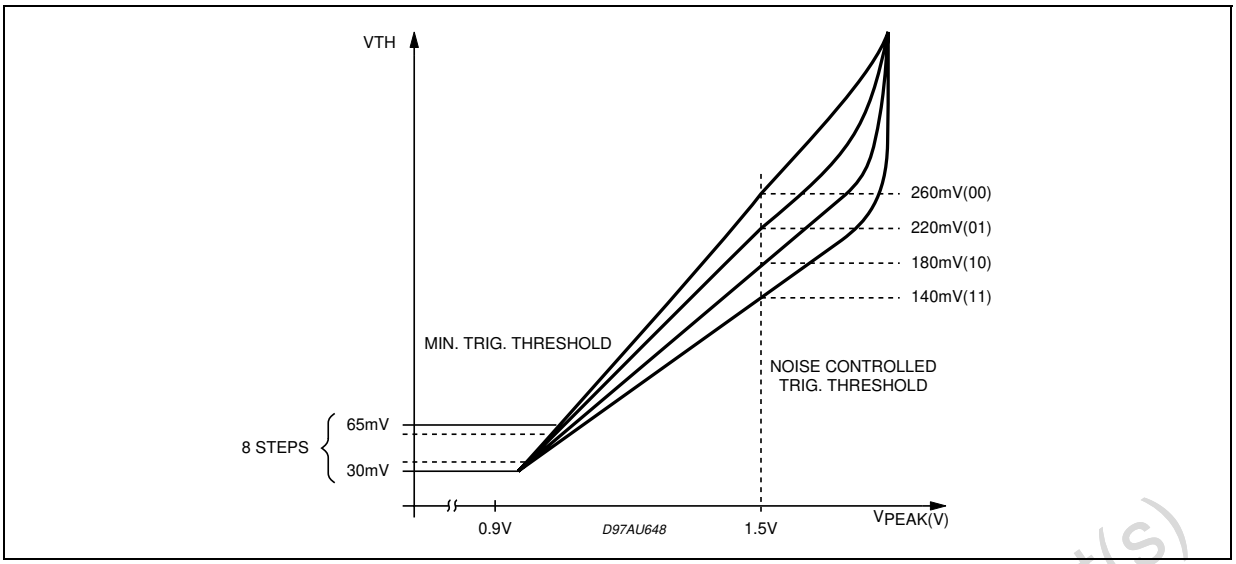


Figure 16. Deviation Controlled Trigger Adjustment

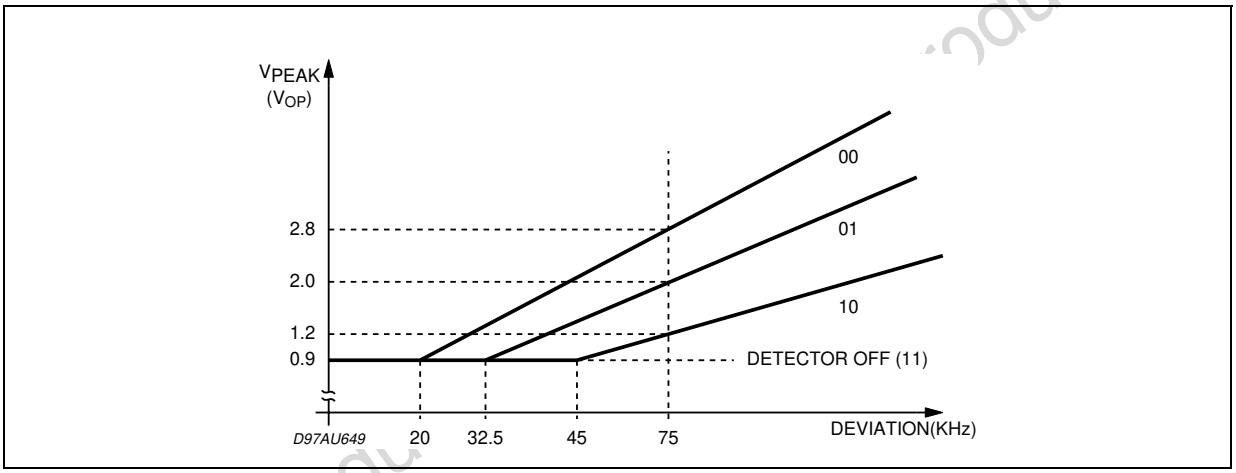
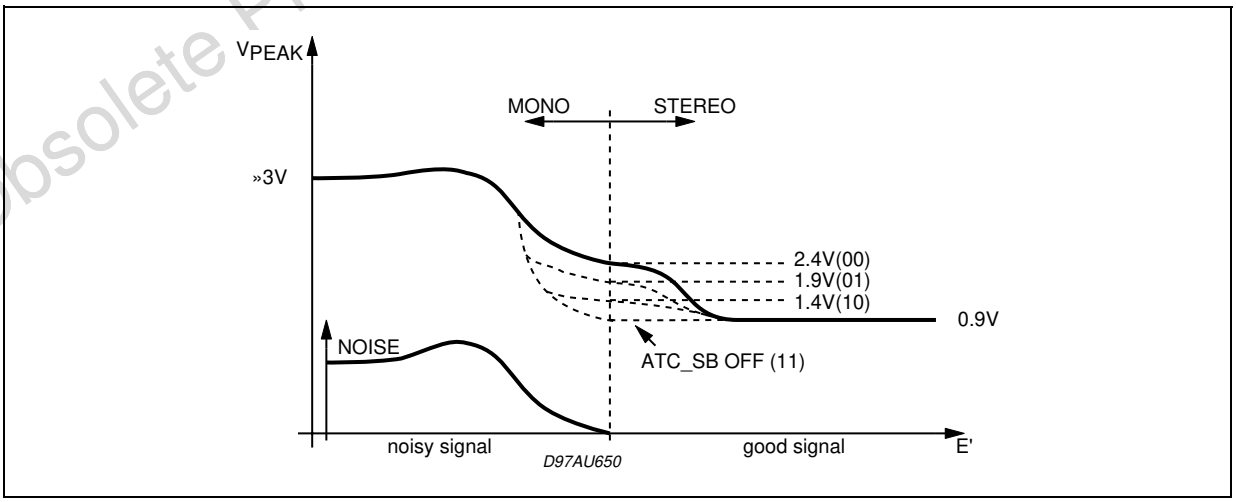


Figure 17. Field strength Controlled Trigger Adjustment



MULTIPATH DETECTOR

Features:

– internal 19kHz band-pass filter
– programmable band-pass and rectifier gain
– two pin solution fully independent usable for external programming
– selectable internal influence on Stereoblend

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CMP}	Center frequency of Multipath-Bandpass	stereo decoder locked on Pilot tone		19		kHz
G_{BPMP}	Band pass Gain	bits D_2, D_1 configuration byte = 00		6		dB
		bits D_2, D_1 configuration byte = 01		12		dB
		bits D_2, D_1 configuration byte = 10		16		dB
		bits D_2, D_1 configuration byte = 11		18		dB
G_{RECTMP}	Rectifier Gain	bits D_7, D_6 configuration byte = 00		7.6		dB
		bits D_7, D_6 configuration byte = 01		4.6		dB
		bits D_7, D_6 configuration byte = 10		0		dB
		bits D_7, D_6 configuration byte = 11		off		
I_{CHMP}	Rectifier Charge Current	bit D_5, configuration byte = 0 bit D_5, configuration byte = 1		0.2 0.4		µA
I_{DISMP}	Rectifier Discharge Current		0.5	1	1.5	mA

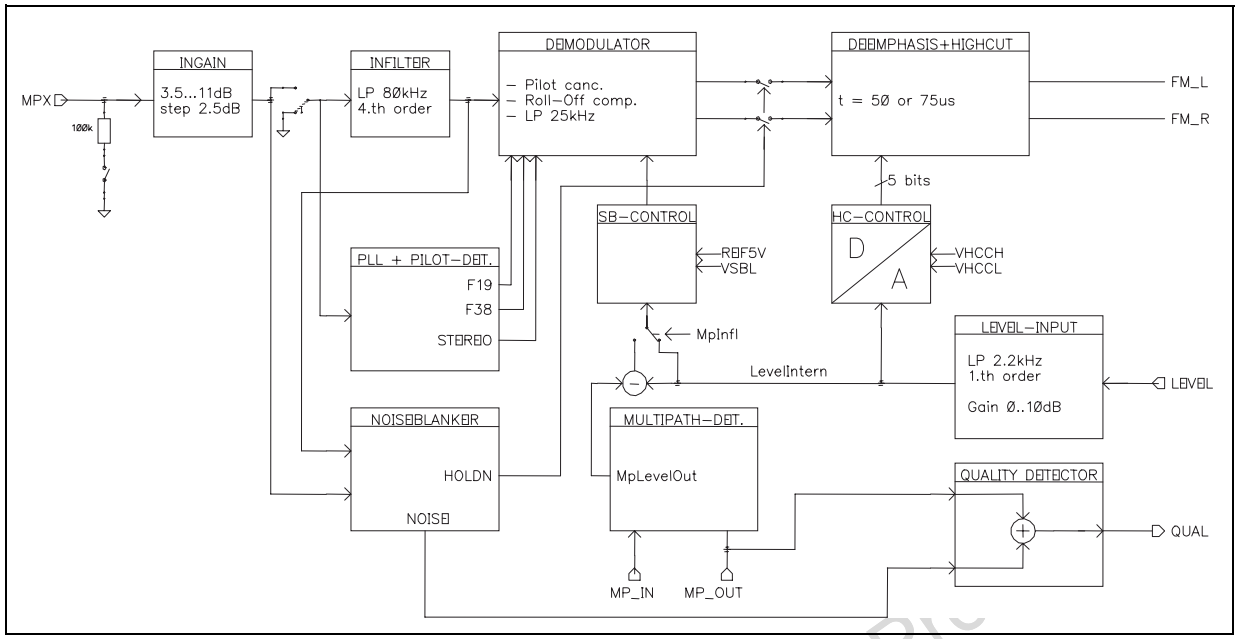
QUALITY DETECTOR

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
A	Multipath Influence Factor	Addr12 / Bit 5+6	00 01 10 11		0.2 0.3 0.4 0.5		dB dB dB dB
A	Noise Influence Factor	Addr16 / Bit 1+2	00 01 10 11		15 12 9 6		dB dB dB dB

FUNCTIONAL DESCRIPTION OF STERO DECODER

Figure 18. Block diagram of the stereo decoder



The stereo decoder-part of the TDA7411 (see Fig. 18) contains all functions necessary to demodulate the MPX-signal like pilot tone-dependent MONO/STEREO-switching as well as "stereoblend" and "highcut". Adaptations like programmable input gain, roll-off compensation, selectable deemphasis time constant and a programmable field strength input allow using different IF-devices.

InGain + Infilter

The InGain stage allows adjusting the MPX-signal to a magnitude of about 1Vrms internally, which is the recommended value. The 4.th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and noise and acts as an anti-aliasing filter for the following switch capacitor filters.

Demodulator

In the demodulator block the left and the right channel are separated from the MPX-signal. In this stage also the 19-kHz pilot tone is canceled. For reaching a high channel separation the TDA7411 offers an I2C-bus programmable roll-off adjustment, which is able to compensate the low pass behavior of the tuner section. If the tuner's attenuation at 38kHz is in a range from 13.8% to 24.6% the A673 needs no external network in front of the MPX-pin. Within this range an adjustment to obtain at least 40dB channel separation is possible. The bits for this adjustment are located together with the field strength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the car radio where the channel separation and the field strength control are trimmed. The setup of the stereoblend characteristics, which is programmable in a wide range.

Deemphasis and Highcut

The deemphasis low pass allows to choose between a time constant of 50µs and 75µs (bit D7, stereo decoder byte). The highcut control range will be in both cases $\tau_{HC} = 2x\ \tau_{Deemp}$. Inside the highcut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5-bit word, which controls the low pass time constant between τ_{Deemp}...$3x\ \tau_{Deemp}$. Thereby the resolution will remain always 5 bits indepen-

dently of the absolute voltage range between the VHCH- and VHCL-values.
The highcut function can be switched off by I2C-bus (bit D7, Field strength byte set to "0").
The setup of the highcut characteristics is described in 2.9.

PLL and Pilot tone-Detector

The PLL has the task to lock on the 19kHz pilot tone during a stereo-transmission to allow a correct demodulation. The included pilot tone-detector enables the demodulation if the pilot tone reaches the selected pilot tone threshold V_{PTHST}. Two different thresholds are available. By reading the status byte of the A673 via I^2C-bus the detector output (signal STEREO, see block diagram) can be checked.

Field Strength Control

The field strength input is used to control the highcut- and the stereoblend-function. In addition the signal can be also used to control the noise blanker thresholds and as input for the multipath detector.

LEVEL-Input and -Gain

To suppress undesired high frequency modulation on the highcut- and stereoblend-function the LEVEL signal is low pass filtered firstly. The filter is a combination of a 1.st-order RC-low pass at 53kHz (working as anti-aliasing filter) and a 1.st-order switched capacitor low pass at 2.2kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF-devices (see test mode section 5: LEVELINTERN). The gain is widely programmable in 16 steps from 0dB to 10dB (step=0.67dB). These 4 bits are located together with the Roll-Off bits in the "Stereo decoder-Adjustment"-byte to simplify a possible adaptation during the production of the car radio.

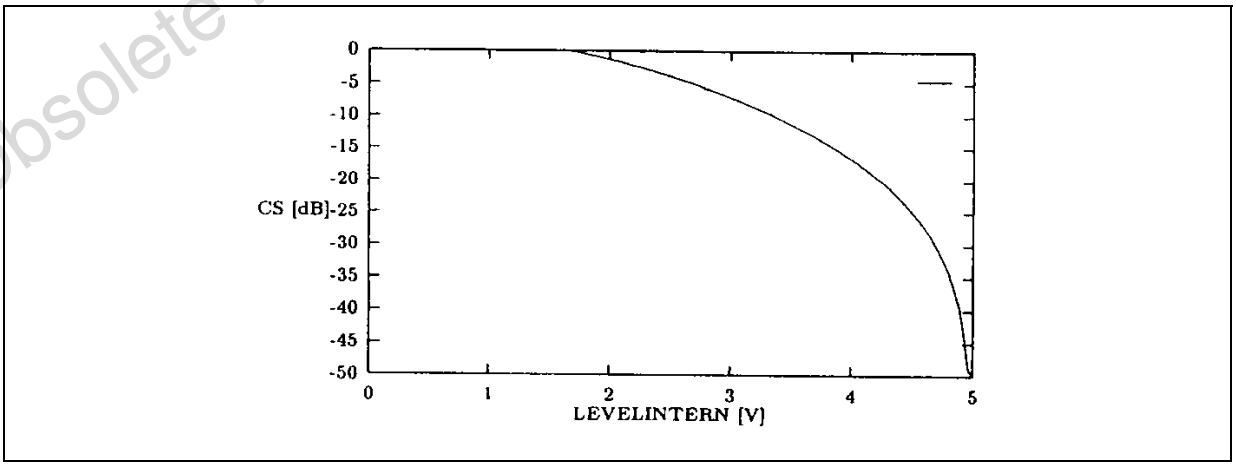
Stereoblend Control

The stereoblend control block converts the internal LEVEL-voltage (LEVELINTERN) into a demodulator compatible analog signal, which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit, which is the internal reference voltage REF5V. The lower limit can be programmed between 29.2 and 58% of REF5V in 4.167% steps (see figs.19, 20).

To adjust the external LEVEL-voltage to the internal range two values must be defined: the LEVEL gain L_G and VSBL (see fig. 20). To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain LG has to be defined. The following equation can be used to estimate the gain:

$$L_G = \frac{REF5V}{\text{Field strenght voltage [STEREO]}}$$

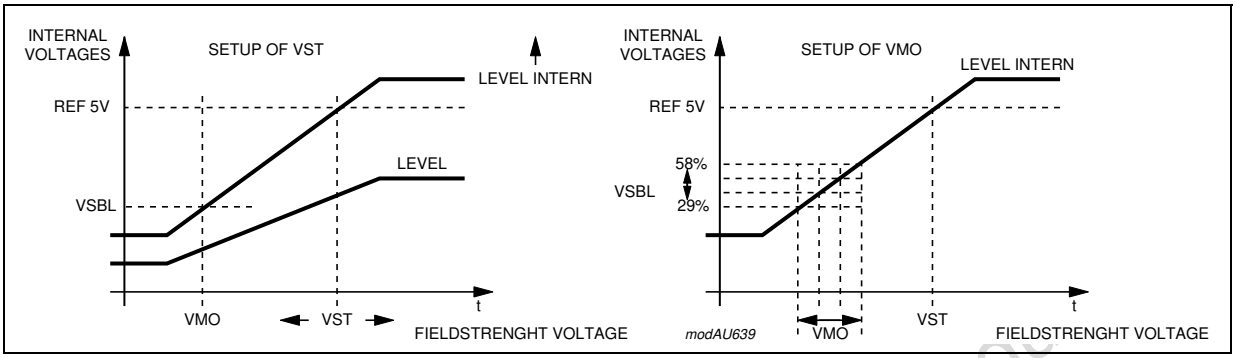
Figure 19. Internal stereo blend characteristics



The gain can be programmed through 4 bits in the "Stereo Decoder Adjustment"-byte. The MONO-voltage VMO (0dB channel separation) can be chosen selecting VSBL.

All necessary internal reference voltages like REF5V are derived from a bandgap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated. But most of the IF-devices are applying a LEVEL-voltage with a TC of 3300ppm. The A673 offers this TC for the reference voltages, too. The TC is selectable with bit D_7 of the "stereo decoder adjustment"-byte.

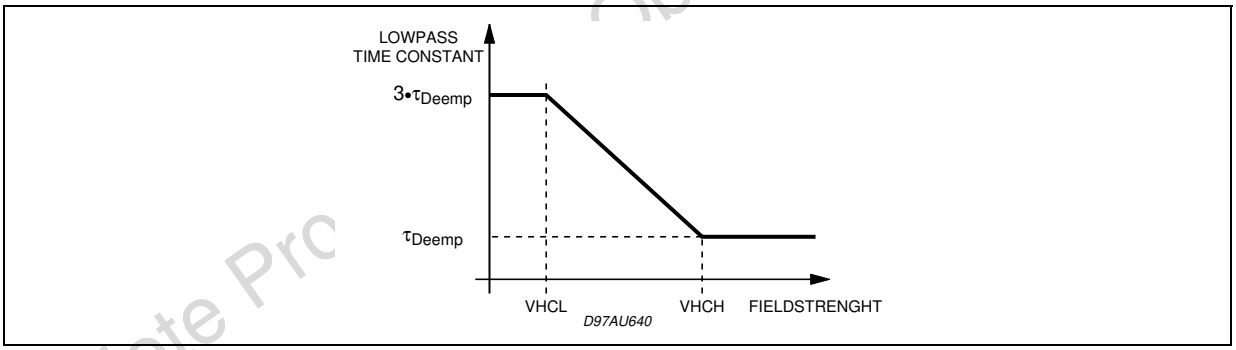
Figure 20. Relation Between Internal and External LEVEL Voltages and Setup of Stereoblend



Highcut Control

The highcut control set-up is similar to the stereoblend control set-up: the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17, 22, 28 or 33% of VHCH (see fig. 21).

Figure 21. High cut characteristics



Functional Description of the Noise Blanker

In the automotive environment spikes produced by the ignition and for example the wiper-motor disturb the MPX-signal. The aim of the noise blanker part is to cancel the audible influence of the spikes. Therefore the output of the stereo decoder is held at the actual voltage for a time between 22 and 38µs (programmable). The block diagram of the noise blanker is given in fig.22