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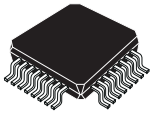
TDA7417

Car radio audio processor

Features

- Input Multiplexer
  - QD: quasi-differential stereo inputs
  - FD: full-differential stereo inputs
  - Mono: Mono input
  - SE1: stereo single-ended input
  - SE2: stereo single-ended input
  - In-Gain 0 to 15dB, 1dB step
  - internal offset-cancellation (AutoZero)
- IN/OUT control
  - Selectable full-differential stereo inputs or Bass output
- Loudness
  - 2nd order frequency response
  - programmable center frequency (400Hz/800Hz/2400Hz)
  - 15dB with 1dB steps
  - soft-step control with programmable blend times
  - selectable low & high frequency boost
- Volume
  - +15dB to -79dB with 1dB step resolution
  - soft-step control with programmable blend times
  - multi-step control
- Bass
  - 2nd order frequency response
  - center frequency programmable in 4 steps (60Hz/80Hz/100Hz/200Hz)
  - Q programmable 1.0/1.25/1.5/2.0
  - DC gain programmable
  - -15 to 15dB with 1dB resolution
  - soft-step control with programmable blend times
- Treble
  - 2nd order frequency response
  - center frequency programmable in 4 steps (10KHz/12.5KHz/15KHz/17.5KHz)
  - -15 to 15dB with 1dB resolution
- High pass
  - 2nd order frequency response
  - center frequency programmable in 3 steps (80Hz/120Hz/160Hz)
- Speaker
  - independent soft step speaker controls, +15dB to -79dB with 1dB steps
  - Independent programmable mix input with 50% mixing ratio for front speakers
  - direct mute
  - multi-step control
- Mute Functions
  - digitally controlled SoftMute with 3 programmable mute-times (0.48ms/0.96ms/123ms)



TQFP32

Description

The TDA7417 is an high performance signal processor specifically designed for car radio applications with fully integrated audio filters.

The digital control allows a full programming of the audioprocessor in a wide range of filter characteristics.

By using BICMOS-process low distortion and low noise are obtained.

Table 1. Device summary

Order codes	Package	Packing
TDA7417	TQFP32	Tray
TDA7417TR	TQFP32	Tape & reel

Contents

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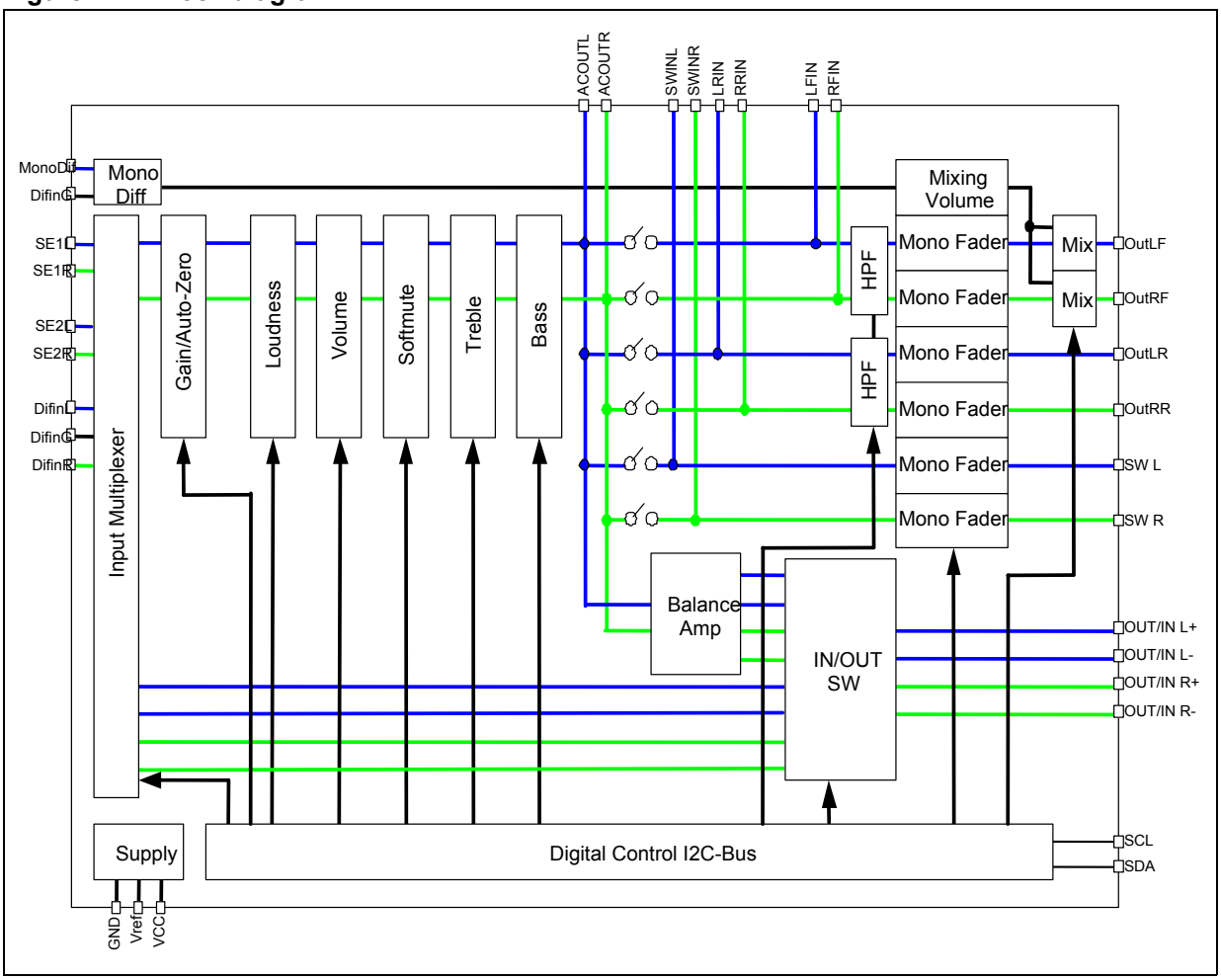
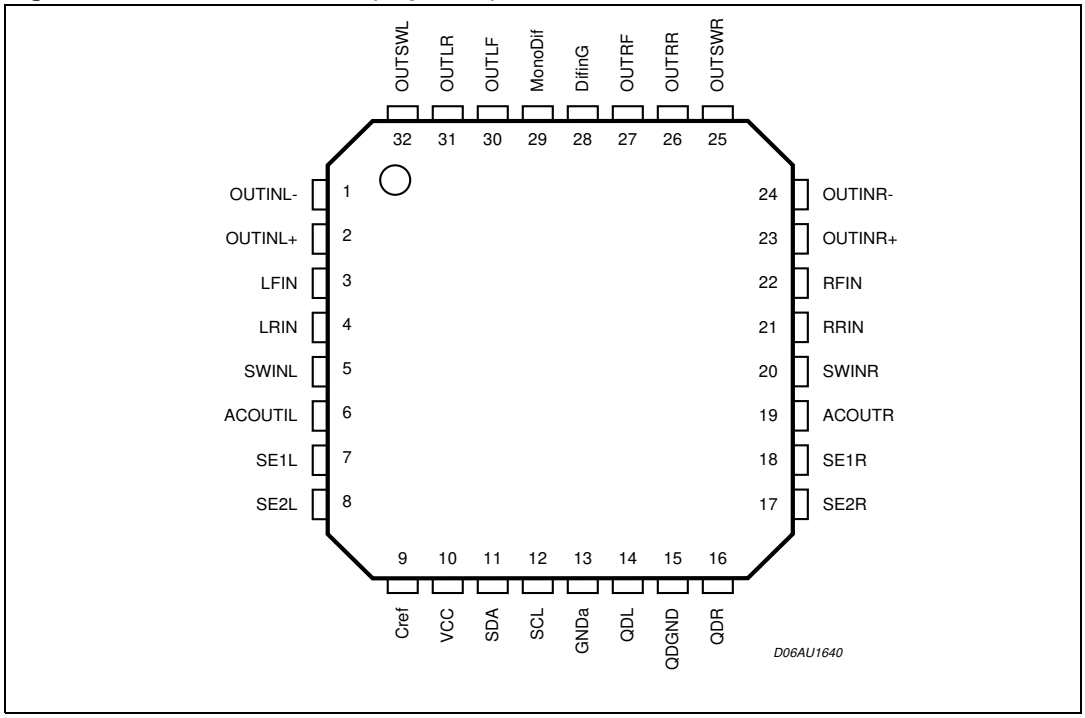
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (Top view)



2.1 Pins description

Table 2. Pins description

NO.	Pin Name	Description	I/O
1	OUTINL-	Left- full-differential stereo input or bass differential output	I/O
2	OUTINL+	Left+ full-differential stereo input or bass differential output	I/O
3	LFIN	Front AC coupling left input	I
4	LRIN	Rear AC coupling left input	I
5	SWINL	SW AC coupling left input	I
6	ACOUTL	AC coupling left output	O
7	SE1L	Single-ended input 1 left channel	I
8	SE2L	Single-ended input 2 left channel	I
9	CREF	Reference capacitor	O
10	VCC	Supply	S
11	SDA	I^2C bus data	I/O
12	SCL	I^2C bus clock	I
13	GNDa	Ground	S

Table 2. Pins description (continued)

NO.	Pin Name	Description	I/O
14	QDL	Pseudo differential stereo input left	I
15	QDGND	Pseudo differential stereo input common	I
16	QDR	Pseudo differential stereo input right	I
17	SE2R	Single-ended input 2 right channel	I
18	SE1R	Single-ended input 1 right channel	I
19	ACOUTR	AC coupling right output	O
20	SWINR	SW AC coupling right input	I
21	RRIN	Rear AC coupling right input	I
22	RFIN	Front AC coupling right input	I
23	OUTINR+	Right+ Full-differential stereo input or Bass differential output	I/O
24	OUTINR-	Right- Full-differential stereo input or Bass differential output	I/O
25	OUTSWR	SW right output	O
26	OUTRR	Rear right output	O
27	OUTRF	Front right output	O
28	DifinG	Mono differential input common	I
29	MonoDif	Mono differential input	I
30	OUTLF	Front left output	O
31	OUTLR	Rear left output	O
32	OUTSWL	SW left output	O

3 Electrical specifications

3.1 Thermal data

Table 3. Thermal data

Symbol	Description	Value	Unit
$R_{Thj\text{-}case}$	Thermal resistance junction-case	13	°C/W

3.2 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	9.5	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C
V_{ESD}	ESD protection (Human Body Model)	±2000	V
V_{ESD}	ESD protection (Change Device Model)	±750	V

3.3 Electrical characteristics

Table 5. Electrical characteristics

V_S = 8.5V; T_{amb}= 25 C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_s	Supply voltage		8	8.5	9	V
I_s	Supply current		25	34	45	mA
INPUT SELECTOR						
Rin	Input resistance	All single ended inputs	70	100	130	kΩ
V_{CL}	Clipping level	THD = 1%	2	2.3		V_{RMS}
S_{IN}	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain		-0.5	0	0.5	dB
$G_{IN\ MAX}$	Max. input gain		14.5	15	15.5	dB
G_{STEP}	Step resolution		0.5	1	1.5	dB
V_{DC}	DC steps	Adjacent gain steps	-5	1	5	mV
		$G_{MIN\ to\ GMAX}$	-15	4	15	mV
V_{offset}	Remaining offset with AutoZero			0.5		mV

Table 5. Electrical characteristics (continued)

V_S = 8.5V; T_{amb}= 25 C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DIFFERENTIAL STEREO INPUTS						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio	$V_{CM=1\ VRMS@\ 1kHz}$	46	60		dB
		$V_{CM=1\ VRMS@\ 10kHz}$	46	60		dB
DIFFERENTIAL MONO INPUTS						
R_{in}	Input resistance	Differential	40	56	72	kΩ
CMRR	Common mode rejection ratio	V_{CM} =1 VRMS@ 1kHz	40	60		dB
		V_{CM} =1 VRMS@ 10kHz	40	60		dB
MIXING CONTROL						
M_{LEVEL}	Mixing ratio	Main / Mix Source		-6/-6		dB
G_{MAX}	Max gain		13	15	17	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
LOUDNESS CONTROL						
A_{MAX}	Max attenuation		14	15	16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_{Peak}	Peak frequency(1)	f_{P1}	360	400	440	Hz
		f_{P2}	720	800	880	Hz
		f_{P3}	2200	2400	2600	Hz
VOLUME CONTROL						
G_{MAX}	Max gain		14	15	16	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	G = -15to +15dB	-1	0	1	dB
		G = -79 to -15dB	-4	0	3	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0dB to G_{MIN}	-7	0.5	7	mV
SOFT MUTE						
A_{MUTE}	Mute attenuation		80	100		dB
T_D	Delay time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	70	123	170	ms

Table 5. Electrical characteristics (continued)

V_S = 8.5V; T_{amb}= 25 C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BASS CONTROL						
Fc	Center frequency (1)	f_{C1}	54	60	66	Hz
		f_{C2}	72	80	88	Hz
		f_{C3}	90	100	110	Hz
		f_{C4}	180	200	220	Hz
Q_{BASS}	Quality factor (1)	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
C_{RANGE}	Control range		±14	±15	±16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on	3.5	4.4	5.5	dB
TREBLE CONTROL						
C_{RANGE}	Control range		±14	±15	±16	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
f_c	Center frequency (1)	f_{C1}	8	10	12	kHz
		f_{C2}	10	12.5	15	kHz
		f_{C3}	12	15	18	kHz
		f_{C4}	14	17.5	21	kHz
HPF						
f_{HP}	Highpass corner frequency (1)	f_{HP1}	72	80	88	Hz
		f_{HP2}	108	120	132	Hz
		f_{HP3}	144	160	176	Hz
SPEAKER ATTENUATORS						
G_{MAX}	Max gain		14	15	16	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MUTE}	Mute attenuation		80	90		dB
E_E	Attenuation set error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-5	0.1	5	mV
AUDIO OUTPUTS						
V_{CL}	Clipping level	THD = 1%	2	2.3		V_{RMS}
R_{OUT}	Output impedance		5	30	100	W
R_L	Output load resistance		2			kΩ
C_L	Output load capacitor				10	nF

Table 5. Electrical characteristics (continued)

V_S = 8.5V; T_{amb}= 25 C; R_L= 10kΩ; all gains = 0dB; f = 1kHz; unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DC}	DC voltage level		4.05	4.25	4.4	V
AC COUPLING						
R_{ACIN}	AC coupling input resistance		35	50	65	kΩ
R_{ACOUT}	AC coupling output resistance		5	50	100	Ω
IN/OUT CONTROL						
R_{in}	Input resistance	Differential	70	100	130	kΩ
CMRR	Common mode rejection ratio	V_{CM} =1 VRMS@ 1kHz	40	60		dB
		V_{CM} =1 VRMS@ 10kHz	40	60		dB
$V_{CL(IN)}$	In clipping level		1.9	2		V_{RMS}
$V_{CL(OUT)}$	Out clipping level		1.9	2		V_{RMS}
R_{OUT}	Output impedance			50	100	Ω
R_{IMPED}	High impedance			200		kΩ
V_{DC}	DC voltage level		3.1	3.3	3.5	V
I^2C TIMING						
VIH	High input voltage for SDA,SCL		2.5			V
VIL	Low input voltage for SDA,SCL				0.7	V
VOL	Low output voltage for SDA				0.4	V
Tr	SDA and SCL rise time				300	ns
Tf	SDA and SCL fall time				300	ns
Tsdah	SCL falling to SDA input hold time		0		0.9	us
Tsdas	SDA input setup time to SCL rising		100			ns
GENERAL						
e_{NO}	Output noise	BW=20Hz to 20 kHz all gain = 0dB, HPF = off		12	25	µV
		BW=20Hz to 20 kHz Output muted		6	15	µV
S/N	Signal to noise ratio	all gain = 0dB flat; V_o =2V_{RMS}	95	100		dB
D	Distortion	V_{IN}=1V_{RMS}; all stages 0dB HPF = off		0.01	0.1	%
S_C	Channel separation left/right		80	90		dB

1. Min and max values are calculated according to simulation results; functionality is guaranteed by measuring a directly correlated parameter

Note: It is not recommended that gain control and Softstep control be adjusted at the same time if they are in the same byte.
It is not allowed to change multistep on/off or softstep on/off during the process of multistep or softstep.

4 Description of the audioprocessor

4.1 Input stages

In the basic configuration, one stereo quasi-differential, one selectable full-differential and two single ended stereo inputs are available. As *Figure 3* shown.

Quasi-differential stereo Input (QD)

The QD input is implemented as a buffered quasi-differential stereo stage with 100kΩ input-impedance at each input. The attenuation is fixed to -3.5dB in order to adapt the incoming signal level.

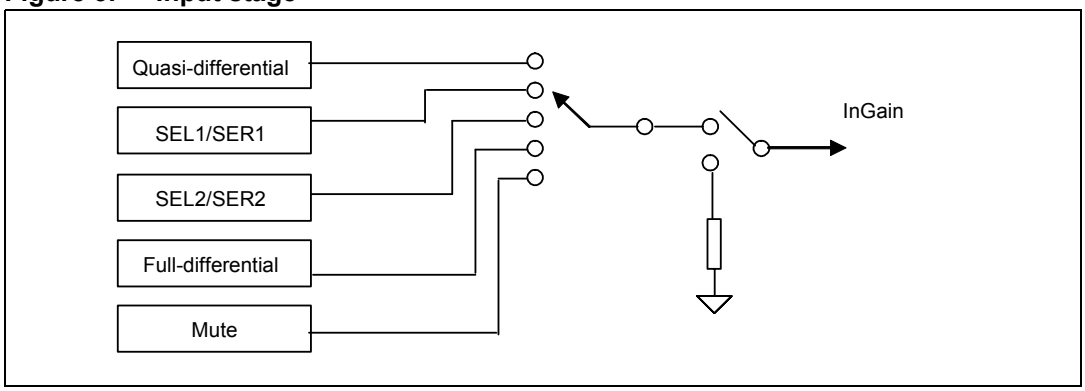
Single-ended stereo input (SE1, SE2)

The input-impedance at each input is 100kΩ and the attenuation is fixed to -3.5dB for incoming signals.

Full differential stereo Input (FD)

The FD input is implemented as a selectable full-differential stereo stage with 50k input-impedance at each input or high impedance status. The attenuation is fixed to -3.5dB in order to adapt the incoming signal level.The high impedance status is 100kΩ

Figure 3. Input stage



4.2 AutoZero

The AutoZero allows a reduction of the number of pins as well as external components by canceling any offset generated by or before the In-Gain-stage (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the input source is changed and needs max. **0.32ms** for the alignment. To avoid audible clicks the Audio processor is muted before the loudness stage during this time.

AutoZero-Remain

In some cases, for example if the µP is executing a refresh cycle of the IIC-Bus-programming, it is not useful to start a new AutoZero-action because no new source is selected and an undesired mute would appear at the outputs. For such applications, it can be switched in the **AutoZero-Remain-Mode** (Bit 6 of the subaddress-byte). If this bit is set to high, the AutoZero will not be invoked and the old adjustment-value remains.

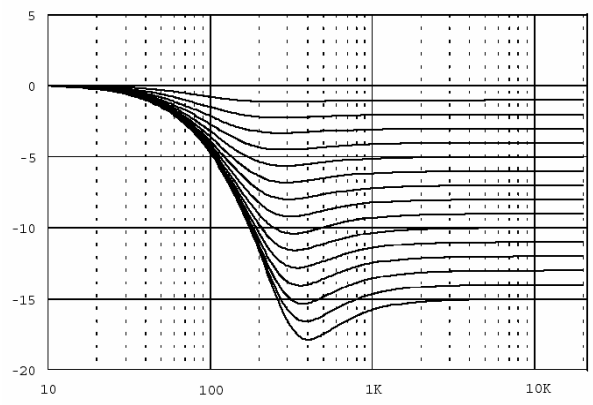
4.3 Loudness

There are four parameters programmable in the loudness stage:

4.3.1 Attenuation

Figure 4 shows the attenuation as a function of frequency at f_P = 400Hz.

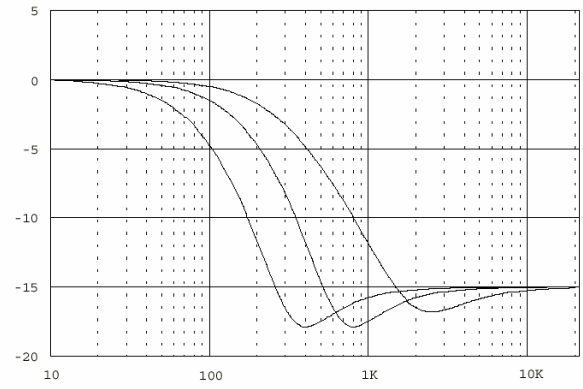
Figure 4. Loudness Attenuation @ f_P = 400Hz



4.3.2 Peak Frequency

Figure 5 shows the four possible peak-frequencies at 400, 800 and 2400Hz.

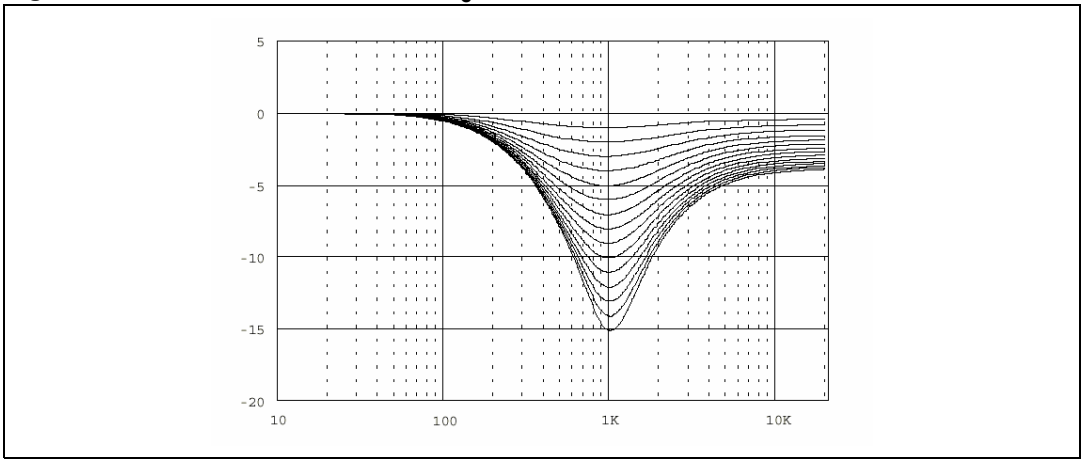
Figure 5. Loudness Center frequencies @ Attn. = 15dB



4.3.3 Low & high frequency boost

Figure 6 shows the different Loudness shapes in low & high frequency boost.

Figure 6. Loudness Attenuation, f_c=2.4kHz



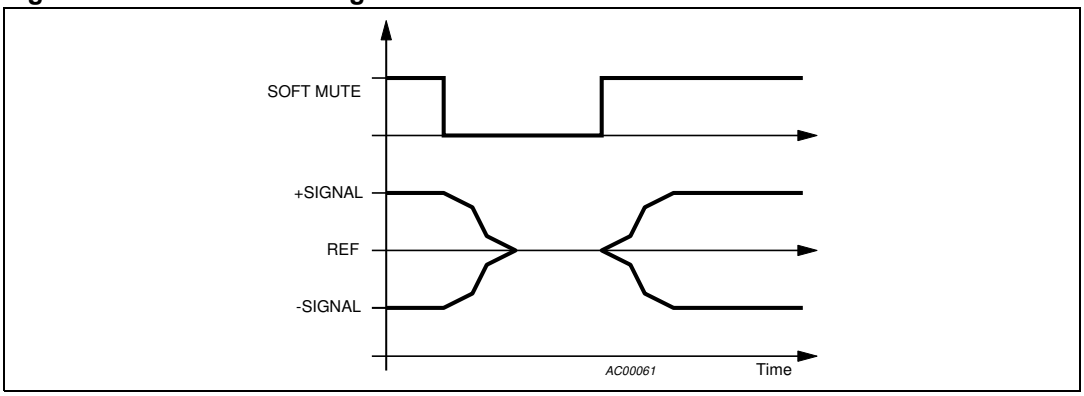
4.3.4 Flat Mode

In flat mode the loudness stage works as a 0dB to -15dB attenuator.

4.4 SoftMute

The digitally controlled Softmute stage allows muting/demuting the signal with a I2C-bus programmable slope. The mute process can be activated by the I^2C-bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

Figure 7. Softmute-Timing



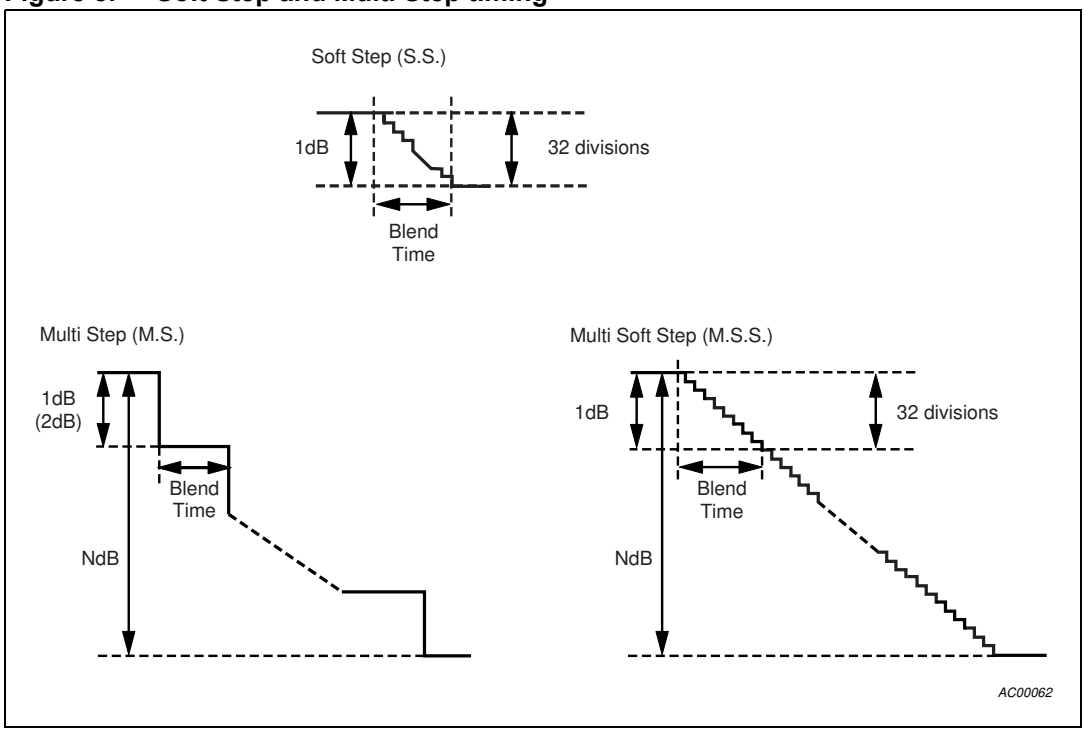
Note: Please notice that a started Mute-action is always terminated and could not be interrupted by a change of the mute -signal

4.5 Multistep and Softstep Volume

When the volume-level is changed audible clicks could appear at the output. The root cause of those clicks

could either be a DC-Offset before the volume-stage or the sudden change of the envelope of the audio signal. With the Multistep and Softstep feature both kinds of clicks could be reduced to a minimum and are no more audible. Multistep feature supports N dB change, each step is 1dB;During 1dB transition, it will have 32 divisions if choosing softstep. The blend-time from one step to the next is user selectable.

Figure 8. Soft Step and Multi Step timing



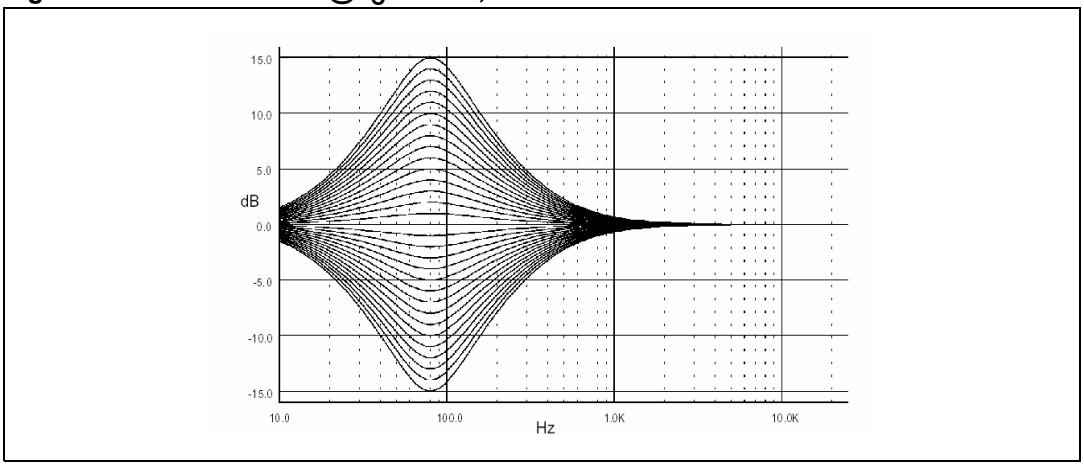
4.6 Bass

There are four parameters programmable in the bass stage:

4.6.1 Attenuation

Figure 9 shows the attenuation as a function of frequency at a center frequency of 80Hz.

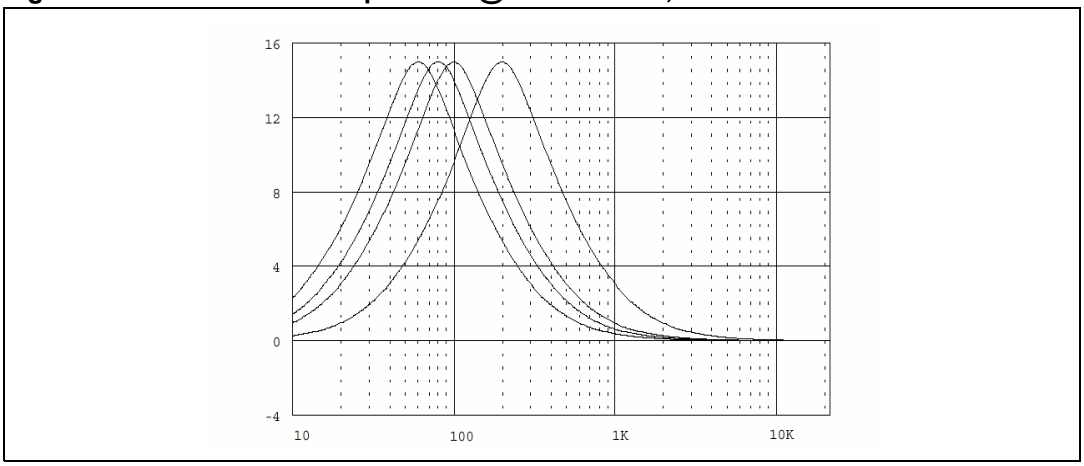
Figure 9. Bass Control @ f_C = 80Hz, Q = 1



4.6.2 Center Frequency

Figure 10 shows the eight possible center frequencies 60, 80, 100 and 200Hz.

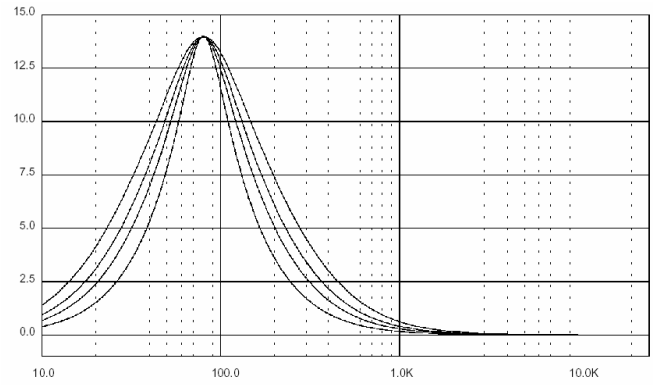
Figure 10. Bass center Frequencies @ Gain = 14dB, Q = 1



4.6.3 Quality Factors

Figure 11 shows the four possible quality factors 1, 1.25, 1.5 and 2.

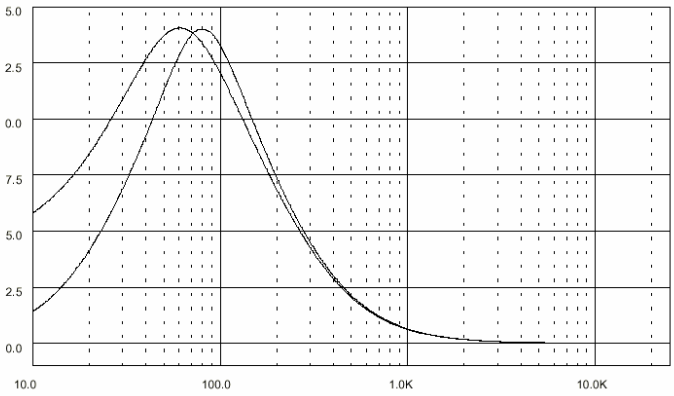
Figure 11. Bass Quality factors @ Gain = 14dB, f_C = 80Hz



4.6.4 DC Mode

It is used for cut only for shelving filter. In this mode the DC-gain is increased by 4.4dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors. *Figure 12* shows DC mode.

Figure 12. Bass normal and DC Mode @ Gain = 14dB, f_c = 80Hz



Note: The center frequency, Q and DC-mode can be set fully independently.

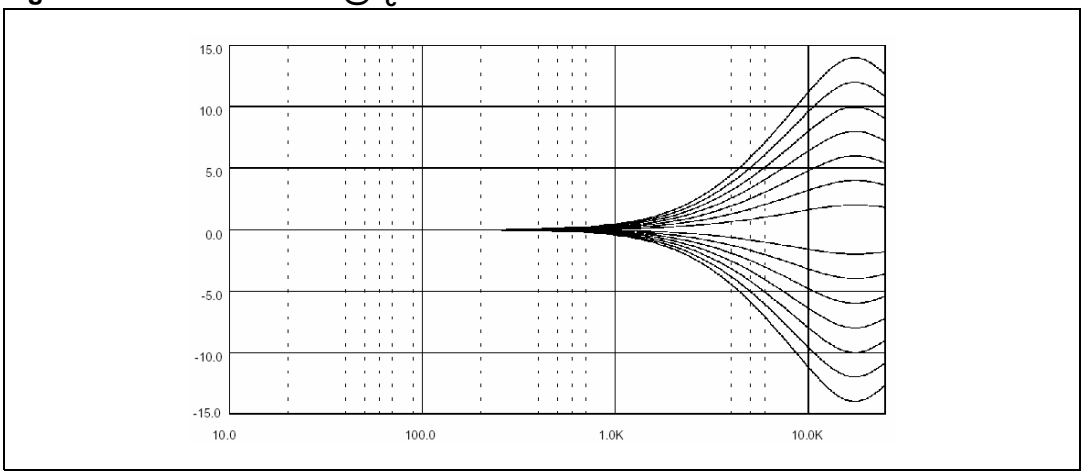
4.7 Treble

There are two parameters programmable in the treble stage:

4.7.1 Attenuation

Figure 13 shows the attenuation as a function of frequency at a center frequency of 17.5kHz.

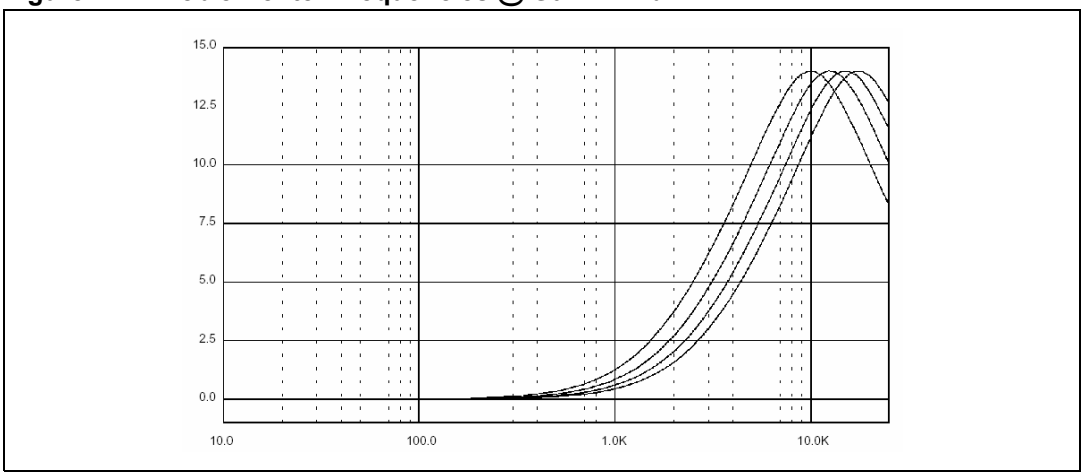
Figure 13. Treble Control @ f_c = 17.5kHz



4.7.2 Center Frequency

Figure 14 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5kHz.

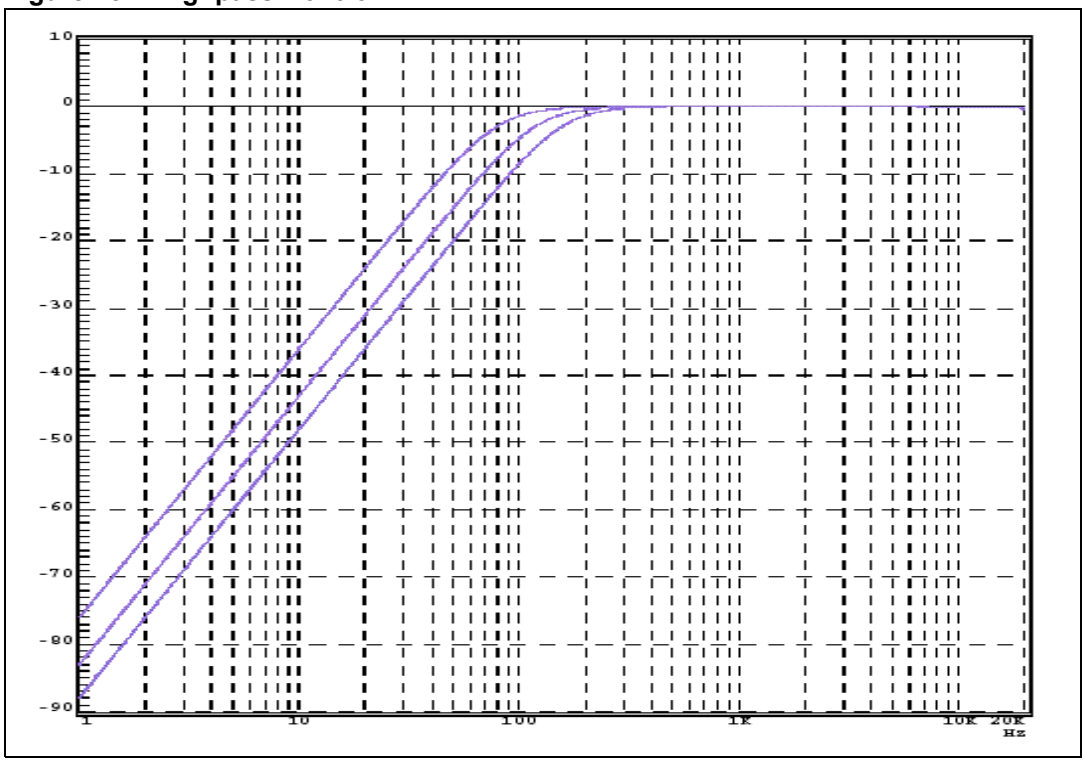
Figure 14. Treble Center Frequencies @ Gain = 14dB



4.8 Highpass filter

The highpass filter has 2 order filter characteristics with programmable cut-off frequency (80/120/160Hz)

Figure 15. Highpass Control

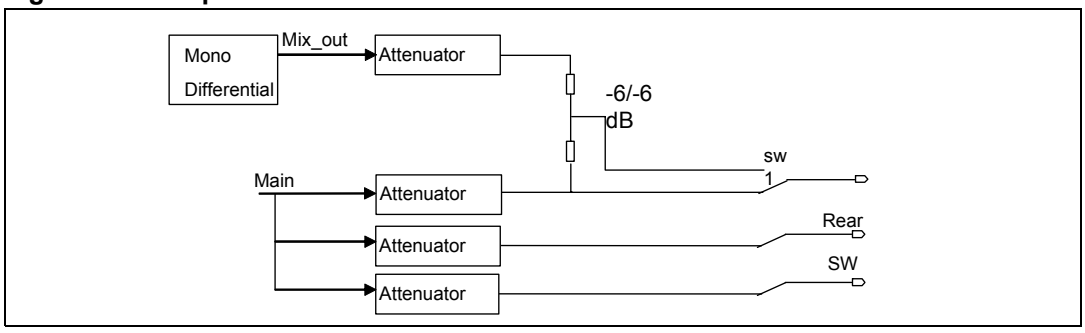


4.9 Output Selector and Mixing

The output-selector allows different sources to connect to the front output. The setup of the output selector is shown in *Figure 16*. A Mixing-stage is placed after the front speaker-attenuator and can be set to mixing-mode.

In normal mode, switch (sw1) turns to down and main signal is directly outputted through front pin. In the mixing mode, switch (sw1) turns up, mono differential signal and main signal are mixed with ratio -6/-6dB. Having a full volume-attenuator for the mix-signal, the stage offers a wide flexibility to adapt the mixing levels.

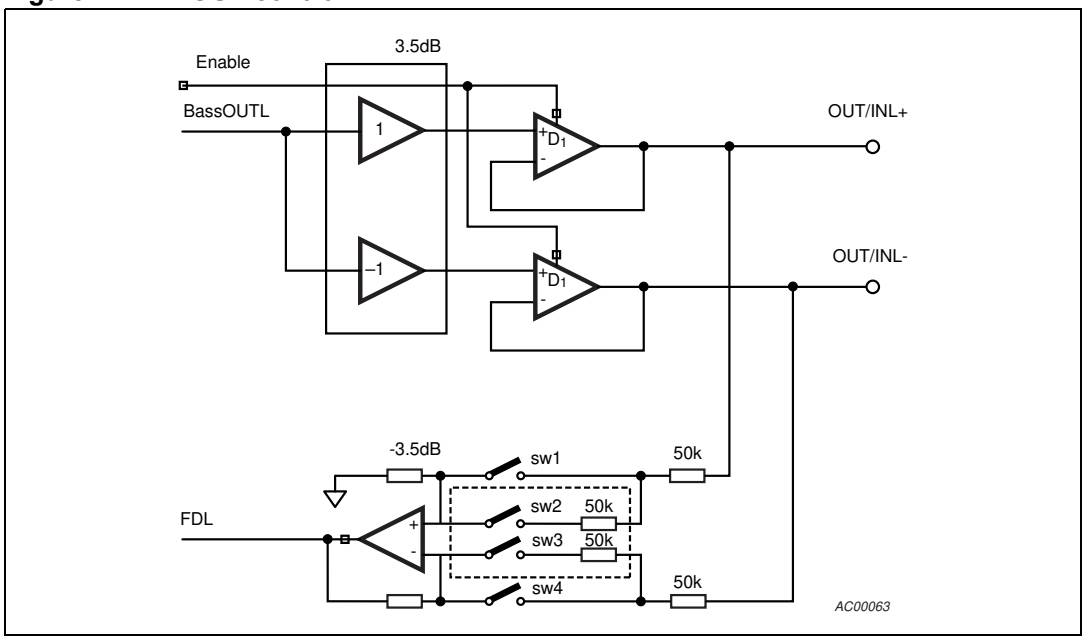
Figure 16. Output Selector



4.10 IN/OUT control

IN/OUT control offers selectable full-differential stereo input or Bass output as figure15 shown. When used as full-differential input, bass buffer output is disabled, full-differential input switch sw1(sw4) closes and sw2(sw3) closes. When used as bass output, full-differential input switch sw1(sw4) opens and sw2(sw3) still closes, single ended bass output signal is converted to full differential output. IN/OUT control supports high impedance status when bass buffer output is disabled, full-differential input switch sw1(sw4) opens and sw2(sw3) closes.

Figure 17. IN/OUT control

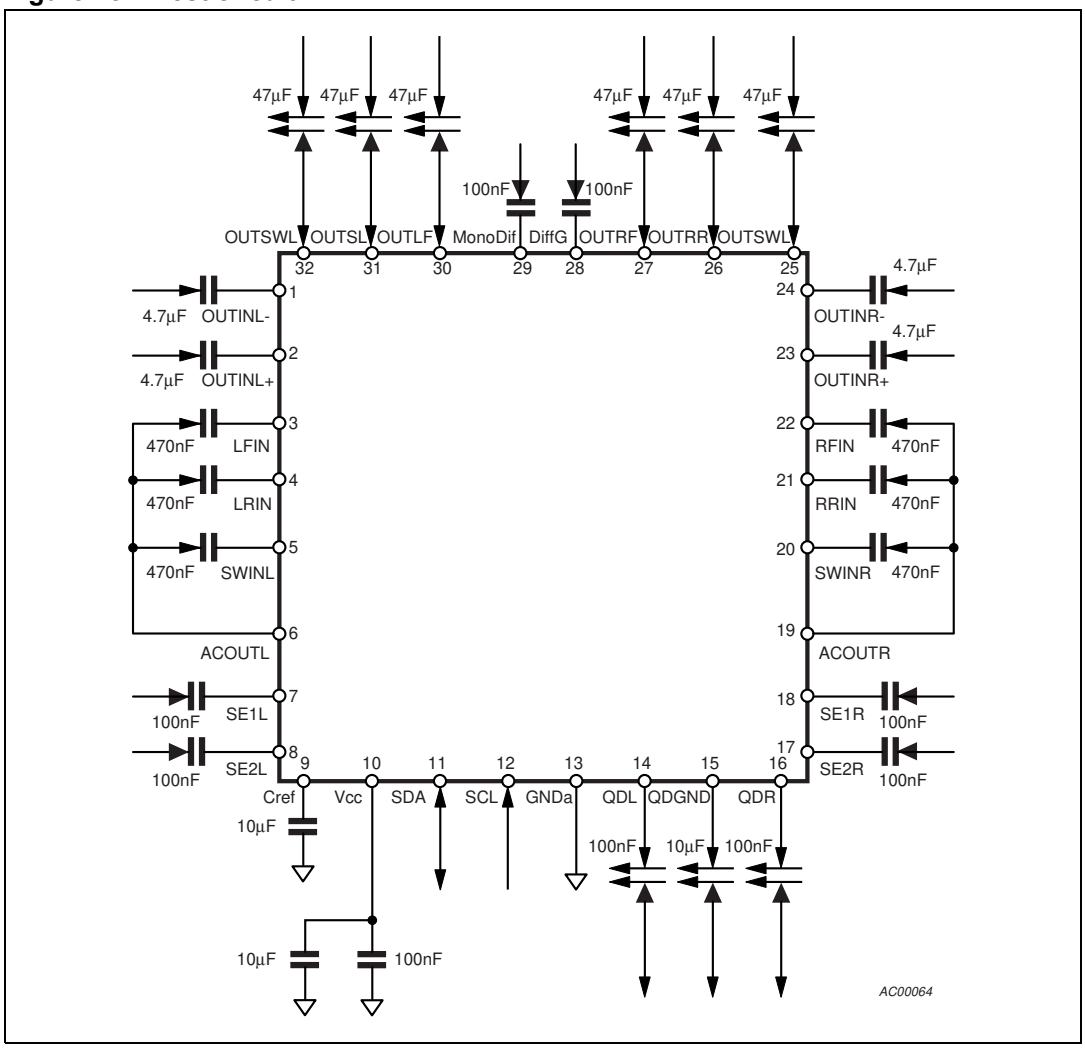


4.11 Audioprocessor Testing

In the test mode, which can be activated by setting bit D7 of the IIC subaddress byte and bit D0 of the testing audioprocessor byte, several internal signals are available at the QDL pin. In this mode, the input resistance of 100kOhm is disconnected from the pin. Internal signals available for testing are listed in the data-byte specification. External clock can be available at the SE1R pin.

4.12 Test circuit

Figure 18. Test circuit



5 I²C Bus specification

5.1 Interface Protocol

The interface protocol comprises:

- a start condition (S)
- a chip address byte (the LSB determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)
- the max. clock speed is 500kbits/s
- 3.3V logic compatible

5.1.1 Receive Mode

S	1	0	0	0	1	0	0	R/W	ACK	TS	AZ	AI	A4	A3	A2	A1	A0	ACK	DATA	ACK	P

S = Start

R/W = "0" -> Receive Mode (Chip can be programmed by P)

"1" -> Transmission Mode (Data could be received by P)

ACK = Acknowledge

P = Stop

TS = Testing mode

AZ = Auto zero remain

AI = Auto increment

5.1.2 Transmission Mode

S	1	0	0	0	1	0	0	R/W	ACK	X	X	X	X	X	X	X	SM	ACK	P

SM = Soft mute activated for main channel

X = Not Used

The transmitted data is automatic updated after each ACK. Transmission can be repeated without new chip address.

5.1.3 Reset Condition

A Power-On-Reset is invoked if the Supply-Voltage is below than 3.5V. After that the following data is written automatically into the registers of all subaddresses:

Table 6. Registers of all subaddresses

MSB							LSB
1	1	1	1	1	1	1	0

6 Serial data assign

6.1 Sub-address

Table 7. Sub-address

MSB							LSB	FUNCTION
I2	I1	I0	A4	A3	A2	A1	A0	
0 1								**Testing Mode** off on
	0 1							**AutoZero Remain** off on
		0 1						**Auto Increment Mode** Off On
			0	0	0	0	0	Main Source Selector
			0	0	0	0	1	Loudness
			0	0	0	1	0	Primary Volume
			0	0	0	1	1	Softmute/Clock Generator
			0	0	1	0	0	Treble Control
			0	0	1	0	1	Bass Control
			0	0	1	1	0	Highpass/Bass Frequency control
			0	0	1	1	1	Smoother/In/Out control
			0	1	0	0	0	Mix volume
			0	1	0	0	1	Mono Fader LF
			0	1	0	1	0	Mono Fader RF
			0	1	0	1	1	Mono Fader LR
			0	1	1	0	0	Mono Fader RR
			0	1	1	0	1	Mono Fader SWL
			0	1	1	1	0	Mono Fader SWR
			0	1	1	1	1	Fader Multistep control
			1	0	0	0	0	Test control

6.1.1 Main Source Selector (0)

Table 8. Main source selector (0)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Source Selector
					0	0	0	QD
					0	0	1	SE1
					0	1	0	SE2
					0	1	1	FD
					1	X	X	Mute
								Input Gain
	0	0	0	0				0dB
	0	0	0	1				1dB
	0	0	1	0				2.dB
	0	0	1	1				3dB
	0	1	0	0				4dB
	0	1	0	1				5dB
	0	1	1	0				6dB
	0	1	1	1				7dB
	1	0	0	0				8dB
	1	0	0	1				9dB
	1	0	1	0				10dB
	1	0	1	1				11dB
	1	1	0	0				12dB
	1	1	0	1				13dB
	1	1	1	0				14dB
	1	1	1	1				15dB
								Auto Zero
0								on
1								off