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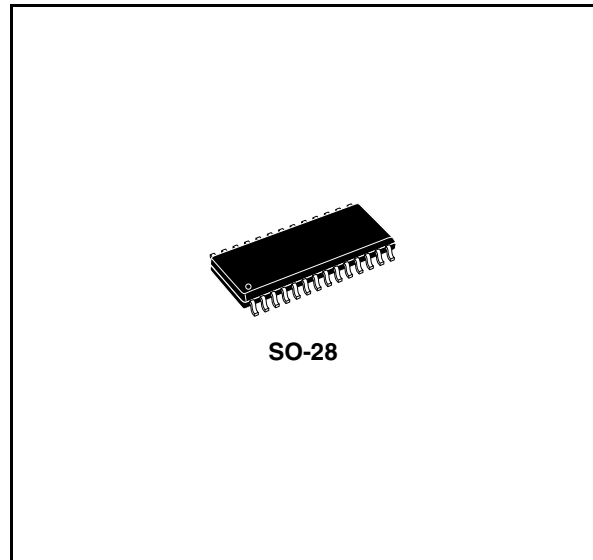


**3 band car audio processor****Features**

- 4 stereo inputs
- Soft-step volume
- Bass, middle, treble and loudness
- Direct mute and soft-mute
- Four independent speaker outputs
- Sub woofer output
- Soft-step speaker/subwoofer control
- 7 bands spectrum analyzer
- Digital control:
  - I<sup>2</sup>C bus interface

**Description**

The TDA7419 is a high performance signal processor specifically designed for car radio applications. The device includes a high performance audioprocessor with fully integrated audio filters.



The digital control allows programming in a wide range of filter characteristics. By the use of BICMOS-process and linear signal processing low distortion and low noise are obtained.

**Table 1. Device summary**

Order code	Package	Packing
TDA7419	SO-28	Tube
TDA7419TR	SO-28	Tape and reel

# Contents

- 1      Block diagram ..... 6**
- 2      Pin description ..... 7**
- 3      Electrical specifications ..... 9**
  - 3.1    Supply ..... 9
  - 3.2    Thermal data ..... 9
  - 3.3    Absolute maximum ratings ..... 9
  - 3.4    Electrical characteristics ..... 10
- 4      Description of the audio processor ..... 14**
  - 4.1    Audio processor features ..... 14
  - 4.2    Input stages ..... 15
    - 4.2.1    Quasi-differential stereo input (QD) ..... 15
    - 4.2.2    Single-ended stereo input (SE1, SE2, SE3/AC2IN) ..... 15
  - 4.3    AutoZero ..... 16
    - 4.3.1    AutoZero remain ..... 16
  - 4.4    Loudness ..... 16
    - 4.4.1    Attenuation ..... 16
    - 4.4.2    Peak frequency ..... 17
    - 4.4.3    Low and high frequency boost ..... 18
    - 4.4.4    Flat mode ..... 18
  - 4.5    Soft-mute ..... 18
    - 4.5.1    Soft-step volume ..... 19
  - 4.6    Bass ..... 19
    - 4.6.1    Attenuation ..... 20
    - 4.6.2    Center frequency ..... 21
    - 4.6.3    Quality factors ..... 21
    - 4.6.4    DC mode ..... 22
  - 4.7    Middle ..... 22
    - 4.7.1    Attenuation ..... 22
    - 4.7.2    Center frequency ..... 23
    - 4.7.3    Quality factors ..... 23

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4.8	Treble .....	24
4.8.1	Attenuation .....	24
4.8.2	Center frequency .....	24
4.9	Subwoofer filter .....	25
4.10	Spectrum analyzer .....	25
4.11	AC coupling .....	26
4.12	HPF applications .....	27
4.13	Output selector and mixing .....	27
4.14	Audioprocessor testing .....	28
4.15	Test circuit .....	28
<b>5</b>	<b>I<sup>2</sup>C bus specification .....</b>	<b>29</b>
5.1	Interface protocol .....	29
5.1.1	Receive mode .....	29
5.1.2	Transmission mode .....	29
5.1.3	Reset condition .....	29
5.2	Subaddress (receive mode) .....	30
5.3	Data byte specification .....	31
<b>6</b>	<b>Package information .....</b>	<b>38</b>
<b>7</b>	<b>Revision history .....</b>	<b>39</b>

## List of tables

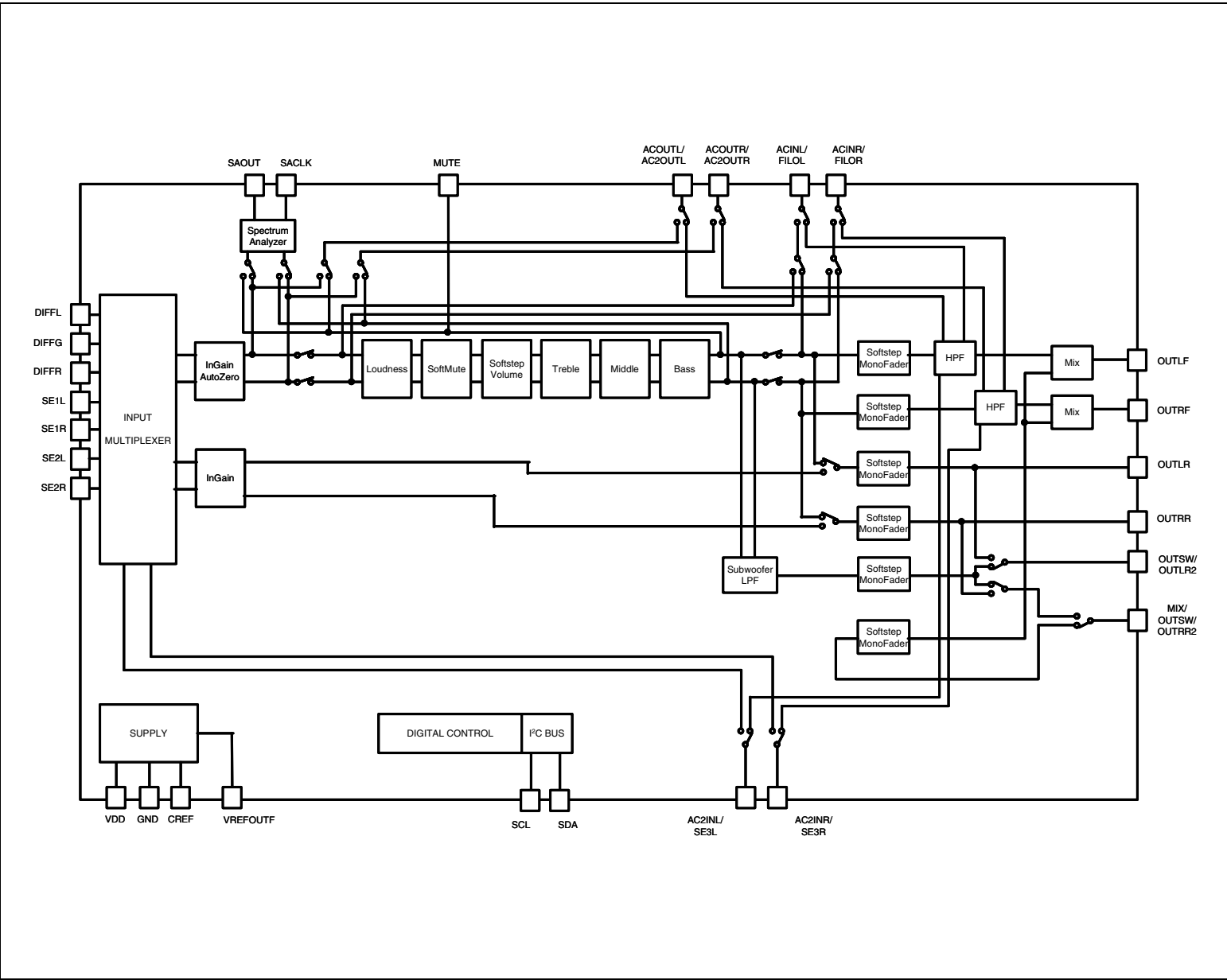
Table 1.	Device summary . . . . .	1
Table 2.	Pin description . . . . .	7
Table 3.	Supply. . . . .	9
Table 4.	Thermal data. . . . .	9
Table 5.	Absolute maximum ratings . . . . .	9
Table 6.	Electrical characteristics . . . . .	10
Table 7.	Subaddress (receive mode). . . . .	30
Table 8.	Main selector (0) . . . . .	31
Table 9.	Main loudness (1) . . . . .	31
Table 10.	Soft-mute / clock generator (2) . . . . .	32
Table 11.	Volume / speaker / mixing / subwoofer attenuation (3, 10-15) . . . . .	32
Table 12.	Treble filter (4) . . . . .	33
Table 13.	Middle filter (5) . . . . .	33
Table 14.	Bass filter (6) . . . . .	34
Table 15.	Second source selector (7) . . . . .	34
Table 16.	Subwoofer /middle / bass (8) . . . . .	35
Table 17.	Mixing / gain effect (9) . . . . .	36
Table 18.	Spectrum analyzer / clock source / AC mode (16) . . . . .	36
Table 19.	Testing audio processor (17) . . . . .	37
Table 20.	Document revision history . . . . .	39

## List of figures

Figure 1.	Block diagram . . . . .	6
Figure 2.	Pin connection (top view) . . . . .	7
Figure 3.	Input stage . . . . .	16
Figure 4.	Loudness attenuation @ $f_P = 400$ Hz. . . . .	17
Figure 5.	Loudness center frequencies @ Attn. = 15 dB. . . . .	17
Figure 6.	Loudness attenuation, $f_C = 2.4$ kHz . . . . .	18
Figure 7.	Soft-mute timing . . . . .	19
Figure 8.	Soft-step timing . . . . .	19
Figure 9.	Bass control @ $f_C = 80$ Hz, $Q = 1$ . . . . .	20
Figure 10.	Bass center frequencies @ gain = 15 dB, $Q = 1$ . . . . .	21
Figure 11.	Bass quality factors @ gain = 14 dB, $f_C = 80$ Hz . . . . .	21
Figure 12.	Bass normal and DC mode @ gain = 14 dB, $f_C = 80$ Hz . . . . .	22
Figure 13.	Middle control @ $f_C = 1$ kHz, $Q = 1$ . . . . .	22
Figure 14.	Middle center frequencies @ gain = 14 dB, $Q = 1$ . . . . .	23
Figure 15.	Middle quality factors @ gain = 14 dB, $f_C = 1$ kHz . . . . .	23
Figure 16.	Treble control @ $f_C = 17.5$ kHz . . . . .	24
Figure 17.	Treble center frequencies @ gain = 15 dB . . . . .	24
Figure 18.	Subwoofer control . . . . .	25
Figure 19.	Spectrum analyzer block diagram . . . . .	25
Figure 20.	Timing of the spectrum analyzer . . . . .	26
Figure 21.	Diagram of AC coupling . . . . .	26
Figure 22.	HPF diagram . . . . .	27
Figure 23.	Output selector . . . . .	27
Figure 24.	Test circuit . . . . .	28
Figure 25.	SO-28 mechanical data and package dimensions . . . . .	38

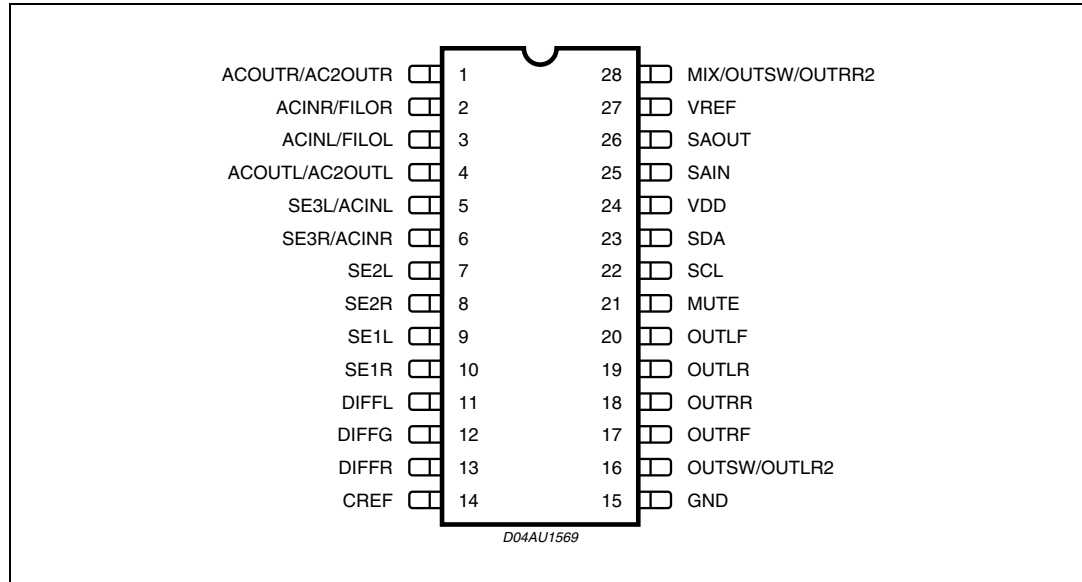
# 1 Block diagram

Figure 1. Block diagram



## 2 Pin description

**Figure 2. Pin connection (top view)**



**Table 2. Pin description**

Pin N#	Pin name	Function	I/O
1	ACOUTR / AC2OUTR	AC coupling right output / HPF filter AC2OUT right channel	O
2	ACINR / FILO R	AC coupling right input / HPF filter FILO right channel	I/O
3	ACINL / FILO L	AC coupling left input / HPF filter FILO left channel	I/O
4	ACOUTL / AC2OUTL	AC coupling left output / HPF filter AC2OUT left channel	O
5	SE3L / ACINL	Single-ended input 3 left channel / AC coupling left input	I
6	SE3R / ACINR	Single-ended input 3 right channel / AC coupling right input	I
7	SE2L	Single-ended input 2 left channel	I
8	SE2R	Single-ended input 2 right channel	I
9	SE1L	Single-ended input 1 left channel	I
10	SE1R	Single-ended input 1 Right channel	I
11	DIFFL	Pseudo differential stereo input left	I
12	DIFFG	Pseudo differential stereo input common	I
13	DIFFR	Pseudo differential stereo input right	I
14	CREF	Reference capacitor	O
15	GND	Ground	S
16	OUTSW / OUTLR2	Subwoofer output / 2 <sup>nd</sup> rear left output	O
17	OUTRF	Front right output	O



Table 2. Pin description (continued)

Pin N#	Pin name	Function	I/O
18	OUTRR	Rear right output	O
19	OUTLR	Rear left output	O
20	OUTLF	Front left output	O
21	MUTE	External mute pin	I
22	SCL	I2C bus clock	I
23	SDA	I2C bus data	I/O
24	VDD	Supply	S
25	SAIN	Spectrum analyzer clock input	I
26	SAOUT	Spectrum analyzer output	O
27	VREF	Vref output	O
28	MIX / OUTSW / OUTRR2	Mix input / Additional subwoofer output / 2 <sup>nd</sup> rear right output	I/O

## 3 Electrical specifications

### 3.1 Supply

Table 3. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_s$	Supply voltage		8.0	8.5	10	V
$I_s$	Supply current	$V_s = 8.5$ V	30	35	40	mA
SVRR	Ripple rejection @ 1 kHz	Audioprocessor (all Filters flat)	60			dB

### 3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{Th\ j-pins}$	Thermal resistance junction to pinsmax	85	°C/W

### 3.3 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_s$	Operating supply voltage	10.5	V
$T_{amb}$	Operating temperature range	-40 to 85	°C
$T_{stg}$	Storage temperature range	-55 to +150	°C
$V_{ESD}$	ESD withstand voltage	Human body model	$\geq \pm 1750$
		Machine model	$\geq \pm 150$
		Charged device model	$\geq \pm 1500$

### 3.4 Electrical characteristics

**Table 6. Electrical characteristics**

$V_S = 8.5V$ ;  $T_{amb} = 25^\circ C$ ;  $R_L = 10k\Omega$ ; all gains = 0 dB;  $f = 1$  kHz; unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Supply</b>						
$V_S$	Supply voltage		8	8.5	10	V
$I_S$	Supply current		27	37	47	mA
<b>Input selector</b>						
$R_{in}$	Input resistance	All single ended inputs	70	100	130	$k\Omega$
$V_{CL}$	Clipping level	All Input	1.8	2		$V_{RMS}$
		QD input	1.7	2		$V_{RMS}$
$S_{IN}$	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. input gain		13	15	17	dB
$G_{STEP}$	Step resolution		0.5	1	1.5	dB
$V_{DC}$	DC steps	Adjacent gain steps	-5	1	5	mV
		$G_{MIN}$ to $G_{MAX}$	-20	4	20	mV
$V_{offset}$	Remaining offset with AutoZero			0.5		mV
<b>Differential stereo inputs</b>						
$R_{in}$	Input resistance	Differential	70	100	130	$K\Omega$
CMRR	Common mode rejection ratio	$V_{CM} = 1$ VRMS @ 1 kHz	46	70		dB
		$V_{CM} = 1$ VRMS @ 10 kHz	46	60		dB
$e_{No}$	Output noise @ speaker outputs	20 Hz to 20 kHz, flat; all stages 0 dB		12		$\mu V$
<b>Mixing control</b>						
$M_{LEVEL}$	Mixing ratio	Main / mix source		-6/-6		dB
$G_{MAX}$	Max gain		13	15	17	dB
$A_{MAX}$	Max attenuation		-83	-79	-75	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
<b>Loudness control</b>						
$A_{MAX}$	Max attenuation		-17	-15	-13	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_{Peak}$	Peak frequency	$f_{P1}$	360	400	440	Hz
		$f_{P2}$	720	800	880	Hz
		$f_{P3}$	2200	2400	2600	Hz

Table 6. Electrical characteristics (continued)

 $V_S = 8.5V$ ;  $T_{amb} = 25^\circ C$ ;  $R_L = 10k\Omega$ ; all gains = 0 dB;  $f = 1$  kHz; unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Volume control</b>						
$G_{MAX}$	Max gain		13	15	17	dB
$A_{MAX}$	Max attenuation		-83	-79	-75	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$E_A$	Attenuation set error	$G = -20$ to $+20$ dB	-0.75	0	+0.75	dB
		$G = -79$ to $-20$ dB	-4	0	3	dB
$E_T$	Tracking error				2	dB
$V_{DC}$	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0dB to $G_{MIN}$	-5	0.5	5	mV
<b>Soft-mute</b>						
$A_{MUTE}$	Mute attenuation		80	100		dB
$T_D$	Delay time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	70	123	170	ms
$V_{TH\ Low}$	Low threshold for SM pin				1	V
$V_{TH\ High}$	High threshold for SM pin		2.5			V
$R_{PU}$	Internal pull-up resistor		32	45	58	k $\Omega$
$V_{PU}$	Internal pull-up voltage			3.3		V
<b>Bass control</b>						
$F_c$	Center frequency	$f_{C1}$	54	60	66	Hz
		$f_{C2}$	72	80	88	Hz
		$f_{C3}$	90	100	110	Hz
		$f_{C4}$	180	200	220	Hz
$Q_{BASS}$	Quality factor	$Q_1$	0.9	1	1.1	
		$Q_2$	1.1	1.25	1.4	
		$Q_3$	1.3	1.5	1.7	
		$Q_4$	1.8	2	2.2	
$C_{RANGE}$	Control range		$\pm 14$	$\pm 15$	$\pm 16$	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$DC_{GAIN}$	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on (shelving filter, use for cut only)		-4.4		dB

**Table 6. Electrical characteristics (continued)**

$V_S = 8.5V$ ;  $T_{amb} = 25^{\circ}C$ ;  $R_L = 10k\Omega$ ; all gains = 0 dB;  $f = 1\text{ kHz}$ ; unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Middle control</b>						
$C_{RANGE}$	Control range		$\pm 14$	$\pm 15$	$\pm 16$	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_c$	Center frequency	$f_{C1}$	400	500	600	Hz
		$f_{C2}$	0.8	1	1.2	kHz
		$f_{C3}$	1.2	1.5	1.8	kHz
		$f_{C4}$	2	2.5	3	kHz
$Q_{BASS}$	Quality factor	$Q_1$	0.45	0.5	0.55	
		$Q_2$	0.65	0.75	0.85	
		$Q_3$	0.9	1	1.1	
		$Q_4$	1.1	1.25	1.4	
<b>Treble control</b>						
$C_{RANGE}$	Clipping level		$\pm 14$	$\pm 15$	$\pm 16$	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$f_c$	Center frequency	$f_{C1}$	8	10	12	kHz
		$f_{C2}$	10	12.5	15	kHz
		$f_{C3}$	12	15	18	kHz
		$f_{C4}$	14	17.5	21	kHz
<b>Speaker attenuators</b>						
$G_{MAX}$	Max gain		14	15	16	dB
$A_{MAX}$	Max attenuation		-83	-79	-75	dB
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$A_{MUTE}$	Mute attenuation		80	90		dB
$E_E$	Attenuation set error				2	dB
$V_{DC}$	DC steps	Adjacent attenuation steps	-5	0.1	5	mV
<b>AUdio outputs</b>						
$V_{CL}$	Clipping level	$d = 0.3\%$	1.8	2		$V_{RMS}$
$R_{OUT}$	Output impedance			30	100	W
$R_L$	Output load resistance		2			k $\Omega$
$C_L$	Output load capacitor				10	nF
$V_{DC}$	DC voltage level		3.8	4.0	4.2	V
<b>Subwoofer attenuator</b>						
$G_{MAX}$	Max gain		14	15	16	dB
$A_{MAX}$	Max attenuation		-83	-79	-75	dB

Table 6. Electrical characteristics (continued)

 $V_S = 8.5V$ ;  $T_{amb} = 25^\circ C$ ;  $R_L = 10k\Omega$ ; all gains = 0 dB;  $f = 1$  kHz; unless otherwise specified

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$A_{STEP}$	Step resolution		0.5	1	1.5	dB
$A_{MUTE}$	Mute attenuation		80	90		dB
$E_E$	Attenuation set error				2	dB
$V_{DC}$	DC steps	Adjacent attenuation steps	-5	1	5	mV
<b>Subwoofer lowpass</b>						
$f_{LP}$	Lowpass corner frequency	$f_{LP1}$	72	80	88	Hz
		$f_{LP2}$	108	120	132	Hz
		$f_{LP3}$	144	160	176	Hz
<b>HPF effect</b>						
$G_{MAX}$	Max gain		21	22	23	dB
$G_{MIN}$	Min gain		3	4	5	dB
$A_{STEP}$	Step resolution		1.5	2	2.5	dB
<b>Spectrum analyzer control</b>						
$V_{SAOut}$	Output voltage range		0		3.3	V
$f_{C1}$	Center frequency band 1		5.5	62	69	Hz
$f_{C2}$	Center frequency band 2		141	157	173	Hz
$f_{C3}$	Center frequency band 3		356	392	436	Hz
$f_{C4}$	Center frequency band 4		0.9	1	1.1	kHz
$f_{C5}$	Center frequency band 5		2.26	2.51	2.76	kHz
$f_{C6}$	Center frequency band 6		5.70	6.34	6.98	kHz
$f_{C7}$	Center frequency band 7		14.4	16	17.6	kHz
Q	Quality factor	Q1	1.62	1.8	1.98	
		Q2	3.15	3.5	3.85	
$f_{SAClk}$	Clock frequency		3		100	kHz
$t_{Sadel}$	Analog output delay time		2			$\mu s$
$t_{repeat}$	Spectrum analyzer repeat time		50			ms
$t_{intres}$	Internal reset time			4.5		ms
<b>General</b>						
$e_{NO}$	Output noise	BW = 20 Hz to 20 kHz all gain = 0dB		12	20	$\mu V$
		BW = 20 Hz to 20 kHz output muted		6	15	$\mu V$
S/N	Signal to noise ratio	all gain = 0 dB flat; $V_o = 2 V_{RMS}$		100		dB
D	Distortion	$V_{IN} = 1 V_{RMS}$ ; all stages 0 dB		0.01	0.1	%
$S_C$	Channel separation left/right		80	90		dB

## 4 Description of the audio processor

### 4.1 Audio processor features

- Input Multiplexer
  - QD / SE: quasi-differential stereo inputs, with selectable single-ended mode
  - SE1: stereo single-ended input
  - SE2: stereo single-ended input
  - SE3 / AC2IN: stereo single-ended input / HPF filter input
  - In-Gain 0 to 15dB, 1dB steps
  - internal offset-cancellation (AutoZero)
  - separate second source-selector
- Mixing stage
  - mixable to front speaker-outputs
- Loudness
  - 2<sup>nd</sup> order frequency response
  - programmable center frequency (400Hz/800Hz/2400Hz)
  - 15 dB with 1 dB steps
  - selectable low and high frequency boost
  - selectable flat-mode (constant attenuation)
- Volume
  - +15 dB to -79 dB with 1 dB step resolution
  - soft-step control with programmable blend times
- Bass
  - 2<sup>nd</sup> order frequency response
  - center frequency programmable in 4 steps (60 Hz/80 Hz/100 Hz/200 Hz)
  - Q programmable 1.0/1.25/1.5/2.0
  - DC gain programmable
  - -15 to 15 dB range with 1 dB resolution
- Middle
  - 2<sup>nd</sup> order frequency response
  - center frequency programmable in 4 steps (500Hz/1KHz/1.5KHz/2.5KHz)
  - Q programmable 0.5/0.75/1.0/1.25
  - DC gain programmable
  - -15 to 15dB range with 1dB resolution
- Treble
  - 2<sup>nd</sup> order frequency response
  - center frequency programmable in 4 steps (10KHz/12.5KHz/15KHz/17.5KHz)
  - -15 to 15dB range with 1dB resolution
- Spectrum analyzer
  - seven bandpass filters
  - 2<sup>nd</sup> order frequency response

- programmable Q factor for different visual appearance
- analog output
- controlled by external serial clock
- Speaker
  - 4 independent soft-step speaker controls, +15dB to -79dB with 1dB steps
  - Independent programmable mix input with 50% mixing ratio for front speakers
  - direct mute
- Subwoofer
  - 2nd order low pass filter with programmable cut off frequency
  - single-ended mono output independent soft-step level control, +15dB to -79dB with 1dB steps
- Mute functions
  - direct mute
  - digitally controlled Soft-mute with 3 programmable mute-times(0.48ms/0.96ms/123ms)
- Effect
  - gain effect, or high pass effect with fixed external components

## 4.2 Input stages

In the basic configuration, one stereo quasi-differential and three (two in case of HPS applications) single ended stereo inputs are available.

### 4.2.1 Quasi-differential stereo input (QD)

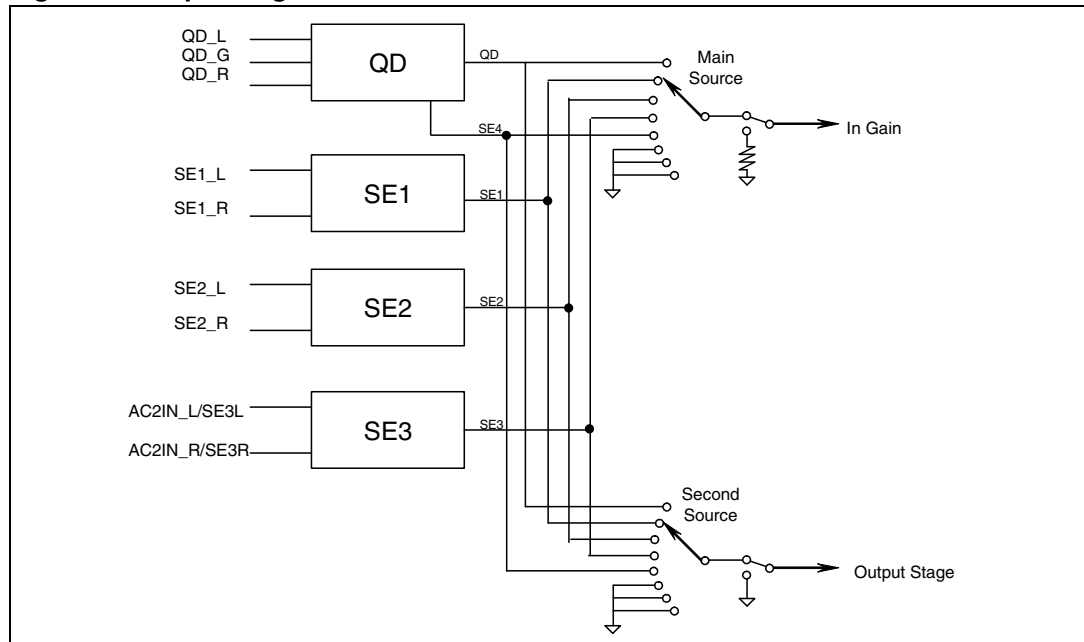
The QD input is implemented as a buffered quasi-differential stereo stage with 100 k $\Omega$  input-impedance at each input. The attenuation is fixed to -3 dB in order to adapt the incoming signal level.

### 4.2.2 Single-ended stereo input (SE1, SE2, SE3/AC2IN)

The input impedance at each input is 100 k $\Omega$  and the attenuation is fixed to -3dB for incoming signals. The input for SE3 is also configurable as part of the interface for external filters in HPS applications (AC2IN)



**Figure 3. Input stage**



### 4.3 AutoZero

The AutoZero allows a reduction of the number of pins as well as external components by canceling any offset generated by or before the In-Gain-stage (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not canceled).

The auto-zeroing is started every time the input source is changed and needs max. 0.3ms for the alignment. To avoid audible clicks the Audio processor is muted before the loudness stage during this time. The AutoZero feature is only present in the main signal-path.

#### 4.3.1 AutoZero remain

In some cases, for example if the  $\mu P$  is executing a refresh cycle of the I<sup>2</sup>C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications, it can be switched in the AutoZero remain mode (bit 6 of the subaddress byte). If this bit is set to high, the AutoZero will not be invoked and the old adjustment-value remains.

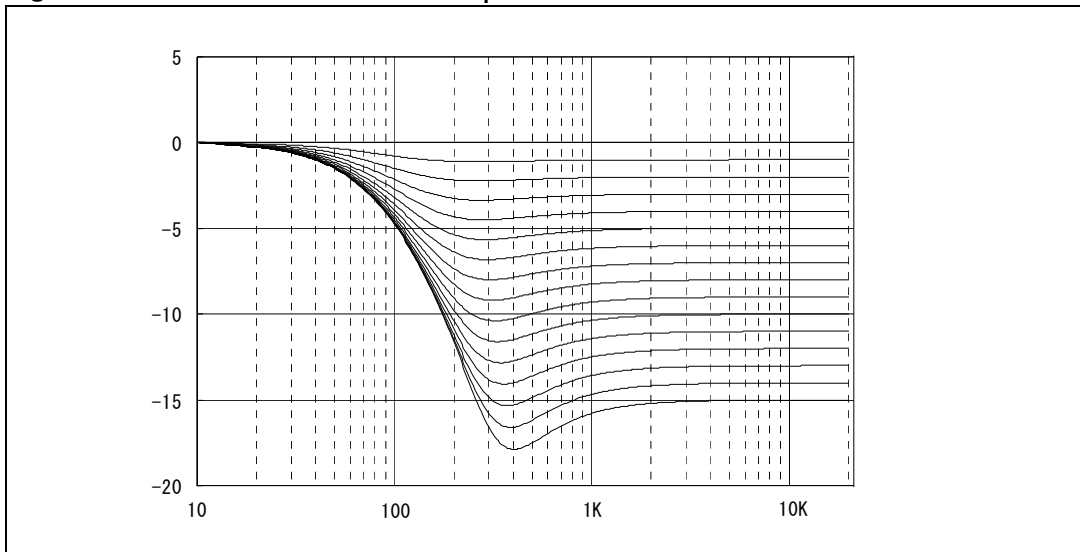
### 4.4 Loudness

There are four parameters programmable in the loudness stage:

#### 4.4.1 Attenuation

*Figure 4* shows the attenuation as a function of frequency at  $f_p = 400$  Hz

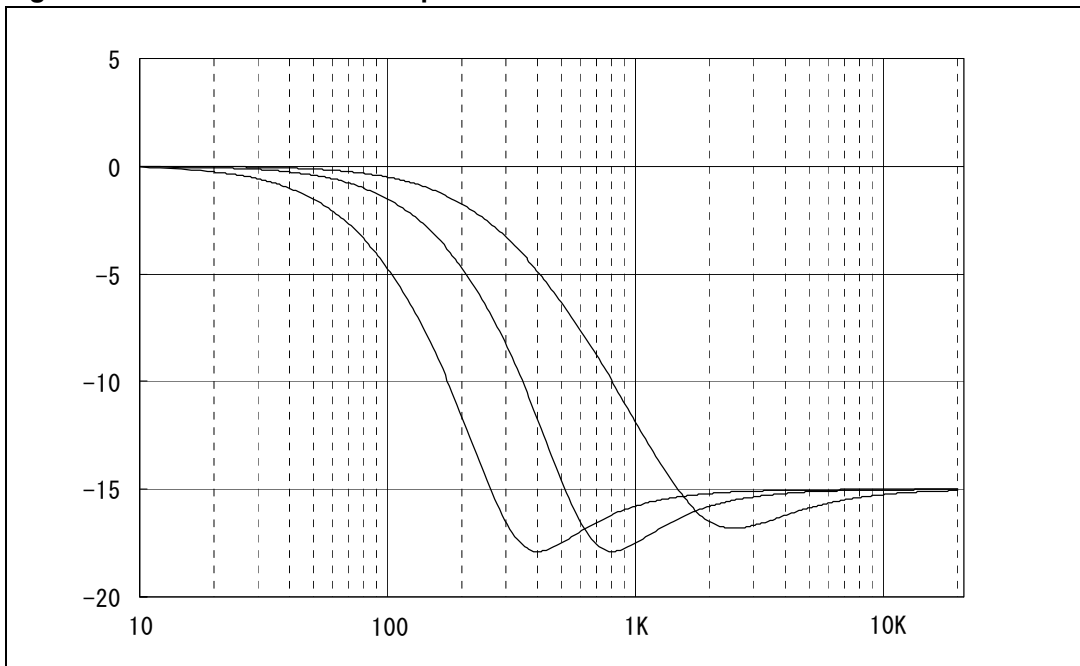
Figure 4. Loudness attenuation @  $f_p = 400$  Hz.



### 4.4.2 Peak frequency

Figure 5 shows the three possible peak frequencies 400 Hz, 800 Hz and 2.4 kHz.

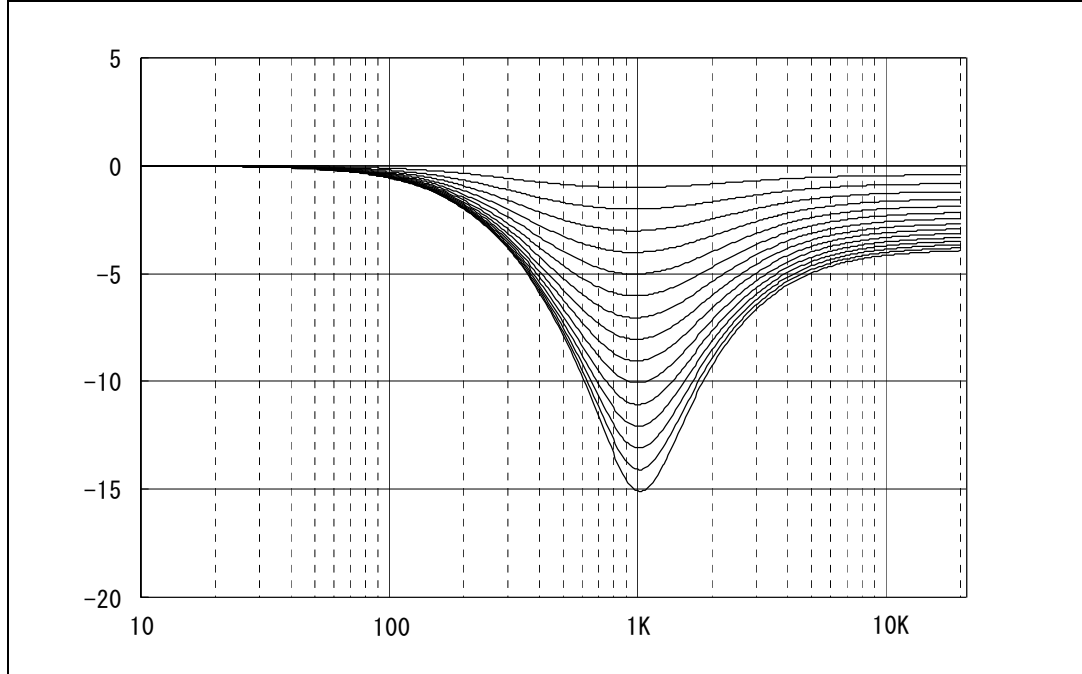
Figure 5. Loudness center frequencies @ Attn. = 15 dB



### 4.4.3 Low and high frequency boost

*Figure 6* shows the different loudness shapes in low and high frequency boost.

**Figure 6. Loudness attenuation,  $f_c = 2.4$  kHz**



### 4.4.4 Flat mode

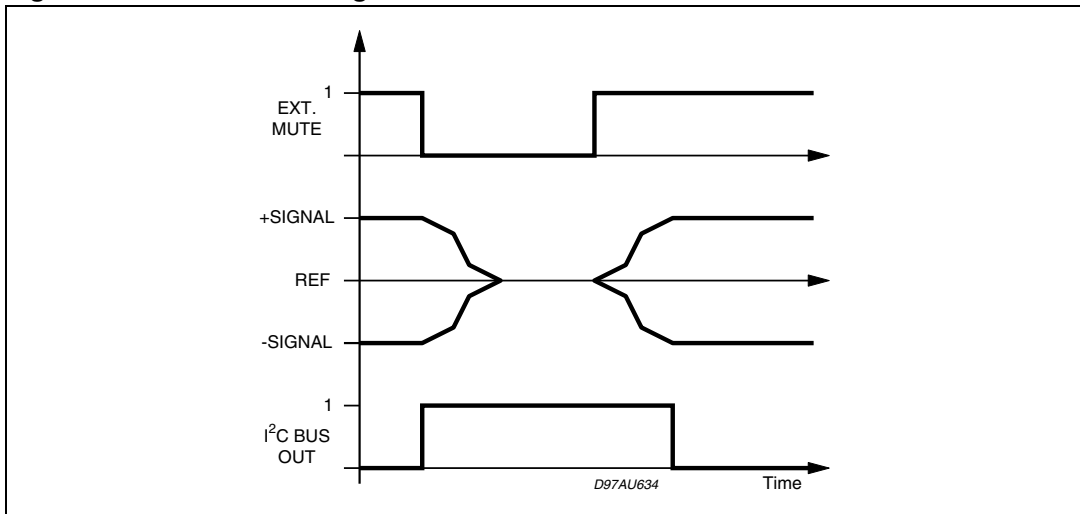
In flat mode the loudness stage works as a 0 dB to -15 dB attenuator.

## 4.5 Soft-mute

The digitally controlled soft-mute stage allows muting/demuting the signal with a I<sup>2</sup>C bus programmable slope. The mute process can either be activated by the soft-mute pin or by the I<sup>2</sup>C bus. This slope is realized in a special S-shaped curve to mute slow in the critical regions (see *Figure 7*).

For timing purposes the bit 0 of the I<sup>2</sup>C bus output register is set to 1 from the start of muting until the end of demuting.

**Figure 7. Soft-mute timing**



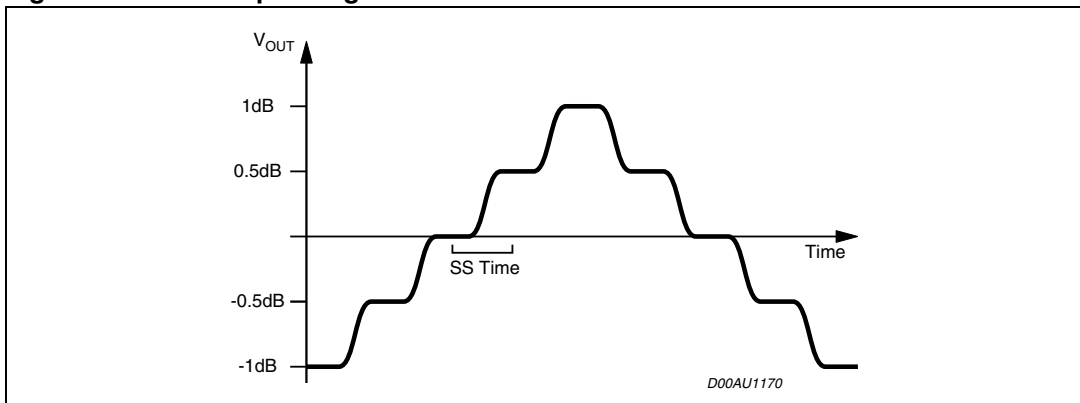
1. Please notice that a started mute-action is always terminated and could not be interrupted by a change of the mute -signal

### 4.5.1 Soft-step volume

When the volume level is changed audible clicks could appear at the output. The root cause of those clicks

could either be a DC-Offset before the volume-stage or the sudden change of the envelope of the audiosignal. With the soft-step feature both kinds of clicks could be reduced to a minimum and are no more audible. The blend-time from one step to the next is programmable in four steps.

**Figure 8. Soft-step timing**



1. For steps more than 0.5dB the Soft-step mode should be deactivated because it could generate a hard 1dB step during the blend-time.

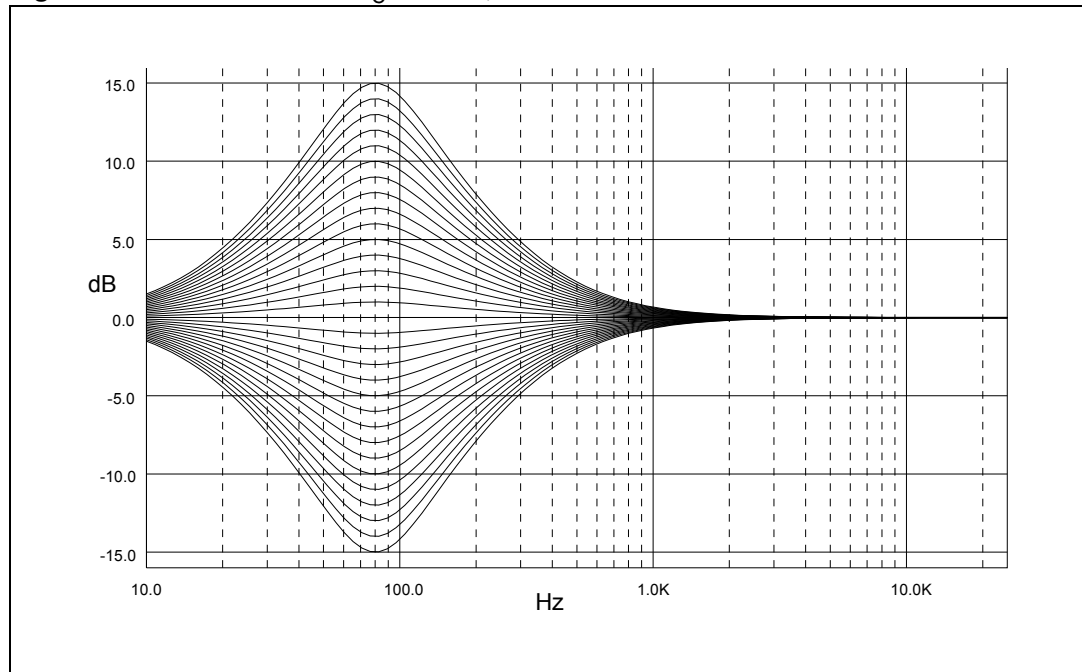
### 4.6 Bass

There are four parameters programmable in the bass stage:

### 4.6.1 Attenuation

*Figure 9* shows the attenuation as a function of frequency at a center frequency of 80 Hz.

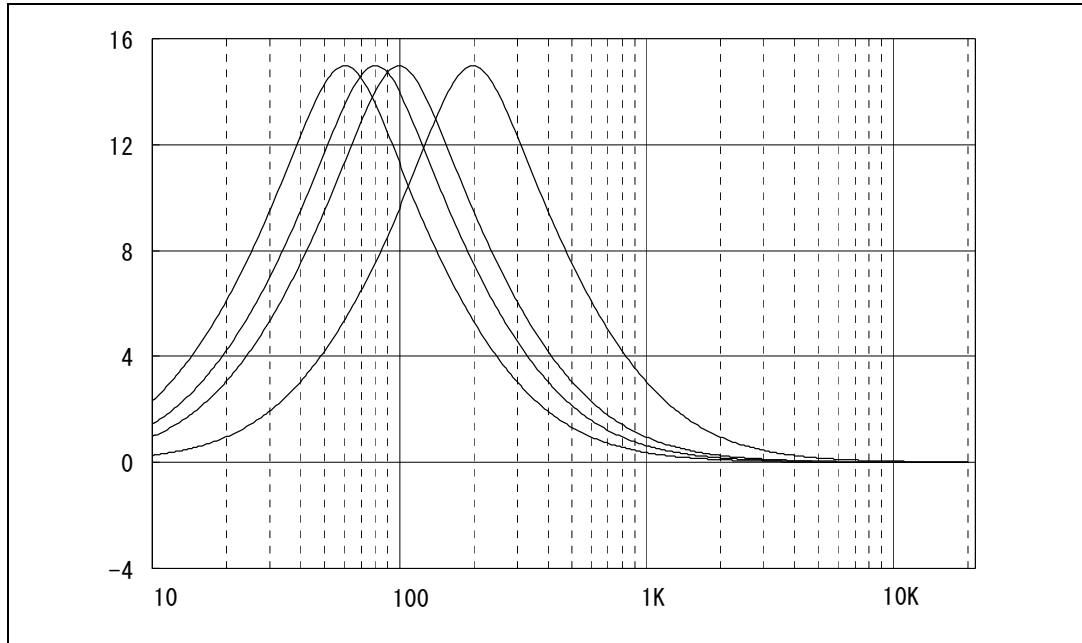
**Figure 9. Bass control @  $f_C = 80$  Hz,  $Q = 1$**



### 4.6.2 Center frequency

Figure 10 shows the four possible center frequencies 60, 80, 100 and 200 Hz.

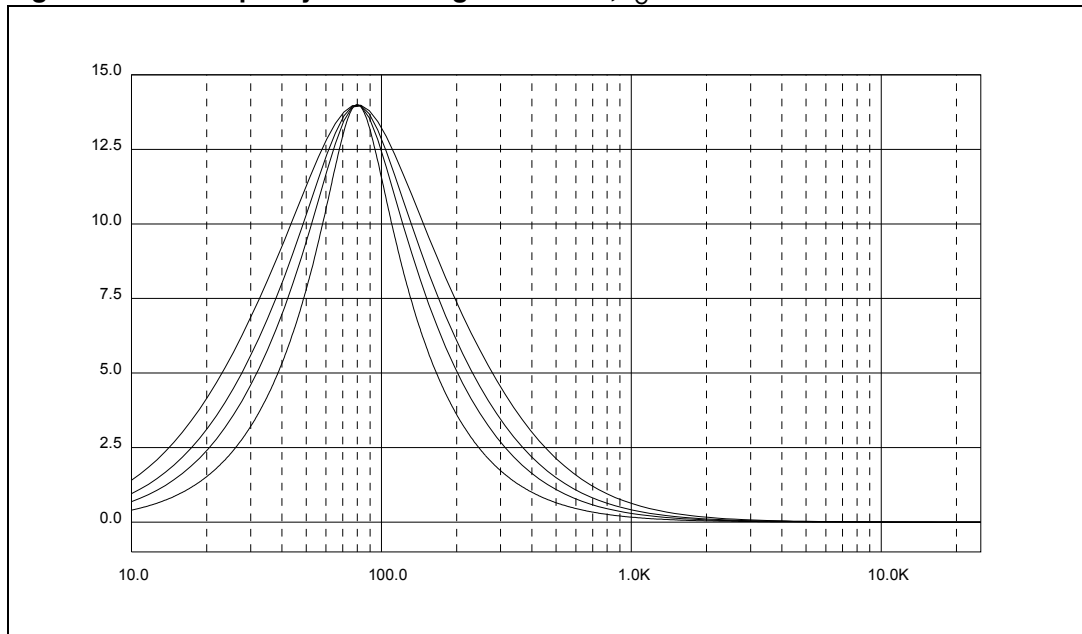
Figure 10. Bass center frequencies @ gain = 15 dB, Q = 1



### 4.6.3 Quality factors

Figure 11 shows the four possible quality factors 1, 1.25, 1.5 and 2.

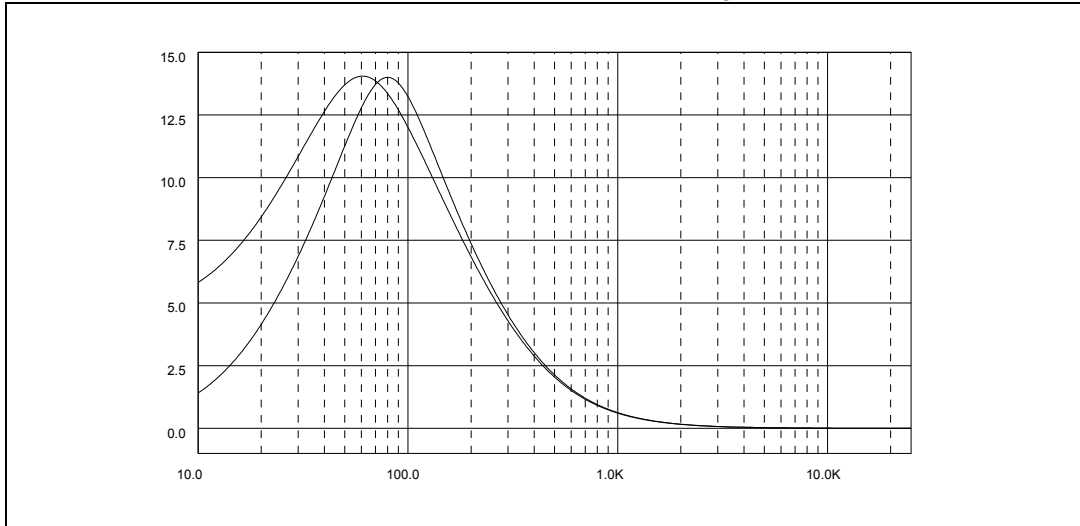
Figure 11. Bass quality factors @ gain = 14 dB,  $f_C = 80$  Hz



### 4.6.4 DC mode

It is used for cut only for shelving filter. In this mode the DC gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

**Figure 12. Bass normal and DC mode @ gain = 14 dB,  $f_C = 80$  Hz**



1. The center frequency, Q and DC-mode can be set fully independently.

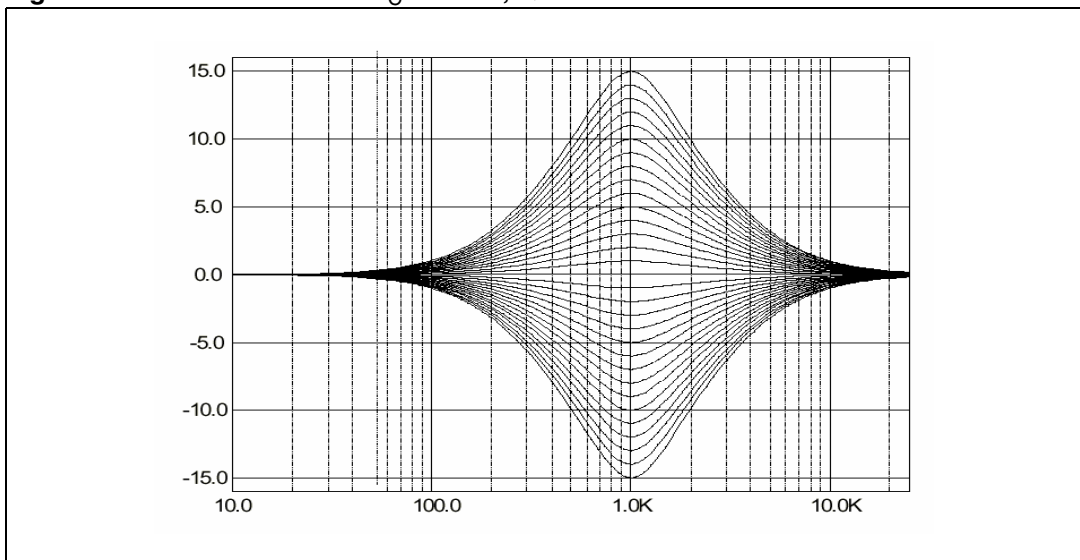
## 4.7 Middle

There are three parameters programmable in the middle stage:

### 4.7.1 Attenuation

*Figure 13* shows the attenuation as a function of frequency at a center frequency of 1 kHz.

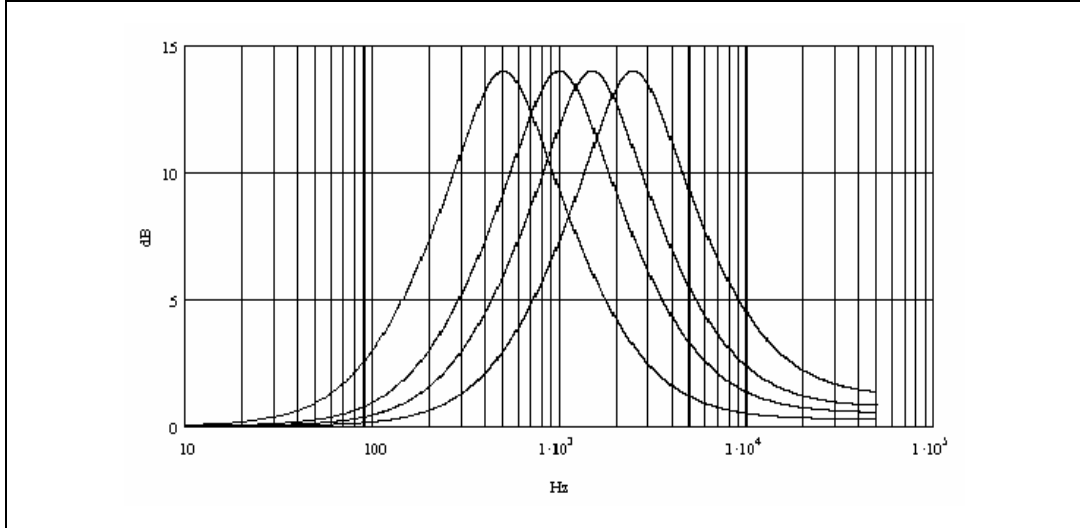
**Figure 13. Middle control @  $f_C = 1$  kHz,  $Q = 1$**



### 4.7.2 Center frequency

Figure 14 shows the four possible center frequencies 500 Hz, 1 kHz, 1.5 kHz and 2.5 kHz.

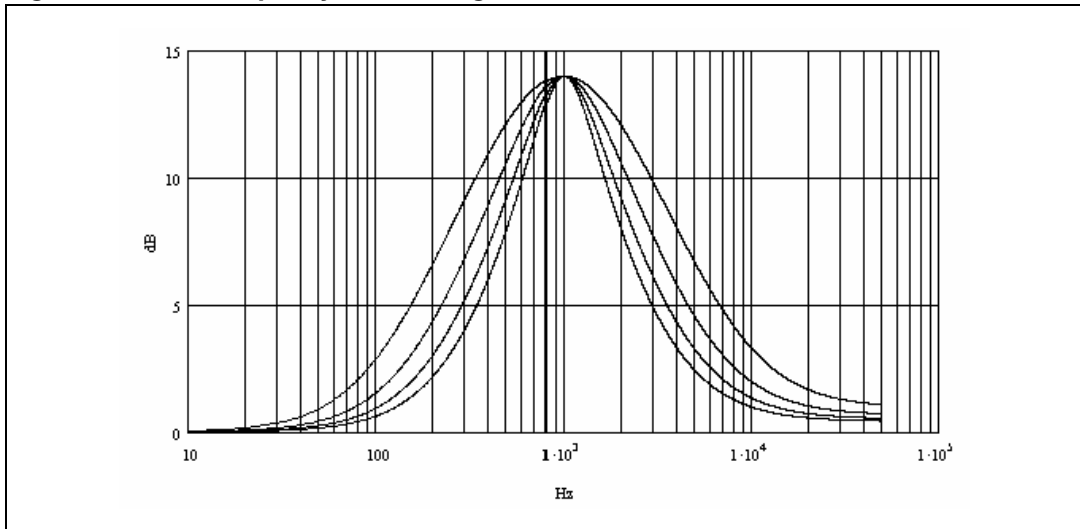
**Figure 14. Middle center frequencies @ gain = 14 dB, Q = 1**



### 4.7.3 Quality factors

Figure 15 shows the four possible quality factors 0.5, 0.75, 1 and 1.25.

**Figure 15. Middle quality factors @ gain = 14 dB, fc = 1 kHz**





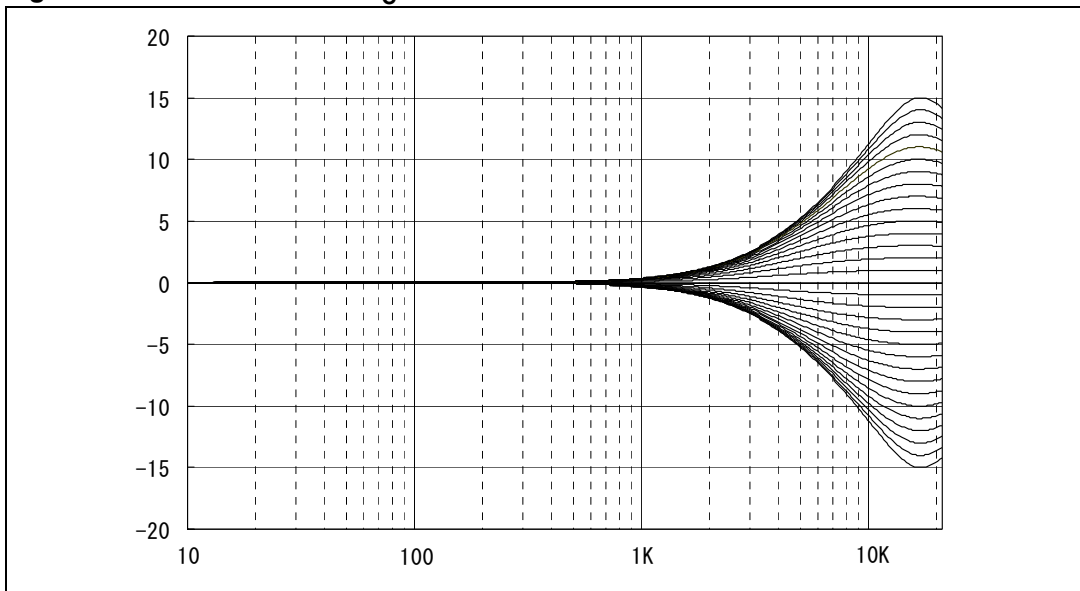
### 4.8 Treble

There are two parameters programmable in the treble stage:

#### 4.8.1 Attenuation

Figure 16 shows the attenuation as a function of frequency at a center frequency of 17.5 kHz.

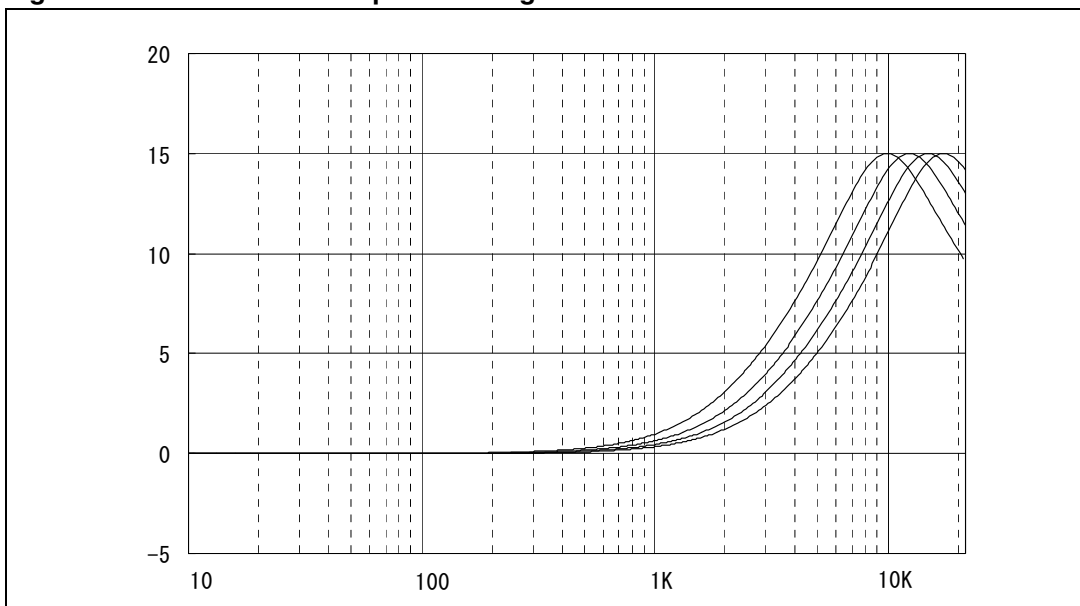
Figure 16. Treble control @  $f_c = 17.5$  kHz



#### 4.8.2 Center frequency

Figure 17 shows the four possible center frequencies 10k, 12.5k, 15k and 17.5 kHz.

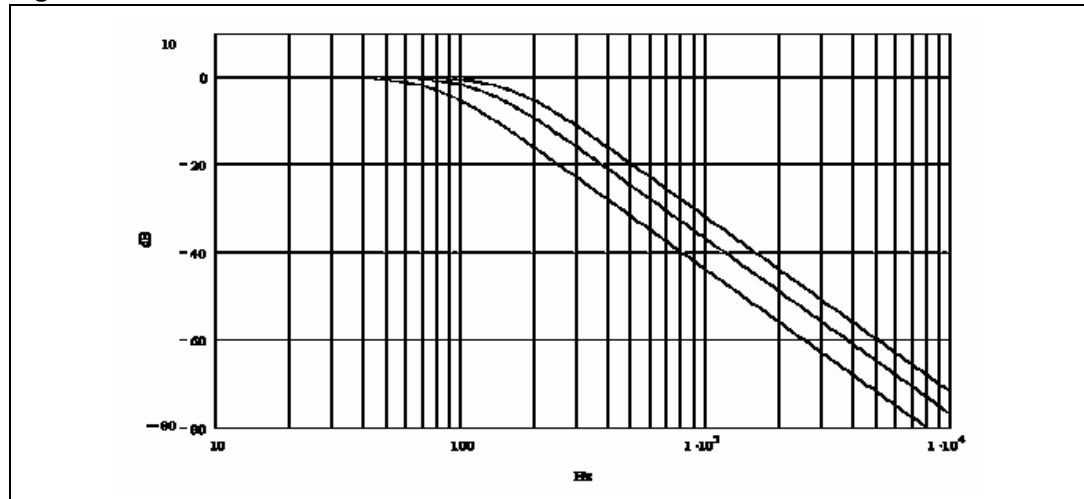
Figure 17. Treble center frequencies @ gain = 15 dB



### 4.9 Subwoofer filter

The subwoofer lowpass filter has butterworth characteristics with programmable cut-off frequency (80/120/160 Hz)

Figure 18. Subwoofer control



### 4.10 Spectrum analyzer

A fully integrated seven-band spectrum analyzer with programmable quality factor is present. The spectrum analyzer consists of seven band pass filters with rectifier and sample capacitor that stores the maximum peak signal level since the last read cycle. This peak signal level can be read by a microprocessor at the SAout pin. To allow easy interfacing to an analog port of the microprocessor, the output voltage at this pin is referred to device ground.

The microprocessor starts a read cycle with the negative going clock edge at the SAck input. On the following positive clock edges, the peak signal level for the band pass filters is subsequently switched to SAout. Each analog output data is valid after the time  $t_{Sadel}$ . A reset of the sample capacitors is induced whenever SAck remains high for the time  $t_{intres}$ . Note that a proper reset requires the clock signal SAck to be held at high potential. Figure 20 shows the block diagram and figure 21 illustrates the read cycle timing of the spectrum analyzer.

Figure 19. Spectrum analyzer block diagram

