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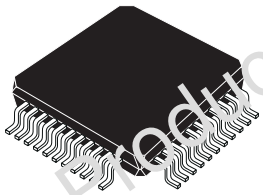
TDA7437N

Digitally controlled audio processor

Features

- Input multiplexer
  - Four stereo, one mono input, and one differential input
  - Selectable input gain for optimal adaptation to different sources
- Fully programmable loudness function
- Volume control in 1dB steps including gain up to 16dB
- Zero crossing mute, soft mute and direct mute
- Bass and treble control
- Four speaker attenuators- four independent speakers control in 1dB steps for balance and fader facilities
- Pause detector programmable threshold
- All functions programmable via serial I^2C bus



LQFP44

Description

The audioprocessor TDA7437N is an upgrade of the TDA731X audioprocessor family.

Due to a highly linear signal processing, using CMOS-switching techniques instead of standard bipolar multipliers, very low distortion and very low noise are obtained. Several new features like softmute, and zero-crossing mute are implemented. The soft Mute function can be activated in two ways either via the serial bus (Mute byte, bit D0), or directly on pin 28 through an I/O line of the microcontroller

Very low DC stepping is obtained by use of a BICMOS technology.

Order codes

Part numbers	Package	Packing
E-TDA7437N	LQFP44 (10x 10x 1.4mm)	Tray
E-TDA7437NTR	LQFP44 (10x 10x 1.4mm)	Tape and reel

Contents

List of tables

List of figures

1 PIN descriptions and electrical specifications

Figure 1. Pin description

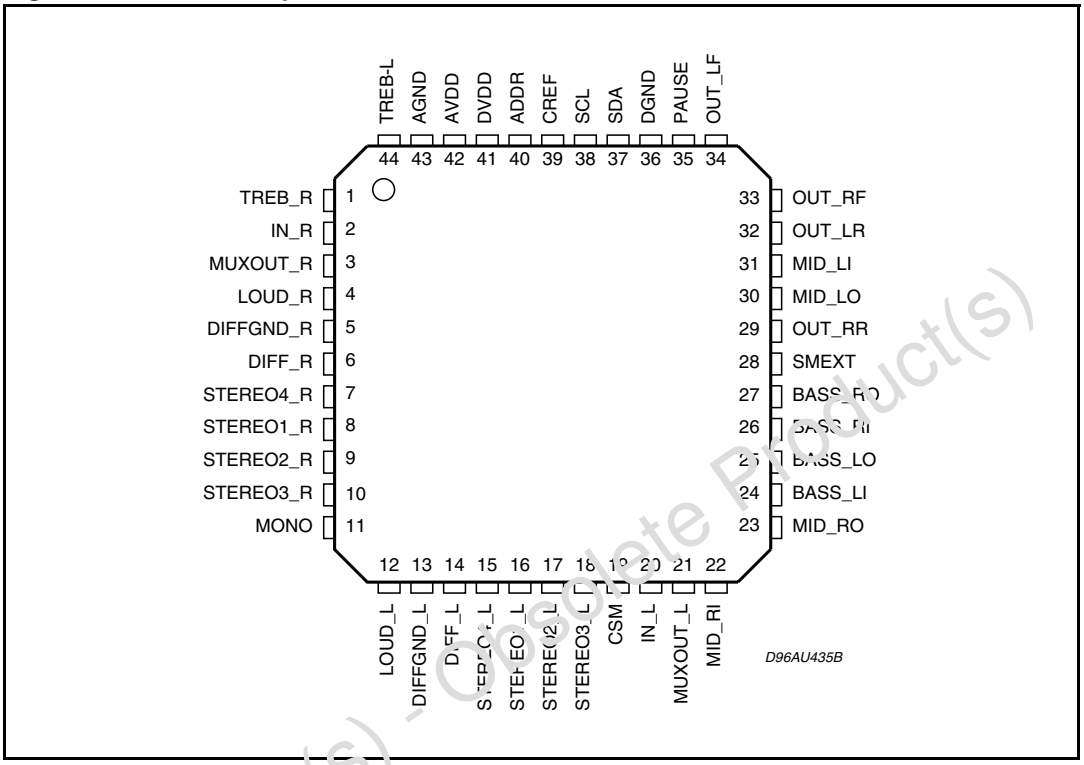


Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AV_{DD}, DV_{DD}	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to pins Max.	150	°C/W

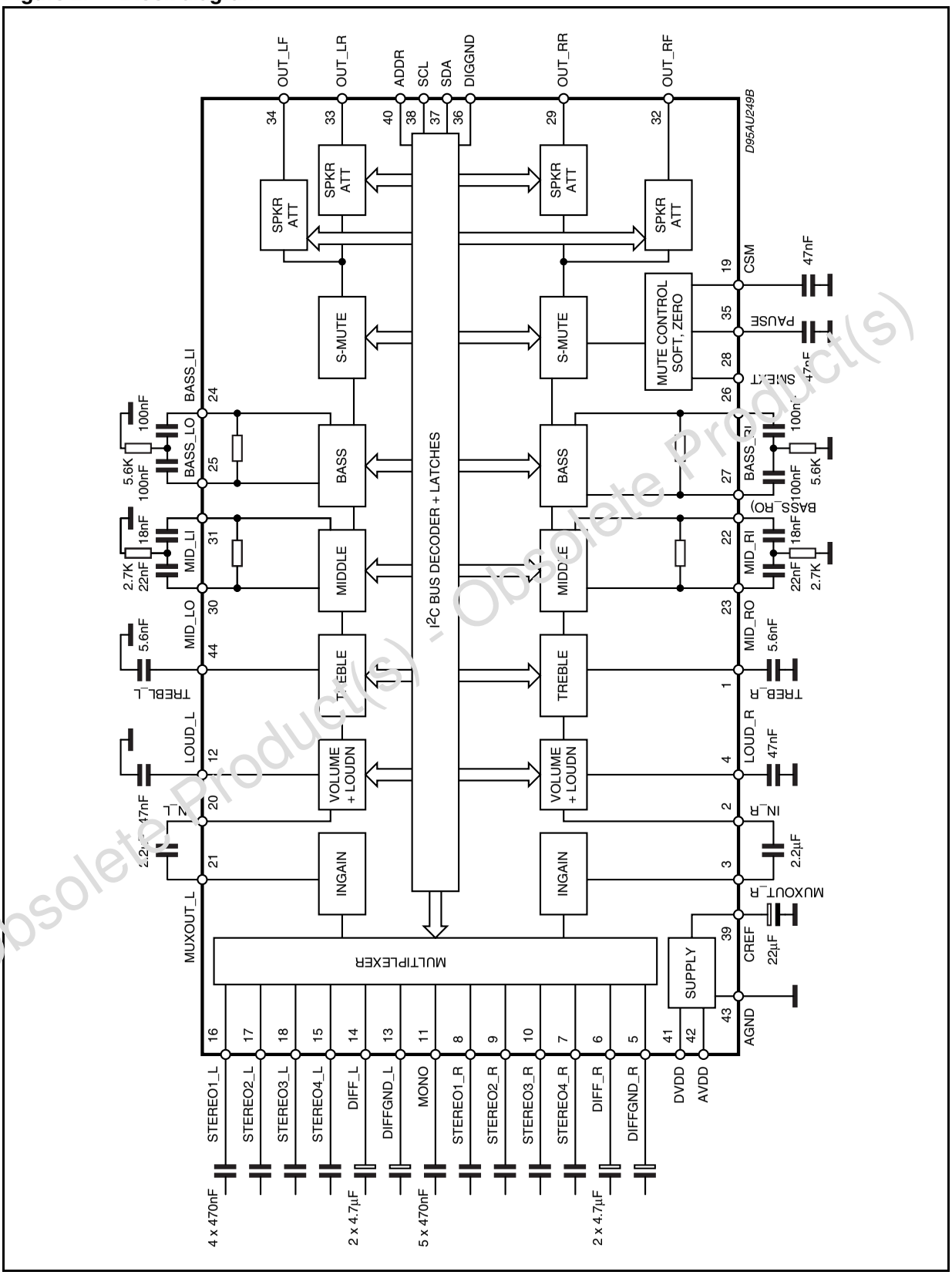
Table 3. Quick reference data

Symbol	Parameter	Min.	Typ.	Max.	Unit
AV_{DD}, DV_{DD}	Supply voltage (AVDD and DVDD must be at the same potential)	6	9	10.2	V
V_{CL}	Max. input signal handling	2.1	2.6		Vrms
THD	Total harmonic distortion V = 1Vrms f = 1KHz		0.01	0.8	%
S/N	Signal to noise ratio		111		dB
S_C	Channel separation f = 1KHz		95		dB

Table 3. Quick reference data (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Input gain 1dB step	0		15	dB
	Volume control 1dB step	-63		16	dB
	Treble control 2dB step	-14		+14	dB
	Bass control 2dB step	-14		+14	dB
	Middle control 2dB step	-14		+14	dB
	Fader and balance control 1dB step	-79		0	dB
	Loudness control 1dB step	0		20	dB
	Mute attenuation		100		dB

Figure 2. Block diagram



2 Electrical characteristics

(AV_{DD}, DV_{DD} = 9V; R_L = 10KΩ; R_g = 50Ω; T_{amb} = 25°C; all gains = 0dB; f = 1KHz. Refer to the test circuit, unless otherwise specified.)

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector (mono and stereo inputs)						
R_I	Input resistance	pin 7 to 11 and 15 to 18	70	100	130	KΩ
V_{CL}	Clipping level	d ≤ 0.3%	2.1	2.6		V_{RMS}
S_I	Input separation		80	95		dB
R_L	Output load resistance		2			KΩ
$G_{I\ MIN}$	Minimum input gain		-0.75	0	+0.75	dB
$G_{I\ MAX}$	Maximum input gain		14	15	16	dB
G_{step}	Step resolution		0.5	1.0	1.5	dB
E_a	Set error		-1.0	0	1.0	dB
V_{DC}	DC steps	Adjacent gain steps		0.5	10	mV
		G_{IMIN} to G_{IMAX}		3		mV
Differential input (Pin 5, 6, 13, 14)						
R_I	Input resistance	Input selector BIT D4 = 0 (0dB)	10	15	20	KΩ
		Input selector BIT D4 = 1(-6dB)	14	20	26	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1V_{RMS} ; f = 1KHz	45	70		dB
d	Distortion	V_I = 1V_{RMS}		0.01	0.08	%
e_{IN}	Input noise	20Hz to 20KHz; Flat; D6 = 0		5		μV
G_{DIFF}	Differential gain	D4 = 0	-1	0	1	dB
		D4 = 1	-7	-6	-5	dB
Volume control						
R_I	Input resistance	Pin 2 and 20	31	44	57	KΩ
G_{MAX}	Maximum gain		15	16	17	dB
A_{MAX}	Maximum attenuation		61	63.75	66.5	dB
A_{STEPC}	Step resolution coarse atten.		0.5	1.0	1.5	dB
E_A	Attenuation set error	G = 16 to -20dB	-1.0	0	1.0	dB
		G = -20 to -63dB	-2.75		2.75	dB
E_t	Tracking error				2	dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DC}	DC steps	Adjacent gain steps	-5		+5	mV
		Adjacent attenuation steps	-3		+3	mV
		From 0dB to A_{MAX}		0.5	5	mV
Loudness control (Pin 4, 12)						
R_I	Internal resistor	Loud = On	35	50	65	KΩ
A_{MAX}	Maximum attenuation		19	20	21	dB
A_{step}	Step resolution		0.5	1	1.5	dB
Zero crossing mute						
V_{TH}	Zero crossing threshold (1)	WIN = 11		35		mV
		WIN = 10		70		mV
		WIN = 01		140		mV
		WIN = 00		280		mV
A_{MUTE}	Mute attenuation		80	100		dB
V_{DC}	DC step	0dB to Mute		0.1	3	mV
Soft mute						
A_{MUTE}	Mute attenuation		50	65		dB
T_{DON}	ON delay time	C_{CSM} = 22nF; 0 to -20dB; I = I_{MAX}	0.8	1.5	2.0	ms
		C_{CSM} = 22nF; 0 to -20dB; I = I_{MIN}	25	45	60	ms
T_{DOFF}	OFF current	V_{CSM} = 0V; I = I_{MAX}	20	40	60	mA
		V_{CSM} = 0V; I = I_{MIN}		2		µA
R_{PINT}	Pullup resistor (pin 28)	(2)		100		KΩ
V_{SMH}	(pin 28) Level high		3.5			V
V_{SML}	(pin 28) Level low	Soft mute active			1	V
Bass control						
C_{range}	Control range		±11.5	±14	±16	dB
A_{step}	Step resolution		1	2	3	dB
R_g	Internal feedback resistance		31	44	57	KΩ
Middle control						
C_{range}	Control range		±11.5	±14	±16	dB
A_{step}	Step resolution		1	2	3	dB
R_g	Internal feedback resistance		17.5	25	32.5	KΩ

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Treble control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{step}	Step resolution		1	2	3	dB
Speaker attenuators						
C_{RANGE}	Control range			79		dB
A_{step}	Step resolution	A_V = 0 to -40dB	0.5	1	1.5	dB
A_{MUTE}	Output mute attenuation	Data word = 1111XXXX	80	100		dB
E_A	Attenuation set error	A_V = 0 to -40dB			1.5	dB
V_{DC}	DC steps	Adjacent attenuation steps		0.1	3	mV
Audio output						
V_{clip}	Clipping level	d = 0.3%	2.1	2.6		Vrms
R_L	Output load resistance		2			KΩ
R_O	Output impedance		50	90	140	W
V_{DC}	DC voltage level		3.5	3.8	4.1	V
Pause detector						
V_{TH}	Pause threshold	WIN = 11		35		mV
		WIN = 10		70		mV
		WIN = 01		140		mV
		WIN = 00		280		mV
I_{DELAY}	Pull-up current		15	25	35	µA
V_{THP}	Pause threshold			3.0		V
General						
V_{CC}	Supply voltage		6	9	10.2	V
I_{CC}	Supply current		7	10	13	mA
PSRR	Power supply rejection ratio	f = 1KHz	70	90		dB
e_{NO}	Output noise	Output muted (B = 20 to 20kHz flat)		4		µV
		All gains 0dB (B = 200 to 20kHz flat)		6	15	µV
E_t	Total tracking error	A_V = 0 to -20dB		0	1	dB
		A_V = -20 to -60dB		0	2	dB
S/N	Signal to noise ratio	All Gains = 0dB; V_O = 2.1Vrms		111		dB
S_C	Channel separation L - R		80	95		dB

Table 4. Electrical characteristics (continued)

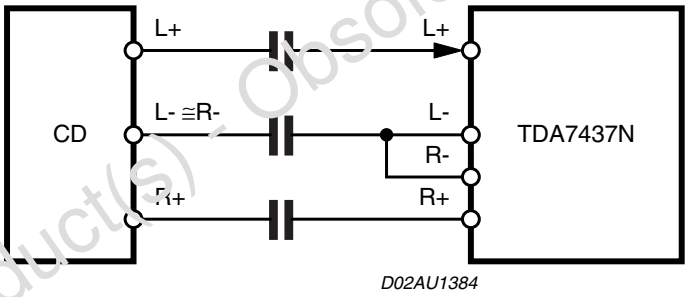
Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
d	Distortion	V_{IN} =1V all gain = 0dB		0.01	0.08	%
Bus inputs						
V_{IL}	Input low voltage				1	V
V_{IN}	Input high voltage		3			V
I_{IN}	Input current	V_{IN} = 0.4V	-5		5	µA
V_O	Output voltage SDA acknowledge	I_O = 1.6mA		0.1	0.4	V

1. WIN represents the MUTE programming bit pair D6, D5 for the zero crossing window threshold
2. Internal pullup resistor to Vs/2; "LOW" = softmute active

Note: The ANGND and DIGGND layout wires must be kept separated. A 50Ω resistor is recommended to be put as far as possible from the device.

The CLD - and CDR - can be short-circuited in applications providing 3 wires CD signal

Figure 3. CLD and CDR



CLD - = DIFFINLGND

CDR - = DIFFINRGND

3 I²C bus interface

Data transmission from the microprocessor to the TDA7437N, and vice versa, takes place through the 2 wires of the I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be externally connected).

3.1 Data validity

As shown in *Figure 4*, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

3.2 Start and stop conditions

As shown in *Figure 5* a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH. A STOP conditions must be sent before each START condition.

3.3 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

3.4 Acknowledge

The master (microprocessor) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see *Figure 6*). The peripheral (audioprocessor) that acknowledges has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse. The audioprocessor which has been addressed has to generate an acknowledgment after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

3.5 Transmission without acknowledgment

To avoid detection of the acknowledge clock pulse of the audioprocessor, the microprocessor can use a simpler transmission: it simply waits one clock pulse, and sends the new data. This is less protected from any errors and will decrease the immunity to noise.

Figure 4. Data validity

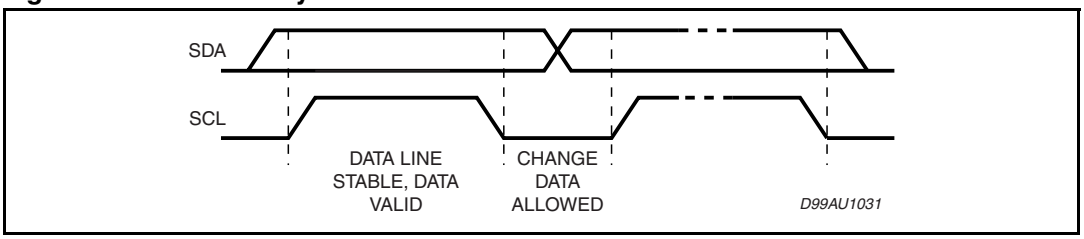


Figure 5. Timing diagram of I²C Bus

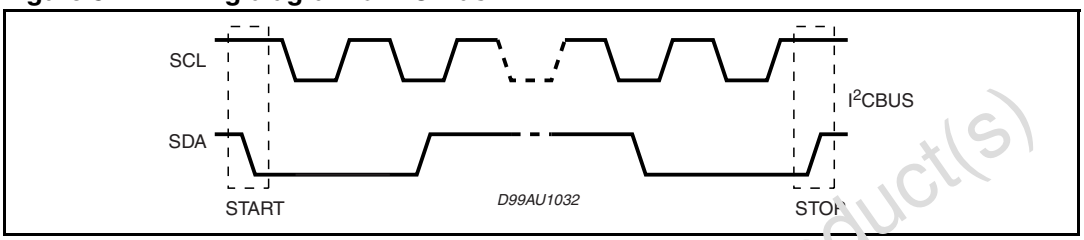
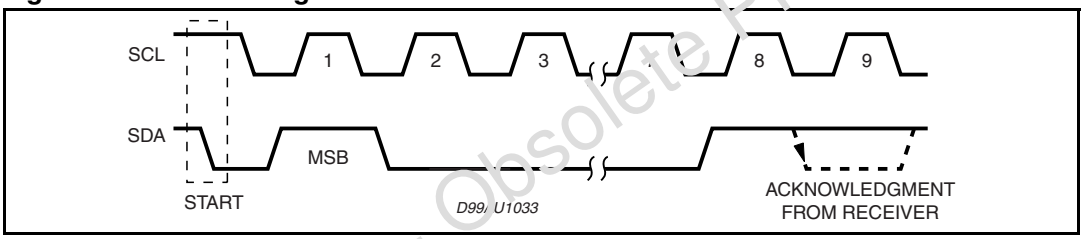


Figure 6. Acknowledge on the I²C Bus

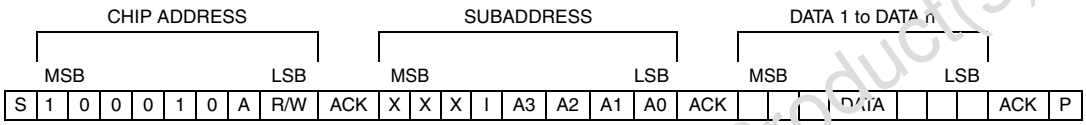


4 Software specification

4.1 Interface protocol

The interface protocol comprises of:

- A start condition (s)
- A chip address byte, (the LSB bit determines read (=1)/write (=0) transmission)
- A subaddress byte.
- A sequence of data (N-bytes + acknowledge)
- A stop condition (P)



ACK = Acknowledge; S = Start; P = Stop; I = Auto increment, X = Not used

Max clock speed 500kbits/s

ADDRpin open A = 0
ADDRpin close to Vs A = 1

4.2 Auto increment

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled.

4.3 Subaddress (receive mode)

Table 5. Subaddress (receive mode)

MSB							LSB	FUNCTION
X	X	X	I	A3	A2	A1	A0	
				0	0	0	0	Input selector
				0	0	0	1	Loudness
				0	0	1	0	Volume
				0	0	1	1	Bass, Treble
				0	1	0	0	Speaker attenuator LF
				0	1	0	1	Speaker attenuator LR
				0	1	1	0	Speaker attenuator RF
				0	1	1	1	Speaker Attenuator RR
				1	0	0	0	Input gain middle
				1	0	0	1	Mute

4.4 Transmitted data

Table 6. Send mode

MSB							LSB
X	X	X	X	X	SM	ZM	P

$\overline{P}$ = Pause (Active low)
ZM = Zero crossing muted (HIGH active)
SM = Soft mute activated (HIGH active)
X = Not used

The transmitted data is automatically updated after each ACK.
Transmission can be repeated without new chipaddress.

4.5 Data byte specification

Table 7. Data byte specification

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1	0	0	0	Differential
				1	0	0	1	Stereo 1
				1	0	1	0	Stereo 2
				1	0	1	1	Stereo 3
				1	1	0	0	Stereo 4
				1	1	0	1	Mono
X	X	X	X	0	X	X	X	DC connect (1)
		0	0					Half-diff 0dB (2)
		0	1					Half-diff -6dB (2)
		1	0					Full-diff 0dB (3)
		1	1					Full-diff -6dB (3)

1. Selected when using a 3 wire differential source (pins 5 and 13 shorted)
2. Selected when using a 4 wire differential source
3. OUTR-INR (OUTL-INR) short circuited internally (no need for external connection

Table 8. Loudness

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Loudness step
		0	0	0	0	0	0	0dB
		0	0	0	0	0	1	1dB
		0	0	0	0	1	0	2dB
		0	0	0	0	1	1	3dB

Table 8. Loudness (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	Loudness step
		0	0	0	1	0	0	4dB
		0	0	0	1	0	1	5dB
		0	0	0	1	1	0	6dB
		0	0	0	1	1	1	7dB
		0	0	1	0	0	0	8dB
		0	0	1	0	0	1	9dB
		0	0	1	0	1	0	10dB
		0	0	1	0	1	1	11dB
		0	0	1	1	0	0	12dB
		0	0	1	1	0	1	13dB
		0	0	1	1	1	0	14dB
		0	0	1	1	1	1	15dB
		0	1	0	0	0	0	16dB
		0	1	0	0	0	1	17dB
		0	1	0	0	1	0	18dB
		0	1	0	0	1	1	19dB
		0	1	0	1	0	0	20dB
		0	1	0	1	0	1	Loudness off
								Fine volume
0	0							0dB
0	1							-0.25dB
1	0							-0.5dB
1	1							-0.75dB

Table 9. Mute

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				0			1	Soft mute on
				0		0	1	soft mute with fast slope
				0		1	1	Soft mute with slow slope
			0	0	1			Zero mute
				1				Direct mute
			1					Reset

Table 9. Mute (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
	0	0	0					Zero cross window (280mV)
	0	1	0					Zero cross window (140mV)
	1	0	0					Zerocross window (70mV)
	1	1	0					Zerocross window (35mV)
0								Non symmetrical bass
1								Symmetrical bass

Table 10. Volume

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
1					0	0	0	0dB
1					0	0	1	-1dB
1					0	1	0	-2dB
1					0	1	1	-3dB
1					1	0	0	-4dB
1					1	0	1	-5dB
1					1	1	0	-6dB
1					1	1	1	-7dB
1								
1	0	0	0	0				16dB
1	0	0	0	1				8dB
1	0	0	1	0				0dB
1	0	0	1	1				-8dB
1	0	1	0	0				-16dB
1	0	1	0	1				-24dB
1	0	1	1	0				-32dB
1	0	1	1	1				-40dB
1	1	0	0	0				-48dB
1	1	0	0	1				-56dB
0	X	X	X	X	X	X	X	Mute

Table 11. Speaker

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								1.25dB step
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	Mute

Table 12. Bass treble

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble step
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB

Table 12. Bass treble (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB
								Bass steps
0	0	0	0					-14dB
0	0	0	1					-12dB
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					0dB
1	1	1	1					0dB
	1	1	0					2dB
1	1	0	1					4dB
	1	0	0					6dB
1	0	1	1					8dB
	0	1	0					10dB
1	0	0	1					126B
1	0	0	0					14dB

Table 13. Input stage gain middle

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
								In-gain step
				0	0	0	0	0dB
				0	0	0	1	1dB
				0	0	1	0	2dB
				0	0	1	1	3dB

Table 13. Input stage gain middle (continued)

MSB							LSB	Function
D7	D6	D5	D4	D3	D2	D1	D0	
				0	1	0	0	4dB
				0	1	0	1	5dB
				0	1	1	0	6dB
				0	1	1	1	7dB
				1	0	0	0	8dB
				1	0	0	1	9dB
				1	0	1	0	10dB
				1	0	1	1	11dB
				1	1	0	0	12dB
				1	1	0	1	13dB
				1	1	1	0	14dB
				1	1	1	1	15dB
								Middle step
0	0	0	0					-14dB
0	0	0	1					-12dB
0	0	1	0					-10dB
0	0	1	1					-8dB
0	1	0	0					-6dB
0	1	0	1					-4dB
0	1	1	0					-2dB
0	1	1	1					0dB
1	1	1	1					0dB
1	1	1	0					2dB
1	1	0	1					4dB
1	1	0	0					6dB
1	0	1	1					8dB
1	0	1	0					10dB
1	0	0	1					126B
1	0	0	0					14dB

5 Mute and pause features

The TDA7437N provides three types of mute, controlled via I^2C bus (see *Table 9* Mute byte register).

5.1 Soft mute

Bit **D0 = 1 → Soft mute ON**

Bit **D0 = 0 → Soft mute OFF**

It allows an automatic soft muting and unmuting of the signal.
The time constant is fixed by an external capacitor Csm inserted between pin Csm and ground.

Once the external capacitor is fixed, two different slopes (time constant) are selectable by programming of bit D1.

Bit **D1 = 0 → fast slope (I=Imax)**

Bit **D1 = 1 → slow slope (I=Imin)**

The soft mute generates a gradually decreasing signal, avoiding big click noise of an immediate high attenuation, without necessity to program a sequence of decreasing volume levels. A response example is reported in *Figure 11* (mute), and *Figure 12* (unmute). The final attenuation obtained with soft mute ON is 60dB typical. The used reference parameter is the delay time taken to reach 20dB attenuation (no matter what the signal level is).

Using a capacitor Csm = 22nF this delay is:

d = 1. 8mswhen selected Fast slope mode (bit D1=0)

d = 25 ms when selected Slow slope mode (bit D1=1

In the application, the soft mute ON programming should be followed by programming of direct mute on (see *5.2*), in order to achieve a final 100dB attenuation. In addition to the I^2C bus programming, the Soft Mute ON can be generated in a fast way by forcing a LOW level at pin SMEXT (TTL Level compatible). This approach is recommended for fast RDS AF switching.

The Soft Mute status can be detected via I^2C bus, reading the Transmitted Byte, bit SM (see *Table 6*).

read bit SM = 1 soft mute status ON

read bit SM = 0 soft mute status OFF

5.2 Direct mute

bit **D3 = 1** Direct mute ON

bit **D3 = 0** Direct mute OFF

The direct mute bit forces an internal immediate signal connection to ground.
It is located just before the Volume/Loudness stage, and gives a typical 100dB attenuation.

5.3 Speakers mute

An additional direct mute function is included in the speakers attenuators stage.

The four output LF, RF, LR, RR can be separately muted by setting the speaker attenuator byte to the value 01111111 binary.

Typical attenuation level 100dB. This mute is useful for fader and balance functions. It should not be applied for system mute/unmute, because it can generate noise due to the offset of previous stages (bass / treble).

5.4 Zero crossing mute

bit **D2 = 1 D4 = 0** zero crossing mute ON

bit **D2 = 0 D4 = 0** zero crossing mute OFF

The mute activation/deactivation is delayed until the signal waveform crosses the DC zero level (Vref level).

The detection works separately for left and right channels (see *Figure 13* and *Figure 14*). Four different window thresholds are software selectable by two dedicated bits.

bit **D6**	bit **D5**	**Window**
0	**0**	Vref DC +/-280mV
0	**1**	Vref DC +/-140mV
1	**0**	Vref DC +/-70mV
1	**1**	Vref DC +/-35mV

The zero crossing mute activation/deactivation starts when the AC signal level falls inside the selected window (internal comparator).

The zero crossing mute (and pause) detector is always active. It can be disabled, if the feature is not used, by forcing the bit **D4 = 1** Zero crossing and pause detector reset.

In this way the internal comparator logic is stopped, eliminating its switching noise.

The zero cross mute status is detected reading the transmitted byte bit ZM.

bit **ZM = 1** zero cross mute status ON

bit **ZM = 0** zero cross mute status OFF

5.5 Pause function

On chip is implemented by a pause detector block.

It uses the same 4 windows threshold selectable for the zero crossing mute, bit D6,D5 byte MUTE (see above). The detector can be put into OFF by forcing bit **D4 = 1**, otherwise it is active.

Pause detector information is available at the PAUSE pin. A capacitor must be connected between the PAUSE pin and ground.

When the incoming signal is detected to be outside the selected window, the external capacitor is discharged. When the signal is inside the window, the capacitor is integrating up (see *Figure 15* and *Figure 16*).

a) by reading directly the Pause pin level.The ON/OFF voltage threshold is 3.0V typical. Pause OFF = level low (< 3.0V) Pause ON = level high (; 3.0V)

b) by reading via I2C bus the transmitted byte, bit PP = 0 pause active. P = 1 no pause detected. The external capacitor value fixes the time constant.

The pull up current is 25uV typical, with input signal

Vin = 1Vrm --; Vdc pin pause = 15mV

Vin = 0Vrms --; Vdc pin pause = 5.62V

For example choosing Cpause = 100nF the charge up constant is about 22ms. Instead with Cpause = 15nF the charge up constant is about 360µs.

The pause detection is useful in applications like RDS, to perform noiseless tuning frequency jumps, avoiding the use of the mute.

5.6 No symmetrical bass cut response

bit **D7 = 0** No symmetrical

bit **D7 = 1** Symmetrical

The bass stage has the option to generate an unsymmetrical response, for cut mode settings (bass level from -2db to - 14dB)

For example using a T-type band pass external

The feature is useful for human ear equalization in a noisy environment, like a car.

See examples in *Figure 17* (symmetrical response) and *Figure 18* (unsymmetrical response).

5.7 Transmitted data (send mode)

bit**P = 0**Pause active

bit**P = 1**No pause detected

bit**ZM = 1**Zero cross mute ON

bit**ZM = 0**Zero cross mute OFF

bit**SM = 1**Soft mute ON

bit**SM = 0**Soft mute OFF

bit**ST = 1**Stereo signal detected (input MPX)

bit**ST = 0**Mono signal detected (input MPX)

The TDA7437N allows the reading of four info bits.

The type (stereo/mono) of received broadcasting signal is easily checked and displayed by using the **ST** bit.

The **P** bit check is useful in tuning jumps without signal muting.

The **SM** soft mute status becomes active immediately, when bit D0 is set to 1 (soft mute ON, MUTE byte) and not when the signal level has reached the 60 dB final attenuation.

5.8 TDA7437N I^2C bus protocol

The protocol is standard I^2C, using subaddress byte plus data bytes (as shown within *Chapter 4*).

The optional autoincrement mode allows to refresh all the bytes registers with transmission of a single subaddress, reducing drastically the total transmission time.

Without autoincrement, subaddress bit **I = 0**, to refresh all the bytes registers (10), it is necessary to transmit 10 times the chip address, the subaddress and the data byte.

Working with a 100Kb/s clock speed the total time would be :

[(9*3+2)*10]bits*10us=2.9ms

Instead using autoincrement mode, subaddress bit I=1, the total time will be:

(9*12+2)*10us=1.1ms.

The autoincrement mode is useful also to refresh partially the data. For example to refresh the 4 speakers attenuators it is possible to program the subaddress Spkr LF (code XX010100), followed by the data byte of SPKR LF, LR, RF, RR in sequence.

Note: that the autoincrement mode has a module 16 counter, whereas the total used register bytes are 10.

It is not correct to refresh all the 10 bytes starting from a subaddress different than XX010000.

For example, using subaddress XX010010 (volume), the registers from Volume to Mute (see *Table 5*) are correctly updated, but the next two transmitted bytes, refer instead to the wanted input selector, and Loudness are discharged. (the solution in this case is to send two separate patterns in autoincrement mode, the first composed by address, subaddress XX010010, 8 data bytes, and the second composed by address, subaddress XX010000, 2 data bytes).

With autoincrement disabled, the protocol allows the transmission in sequence of N data bytes of a specific register, without the necessity to resend the address and subaddress bytes, each time.

This feature can be implemented, for example, if a gradual volume change has to be performed (the MCU does not send the STOP condition, but keeps the TDA7437N communication active).

Warning: The TDA7437N always needs to receive a STOP condition, before beginning a new START condition. The device doesn't recognize a START condition if a previously active communication was not ended by a STOP condition.