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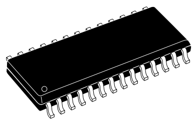
Car radio signal processor

Not For New Design

Features

- High performance signal processor for car radio systems
- Device includes audio processor, stereo decoder, noise blanker and multipath detector
- No external components required
- Fully programmable via I^2C bus
- Low distortion
- Low noise



SO-28

Description

The TDA7461 is a high performance signal processor specifically designed for car radio applications.

The device includes a complete audioprocessor and a stereo decoder with noise blanker, stereo blend and all signal processing functions necessary for state-of-the-art as well as future car radio systems.

Switched-capacitors design technique allows to obtain all these features without external components or adjustments. This means that higher quality and reliability walks alongside an overall cost saving. The CSP is fully programmable by I^2C bus interface allowing to customize key device parameters and especially filter characteristics.

The BiCMOS process combined with the optimized signal processing assure low noise and low distortion performances.

Table 1. Device summary

Order code	Package	Packing
TDA7461ND	SO-28	Tube
TDA7461NDTR	SO-28	Tape and reel
E-TDA7461ND(1)	SO-28	Tube
E-TDA7461NDTR(1)	SO-28	Tape and reel

1. Device in ECOPACK® package, see *Chapter 7: Package information on page 46*.

Contents

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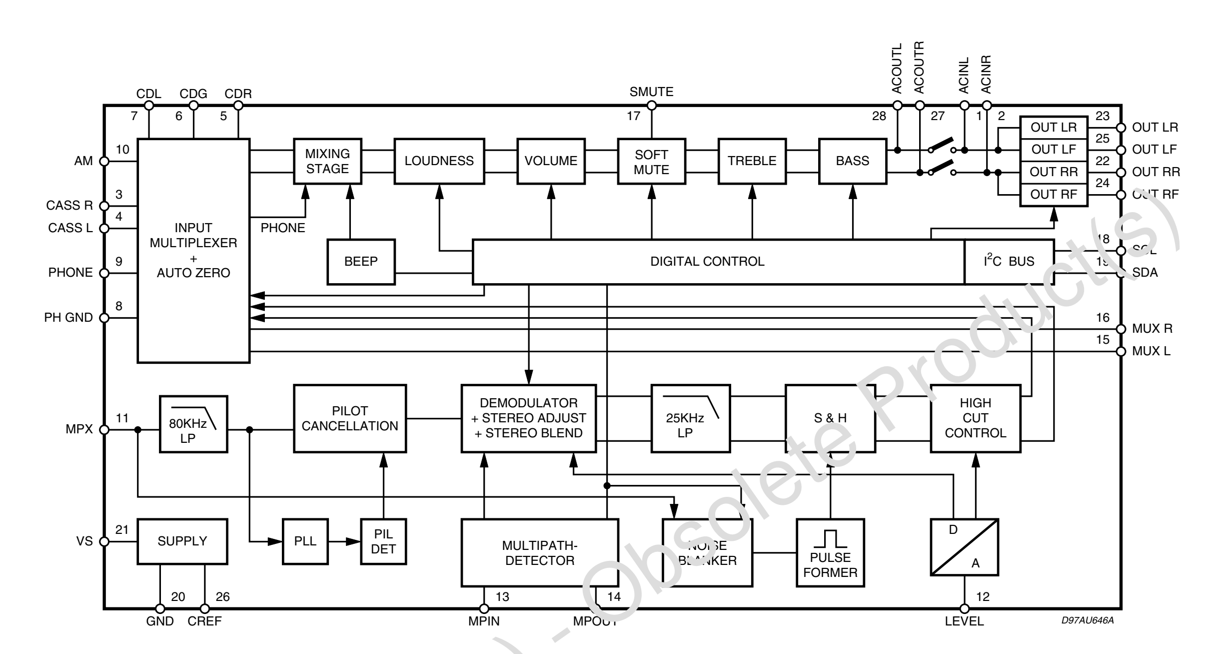
List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

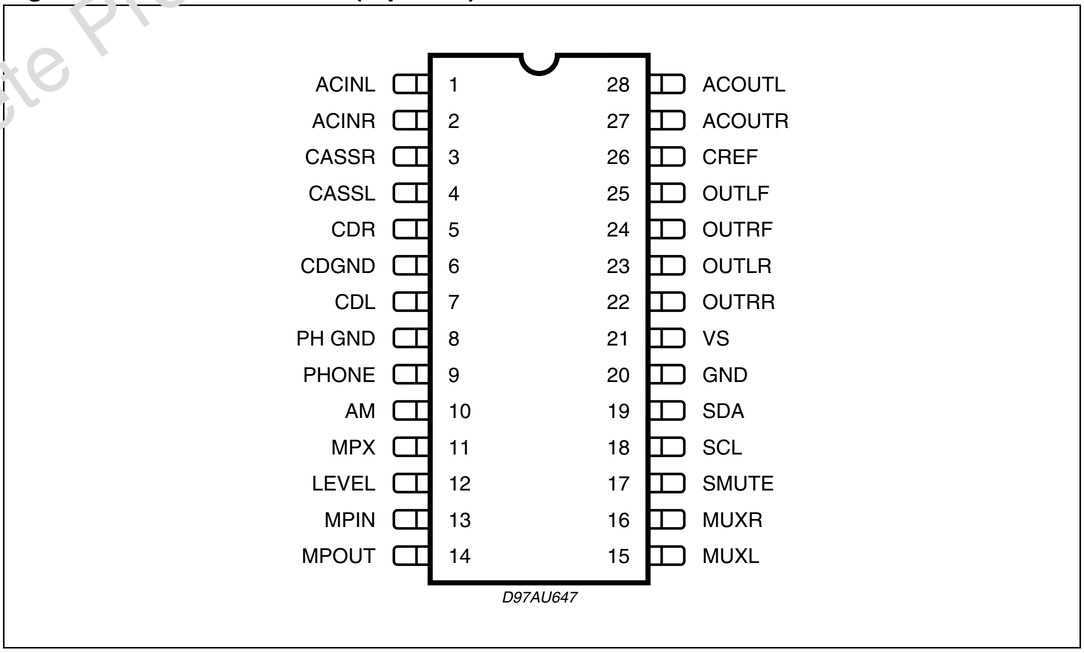


Table 2. Pin description

N.	Name	Function	Type
1	ACINL	Speaker stage input left	I
2	ACINR	Speaker stage input right	I
3	CASSR	Cassette input right	I
4	CASSL	Cassette input left	I
5	CDR	CD right channel input	I
6	CDGND	Ground reference CD	I
7	CDL	CD left channel input	I
8	PHGND	Phone ground	I
9	PHONE	Phone input	I
10	AM	AM input	I
11	MPX	FM input (MPX)	I
12	LEVEL	Level input stereo decoder	I
13	MPIN	Multipath detector input	I
14	MPOUT	Multipath detector output	O
15	MUXL	Multiplexer output left channel (stereo decoder output left selectable [1]	O
16	MUXR	Multiplexer output right channel (stereo decoder output right selectable [1])	O
17	SMUTE	Soft mute drive	I
18	SCL	I^2C clock line	I/O
19	SDA	I^2C data line	I/O
20	GND	Supply ground	S
21	VS	Supply voltage	S
22	OUTRR	Right rear speaker output	O
23	OUTLR	Left rear speaker output	O
24	OUTRF	Right front speaker output	O
25	OUTLF	Left front speaker output	O
26	CREF	Reference capacitor pin	S
27	ACOUTR	Pre-speaker AC output right channel	O
28	ACOUTL	Pre-speaker AC output left channel	O

1. See data byte specification - speaker attenuator

Pin type:

I = Input
O = Output
I/O = Input/Output
S = Supply

2 Electrical specification

2.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	10.5	V
T_{amb}	Operating ambient temperature range	-40 to 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

2.2 Supply

Table 4. Supply

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage		7.5	9	10	V
I_S	Supply current	V_S = 9V	25	30	35	mA
SVRR	Ripple rejection @ 1 kHz	Audioprocessor (all filters flat)		60		dB
		Stereo decoder + Audioprocessor		45		dB

2.3 ESD

All pins are protected against ESD according to the MIL883 standard.

2.4 Thermal data

Table 5. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}pins}$	Thermal resistance junction to pins max	85	°C/W

2.5 Audio processor part feature

2.5.1 Input multiplexer

- Fully differential or quasi-differential CD and cassette stereo input
- AM mono or stereo input
- Phone differential or single ended input
- Internal beep with 2 frequencies (selectable)
- Mixable phone and beep signals
- Loudness
- Second order frequency response
- Programmable center frequency and quality factor
- 15 x 1 dB steps
- Selectable flat-mode (constant attenuation)

2.5.2 Volume control

- 1 dB attenuator
- Max. gain 20 dB
- Max. attenuation 79 dB
- Soft-step gain control

2.5.3 Bass control

- 2^{nd} order frequency response
- Center frequency programmable in 4 (5) steps
- DC gain programmable
- 7 x 2 dB steps

2.5.4 Treble control

- 2^{nd} order frequency response
- Center frequency programmable in 4 steps
- 7 x 2 dB steps

2.5.5 Speaker control

4 independent speaker controls (1 dB steps control range 50 dB)

2.5.6 Mute function

- Direct mute
- Digitally controlled softmute with 4 programmable time constants

2.6 Audio processor electrical characteristics

Table 6. Audio processor electrical characteristics
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Input selector						
R_{in}	Input resistance	all inputs except phone	70	100	130	KΩ
V_{CL}	Clipping level		2.2	2.6		VRMS
S_{IN}	Input separation		80	100		dB
$G_{IN\ MIN}$	Min. input gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. input gain		13	14	15	dB
G_{STEP}	Step resolution		1	2	3	dB
V_{DC}	DC Steps	Adjacent gain step	-5	0	+5	mV
		G_{MIN} to G_{MAX}	-5	1	+5	mV
Differential CD stereo input						
Rin	Input resistance	Differential	70	100	130	KΩ
		Common mode	20	30	40	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1 V_{RMS} @ 1 kHz	45	70		dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	45	60		dB
eN	Output noise @ speaker output	20 Hz to 20 kHz flat; all stages 0dB		9	15	µV
Differential phone input						
R_{in}	Input resistance	Differential	10	15	20	KΩ
		Common mode	20	30	40	KΩ
CMRR	Common mode rejection ratio	V_{CM} = 1 V_{RMS} @ 1 kHz	45	70		dB
		V_{CM} = 1 V_{RMS} @ 10 kHz	45	60		dB
Beep control						
V_{RMS}	Beep level		250	350	500	mV
f_{BMIN}	Lower beep frequency		570	600	630	Hz
f_{BMAX}	Higher beep frequency		1.15	1.2	1.25	KHz
Mixing control						
M_{LEVEL}	Mixing level	Source	-1	0	1	dB
		Source	-5	-6	-7	dB
		Source	-10	-12	-14	dB
		Beep/Phone	-1	0	1	dB
Volume control						
G_{MAX}	Max gain		19	20	21	dB
A_{MAX}	Max attenuation		-83	-79	-75	dB

Table 6. **Audio processor electrical characteristics (continued)**
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
A_{STEP}	Step resolution		0.5	1	1.5	dB
E_A	Attenuation set error	G = -20 to 20 dB	-1.25	0	1.25	dB
		G = -60 to 20 dB	-4	0	3	dB
E_T	Tracking error				2	dB
V_{DC}	DC steps	Adjacent attenuation steps	-3	0.1	3	mV
		From 0 dB to GMIN	-7	0.5	+7	mV
LOudness control						
A_{STEP}	Step resolution		0.5	1	1.5	dB
A_{MAX}	Max. attenuation		-16	-15	-14	dB
f_{CMIN}	Lower center frequency		180	200	220	Hz
f_{CMAX}	Higher center frequency		360	400	440	Hz
Soft mute						
A_{MUTE}	Mute attenuation		60	100		dB
T_D	Delay time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	20	40.4	60	ms
		T4	200	324	600	ms
V_{THlow}	Low threshold for SM pin(1)				1	V
V_{THhigh}	High threshold for SM pin		2.5			V
R_{PU}	Internal pull-up resistor		70	100	130	KΩ
V_{PU}	Pull-up voltage			4.7		V
Soft step						
T_{SW}	Switch time		5	10	15	ms
Bass control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
f_C	Center frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100(2)	110	Hz
Q_{BASS}	Quality factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	

Table 6. Audio processor electrical characteristics (continued)
(V_S = 9 V; T_{amb} = 25 °C; R_L = 10 kΩ; all gains = 0 dB; f = 1 kHz; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
DC_{GAIN}	Bass-DC-gain	DC = off	-1	0	+1	dB
		DC = on	4	4.4	6	dB
Treble control						
C_{RANGE}	Control range		±13	±14	±15	dB
A_{STEP}	Step resolution		1	2	3	dB
fc	Center frequency	f_{C1}	8	10	12	KHz
		f_{C2}	10	12.5	15	KHz
		f_{C3}	12	15	18	KHz
		f_{C4}	14	17.5	21	KHz
Speaker attenuator						
C_{RANGE}	Control range		-58	-50	-47	dB
A_{STEP}	Step resolution		0.5	1	2	dB
A_{MUTE}	Output mute attenuation		80	90		dB
E_E	Attenuation set error		-2		2	dB
V_{DC}	DC steps			0.1	5	mV
Audio outputs						
V_{CLIP}	Clipping level		2.2	2.6		V_{RMS}
R_L	Output load resistance		2			KΩ
C_L	Output load capacitance				10	nF
R_{OUT}	Output Impedance			30	100	W
V_{DC}	DC voltage level		3.6	3.8	4.0	V
General						
e_{NO}	Output noise	BW = 20 Hz to 20 kHz output muted		3	15	µV
		all gain = 0 dB BW = 20 Hz to 20 kHz		6.5	15	µV
S/N	Signal to noise ratio	all gain = 0 dB flat; V_O = 2 V_{RMS}		106		dB
		bass treble at 12 dB; V_O = 2.6V_{RMS}		100		dB
d	Distortion	V_{IN}= 1 V_{RMS}; all stages 0 dB		0.002	0.1	%
		V_{IN}= 1 V_{RMS}; bass & treble = 12 dB		0.05	0.1	%
S_C	Channel separation left/right		80	100		dB
E_T	Total tracking error	A_V = 0 to -20 dB	-1	0	1	dB
		A_V= -20 to -60 dB	-2	0	2	dB

1. The SM pin is active low (Mute = 0)
2. See description of audioprocessor part - bass & treble filter characteristics programming

3 Description of the audio processor part

3.1 Programmable input matrix

The programmable input matrix of the TDA7461 offers several possibilities to adapt the audioprocessor to the desired application. In to the standard application we have:

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereo decoder input.

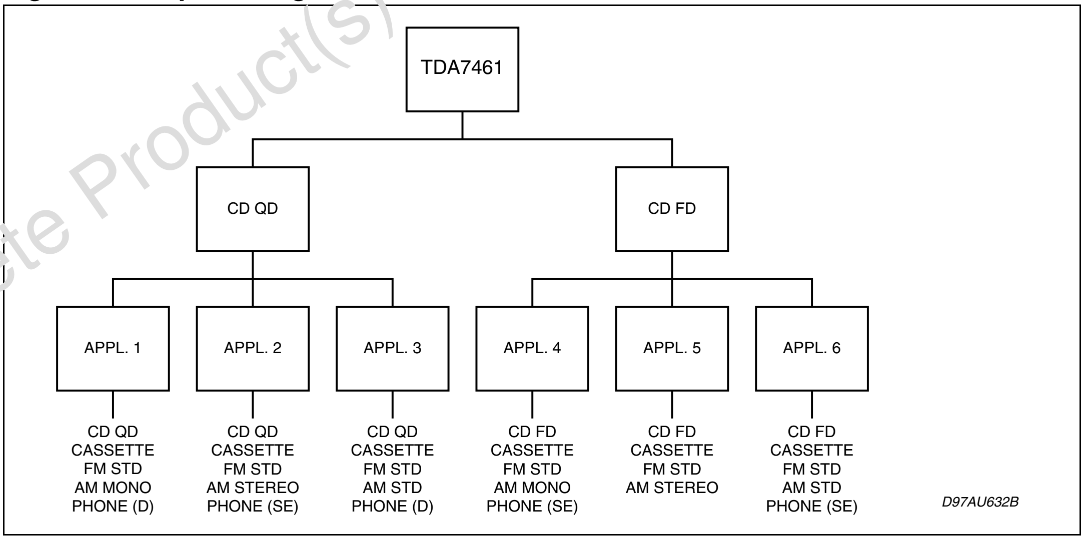
The input matrix can be configured by only 2 bits: bits 3 and 4 of subaddress 0. Basically the bit of subaddress 13 is fixed by the application and has to be programmed only once at the startup of the IC.

For many configurations the two bits are also fixed during one application (e.g. the standard application) and a change of the input source can be done by loading the first three bits of subaddress 0.

In other configurations for some sources a programming of bit 3 and 4 of subaddress 0 is necessary in addition to the three source selection bits. In every case only the subaddress 0 has to be changed to switch from one source to another.

The following picture shows the input and source programming flow:

Figure 3. Input configuration tree



1. In AMSTD configuration the AM mono signal is lead through the FM stereo decoder part to use its additional filters.

Table 7. Input and source programming

Appl. N#	Pin number				Programming [1]	
	6	8	9	10		
1	CD_{GND}	$Phone_{GND}$	Phone	AM_{MONO}	Startup	0/xxx11xxx
2	CD_{GND}	$Phone_{GND}$	AMRIGHT	AM_{LEFT}	Startup	0/xxxx1xxx
					FM	0/xxx11100
					AM	0/xxx01011
					Phone	0/xxx11010
3	CD_{GND}	$Phone_{GND}$	Phone	AMSTD	Startup	0/xxxx1xxx
					FM	0/xxx11100
					AM	0/xxx01100
					Phone	0/xxx11010
4	CDR_{GND}	CDL_{GND}	Phone	AM_{MONO}	Startup	0/xxxx0xxx
5	CDR_{GND}	CDL_{GND}	AMRIGHT	AM_{LEFT}	Startup	0/xxxx0xxx
					FM	0/xxx10100
					AM	0/xxx00011
6	CDR_{GND}	CDL_{GND}	Phone	AM_{STD}	Startup	0/xxxx0xxx
					FM	0/xxx10100
					AM	0/xxx00100
					Phone	0/xxx10010

1. Syntax 0/xxx11100 means: SUBADDRESS = 0 - DATA BYTE = xxx11100 (x - don't care).

3.1.1 How to find the right input configuration

The best way to come to the desired configuration may be to go through the application tree from the top to the bottom while making the specific decisions.

This way will lead to one of the six possible applications. Then take the number of the application and go into the pinning table. Here you will find the special pinout as well as the special programming codes for selecting sources.

For example in Appl. 6 the TDA7461 has to be configured while startup with the data byte 0/xxxx0xxx.

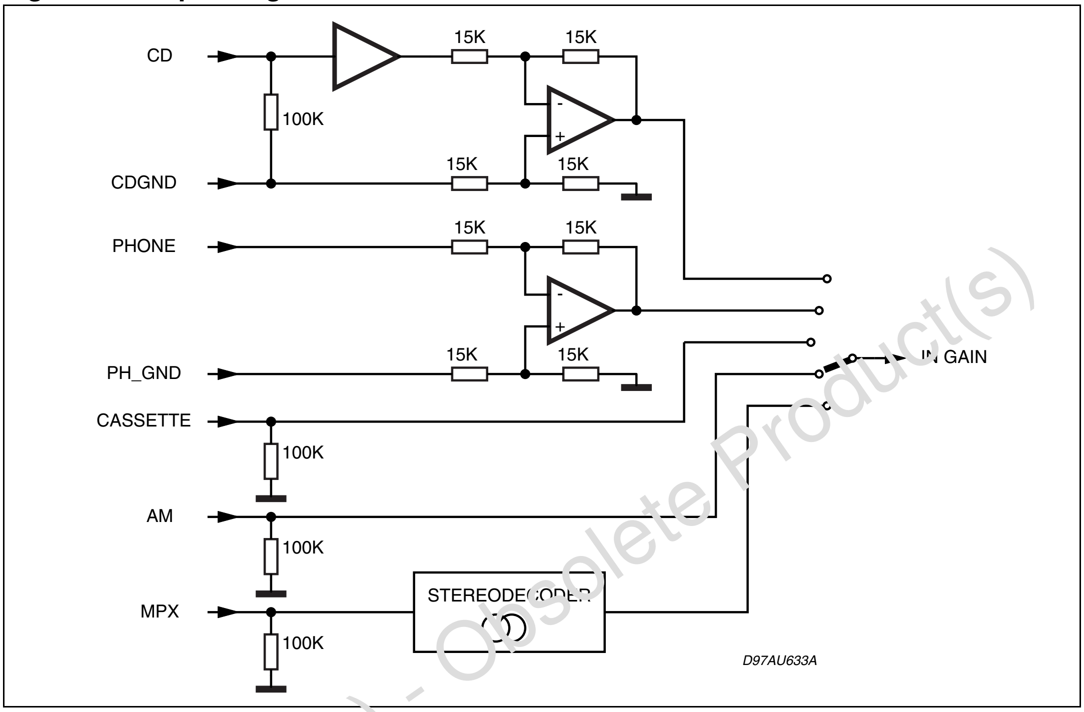
To select the FM, AM or phone source the last five significant bits of subaddress 0 have to be changed, for any other source the last three bits are sufficient (see data byte specification).

3.1.2 Input stages

Most of the input circuits are the same as in previous ST audio processors with exception of the CD inputs (see *Figure 4*). In the meantime there are some CD players in the market having a significant high source impedance which affects strongly the common mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common mode rejection even with those CD players.

The TDA7461 can be configured with an additional input; if the AC coupling before the speaker stage is not used (bit 7 in subaddress 5 set to "1") ACINL and ACINR pins can be used as an additional stereo input.

Figure 4. Input stages



3.1.3 AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid that effect a special offset cancellation stage called AutoZero is implemented.

To avoid audible clicks the audioprocessor is muted before the loudness stage during this time. In some cases, for example if the µP is executing a refresh cycle of the I^2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7461 could be switched in the "Auto Zero Remain" mode (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

3.2 Mux output

The MUX_L and MUX_R outputs can provide selectively the output of the input multiplexer (Speaker RF register, Byte 8, bit 6=1) or the output of the stereo decoder (Speaker RF register Byte 8 bit 6=0).

If bit D3 byte 10 (Stdec Register) is set to 1, then the stdec signal is automatically muted, when another source is selected at the input multiplexer.

If bit D3 byte 10 (Stdec Register) is set to 0, then the stdec signal will be always available at the Mux out pins, no matter which is the selected source.

The selection of the stereodecoder input, via a special procedure, is recommended.

1. Soft Mute or Mute the signal path
2. Temporary deselect the stereodec
3. Wait 100-200 ms to allow the stdec internal filters to settle
4. Select sterodec input (with automatic autozero)

This procedure guarantees an optimum offsetcancellation, avoiding big DC offsets due to the autozero circuitry, which otherwise could try to compensate the signal sourced at the MPX input instead of the stereodecoder intrinsic offset.

3.3 Mixing stage

This stage offers the possibility to mix the internal beep or the phone signal to any other source.

Due to the fact that the mixing stage is also located behind the In-Gain stage fine adjustments of the main source level can be done in this way.

3.3.1 Loudness

There are four parameters programmable in the loudness stage (see *Figure 5*, *6* and *7*):

- Attenuation
- Center frequency
- Loudness Q
- Flat Mode: in this mode the loudness stage works as a 0 - 15dB attenuator.

Figure 5. Loudness attenuation @ fc = 400 Hz (second order)

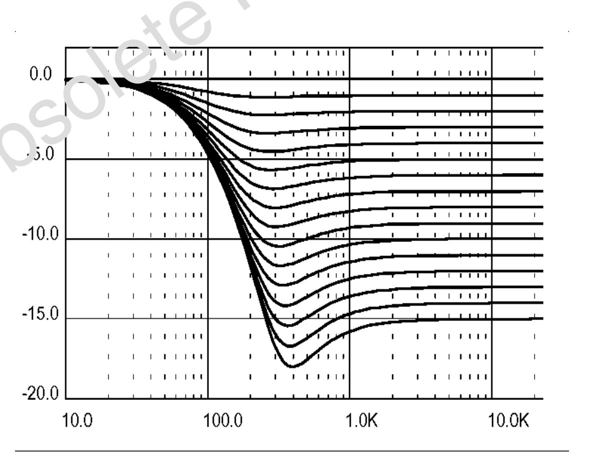


Figure 6. Loudness center frequency @ Atten. = 15 dB (second order)

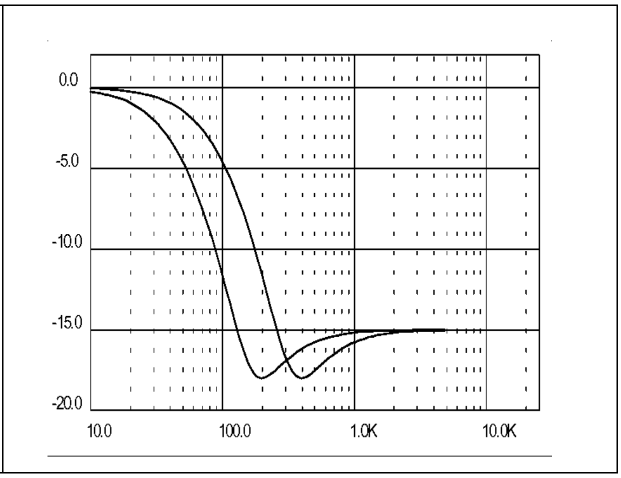
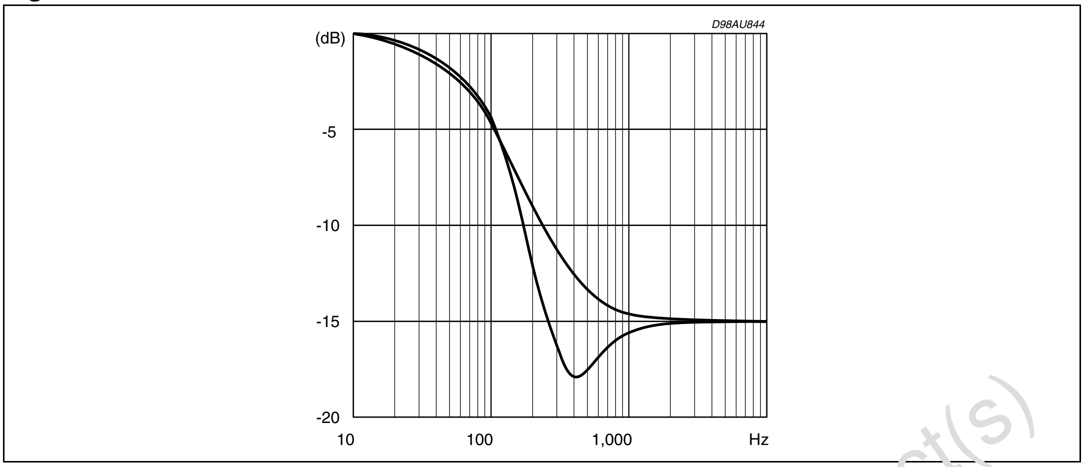


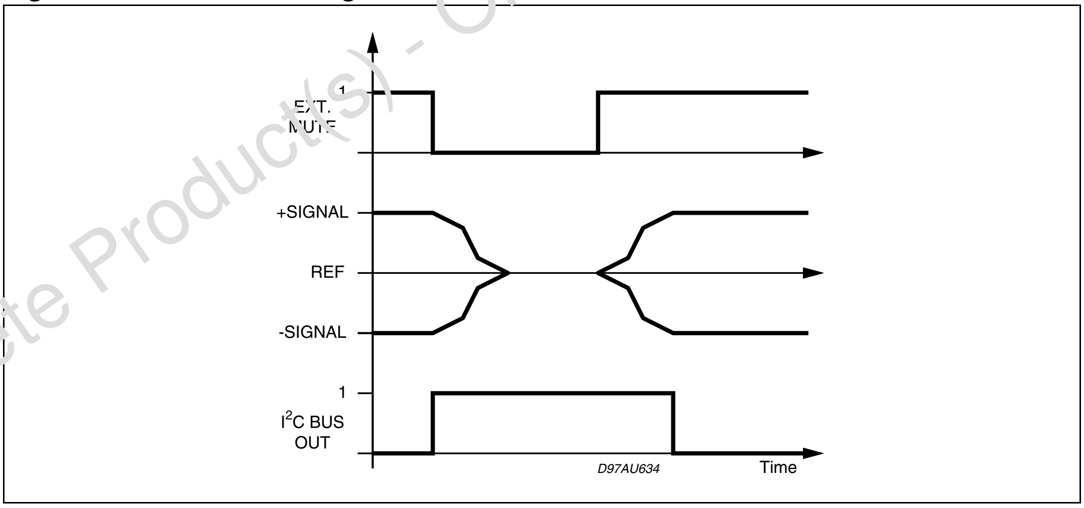
Figure 7. Loudness attenuation = 15 dB @ fc = 400 Hz



3.3.2 Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^{2}C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^{2}C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see *Figure 8*). For timing purposes the Bit 3 of the I^{2}C bus output register is set to 1 from the start of muting until the end of demuting.

Figure 8. Softmute timing

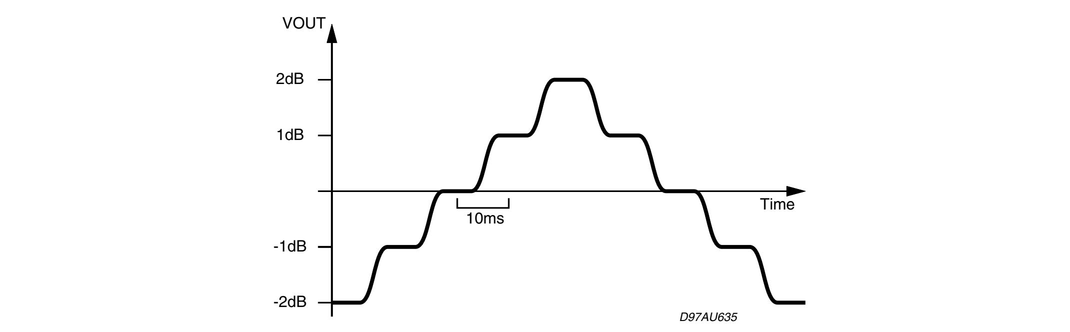


1. Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

3.3.3 Soft step volume

When volume level is changed often an audible click appears at the output. The root cause of those clicks could be either a DC offset before the volume stage or the sudden change of the envelope of the audio signal. With the Soft step feature both kinds of clicks could be reduced to a minimum and are no more audible (see *Figure 9*).

Figure 9. Soft step timing



1. For steps more than 1dB the soft step mode should be deactivated because it could generate a 1dB error during the blend-time.

3.3.4 Bass

There are three parameters programmable in the bass stage (see *Figure 10*, *11*, *12*, *13*):

- Attenuation
- Center Frequency (60, 70, 80 and 100 Hz)
- Quality Factors (1, 1.25, 1.5 and 2)

3.3.5 DC mode

In this mode the DC gain is increased by 4.4 dB. In addition the programmed center frequency and quality factor is decreased by 25 % which can be used to reach alternative center frequencies or quality factors.

3.3.6 Treble

There are two parameters programmable in the treble stage (see *Figure 14*, *15*):

- Attenuation
- Center frequency (10, 12.5, 15 and 17.5 kHz).

3.3.7 Speaker attenuator

Due to practical aspects the steps in the speaker attenuator are not linear over the full range. At attenuations more than 24 dB the steps increase from 1.5 dB to 10 dB (please see data byte specification).

Figure 10. Bass control @ fc = 80 Hz, Q = 1

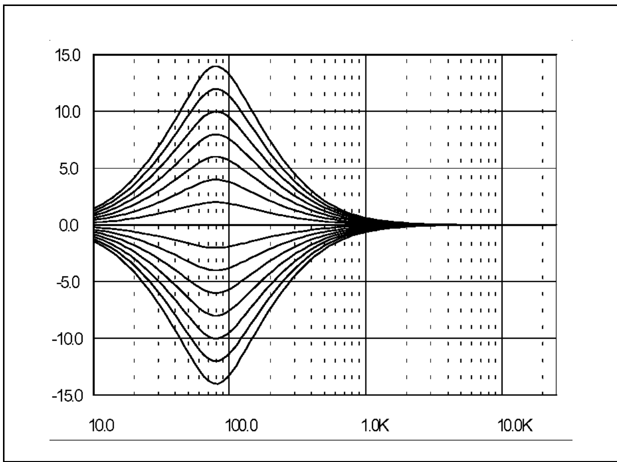


Figure 11. Bass center @ Gain = 14 dB, Q = 1

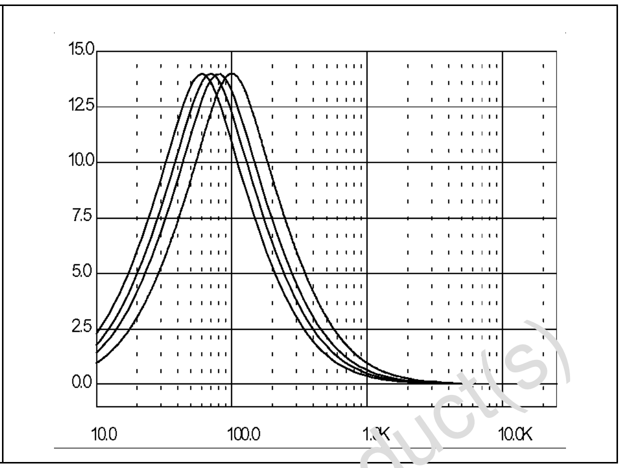


Figure 12. Bass quality factors @ Gain = 14 dB, fc = 80 Hz

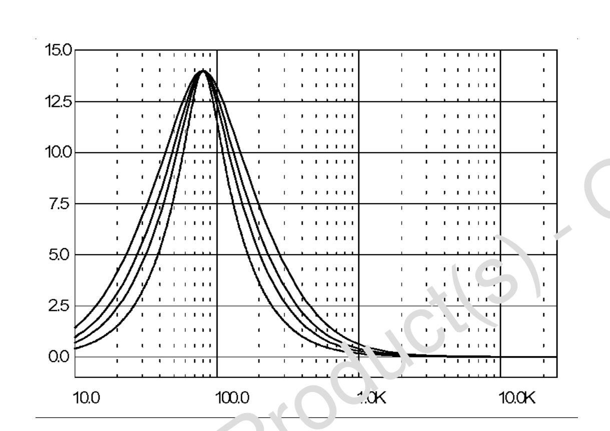


Figure 13. Bass normal and DC mode @ Gain = 14 dB, fc = 80 Hz [(1)]

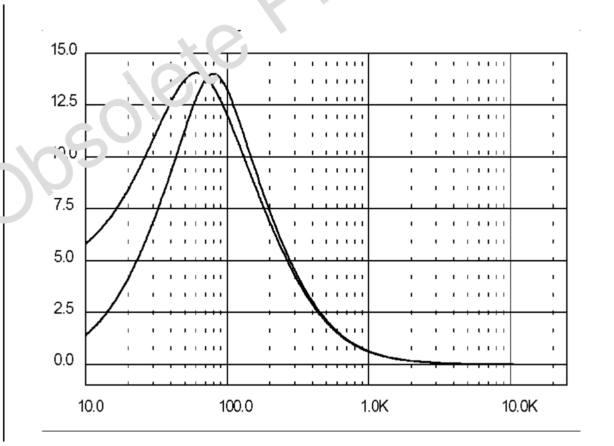


Figure 14. Treble control @ fc = 17.5 kHz)

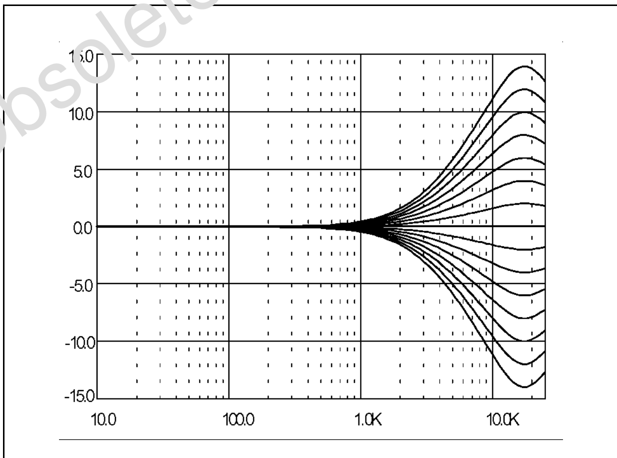
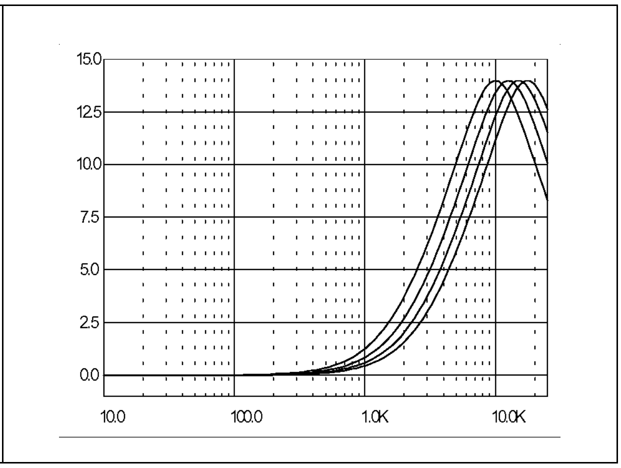


Figure 15. Treble center frequencies @ Gain = 14 dB



(1) In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100 Hz.

4 Stereo decoder part

4.1 Stereo decoder feature

- No external components necessary
- PLL with adjustment free fully integrated VCO
- Automatic pilot dependent mono/stereo switching
- Very high suppression of intermodulation and interference
- Programmable roll-off compensation
- Dedicated RDS Softmute
- High cut and stereo blend characteristics programmable in a wide range
- Internal Noise blanker with threshold controls
- Multipath detector with programmable internal/external influence
- I^2C bus control of all necessary functions

4.2 Stereo decoder electrical characteristics

Table 8. Stereo decoder electrical characteristics
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN}	MPX input level	Input gain = 3.5 dB		0.5	1.25	VRMS
R_{in}	Input resistance		70	100	130	KΩ
G_{min}	Minimum input gain		1.5	3.5	4.5	dB
G_{max}	Max input gain		8.5	11	12.5	dB
G_{STEP}	Step resolution		1.75	2.5	3.25	dB
SVRR	Supply voltage ripple rejection	V_{ripple} = 100 mV, f = 1 kHz		55		dB
a	Max channel separation		30	50		dB
THD	Total harmonic distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus noise to noise ratio	S = 2 V_{rms}	80	91		dB
Mono/stereo switch						
V_{PTHST1}	Pilot threshold voltage	for Stereo, PTH = 1	10	15	25	mV
V_{PTHST0}	Pilot threshold voltage	for Stereo, PTH = 0	15	25	35	mV
V_{PTHMO1}	Pilot threshold voltage	for Mono, PTH = 1	7	12	17	mV
V_{PTHMO0}	Pilot threshold voltage	for Stereo, PTH = 0	10	19	25	mV
PLL						
Δf/f	Capture range		0.5			%

Table 8. Stereo decoder electrical characteristics (continued)
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
De-emphasis and high cut (1)						
τ_{HC50}	De-emphasis time constant	Bit = 7, Subadr. 10 = 0 V_{LEVEL} >> V_{HCH}	25	50	75	µs
τ_{HC75}	De-emphasis time constant	Bit = 7, Subadr. 10 = 1 V_{LEVEL} >> V_{HCH}	50	75	100	µs
τ_{HC50}	High cut time constant	Bit = 7, Subadr. 10 = 0 V_{LEVEL} >> V_{HCL}	100	150	200	µs
τ_{HC75}	High cut time constant	Bit = 7, Subadr. 10 = 1 V_{LEVEL} >> V_{HCL}	150	225	300	µs
Stereo blend and high cut-control						
REF5V	Internal reference voltage		4.7	5	5.3	V
TC_{REF5V}	Temperature coefficient			3300		ppm
L_{Gmin}	Min. level gain		-1	0	+1	dB
L_{Gmax}	Max. level gain		8	10	12	dB
L_{Gstep}	Level gain step resolution		0.3	0.67	1.0	dB
V_{SBLmin}	Min. voltage for mono		29	33	37	%REF5V
V_{SBLmax}	Max. voltage for mono		54	58	62	%REF5V
$V_{SBLstep}$	Step resolution		5.0	8.4	12	%REF5V
$VHCH_{min}$	Min.voltage for no high cut		36	42	46	%REF5V
$VHCH_{max}$	Max. voltage for no high cut		62	66	70	%REF5V
$VHCH_{step}$	Step resolution		5	8.4	12	%REF5V
$VHCL_{min}$	Min. voltage for full high cut		13	17	21	%VHCH
$VHCL_{max}$	Max. voltage for full high cut		29	33	37	%VHCH
Carrier and harmonic suppression at the output						
α19	Pilot signal	f = 19 kHz	40	50		dB
α38	Sub carrier	f = 38 kHz		75		dB
α57	Sub carrier	f = 57 kHz		62		dB
α76	Sub carrier	f = 76 kHz		90		dB
Intermodulation (2))						
α2	Pilot signal	f_{mod} = 10 kHz f_{spur} = 1 kHz;		65		dB
α3		f_{mod} = 13 kHz; f_{spur} = 1 kHz;		75		dB

Table 8. Stereo decoder electrical characteristics (continued)
(V_S = 9 V; de-emphasis time constant = 50 µs, V_{MPX} = 500 mV, 75 kHz deviation, f = 1 kHz. G_I = 6 dB, T_{amb} = 25 °C; unless otherwise specified)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Traffic radio (3)						
α57	Signal	f = 57 kHz		70		dB
SCA - Subsidiary communications authorization (4)						
α67	Signal	f = 67 kHz		75		dB
ACI - Adjacent channel interference (5)						
α114	Signal	f = 114 kHz		95		dB
α190	Signal	f = 190 kHz		84		dB

1. By design/characterization but functionally guaranteed through dedicated test mode structure
2. Intermodulation Suppression: measured with: 91% pilot signal; fm = 10kHz or 13kHz.
3. Traffic radio (V.F.) suppression: measured with: 91 % stereo signal; 9 % pilot signal; fm=1 kHz, 5% sub carrier (f = 57 kHz, fm = 23 Hz AM, m = 60 %)
4. SCA (subsidiary communications authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1 kHz; 1 0% SCA sub carrier (fs = 6 7 kHz, unmodulated).
5. ACI (adjacent channel interference) measured with: 90% mono signal; 9% pilot signal; fm = 1 kHz; 1% spurious signal (fs = 110 kHz or 186 kHz, unmodulated).

4.3 Noise blanker part

- internal 2nd order 140 kHz high pass filter
- programmable trigger threshold
- additional circuits for trigger adjustment (deviation, field-strength)
- very low offset current during hold time
- four selectable pulse suppression times

Table 9. Noise blanker electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger threshold (1), (2)	meas. with V_{PEAK} = 0.9V	NBT = 111		30		mV_{OP}
			NBT = 110		35		mV_{OP}
			NBT = 101		40		mV_{OP}
			NBT = 100		45		mV_{OP}
			NBT = 011		50		mV_{OP}
			NBT = 010		55		mV_{OP}
			NBT = 001		60		mV_{OP}
			NBT = 000		65		mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger Threshold(3)	meas. with V_{PEAK} = 1.5V	NCT = 00		260		mV_{OP}
			NCT = 01		220		mV_{OP}
			NCT = 10		180		mV_{OP}
			NCT = 11		140		mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV		0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 100mV; f = 150KHz		2.2	2.5	2.9	V
$V_{RECT\ DEV}$	Deviation dependent(4) rectifier voltage	means. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	mV_{OP}
			OVD = 10	0.9	1.2	1.5	mV_{OP}
			OVD = 01	1.7	2.0	2.3	mV_{OP}
			OVD = 00	2.5	2.8	3.1	mV_{OP}
$V_{RECT\ FS}$	Fieldstrength controlled (5) rectifier voltage	means. with V_{MPX} = 0mV V_{LEVEL} << V_{SBL} (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	1.0	1.3	1.6	V
			FSC = 01	1.5	1.8	2.1	V
			FSC = 00	2.0	2.3	2.6	V

1. All thresholds are measured using a pulse with T_R = 2 µs, T_{HIGH} = 2 µs and T_F = 10 µs.
2. NBT represents the Noise blanker-Byte bits D2; D0 for the noise blanker trigger threshold
3. NAT represents the Noise blanker-Byte bit pair D4,D3 for the noise controlled trigger adjustment
4. OVD represents the Noise blanker-Byte bit pair D7,D6 for the over deviation detector
5. FSC represents the Fieldstrength-Byte bit pair D1,D0 for the fieldstrength control

Figure 16. Noise blanker diagram

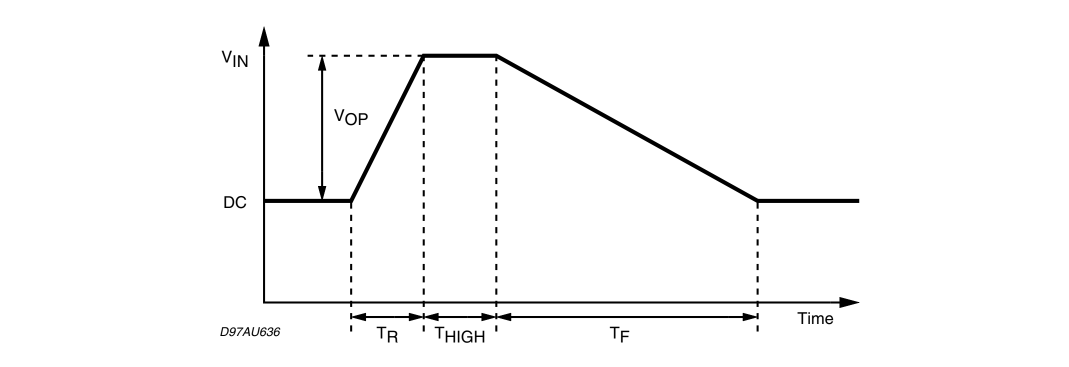


Figure 17. Trigger threshold vs. V_{PEAK}

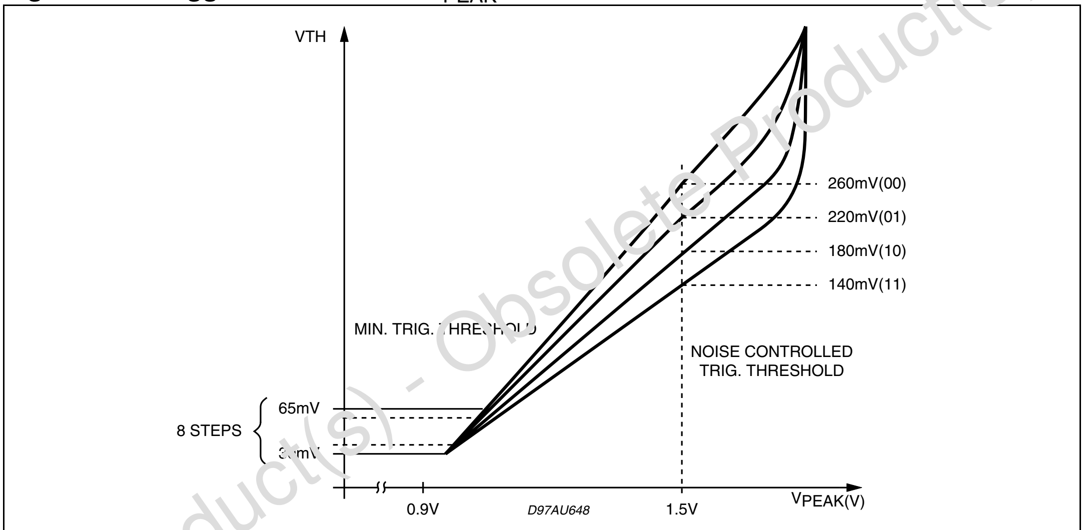


Figure 18. Deviation controlled trigger adjustment

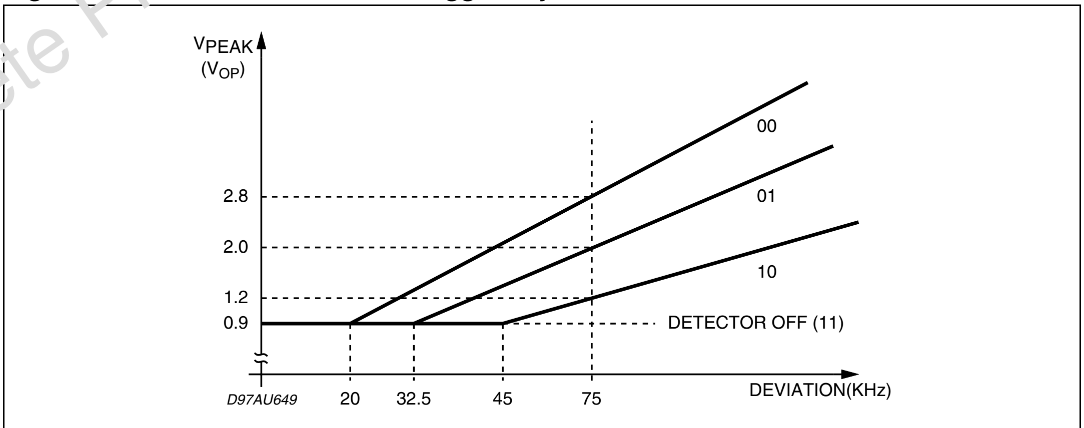
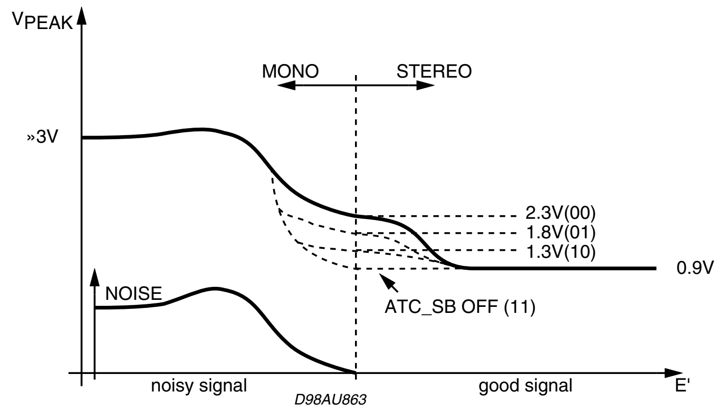


Figure 19. Fieldstrength controlled trigger adjustment



4.4 Multipath detector

- Internal 19 kHz bandpass filter
- Programmable bandpass and rectifier gain
- Two pin solution fully independent usable for external programming
- Selectable internal influence on Stereo blend

Table 10. Multipath detector electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{CMP}	Center frequency of multipath- bandpass	stereo decoder locked on pilot tone		19		KHz
G_{BPMP}	Bandpass gain	bits D_2, D_1 configuration byte = 00		6		dB
		bits D_2, D_1 configuration byte = 01		16		dB
		bits D_2, D_1 configuration byte = 10		12		dB
		bits D_2, D_1 configuration byte = 11		18		dB
G_{RECTMP}	Rectifier gain	bits D_7, D_6 configuration byte = 00		7.6		dB
		bits D_7, D_6 configuration byte = 01		4.6		dB
		bits D_7, D_6 configuration byte = 10		0		dB
I_{CHMP}	Rectifier charge current			1		µA
I_{DISMP}	Rectifier discharge current			1.5		mA