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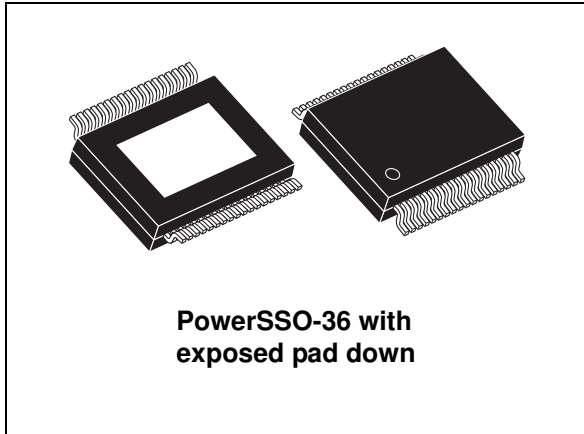
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20 W + 20 W dual BTL class-D audio amplifier

Datasheet - production data



Description

The TDA7491HV is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no separate heatsink is required.

The TDA7491HV is pin-to-pin compatible with the TDA7491P and TDA7491LP.

Features

- 20 W + 20 W continuous output power:
 $R_L = 8 \Omega$, THD = 10% at $V_{CC} = 18 \text{ V}$
- Wide-range single-supply operation (5 V - 18 V)
- High efficiency ($\eta = 90\%$)
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common mode noise
- No 'pop' at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
TDA7491HV13TR	-40 to 85°C	PowerSSO-36 EPD	Tape and reel

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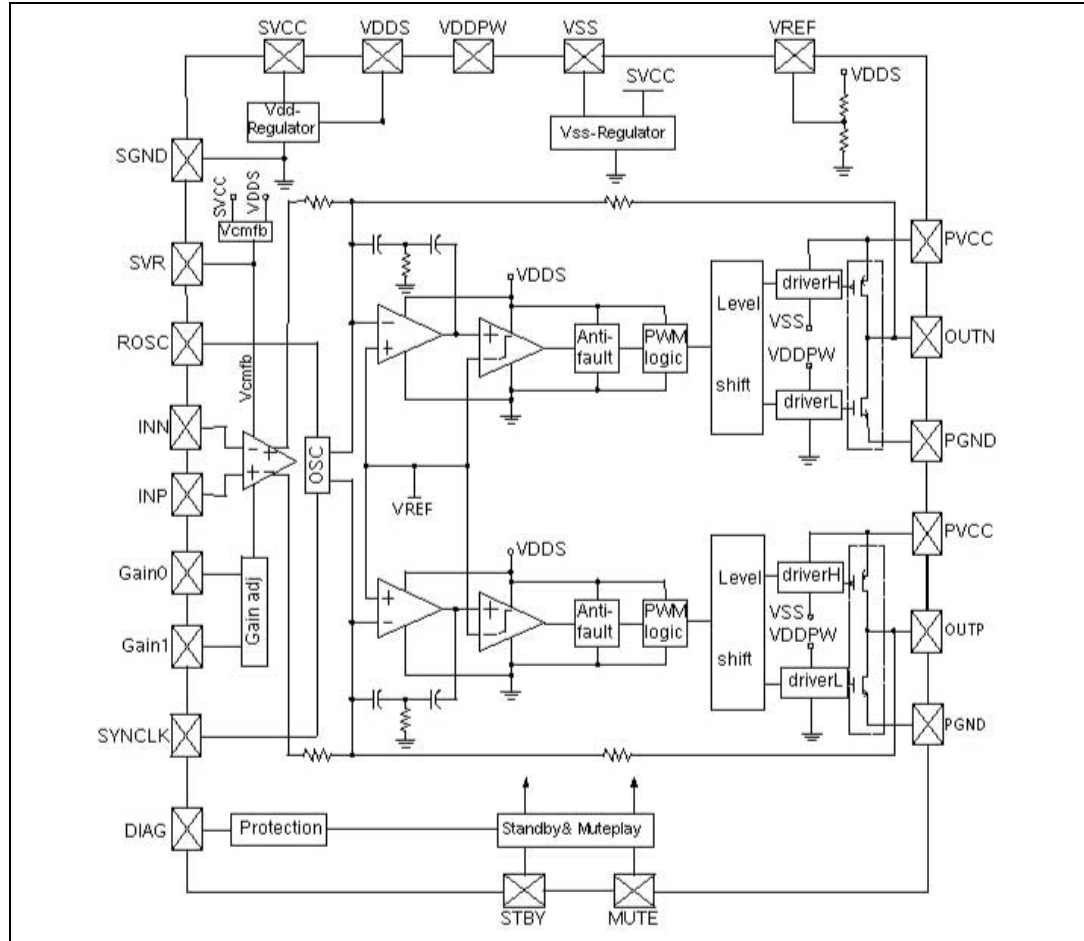
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1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491HV.

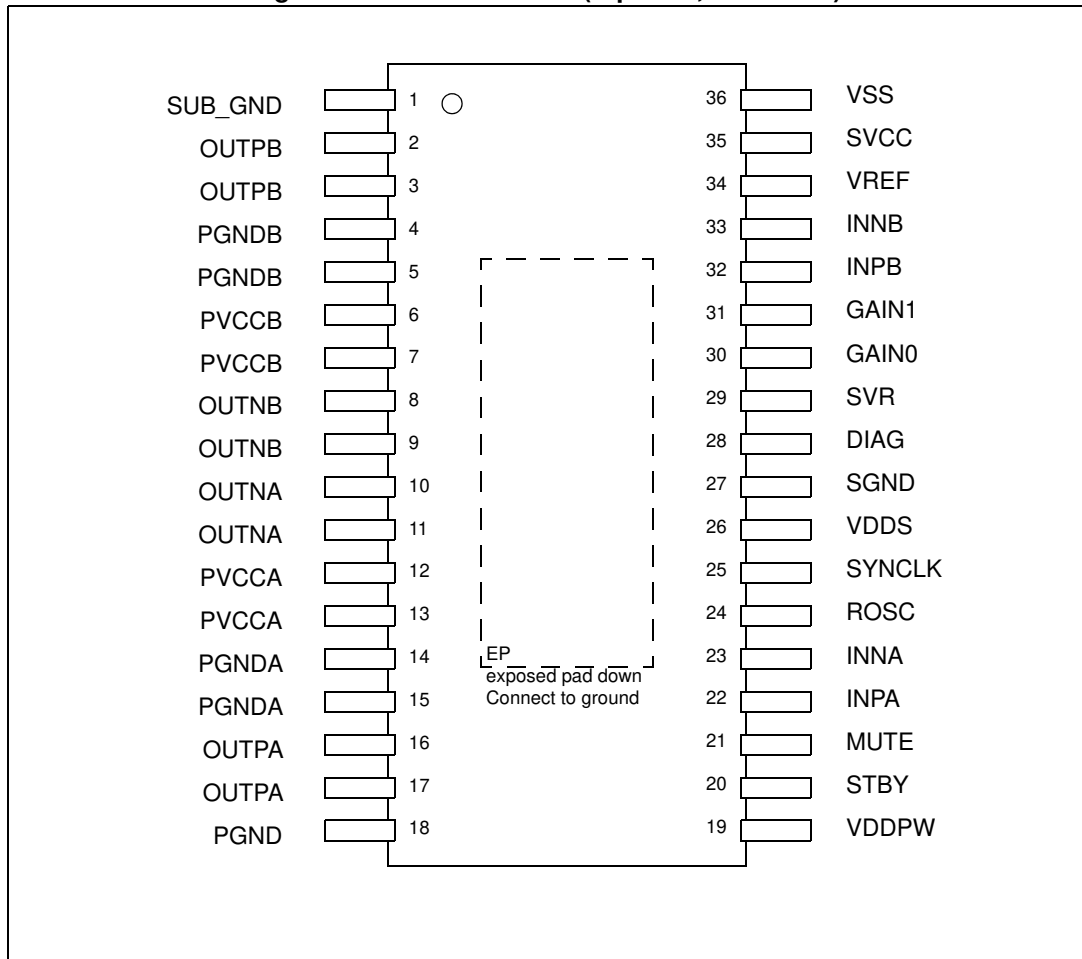
Figure 1. Internal block diagram (one channel only)



2 Pin description

2.1 Pinout

Figure 2. Pin connections (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Pin n°	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM for right channel
4,5	PGNDB	POWER	Power stage ground for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for left channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage ground for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage ground
19	VDDPW	OUT	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for ground-plane heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage for pins PVCCA, PVCCB	23	V
V_i	Voltage limits for input pins STBY,MUTE,INNA,INPA,INNB INPB,GAIN0,GAIN1	-0.3 TO 3.6	V
T_{op}	Operating temperature	-40 to 85	°C
T_j	Junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

3.2 Thermal data

Refer also to [Section 7.9: Heatsink requirements on page 40](#).

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j-case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j-amb}$	Thermal resistance, junction to ambient (mounted on recommended PCB) ⁽¹⁾	-	24	-	

1. FR4 with vias to copper area of 9 cm².

3.3 Electrical specifications

Unless otherwise stated, the results in [Table 5](#) below are given for the conditions:

$V_{CC} = 18\text{ V}$, R_L (load) = 8 Ω , $R_{OSC} = R3 = 39\text{ k}\Omega$, $C8 = 100\text{ nF}$, $f = 1\text{ kHz}$, $G_V = 20\text{ dB}$, and $T_{amb} = 25\text{ °C}$.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	5	-	18	V
I_q	Total quiescent current	-	-	26	35	mA
I_{qSTBY}	Quiescent current in standby	-	-	2.5	5.0	μA
V_{OS}	Output offset voltage	Play mode	-100	-	100	mV
		Mute mode	-60	-	60	mV
I_{OCP}	Overcurrent protection threshold	$R_L = 0\ \Omega$	3	5	-	A
T_j	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	54	60	-	k Ω

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{UVP}	Undervoltage protection threshold	-	-	-	4.5	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	20	-	W
		THD = 1%	-	16	-	
P_o	Output power	$R_L = 8 \Omega$, THD = 10% $V_{CC} = 12 V$	-	9.5	-	W
		$R_L = 8 \Omega$, THD = 1% $V_{CC} = 12 V$	-	7.2	-	
P_D	Dissipated power	$P_o = 20 W + 20 W$, THD = 10%	-	4.0	-	W
η	Efficiency	$P_o = 20 W + 20 W$	80	90	-	%
THD	Total harmonic distortion	$P_o = 1 W$	-	0.1	-	%
G_V	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG_V	Gain matching	-	-1	-	1	dB
CT	Cross talk	$f = 1 kHz$, $P_o = 1 W$	-	70	-	dB
eN	Total input noise	A Curve, $G_V = 20 dB$	-	15	-	μV
		$f = 22 Hz$ to $22 kHz$	-	20	-	
SVRR	Supply voltage rejection ratio	$f_r = 100 Hz$, $V_r = 1 V_{pp}$, $C_{SVR} = 10 \mu F$	-	50	-	dB
T_r, T_f	Rise and fall times	-	-	40	-	ns
f_{SW}	Switching frequency	Internal oscillator, master mode	290	320	350	kHz
f_{SWR}	Switching frequency range	(1)	250	-	400	kHz
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	$V_{MUTE} = low$ $V_{STBY} = high$	-	80	-	dB
Function mode	Standby, mute and play modes	$V_{STBY} < 0.5 V$ $V_{MUTE} = X$	Standby			-
		$V_{STBY} > 2.9 V$, $V_{MUTE} < 0.8 V$	Mute			-
		$V_{STBY} > 2.9 V$, $V_{MUTE} > 2.9 V$	Play			-

1. Refer to [Section 7.4: Internal and external clocks on page 36](#).

4 Characterization curves

The following characterization curves were made using the TDA7491HV demo board. The LC filter for the 4-Ω load uses components of 15 μH and 470 nF, whilst that for the 6-Ω load uses 22 μH and 220 nF and that for the 8-Ω load uses 33 μH and 220 nF.

4.1 With 4 Ω load at V_{CC} = 14 V

Figure 3. Output power vs. supply voltage

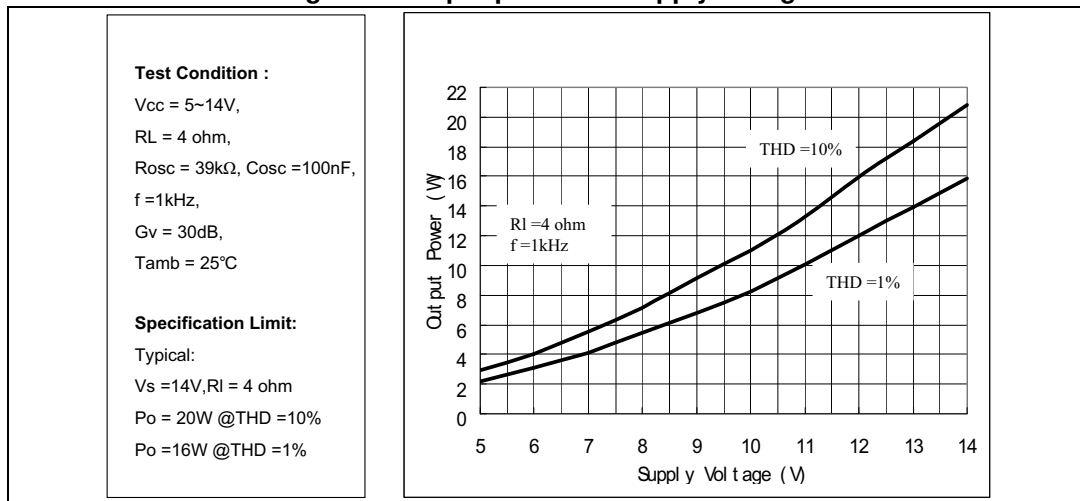


Figure 4. THD vs. output power (1 kHz)

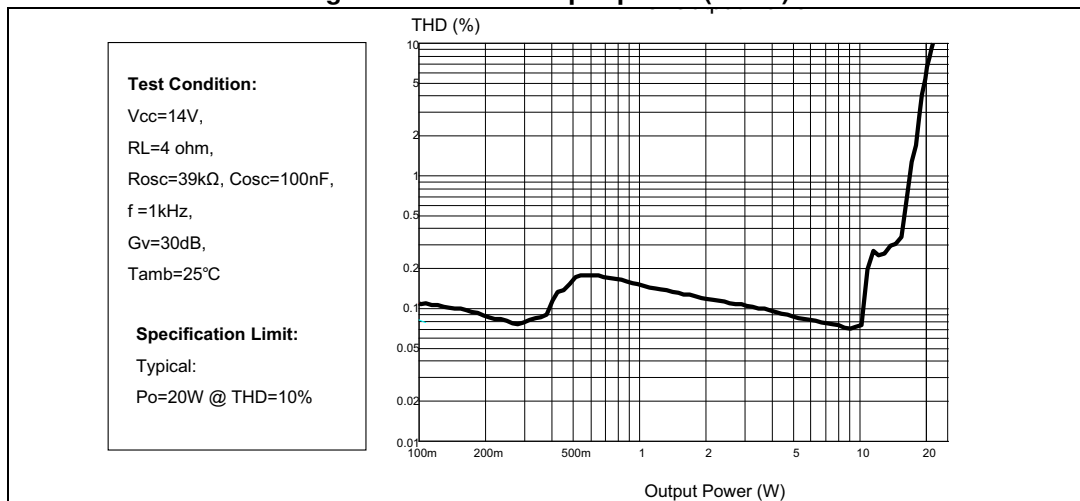


Figure 5. THD vs. output power (100 Hz)

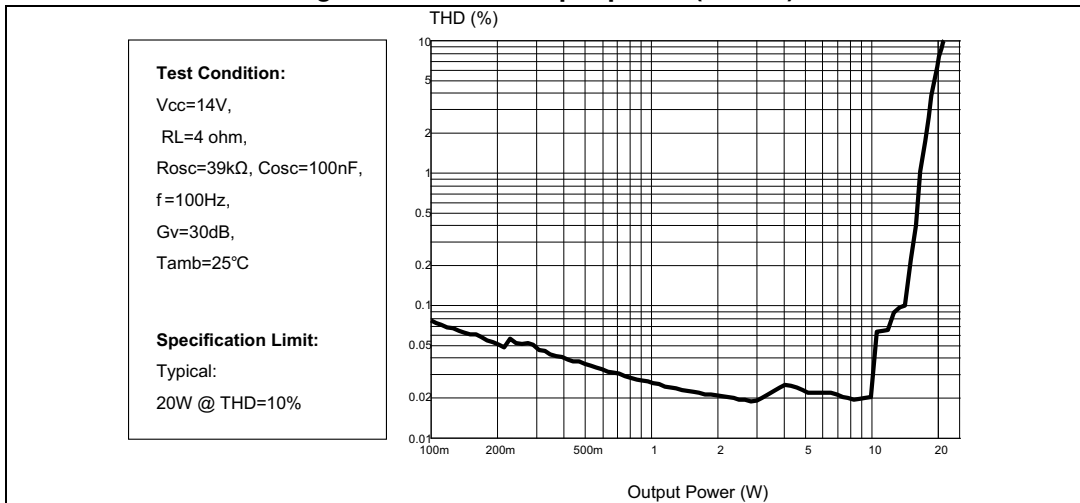


Figure 6. THD vs. frequency

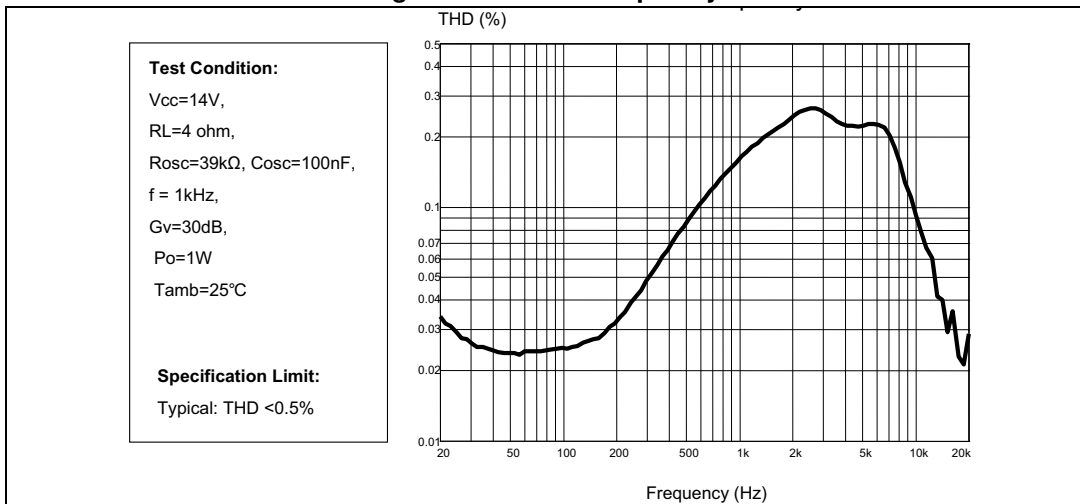


Figure 7. Frequency response

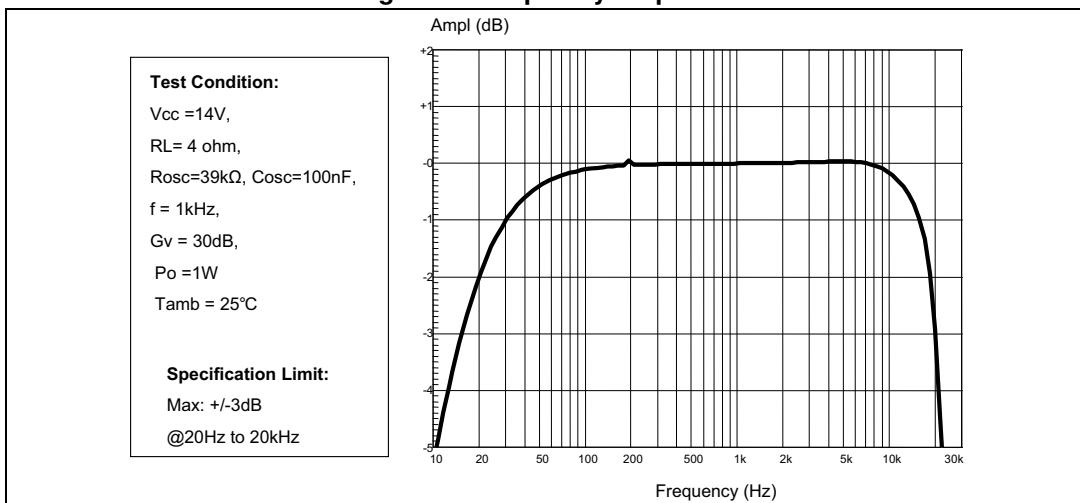


Figure 8. Crosstalk vs. frequency

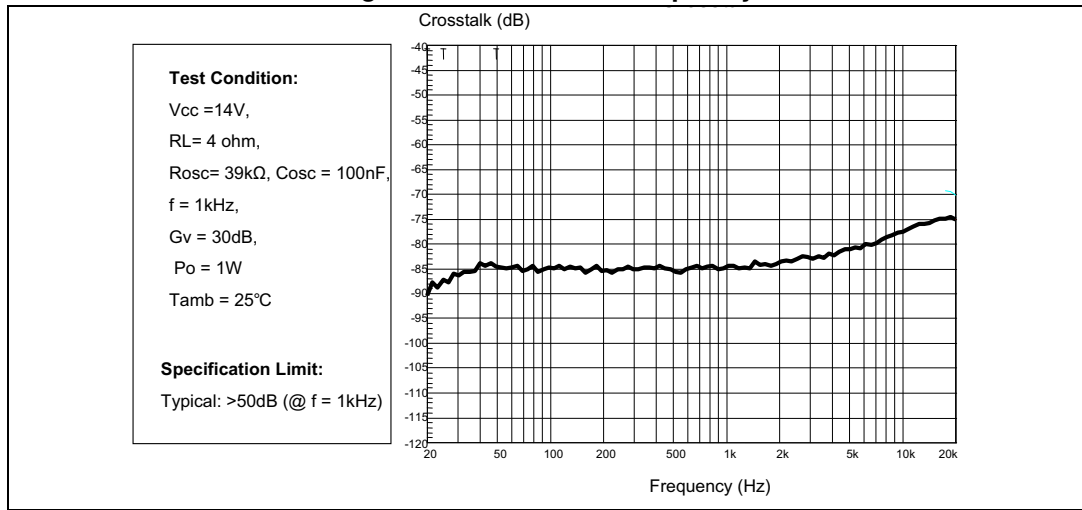


Figure 9. FFT (0 dB)

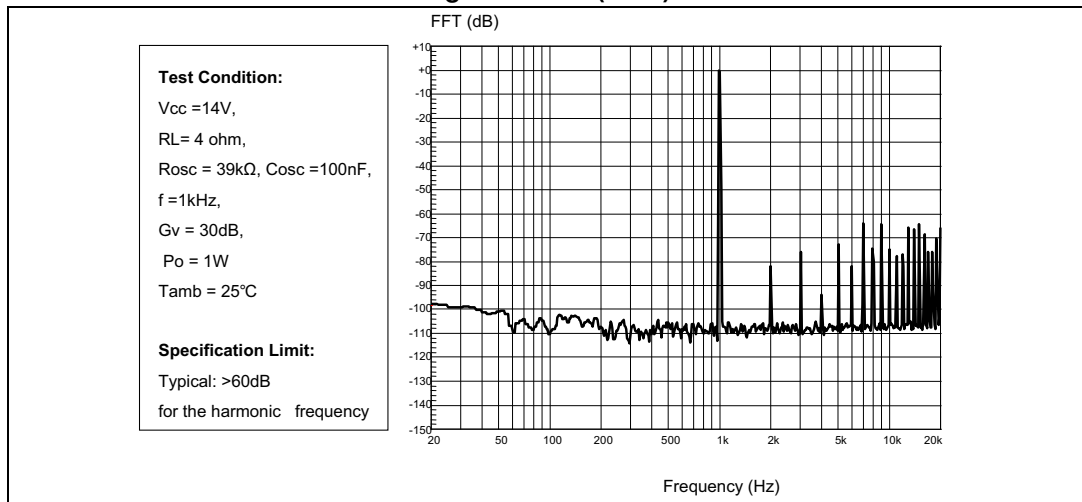


Figure 10. FFT (-60 dB)

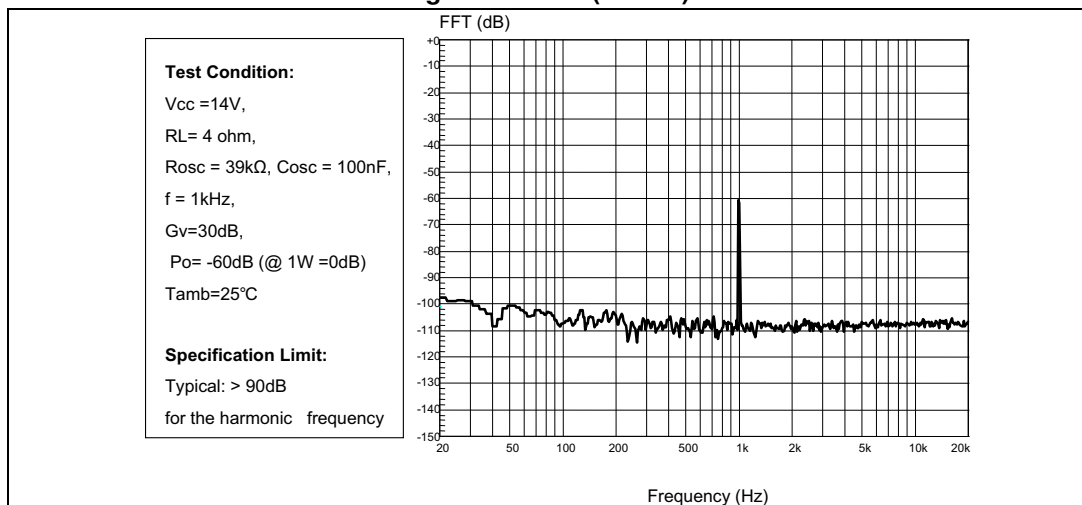


Figure 11. Power supply rejection ratio vs. frequency

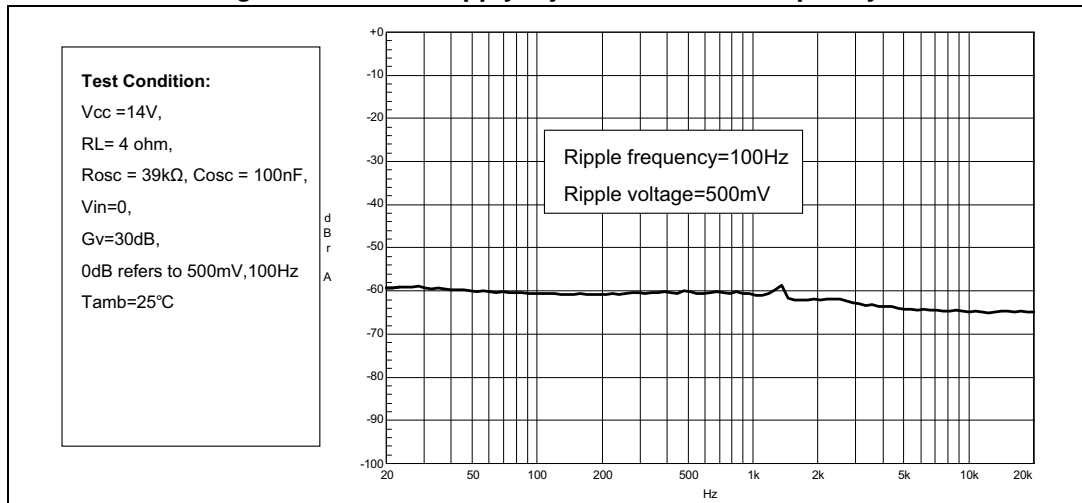


Figure 12. Power dissipation and efficiency vs. output power

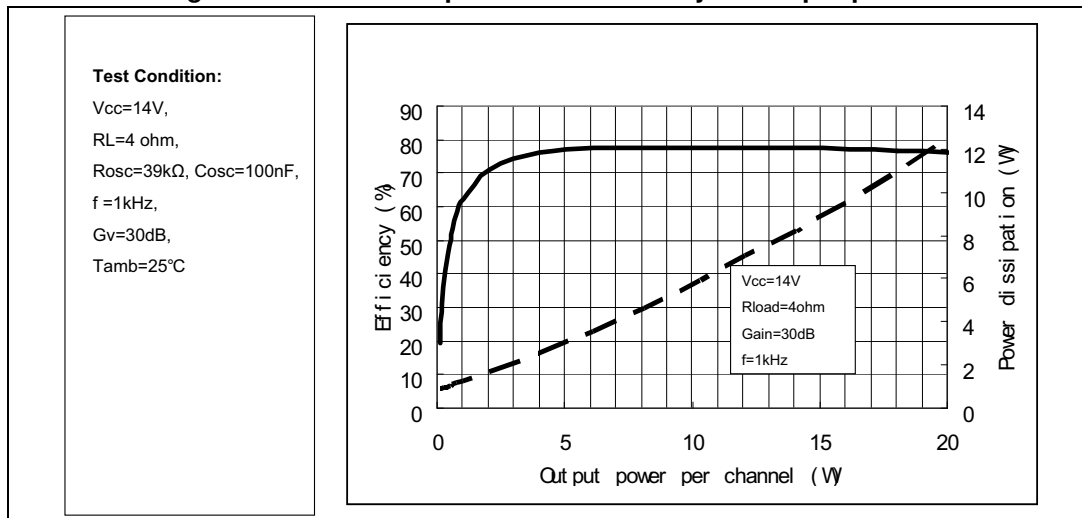


Figure 13. Closed-loop gain vs. frequency

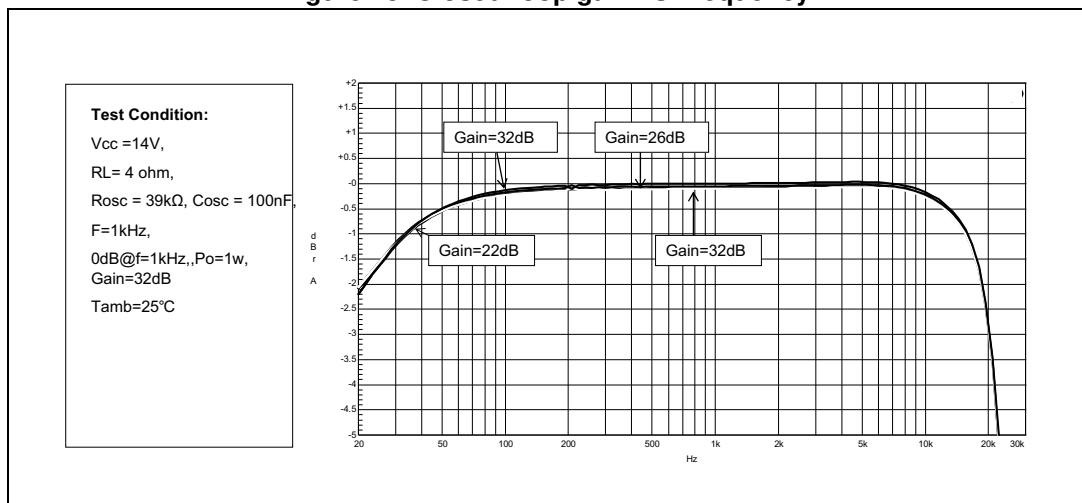


Figure 14. Current consumption vs. voltage on pin MUTE

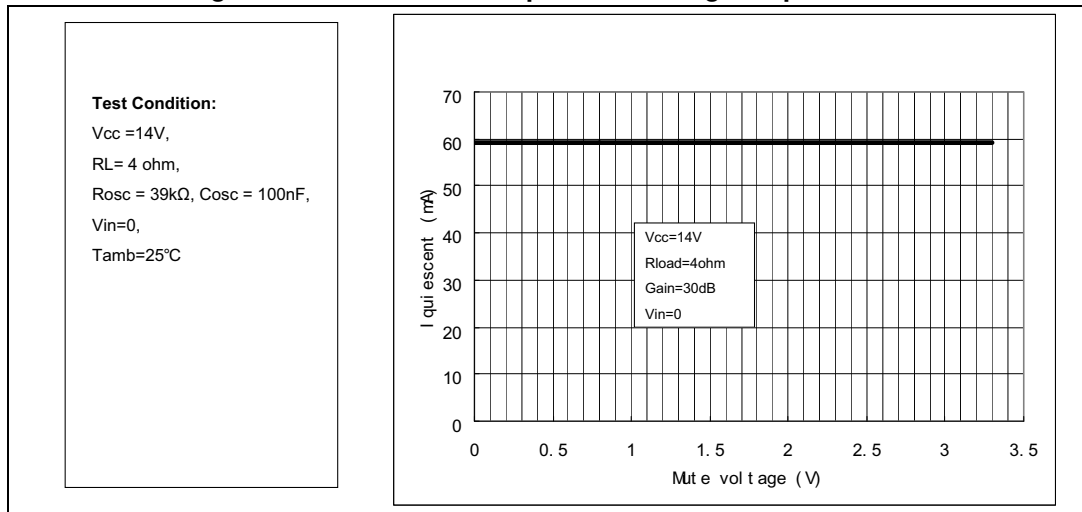


Figure 15. Attenuation vs. voltage on pin MUTE

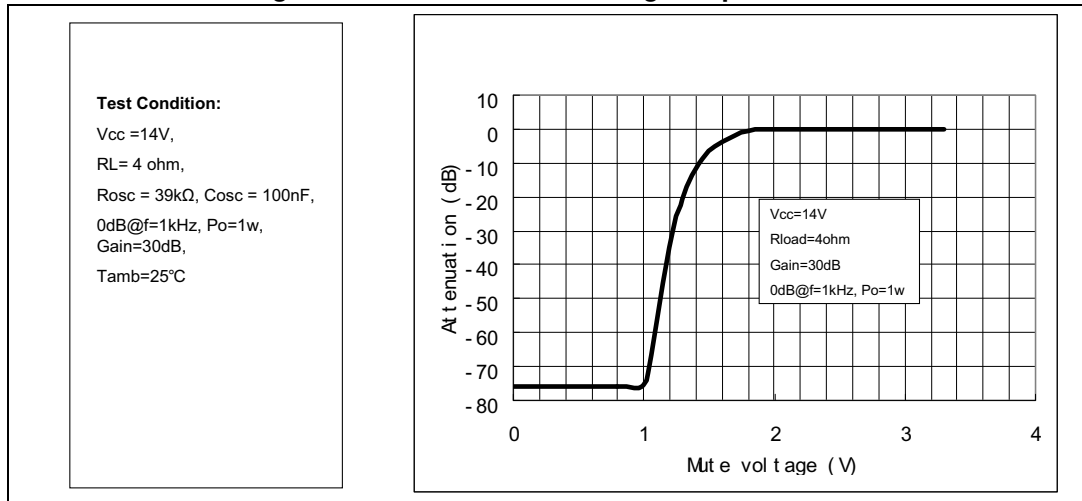


Figure 16. Current consumption vs. voltage on pin STBY

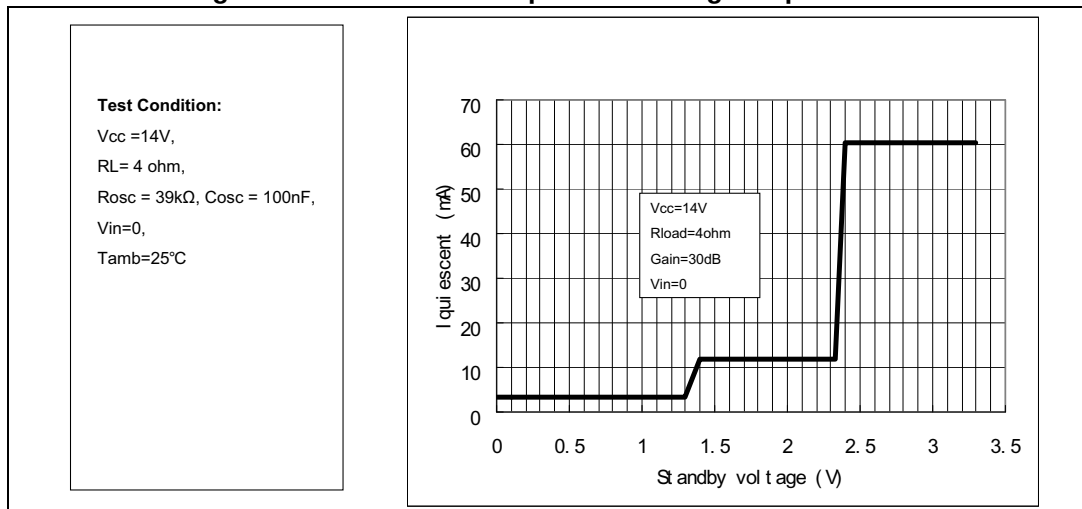
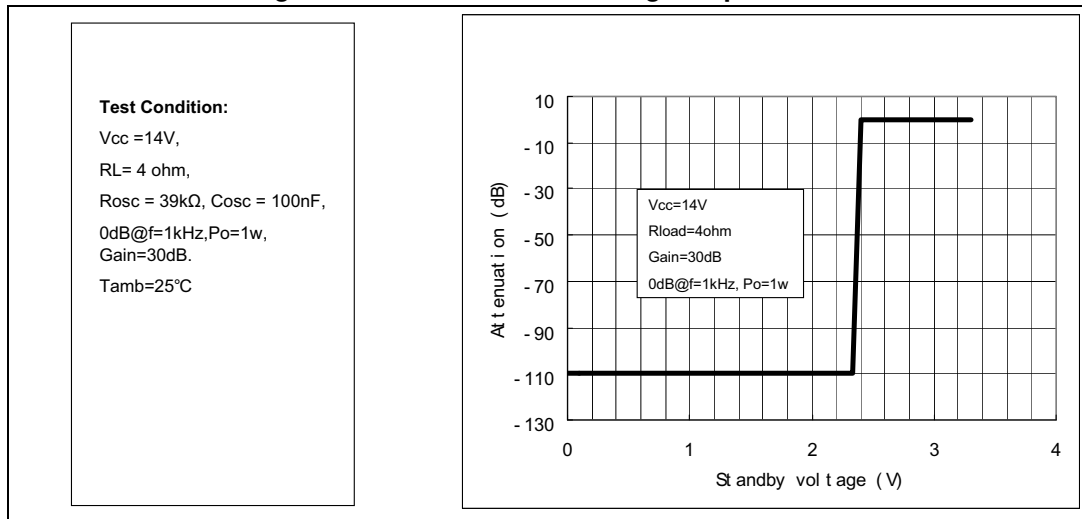


Figure 17. Attenuation vs. voltage on pin STBY



4.2 With 6 Ω load at V_{CC} = 16 V

Figure 18. Output power vs. supply voltage

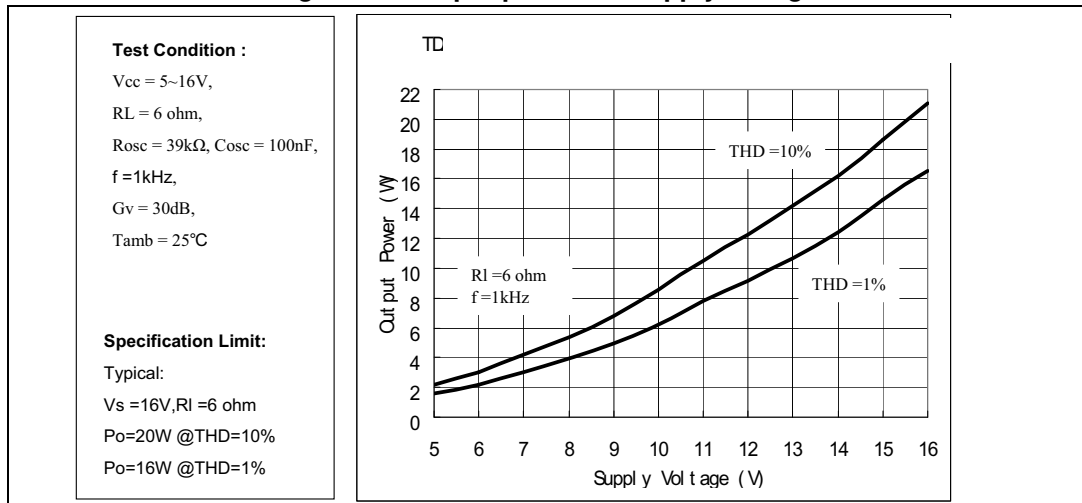


Figure 19. THD vs. output power (1 kHz)

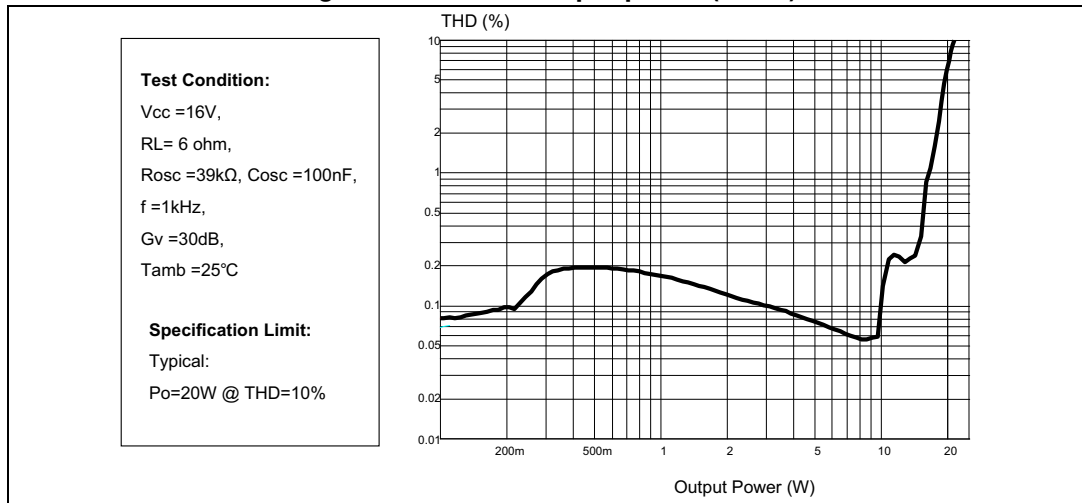


Figure 20. THD vs. output power (100 Hz)

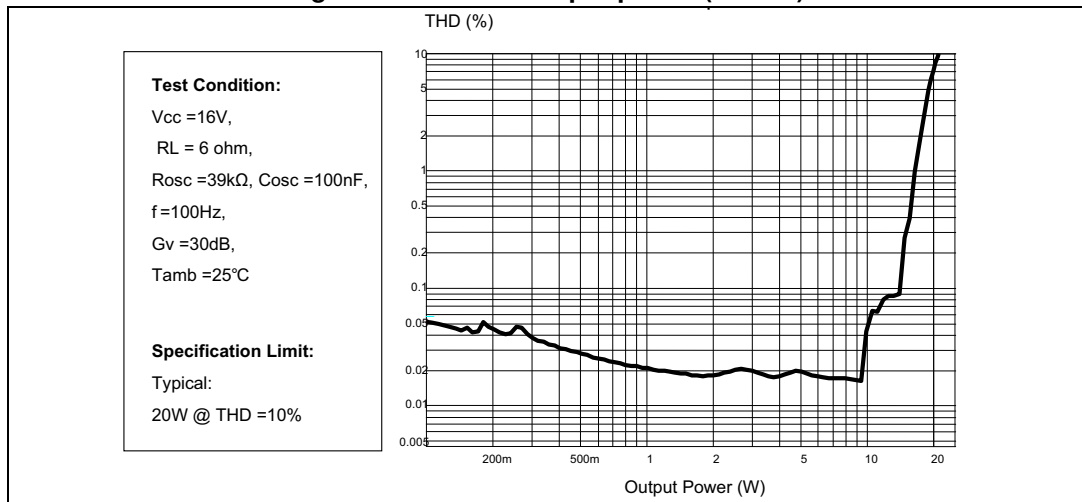


Figure 21. THD vs. frequency

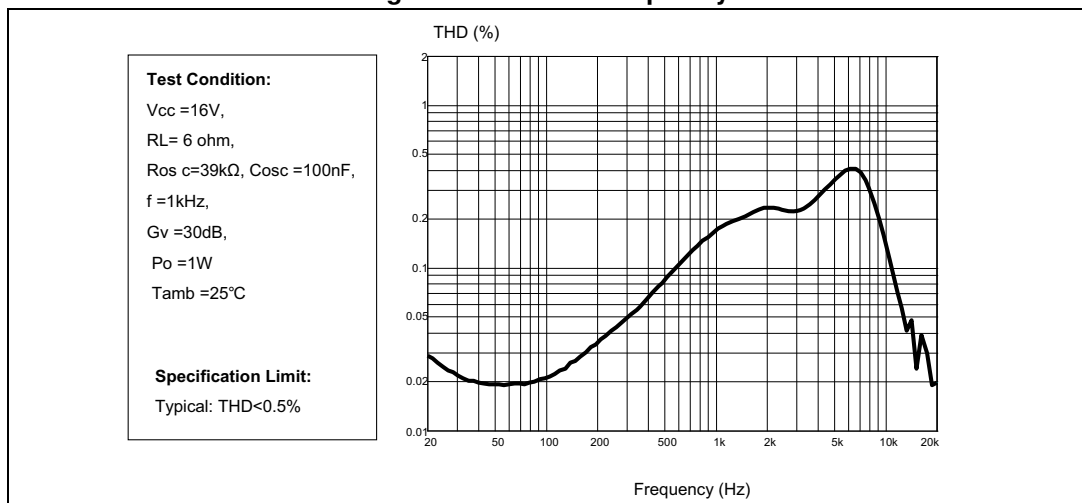


Figure 22. Frequency response

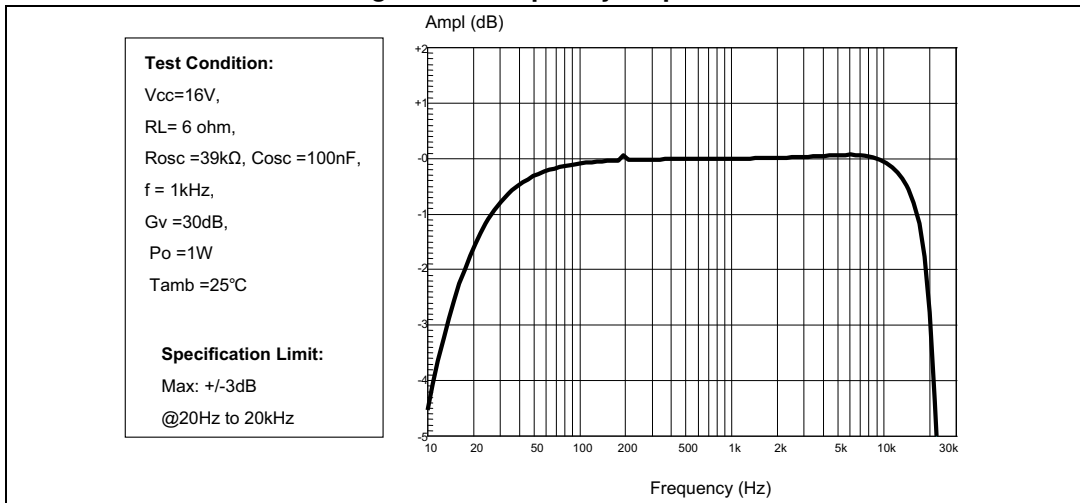


Figure 23. Crosstalk vs. frequency

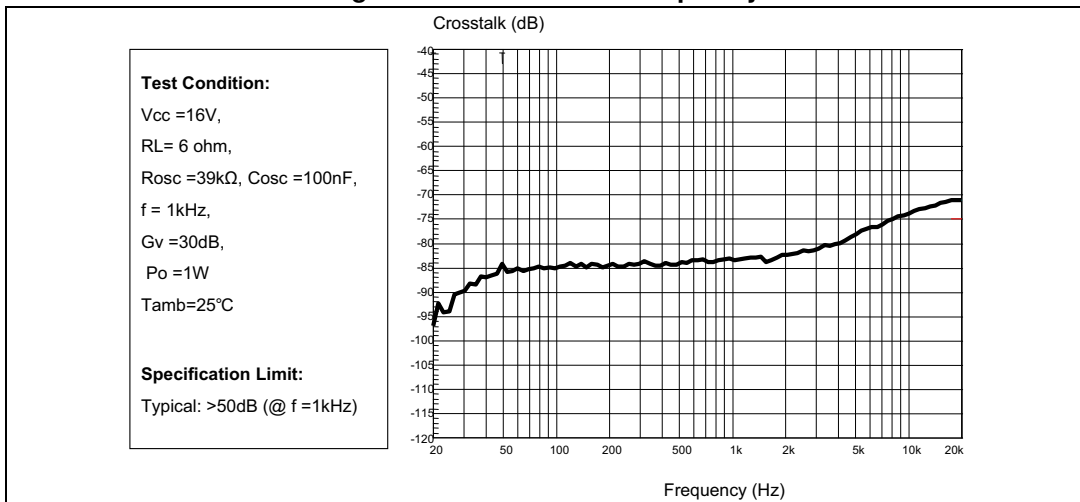


Figure 24. FFT (0 dB)

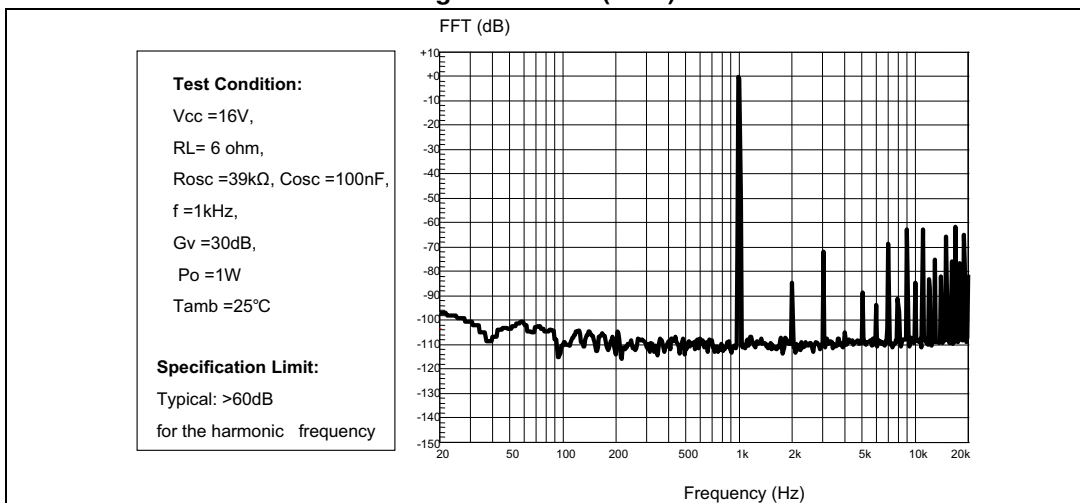


Figure 25. FFT (-60 dB)

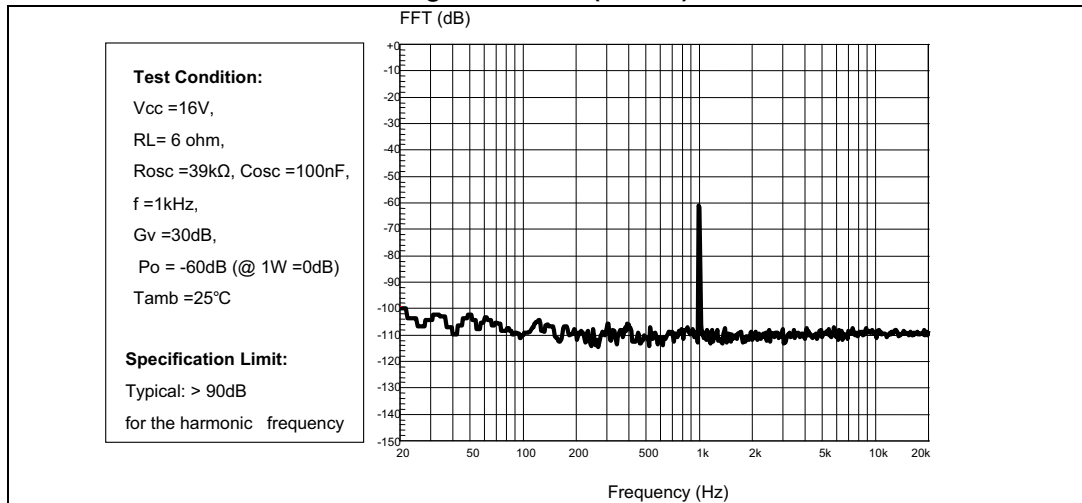


Figure 26. Power supply rejection ratio vs. frequency

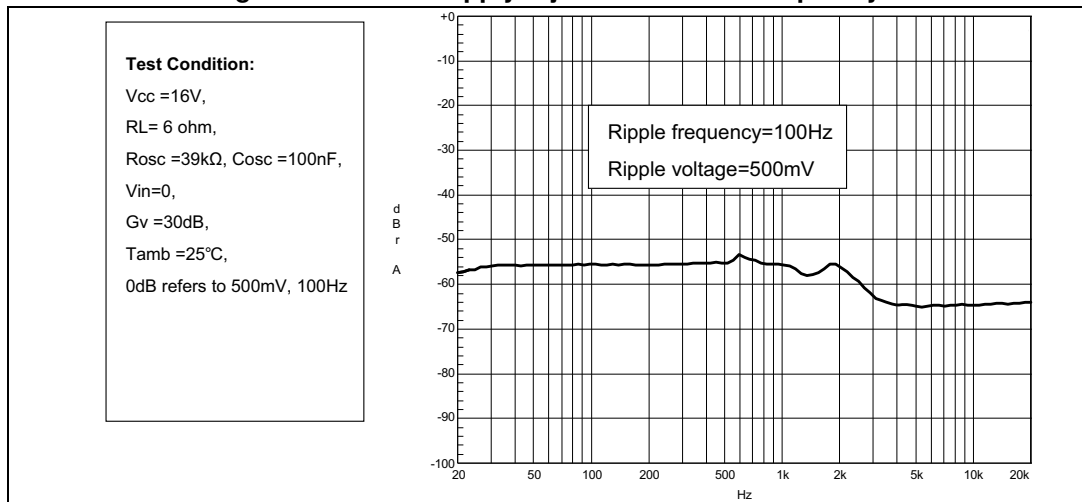


Figure 27. Power dissipation and efficiency vs. output power

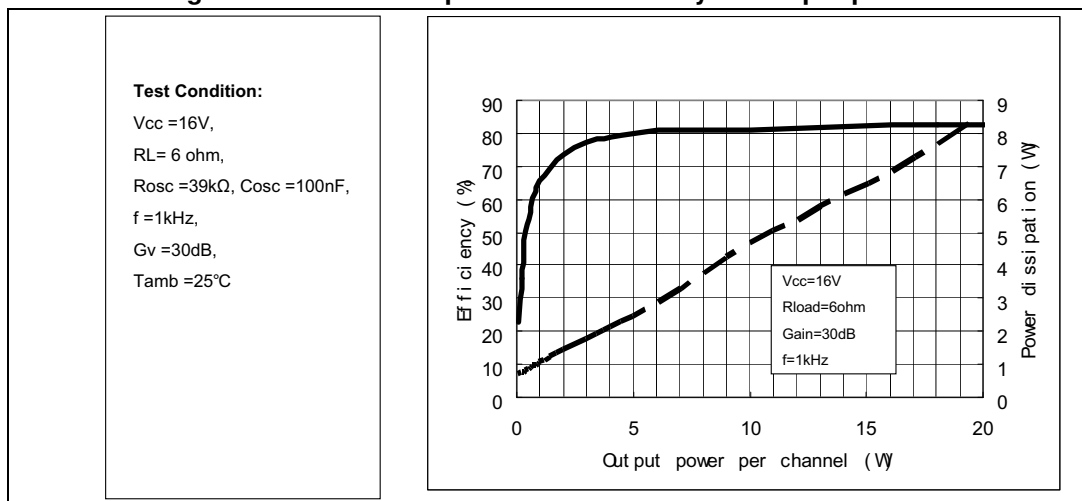


Figure 28. Closed-loop gain vs. frequency

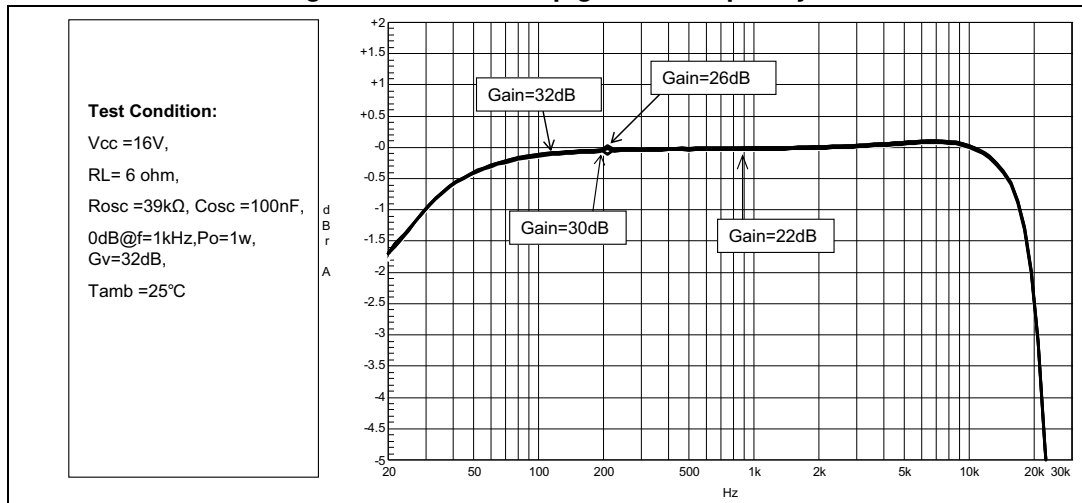


Figure 29. Current consumption vs. voltage on pin MUTE

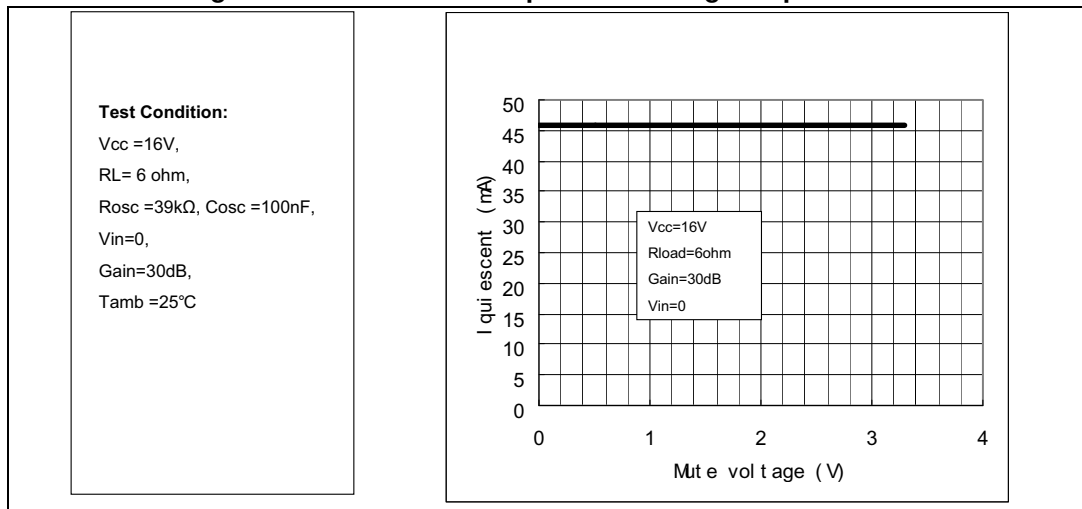


Figure 30. Attenuation vs. voltage on pin MUTE

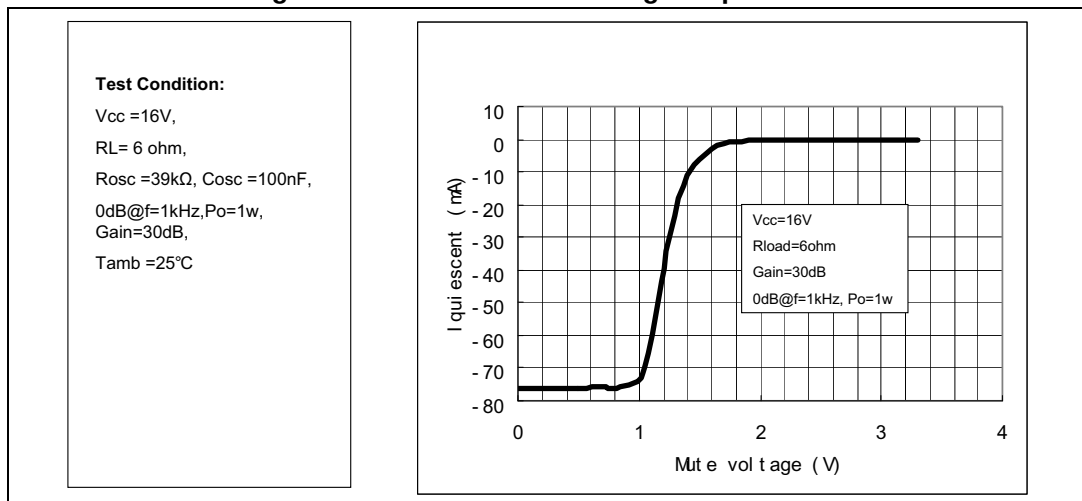


Figure 31. Current consumption vs. voltage on pin STBY

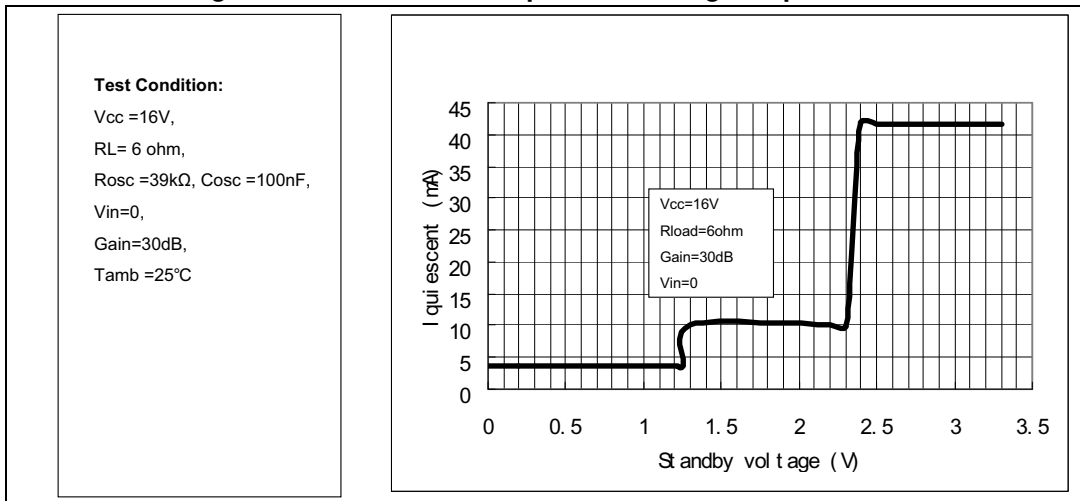
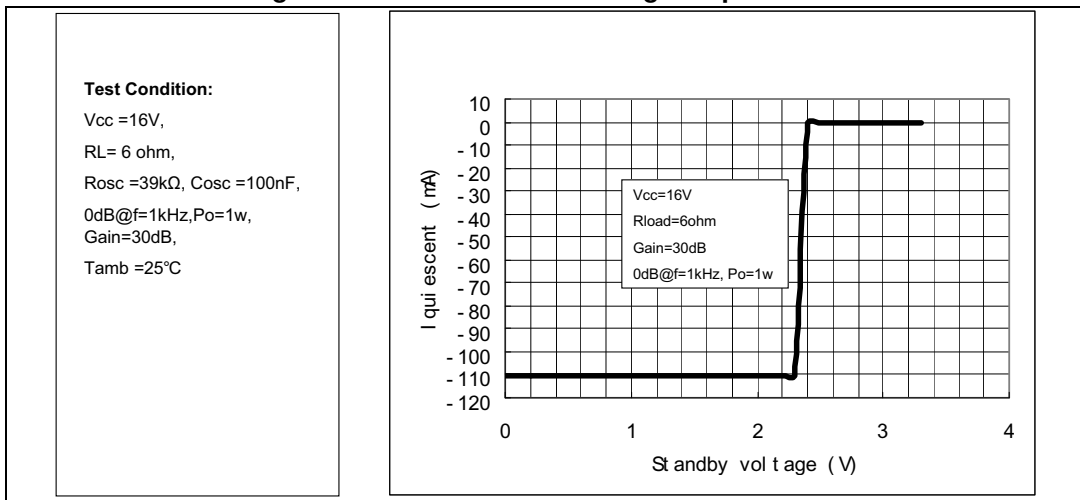


Figure 32. Attenuation vs. voltage on pin STBY



4.3 With 8 Ω load at V_{CC} = 18 V

Figure 33. Output power vs. supply voltage

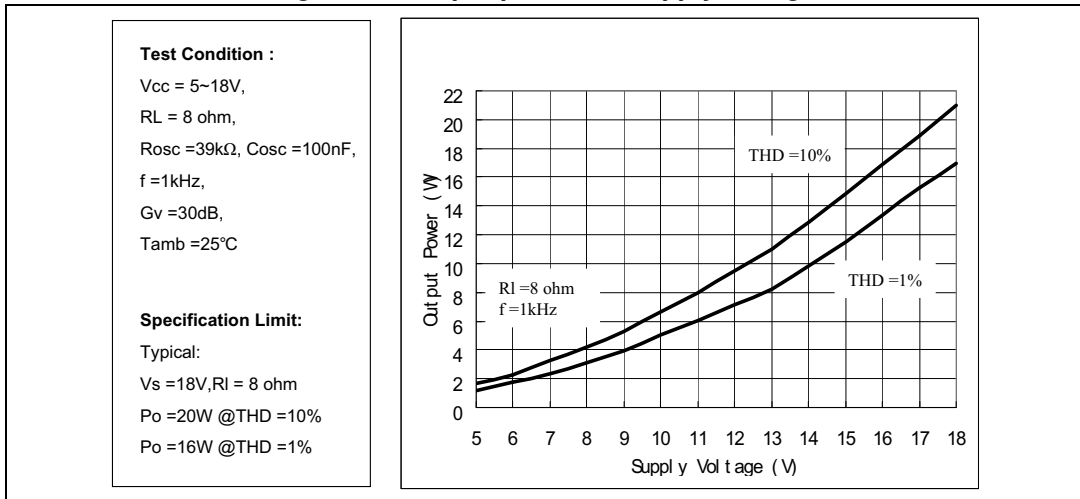


Figure 34. THD vs. output power (1 kHz)

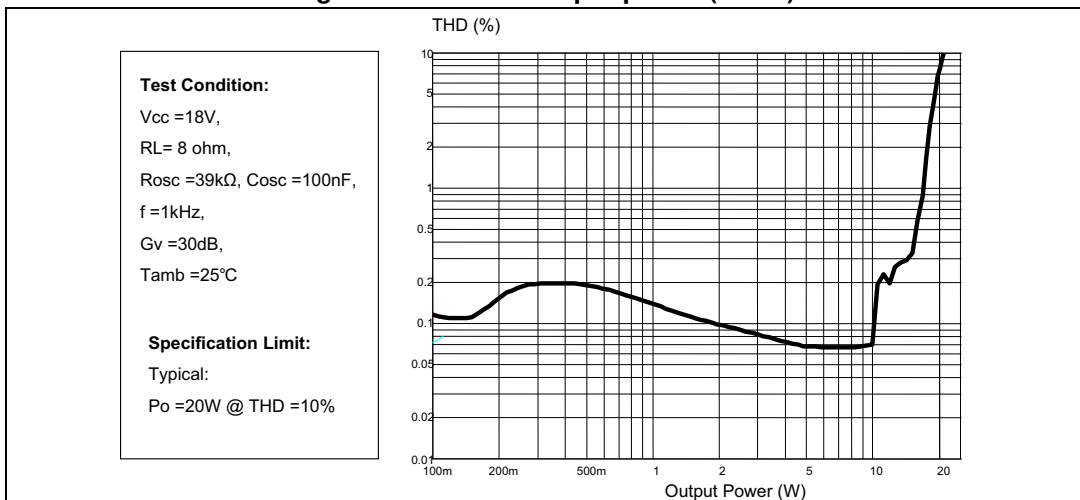


Figure 35. THD vs. output power (100 Hz)

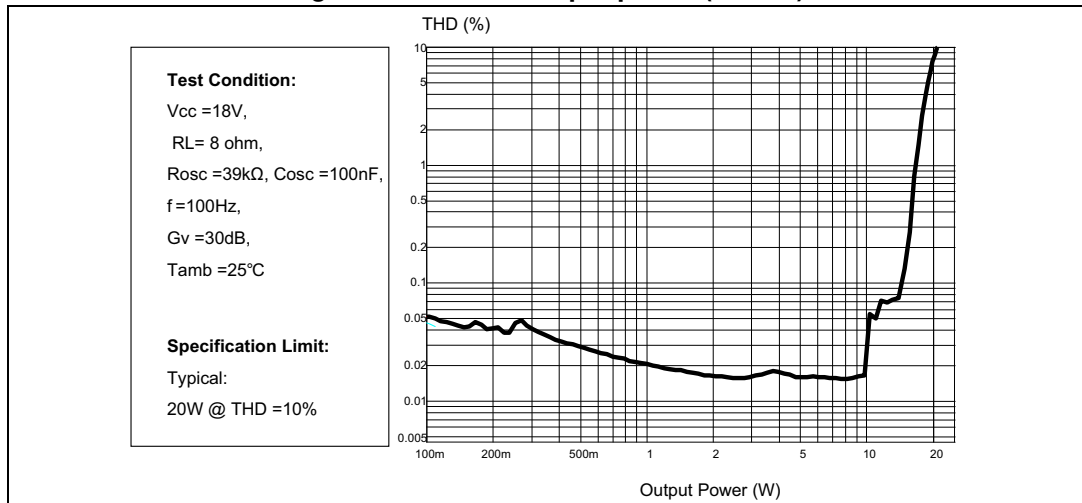


Figure 36. THD vs. frequency

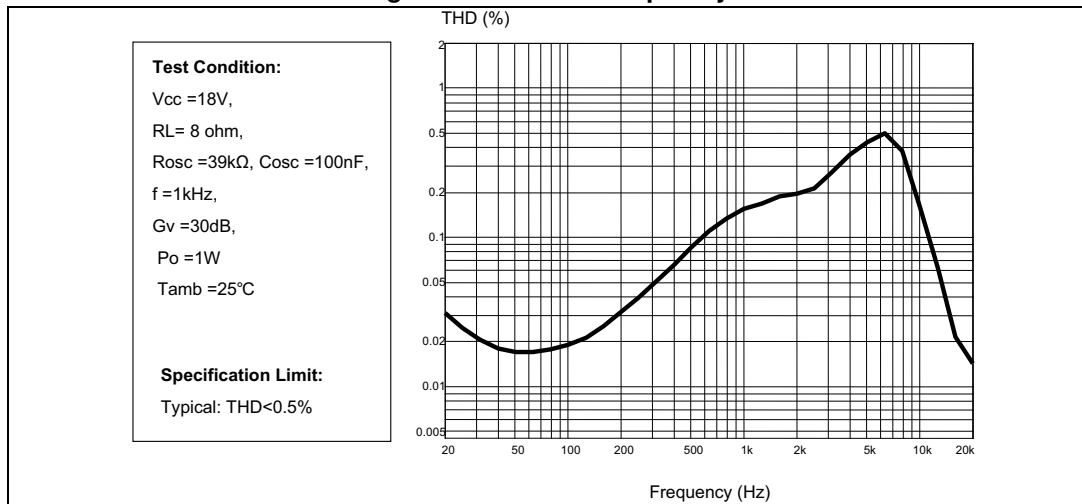


Figure 37. Frequency response

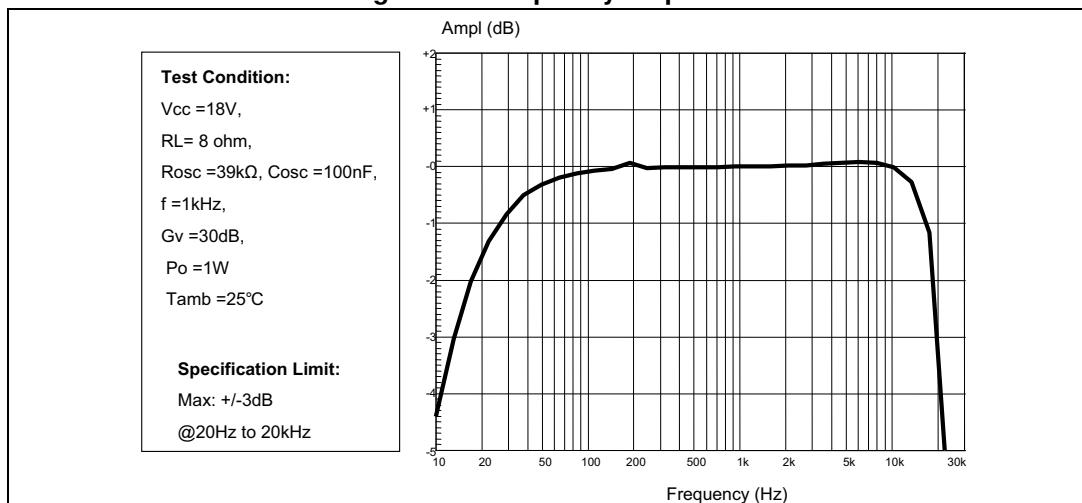


Figure 38. Crosstalk vs. frequency

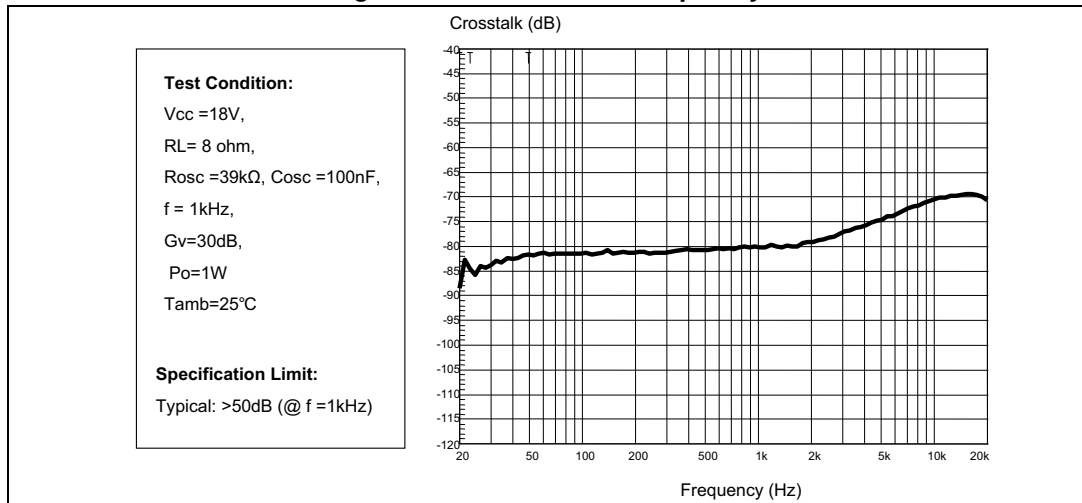


Figure 39. FFT (0 dB)

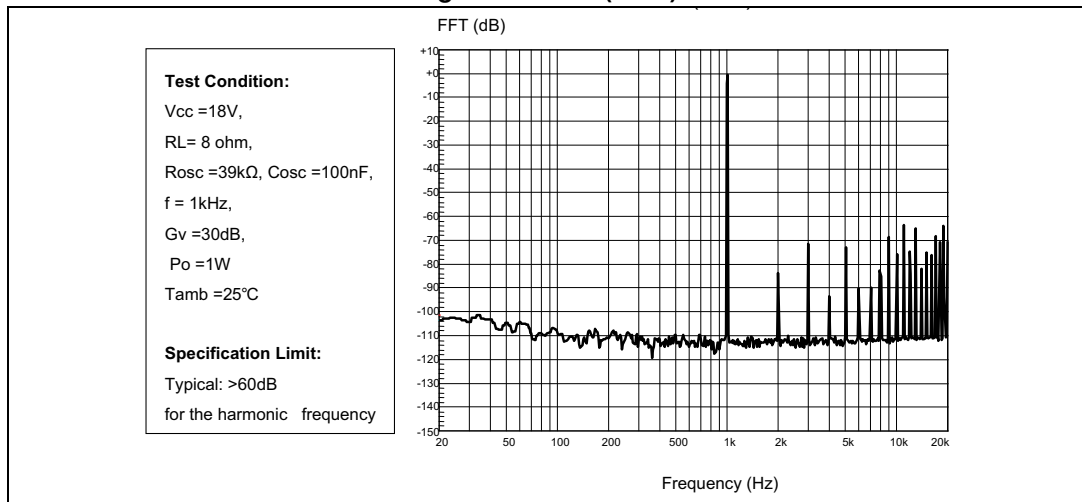


Figure 40. FFT (-60 dB)

