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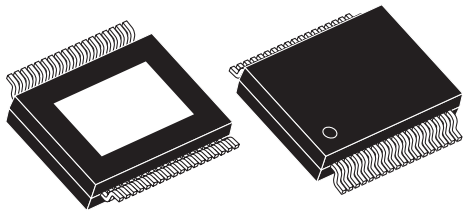
TDA7491LP

2 x 5-watt dual BTL class-D audio amplifier

Features

- 5 W + 5 W continuous output power: R_L = 8 Ω, THD = 10% at V_{CC} = 9 V
- 5 W + 5 W continuous output power: R_L = 4 Ω, THD = 10% at V_{CC} = 6.6 V
- Wide range single supply operation (5 V - 14 V)
- High efficiency (η = 90%)
- Four selectable, fixed gain settings of nominally 20 dB, 26 dB, 30 dB and 32 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- No ‘pop’ at turn-on/off
- Standby and mute features
- Short-circuit protection
- Thermal overload protection
- Externally synchronizable



PowerSSO-36 with exposed pad down

Description

The TDA7491LP is a dual BTL class-D audio amplifier with single power supply designed for LCD TVs and monitors.

Thanks to the high efficiency and exposed-pad-down (EPD) package no separate heatsink is required.

Furthermore, the filterless operation allows a reduction in the external component count.

The TDA7491LP is pin-to-pin compatible with the TDA7491P and TDA7491HV.

Table 1. Device summary

Order code	Operating temperature	Package	Packaging
TDA7491LP	-40 to 85 °C	PowerSSO-36 EPD	Tube
TDA7491LP13TR	-40 to 85 °C	PowerSSO-36 EPD	Tape and reel

Contents

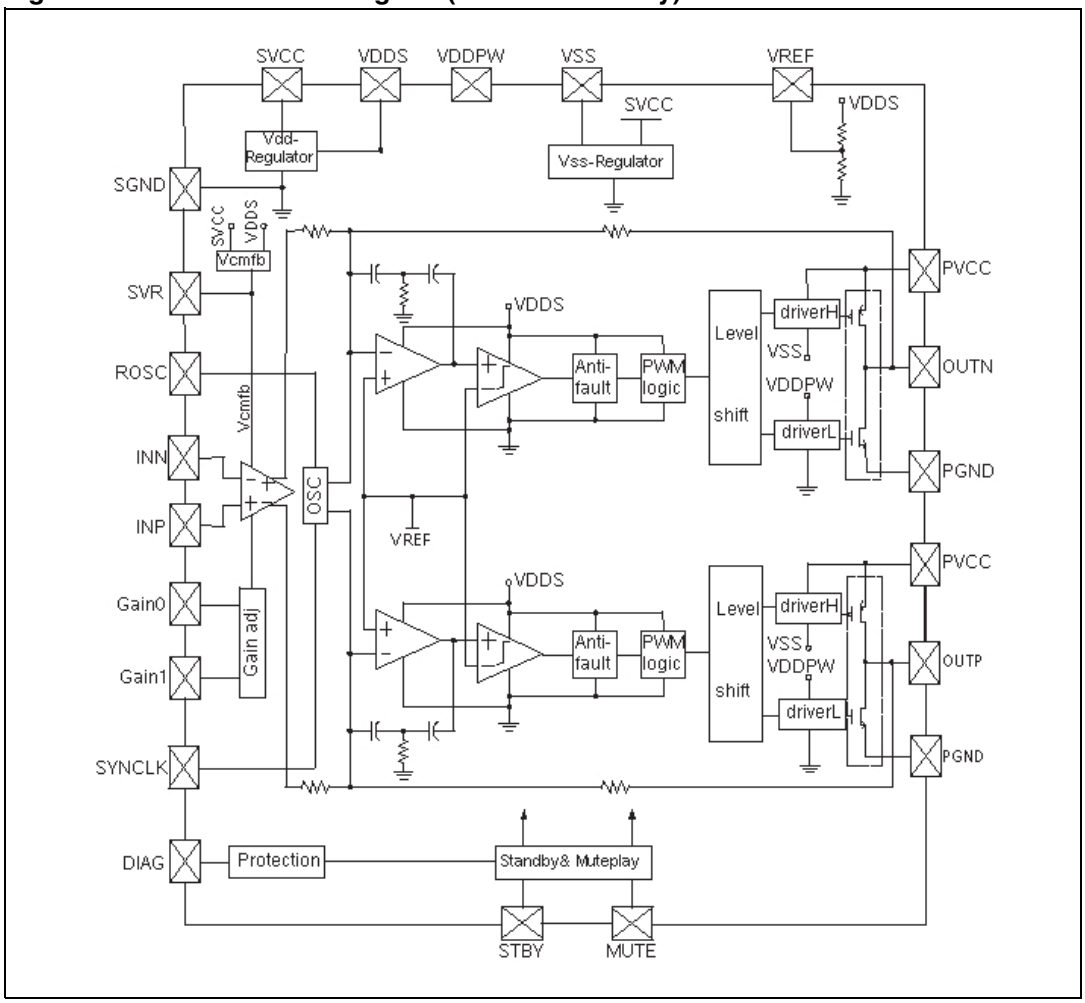
List of tables

List of figures

1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7491LP.

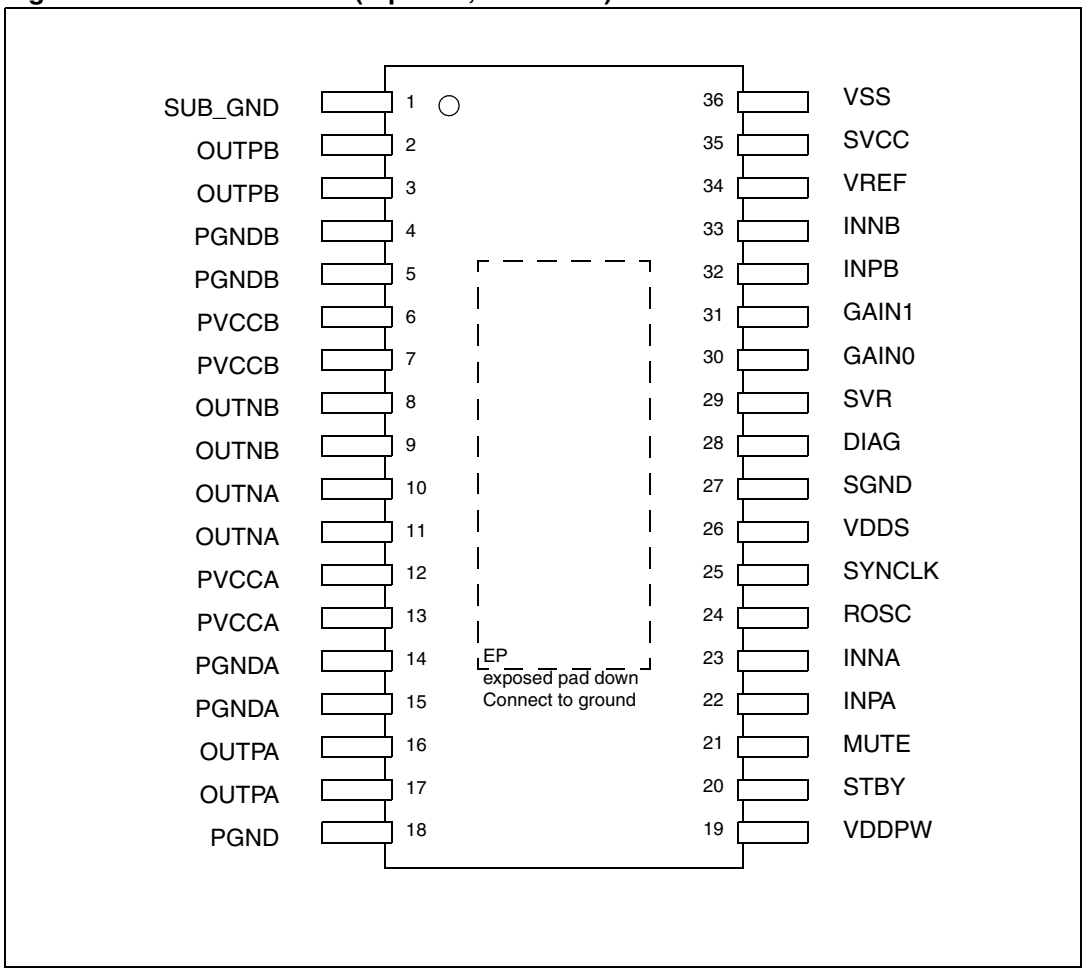
Figure 1. Internal block diagram (one channel only)



2 Pin description

2.1 Pin out

Figure 2. Pin connection (top view, PCB view)



2.2 Pin list

Table 2. Pin description list

Number	Name	Type	Description
1	SUB_GND	POWER	Connect to the frame
2,3	OUTPB	OUT	Positive PWM output for right channel
4,5	PGNDB	POWER	Power stage ground for right channel
6,7	PVCCB	POWER	Power supply for right channel
8,9	OUTNB	OUT	Negative PWM output for right channel
10,11	OUTNA	OUT	Negative PWM output for left channel
12,13	PVCCA	POWER	Power supply for left channel
14,15	PGNDA	POWER	Power stage ground for left channel
16,17	OUTPA	OUT	Positive PWM output for left channel
18	PGND	POWER	Power stage ground
19	VDDPW	OUT	3.3-V (nominal) regulator output referred to ground for power stage
20	STBY	INPUT	Standby mode control
21	MUTE	INPUT	Mute mode control
22	INPA	INPUT	Positive differential input of left channel
23	INNA	INPUT	Negative differential input of left channel
24	ROSC	OUT	Master oscillator frequency-setting pin
25	SYNCLCK	IN/OUT	Clock in/out for external oscillator
26	VDDS	OUT	3.3-V (nominal) regulator output referred to ground for signal blocks
27	SGND	POWER	Signal ground
28	DIAG	OUT	Open-drain diagnostic output
29	SVR	OUT	Supply voltage rejection
30	GAIN0	INPUT	Gain setting input 1
31	GAIN1	INPUT	Gain setting input 2
32	INPB	INPUT	Positive differential input of right channel
33	INNB	INPUT	Negative differential input of right channel
34	VREF	OUT	Half VDDS (nominal) referred to ground
35	SVCC	POWER	Signal power supply
36	VSS	OUT	3.3-V (nominal) regulator output referred to power supply
-	EP	-	Exposed pad for ground-plane heatsink, to be connected to GND

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	18	V
V_I	Voltage limits for input pins STBY, MUTE, INNA, INPA, INNB, INPB, GAIN0, GAIN1	-0.3 to 3.6	V
T_{op}	Operating temperature	-40 to 85	°C
T_j	Operating junction temperature	-40 to 150	°C
T_{stg}	Storage temperature	-40 to 150	°C

3.2 Thermal data

Refer also to *Section 5.9: Heatsink requirements on page 32*.

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction to case	-	2	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction to ambient	-	24	-	

3.3 Electrical specifications

Unless otherwise stated, the results in *Table 5* below are given for the conditions: V_{CC} = 9 V, R_L (load) = 8Ω, R_{OSC} = R3 = 39 kΩ, C8 = 100 nF, f = 1 kHz, G_V = 20 dB, and T_{amb} = 25 °C.

Table 5. Electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply voltage	-	5	-	14	V
I_q	Total quiescent current	Without LC filter	-	26	35	mA
I_{qSTBY}	Quiescent current in standby	-	-	-	10	µA
V_{OS}	Output offset voltage	Play mode	-100	-	100	mV
		Mute mode	-60	-	60	mV
I_{OCP}	Overcurrent protection threshold	R_L = 0 Ω	3	-	-	A
T_j	Junction temperature at thermal shutdown	-	-	150	-	°C
R_i	Input resistance	Differential input	54	68	-	kΩ
V_{UVP}	Undervoltage protection threshold	-	-	-	4.5	V
R_{dsON}	Power transistor on resistance	High side	-	0.2	-	Ω
		Low side	-	0.2	-	
P_o	Output power	THD = 10%	-	5.0	-	W
		THD = 1%	-	4.0	-	
P_o	Output power	R_L = 4 Ω, THD = 10%, V_{CC} = 6.6 V	-	5.0	-	W
		R_L = 4 Ω, THD = 1%, V_{CC} = 6.6 V	-	4.0	-	
P_D	Dissipated power	P_o = 5 W + 5 W, THD = 10%	-	1.0	-	W
η	Efficiency	P_o = 5 W + 5 W, R_L = 8 Ω, THD = 10%, V_{CC} = 9 V	-	90	-	%
THD	Total harmonic distortion	P_o = 1 W	-	0.1	-	%
G_V	Closed loop gain	GAIN0 = L, GAIN1 = L	18	20	22	dB
		GAIN0 = L, GAIN1 = H	24	26	28	
		GAIN0 = H, GAIN1 = L	28	30	32	
		GAIN0 = H, GAIN1 = H	30	32	34	
ΔG_V	Gain matching	-	-1	-	1	dB
CT	Crosstalk	f = 1 kHz, P_o = 1 W	-	70	-	dB
eN	Total input noise	A Curve, G_V = 20 dB	-	15	-	µV
		f = 22 Hz to 22 kHz	-	20	-	

Table 5. Electrical specifications (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
SVRR	Supply voltage rejection ratio	fr = 100 Hz, Vr = 1 Vpp, C_{SVR} = 10 µF	-	50	-	dB
T_r, T_f	Rise and fall times	-	-	40	-	ns
f_{SW}	Switching frequency	Internal oscillator, master mode	290	320	350	kHz
f_{SWR}	Switching frequency range	(1)	250	-	400	kHz
V_{inH}	Digital input high (H)	-	2.3	-	-	V
V_{inL}	Digital input low (L)		-	-	0.8	
A_{MUTE}	Mute attenuation	V_{MUTE} = low, V_{STBY} = high	-	80	-	dB
Function mode	Standby, mute and play modes	V_{STBY} < 0.5 V V_{MUTE} = X	Standby			-
		V_{STBY} > 2.9 V V_{MUTE} < 0.8 V	Mute			-
		V_{STBY} > 2.9 V V_{MUTE} > 2.9 V	Play			-

1. Refer to *Section 5.5: Internal and external clocks on page 27*.

4 Characterization curves

The following characterization curves were made using the TDA7491LP demo board. The LC filter for the 4-Ω load uses components of 15 µH and 470 nF and that for the 8-Ω load uses 33 µH and 220 nF.

4.1 With 4-Ω load at V_{CC} = 6.6 V

Figure 3. Output power vs. supply voltage

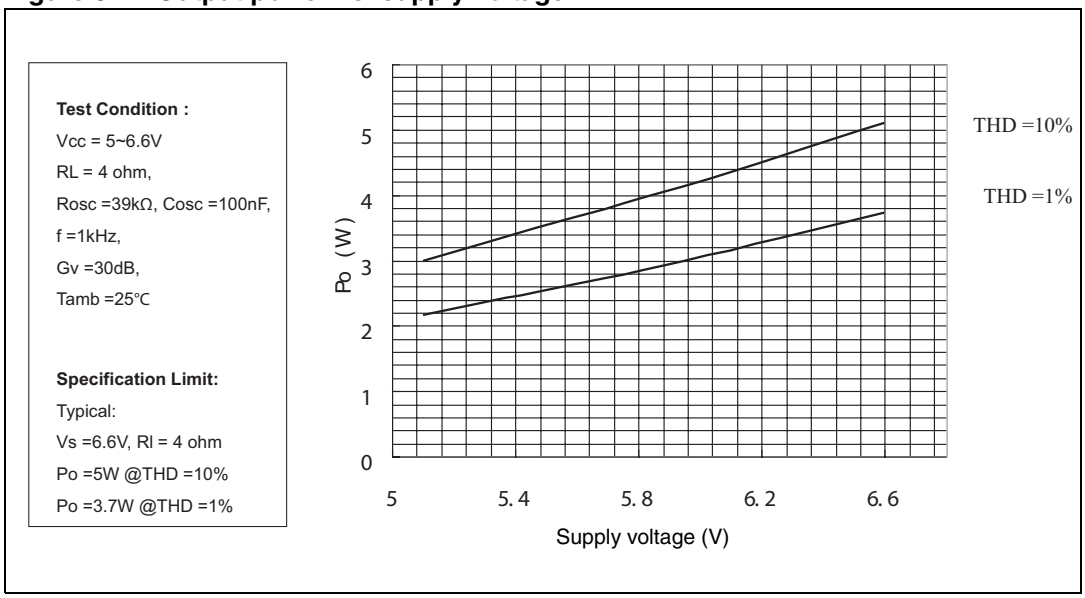


Figure 4. THD vs. output power (1 kHz)

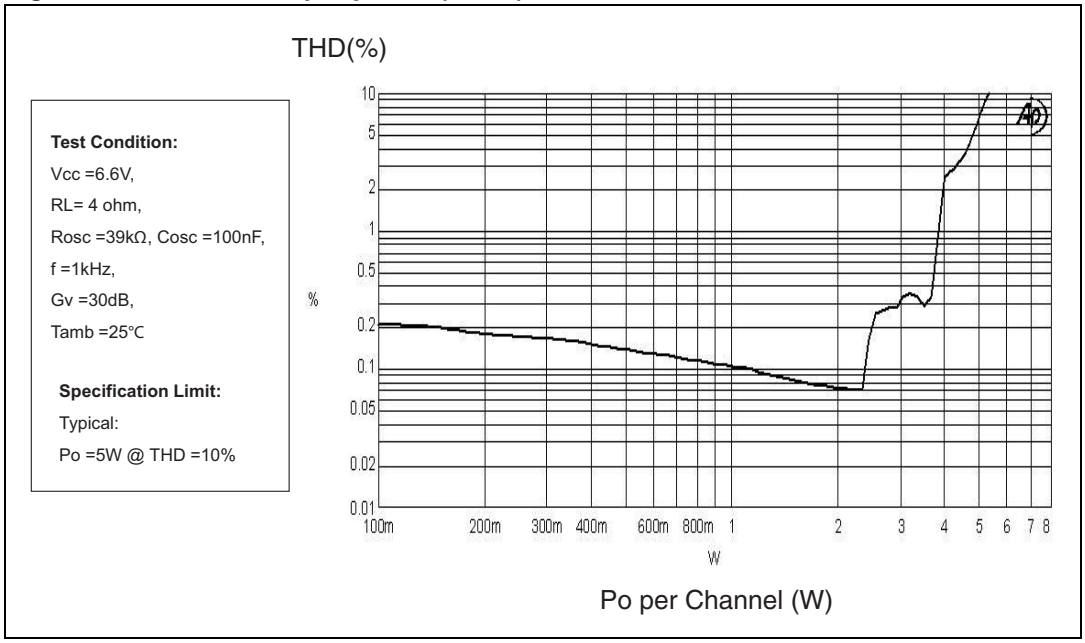


Figure 5. THD vs. output power (100 Hz)

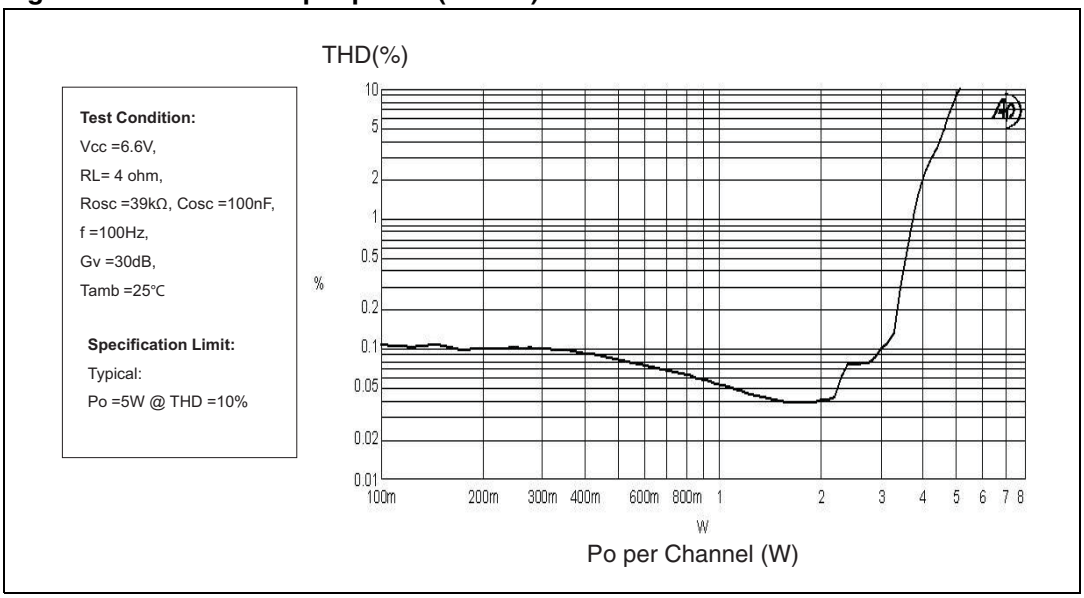


Figure 6. THD vs. frequency

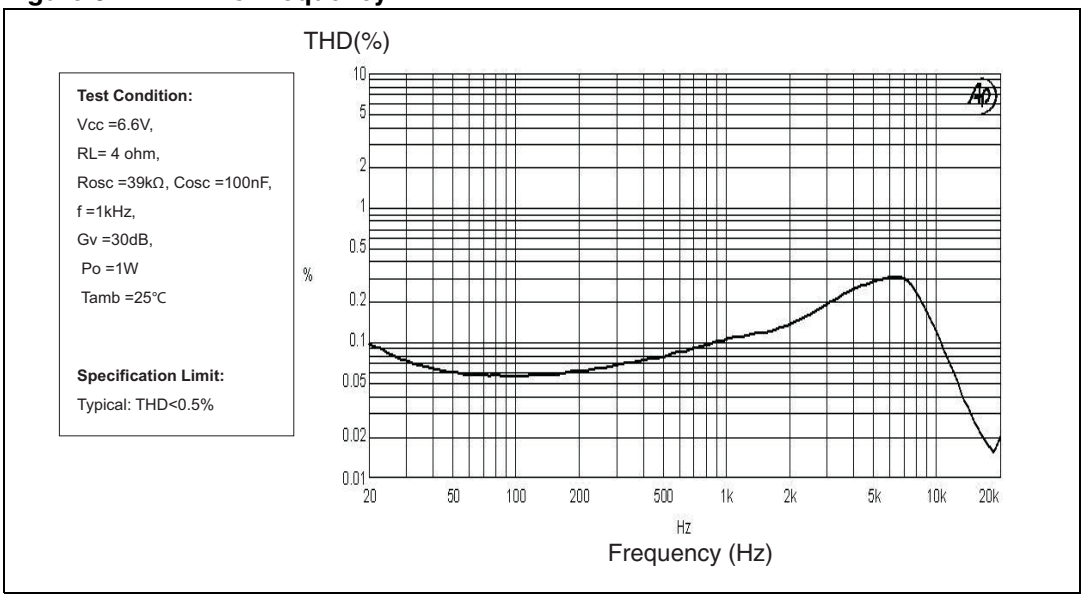


Figure 7. Frequency response

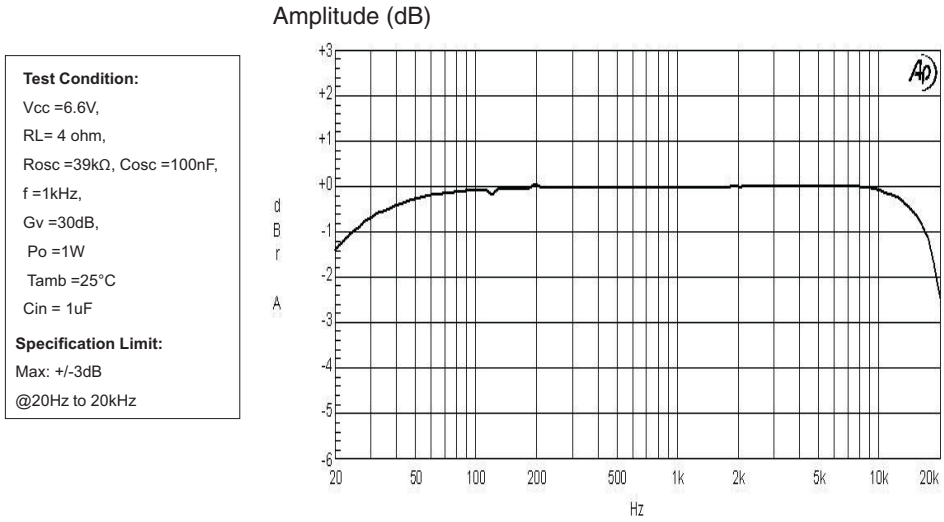


Figure 8. Crosstalk vs. frequency

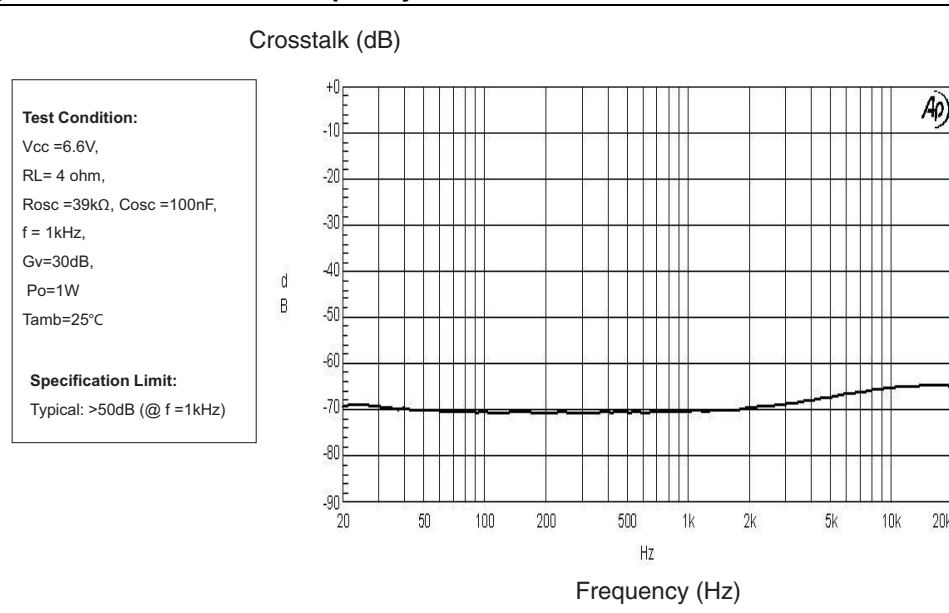


Figure 9. FFT (0 dB)

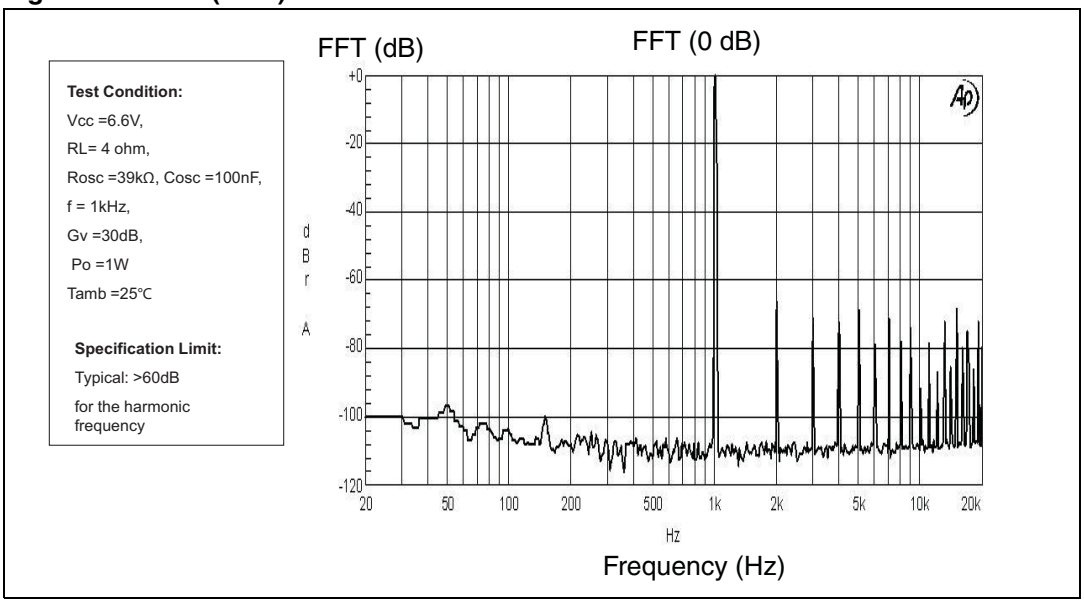


Figure 10. FFT (-60 dB)

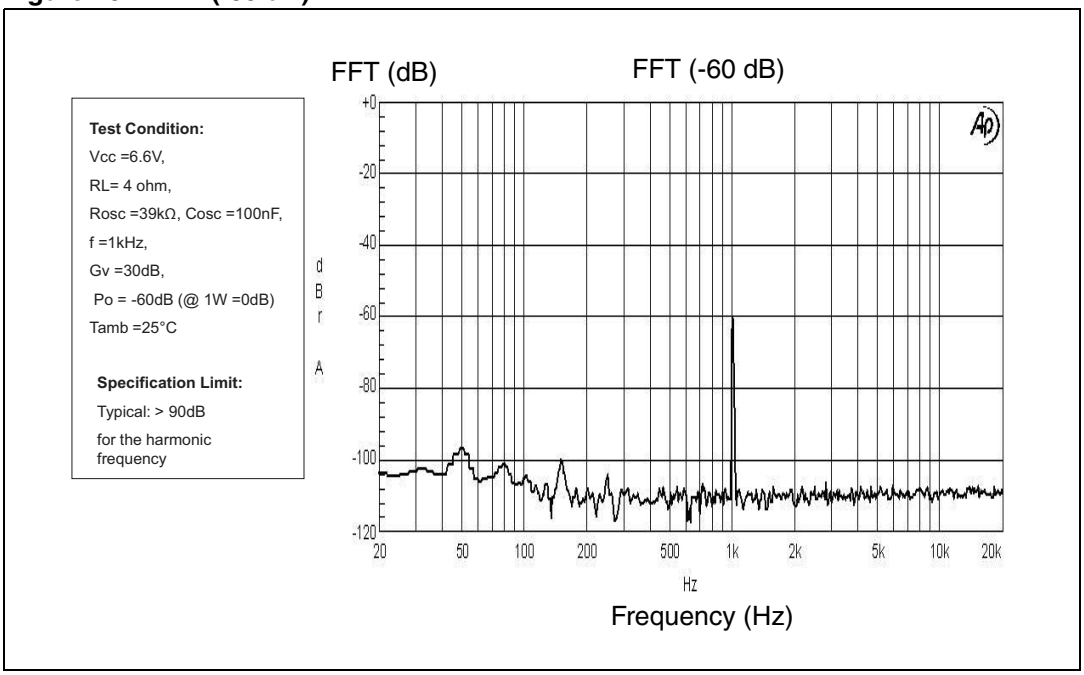


Figure 11. Power supply rejection ratio vs. frequency

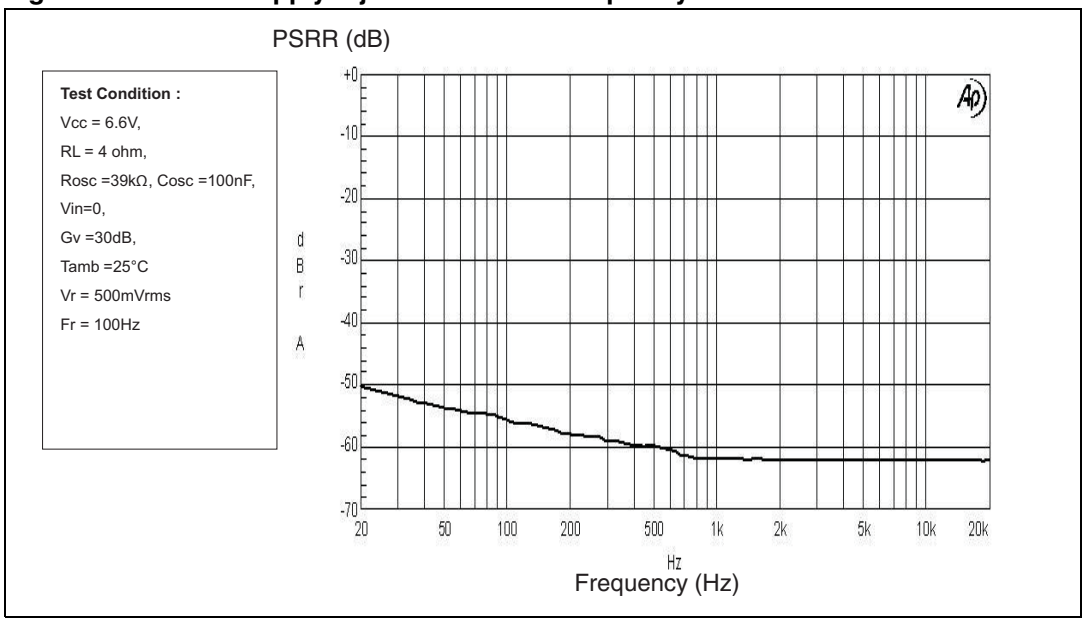


Figure 12. Power dissipation and efficiency vs. output power

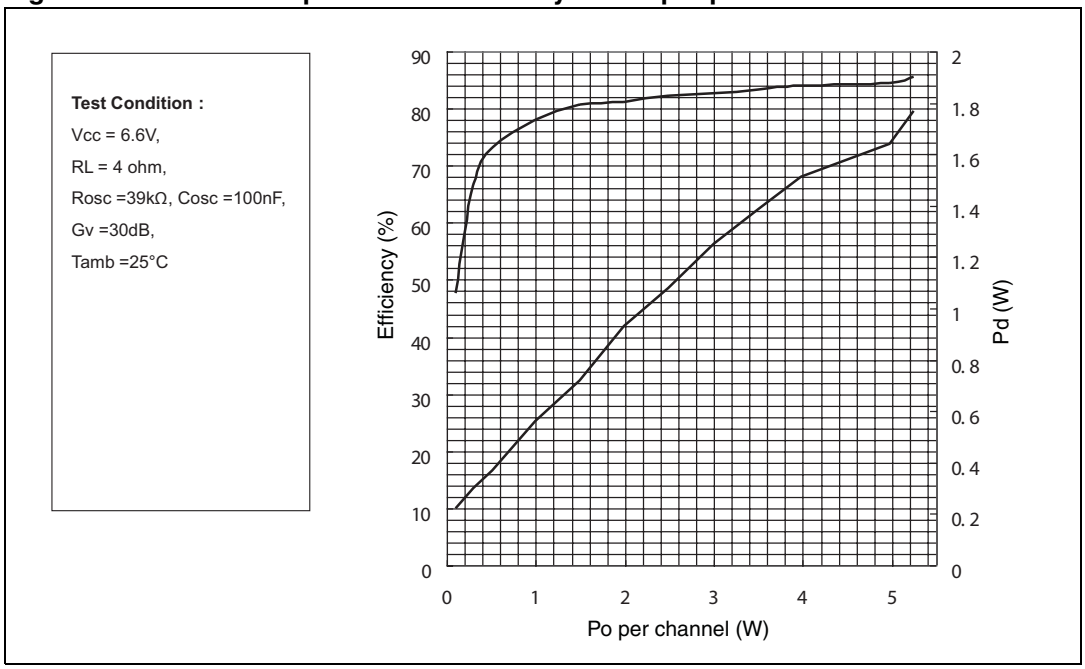


Figure 13. Attenuation vs. voltage on pin MUTE

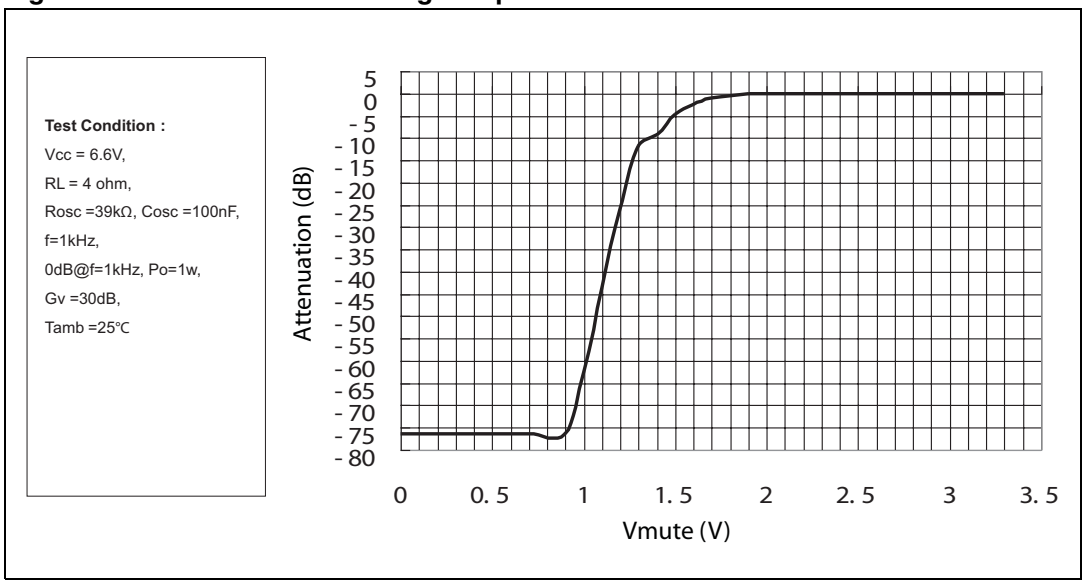


Figure 14. Current consumption vs. voltage on pin STBY

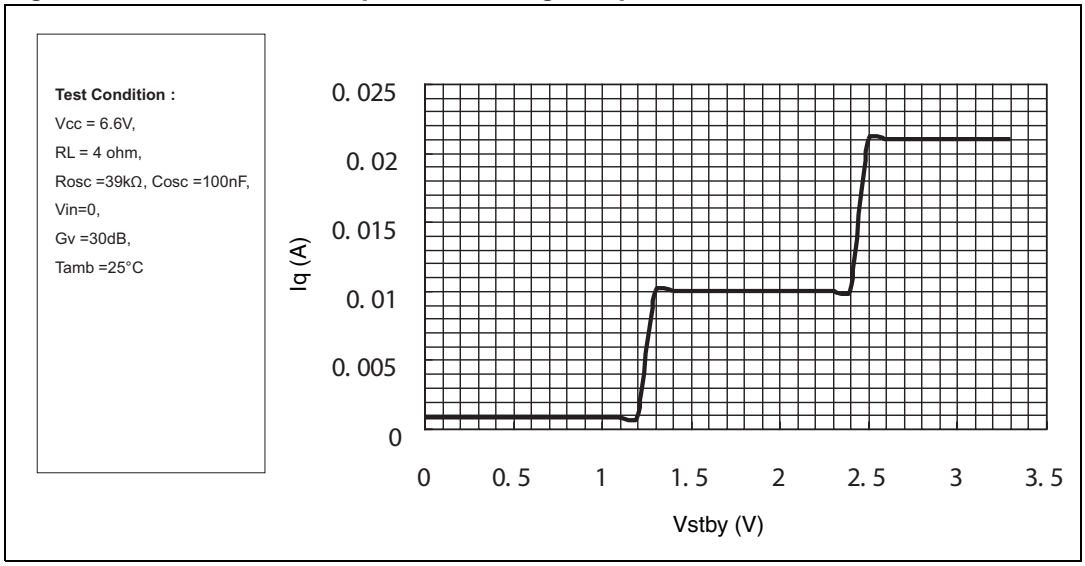
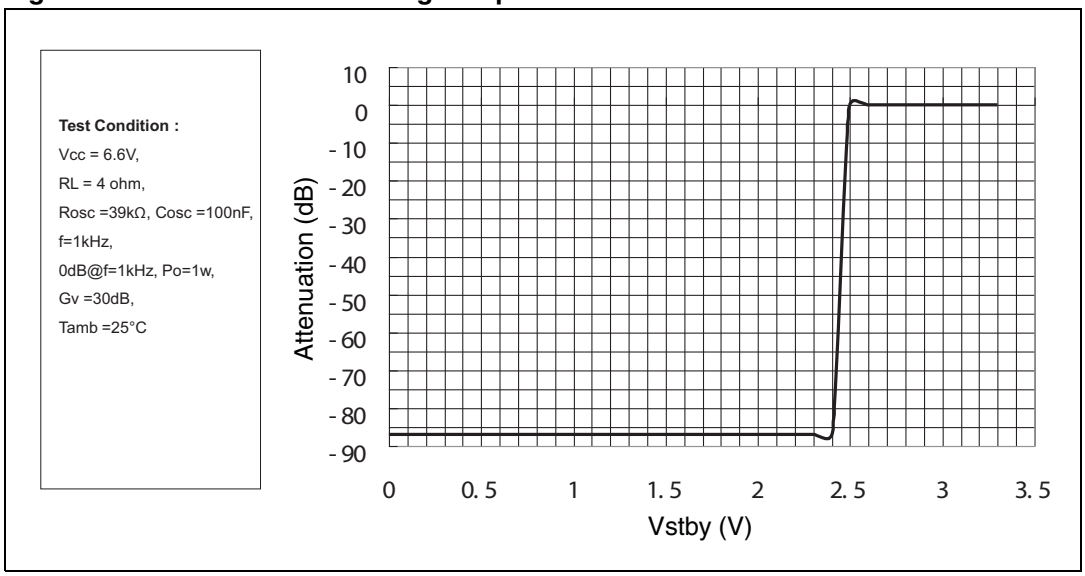


Figure 15. Attenuation vs. voltage on pin STBY



4.2 With 8-Ω load at V_{CC} = 9 V

Figure 16. Output power vs. supply voltage

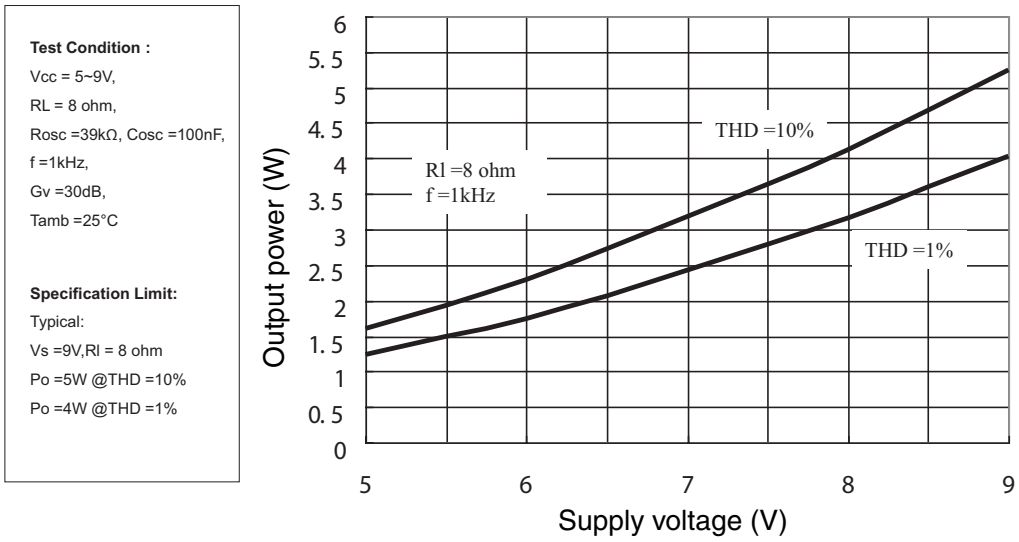


Figure 17. THD vs. output power (1 kHz)

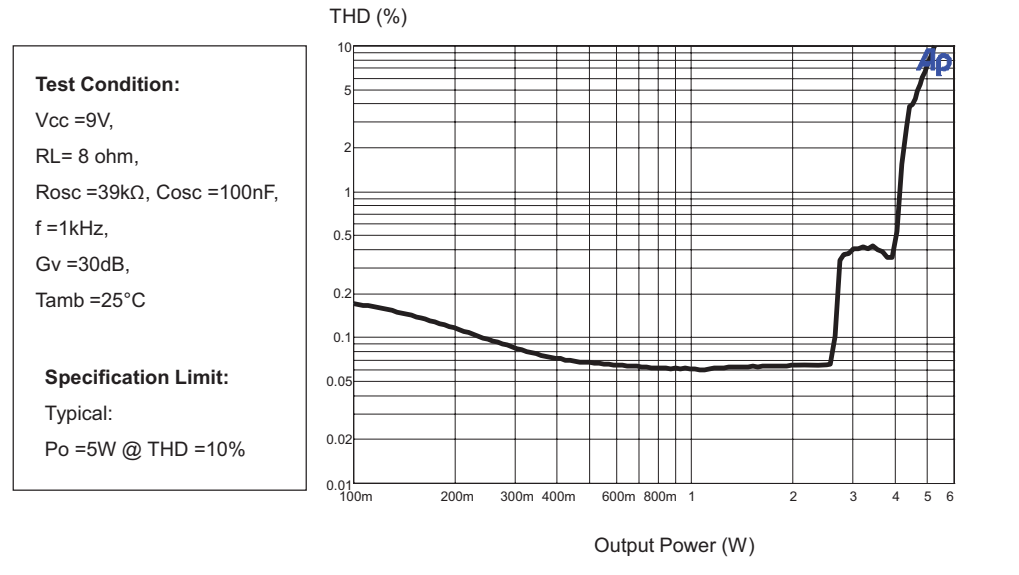


Figure 18. THD vs. output power (100 Hz)

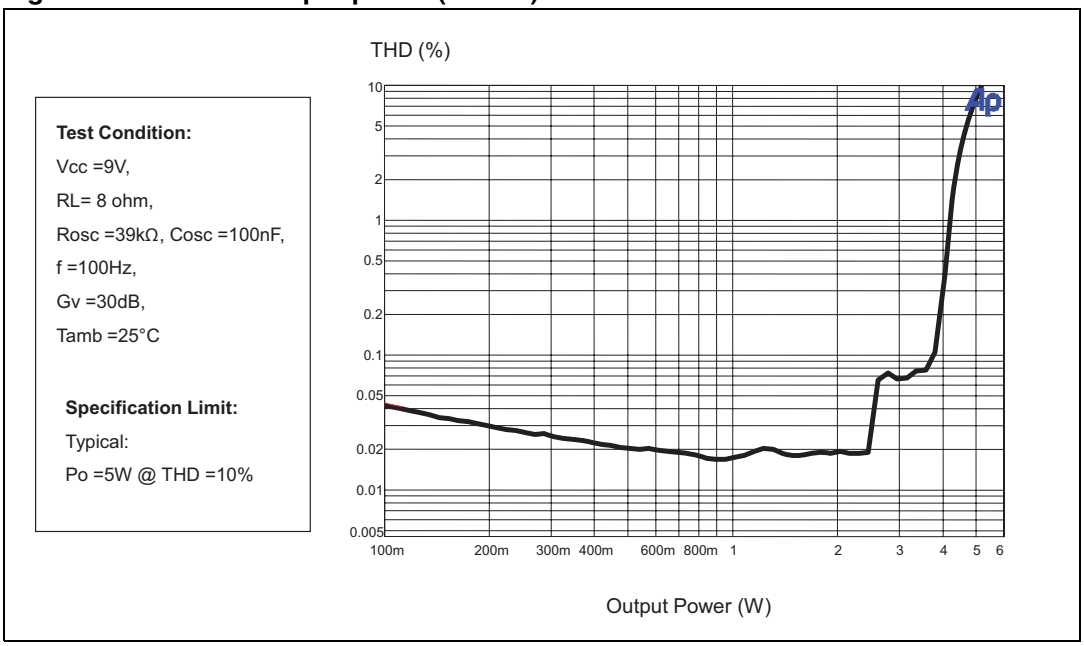


Figure 19. THD vs. frequency

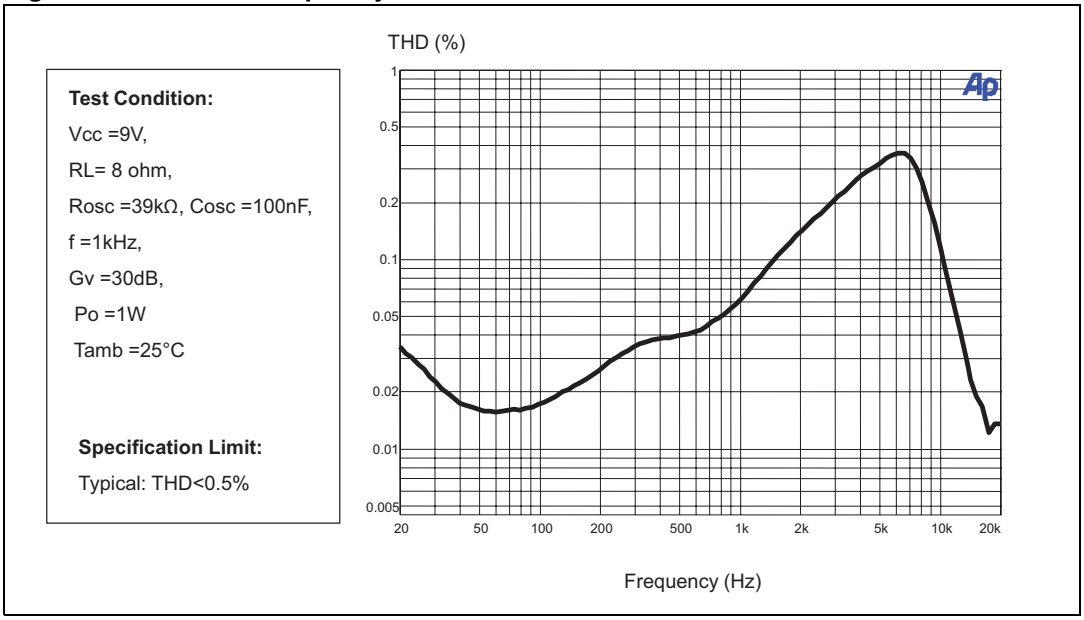


Figure 20. Frequency response

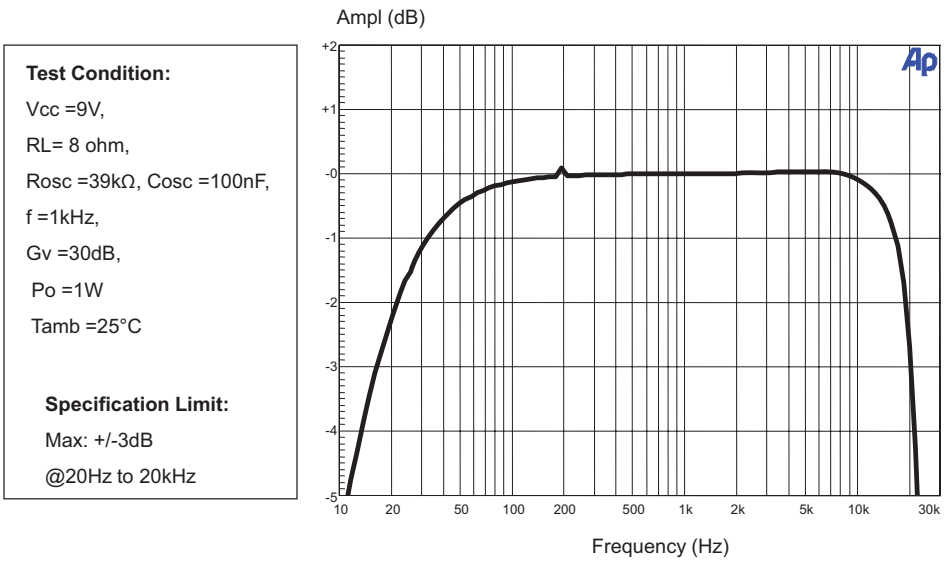


Figure 21. Crosstalk vs. frequency

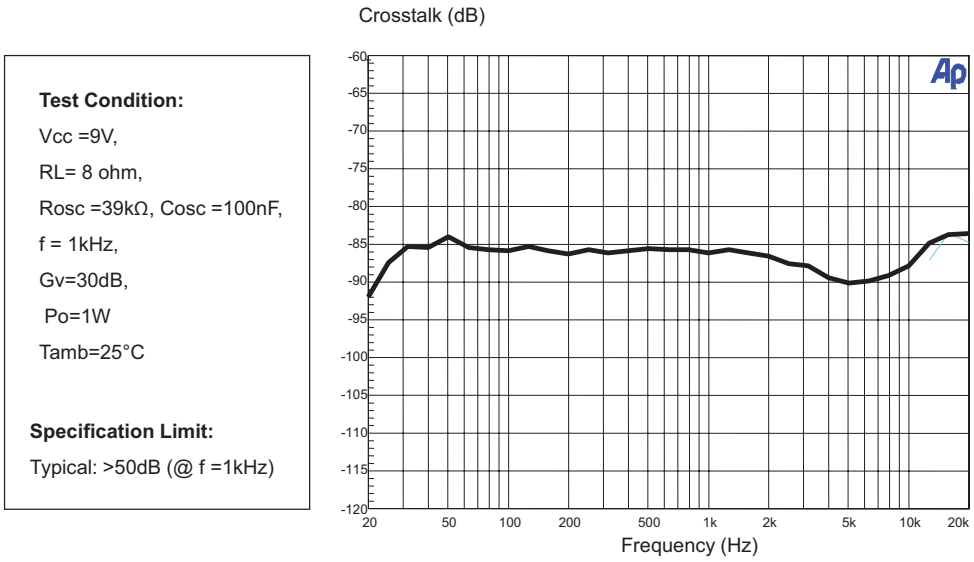


Figure 22. FFT (0 dB)

Test Condition:
Vcc =9V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f = 1kHz,
Gv =30dB,
Po =1W
Tamb =25°C

Specification Limit:
Typical: >60dB
for the harmonic frequency

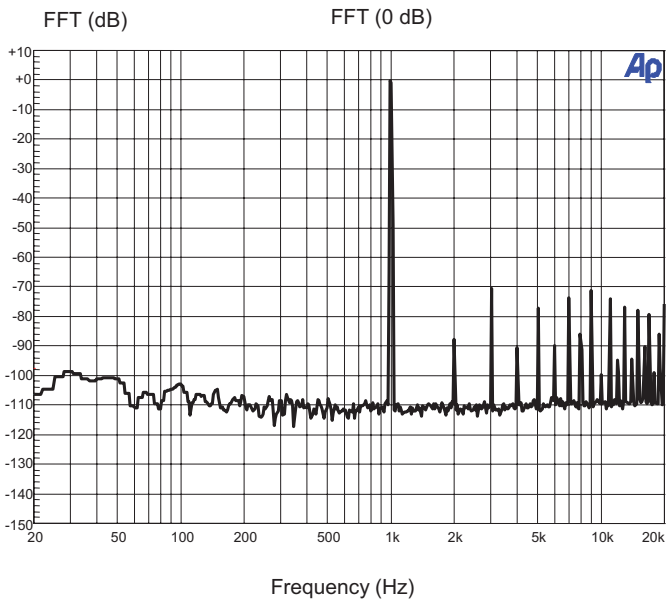


Figure 23. FFT (-60 dB)

Test Condition:
Vcc =9V,
RL= 8 ohm,
Rosc =39kΩ, Cosc =100nF,
f =1kHz,
Gv =30dB,
Po = -60dB (@ 1W =0dB)
Tamb =25°C

Specification Limit:
Typical: > 90dB
for the harmonic frequency

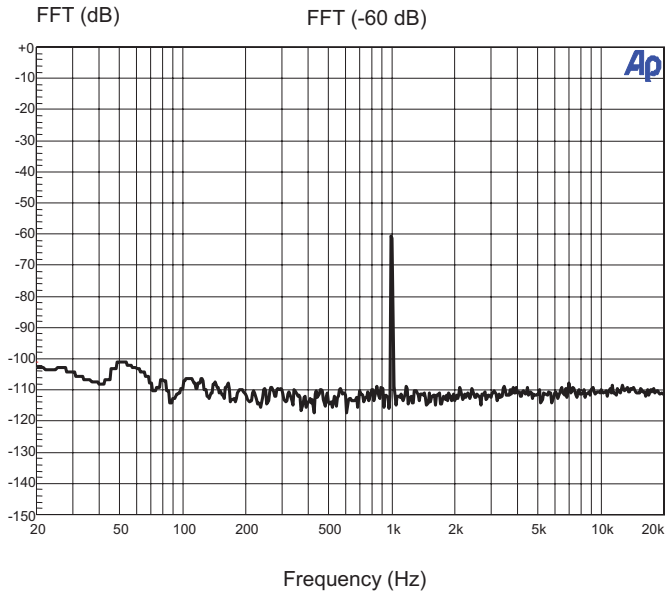


Figure 24. Power supply rejection ratio vs. frequency

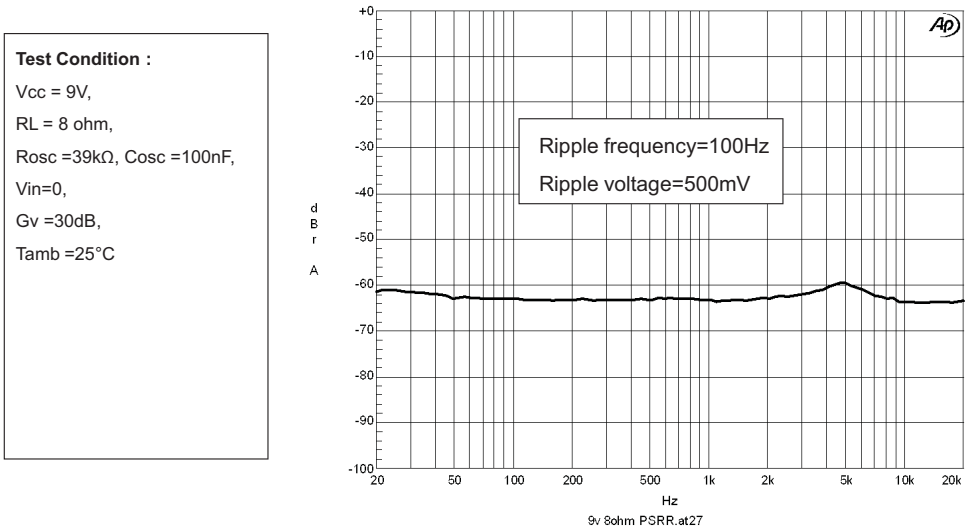
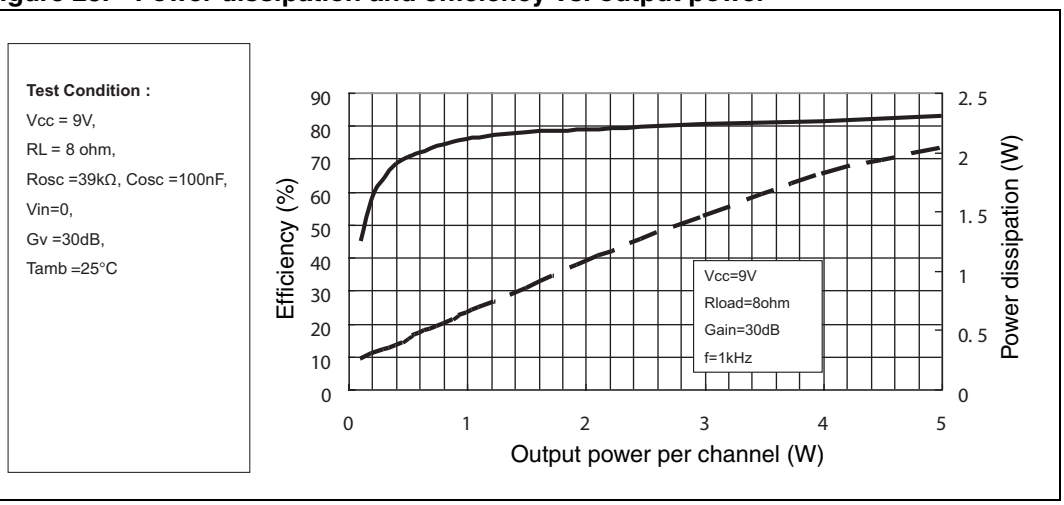


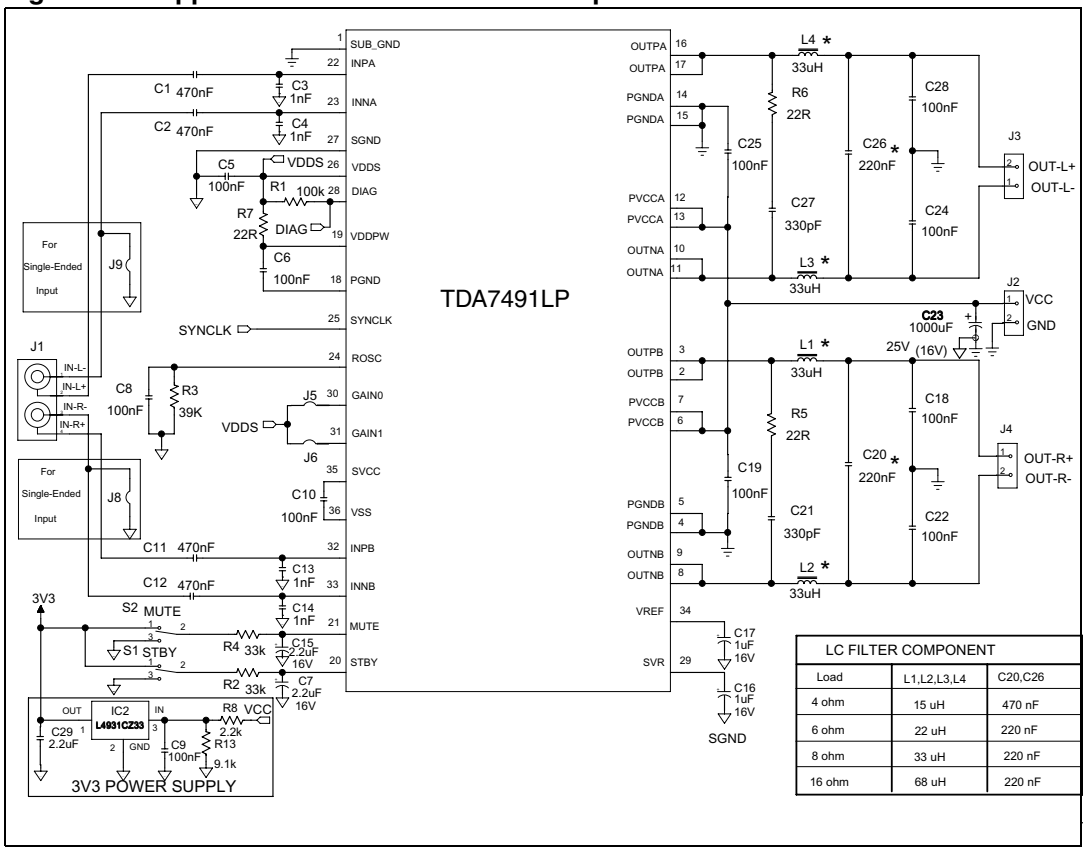
Figure 25. Power dissipation and efficiency vs. output power



5 Applications information

5.1 Applications circuit

Figure 26. Applications circuit for class-D amplifier



LC FILTER COMPONENT		
Load	L1,L2,L3,L4	C20,C26
4 ohm	15 uH	470 nF
6 ohm	22 uH	220 nF
8 ohm	33 uH	220 nF
16 ohm	68 uH	220 nF

5.2 Mode selection

The three operating modes, defined below, of the TDA7491LP are set by the two inputs STBY (pin 20) and MUTE (pin 21) as shown in *Table 6*.

- Standby mode: all circuits are turned off, very low current consumption.
- Mute mode: inputs are connected to ground and the positive and negative PWM outputs are at 50% duty cycle.
- Play mode: the amplifiers are active.

The protection functions of the TDA7491LP are implemented by pulling down the voltages of the STBY and MUTE inputs shown in *Figure 27*. The input current of the corresponding pins must be limited to 200 µA.

Table 6. Mode settings

Mode	Voltage level on pin STBY	Voltage level on pin MUTE
Standby	L (1)	X (don't care)
Mute	H (1)	L
Play	H	H

1. Refer to V_{STBY} and V_{MUTE} in *Table 5: Electrical specifications on page 10* for the drive levels for L and H

Figure 27. Standby and mute circuits

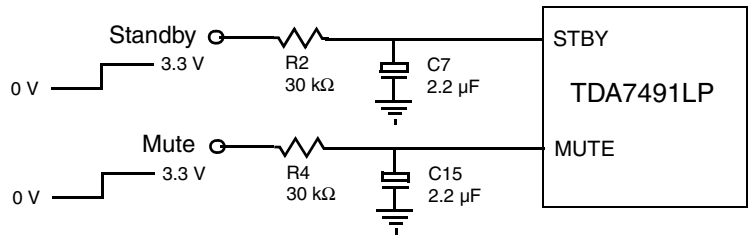


Figure 28. Turn-on/off sequence for minimizing speaker "pop"