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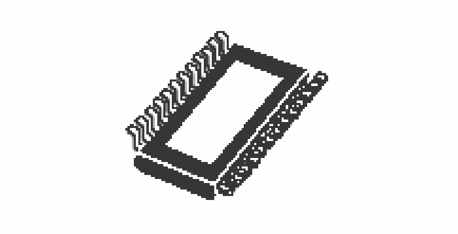
TDA7493

3-watt + 3-watt dual BTL class-D audio amplifier

Features

- 3.0 W + 3.0 W of continuous output power with R_L = 4 Ω, THD = 10%, V_{CC} = 5 V (filterless)
- 2.8 W + 2.8 W of continuous output power with R_L = 4 Ω, THD = 10%, V_{CC} = 5 V (with filter)
- Single supply voltage range 3.0 V to 5.5 V
- High efficiency (η = 83%)
- Four selectable, fixed gain settings of 6 dB, 12 dB, 15.6 dB and 18 dB
- Differential inputs minimize common-mode noise
- Filterless operation
- Standby feature
- Short-circuit protection
- Thermal-overload protection
- Externally synchronizable



HTSSOP24 package with exposed pad down

Description

The TDA7493 is a dual BTL class-D audio amplifier, specially designed for LCD TV, LCD monitors or small speakers on cradles with single-supply operation.

The filterless operation allows the external component count to be reduced.

The TDA7493 is assembled in the HTSSOP24 package. Thanks to the high efficiency and to the exposed-pad-down (EPD) package no separate heatsink is required.

Table 1. Device summary

Order codes	Operating temperature range	Package	Packaging
TDA7493	0 to 70 °C	HTSSOP24 (EPD)	Tube
TDA749313TR	0 to 70 °C	HTSSOP24 (EPD)	Tape and reel

Contents

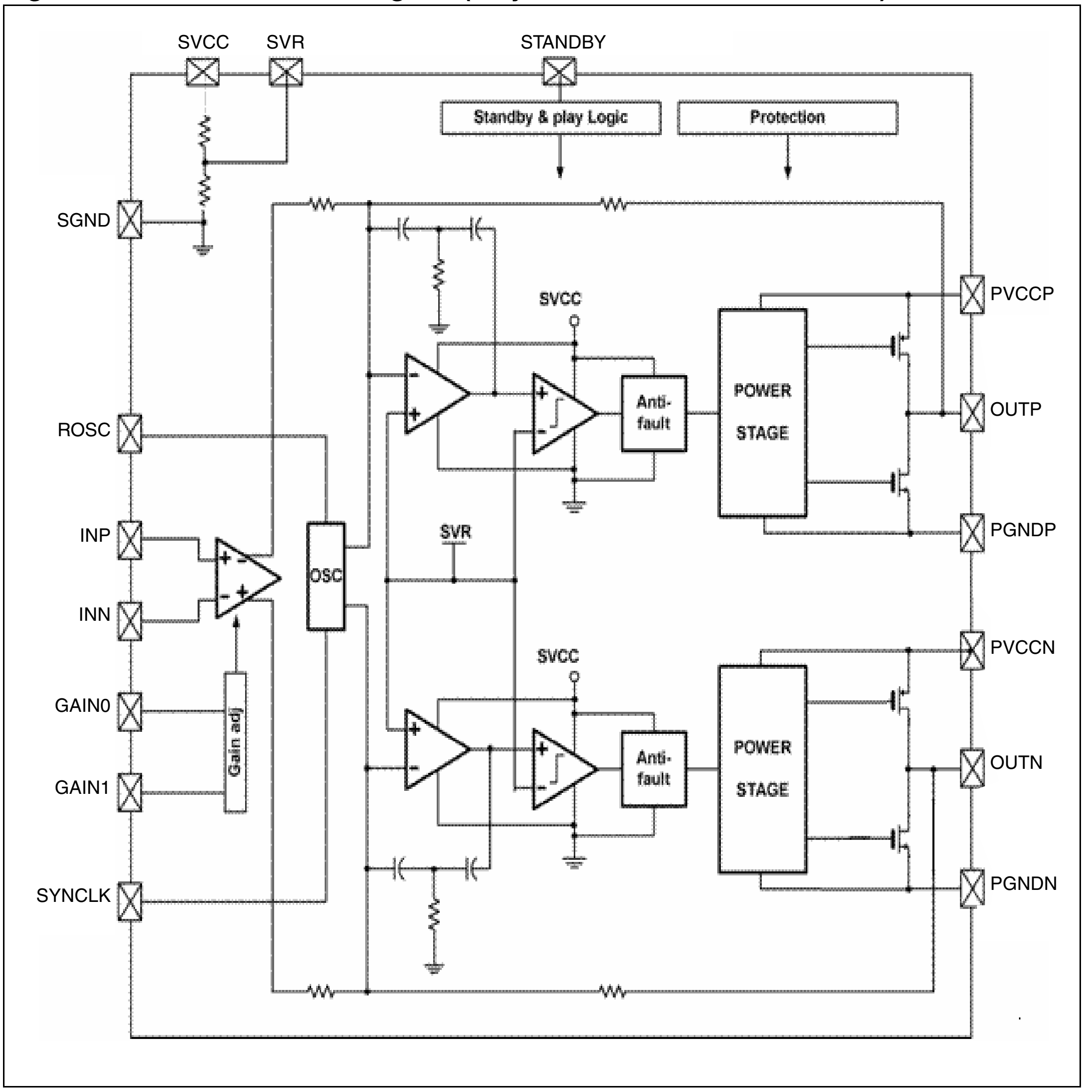
List of figures

List of tables

1 Device block diagram

Figure 1 shows the block diagram of one of the two identical channels of the TDA7493.

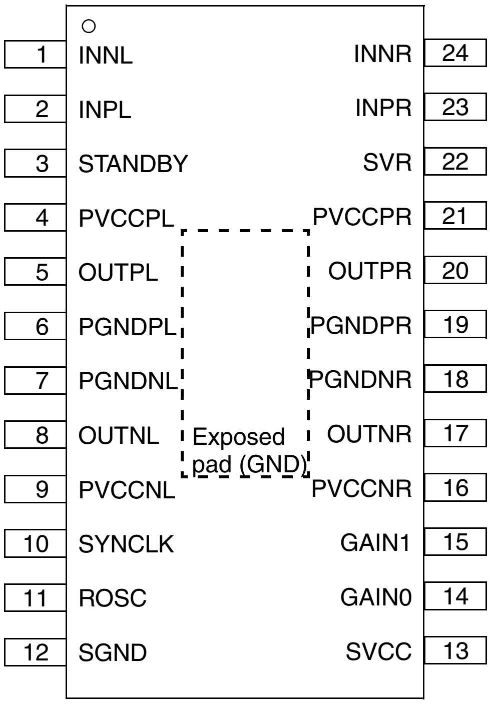
Figure 1. TDA7493 block diagram (only one of two channels shown)



2 Pin description

2.1 Pin-out

Figure 2. Pin connection (top view)



The exposed pad is the device ground and must be connected appropriately

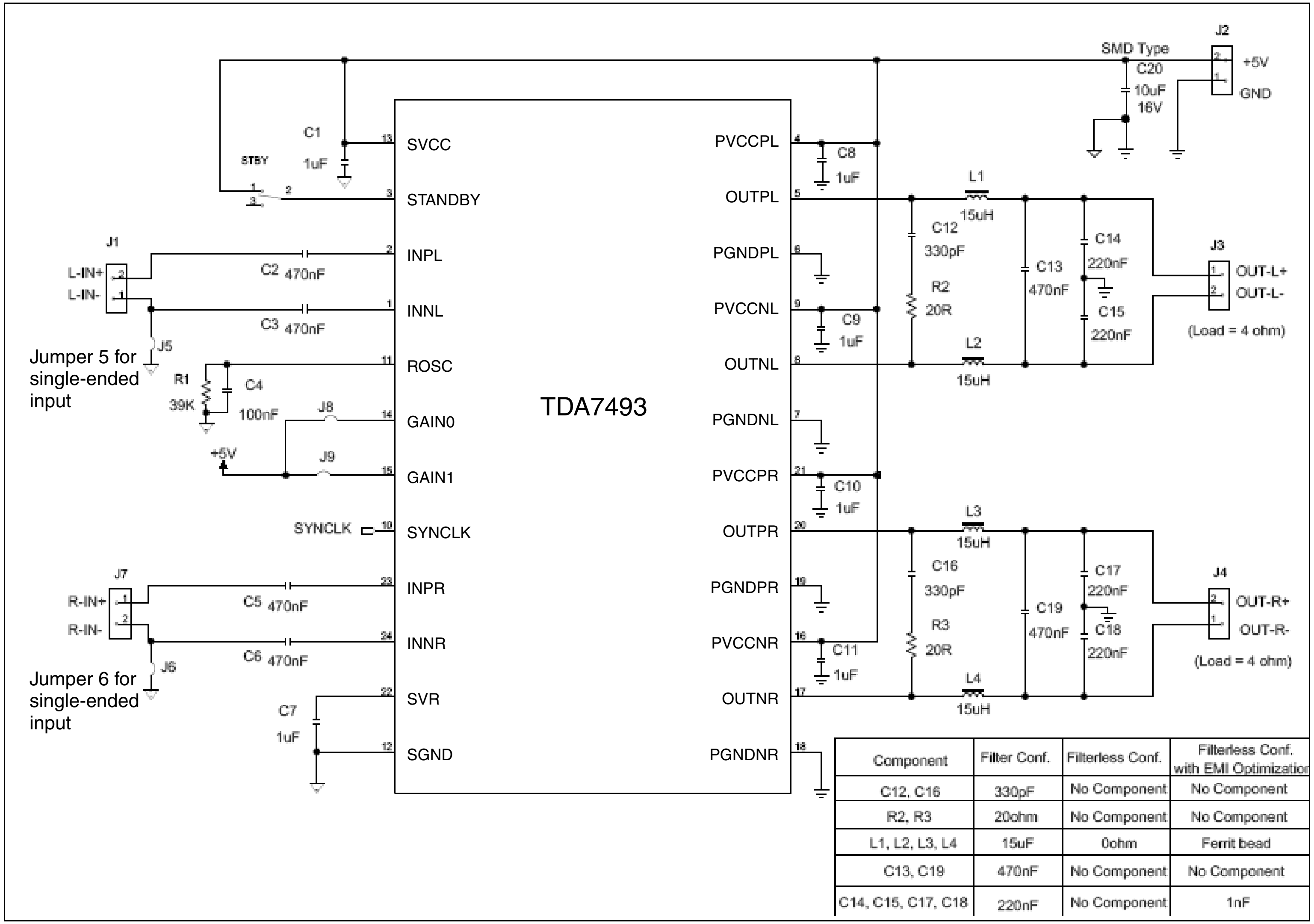
2.2 Pin list

Table 2. Pin list

Number	Name	Type	Description
1	INNL	IN	Negative differential input of left channel
2	INPL	IN	Positive differential input of left channel
3	STANDBY	IN	Standby mode control (digital): 0: standby 1: play
4	PVCCPL	POWER	Power supply for positive branch in left channel
5	OUTPL	OUT	Positive PWM output for left channel
6	PGNDPL	POWER	Power stage ground for left channel
7	PGNDNL	POWER	Power stage ground for left channel
8	OUTNL	OUT	Negative PWM output for left channel
9	PVCCNL	POWER	Power supply for negative branch in left channel
10	SYNCLK	IN/OUT	Clock in/out for external oscillator
11	ROSC	OUT	Master oscillator frequency setting pin
12	SGND	POWER	Signal ground
13	SVCC	POWER	Signal power supply
14	GAIN0	IN	Gain setting input 1
15	GAIN1	IN	Gain setting input 2
16	PVCCNR	POWER	Power supply for negative branch in right channel
17	OUTNR	OUT	Negative PWM output for right channel
18	PGNDNR	POWER	Power stage ground for right channel
19	PGNDPR	POWER	Power stage ground for right channel
20	OUTPR	OUT	Positive PWM output for right channel
21	PVCCPR	POWER	Power supply for positive branch in right channel
22	SVR	OUTPUT	Supply voltage rejection
23	INPR	IN	Positive differential input of right channel
24	INNR	IN	Negative differential input of right channel

3 Applications circuit

Figure 3. Typical application circuit



Component	Filter Conf.	Filterless Conf.	Filterless Conf. with EMI Optimizatio
C12, C16	330pF	No Component	No Component
R2, R3	20ohm	No Component	No Component
L1, L2, L3, L4	15uF	0ohm	Ferrit bead
C13, C19	470nF	No Component	No Component
C14, C15, C17, C18	220nF	No Component	1nF

4 Electrical specifications

4.1 Absolute maximum ratings

Table 3. Absolute maximum rating

Symbol	Parameter	Negative value	Positive value	Unit
V_{CC}	DC supply on pins PVCCPL, PVCCPR, PVCCNL, PVCCNR, SVCC	-0.3	6	V
$V_{CC\_STANDBY}$	Standby DC supply on pins PVCCPL, PVCCPR, PVCCNL, PVCCNR, SVCC	-0.3	7	V
Vi	Input on pins STANDBY, INNL, INPL, INNR, INPR, GAIN0, GAIN1	-0.3	6	V
Top	Operating temperature	0	70	°C
Tstg, Tj	Storage and junction temperature	-40	150	°C

4.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Min	Typ	Max	Unit
Rth j-case	Thermal resistance junction to case	-	2	3	°C/W
Rth j-amb	Thermal resistance junction to ambient (on recommended PCB) (1)	-	37	-	°C/W

1. FR4 with via holes, copper area 9 cm² as explained in *Chapter 8 on page 28*.

4.3 Electrical characteristics

Refer to *Figure 3: Typical application circuit*, V_{CC} = 5 V, R_L (load) = 4 Ω, R1 = 39 kΩ, C4 = 100 nF, f = 1 kHz, G_V = 18 dB, Tamb = 25 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Supply range	-	3.0	-	5.5	V
Iq	Total quiescent current	No filter, no load	-	7	-	mA
Vos	Output offset voltage	Vi = 0, Gv = 6 dB, no load	-20	-	20	mV
Po	Output power (filterless)	THD = 10%	-	3.0	-	W
		THD = 1%	-	2.4	-	W
Po	Output power (with filter)	THD = 10%	-	2.8	-	W
		THD = 1%	-	2.2	-	W

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Pd	Dissipated power	Po = 2.8 W + 2.8 W, THD = 10%		-	1.1	-	W
η	Efficiency	Po = 2.8 W + 2.8 W, R_L = 4 Ω		-	83	-	%
THD	Total harmonic distortion	R_L = 4 Ω, Po = 0.5 W		-	0.05	-	%
Tj	Thermal shut-down junction temperature	-		-	150	-	°C
G_V	Closed loop gain	GAIN0 = low	GAIN1 = low	-	6.0	-	dB
			GAIN1 = high	-	12.0	-	
		GAIN0 = high	GAIN1 = low	-	15.6	-	
			GAIN1 = high	-	18.0	-	
GV	Gain matching	-		-1	-	1	dB
CT	Crosstalk	f = 1 kHz		-	60	-	dB
eN	Total output noise	A curve, Gv = 18 dB		-	50	-	µV
		f = 22 Hz to 22 kHz, Gv = 18 dB		-	60	-	µV
Ri	Input resistance	Differential Input		-	60	-	kΩ
SVRR	Supply voltage rejection ratio	f_r = 100 Hz, Vr = 0.5 V, C_{SVR} = 1 µF		-	55	-	dB
V_{OVP}	Overvoltage protection threshold	-		-	5.8	-	V
t_r, t_f	Rising and falling time	-		-	10	-	ns
R_{DSON}	Power transistor on resistance	High side		-	0.44	-	Ω
		Low side		-	0.36	-	
f_{SW}	Switching frequency	Internal oscillator		-	315	-	kHz
f_{SWR}	Output switching frequency range	With internal oscillator (1)		250	-	400	kHz
		With external oscillator (2)		250	-	400	kHz
$I_{qSTANDBY}$	Quiescent current in standby	-		-	1	-	µA
Function mode	Standby and play	STANDBY = high		Play			-
		STANDBY = low		Standby			
Digital inputs	Digital input thresholds	High		0.7 * V_{CC}	-	-	V
		Low		-	-	0.3 * V_{CC}	V

1. $f_{SW} = 10^6 / (R_{OSC} * 64 + 840)$
   $f_{SYNC} = 2 * f_{SW}$ with R1 = 39 kΩ and f_{SW} in kHz
2. $f_{SW} = f_{SYNC} / 2$ with the frequency of external oscillator

5 Applications information

5.1 Mode selection

Pin STANDBY selects the operating mode, namely standby or play.

- In standby mode, all the circuits are turned off and there is very low leakage current.
- In play mode, the amplifiers are powered up.

During the turn on/off sequence, there are four operational states: standby, pre-charge, mute and play. The pre-charge and mute states are two internal transient states to set up the normal operating condition and to reduce the speaker pop noise.

Table 6. Mode selection

Logic level on pin STANDBY	Mode
0	Standby
1	Play

Note: An internal pull-down resistor on pin STANDBY ensures that the default mode is standby.

5.2 Gain setting

The close loop gain is set by pins GAIN0 and GAIN1 as shown below in *Table 7*. The gain setting is implemented by changing the feedback resistors of the amplifiers.

Table 7. Gain selection

Logic level on pin GAIN0	Logic level on pin GAIN1	Gv (nominal)
0	0	6.0 dB
0	1	12.0 dB
1	0	15.6 dB
1	1	18.0 dB

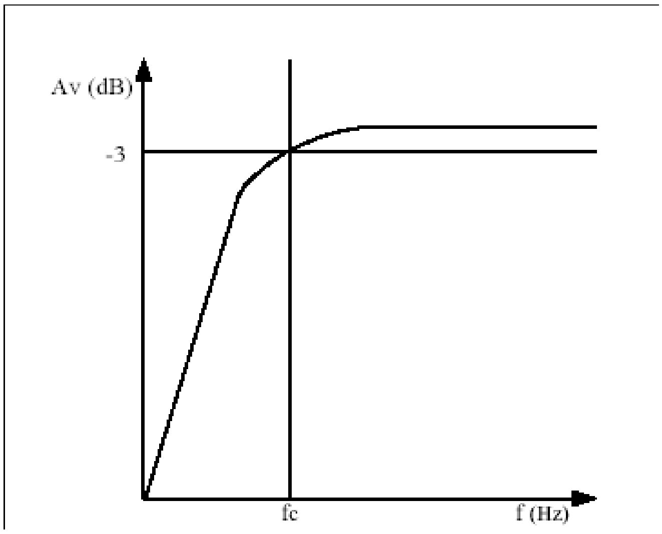
Note: Internal pull-down resistors on pins GAIN0 and GAIN1 ensure that the default gain is 6 dB.

5.3 Input resistance and capacitance

The input impedance is set by an internal resistor, Ri, of value 60 kΩ. An input coupling capacitor (Ci) is required on each input line. These two components together form a high-pass filter whose cutoff frequency is:

$f_C = 1 / (2 * \pi * Ri * Ci)$

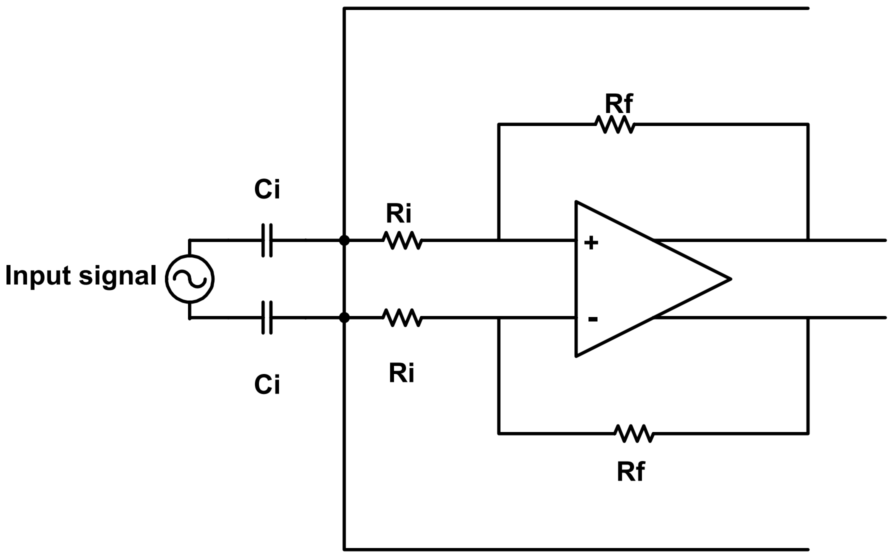
Figure 4. Input high-pass RC filter



The value of Ci is chosen depending on the application and the speaker system. For a cut-off frequency less than 20 Hz, the input capacitors could be 470 nF each.

If a polarized capacitor is used, it is important to connect the positive side of the capacitor to the terminal with higher DC voltage. The DC voltage on the input pins is V_{CC} / 2.

Figure 5. Device input structure

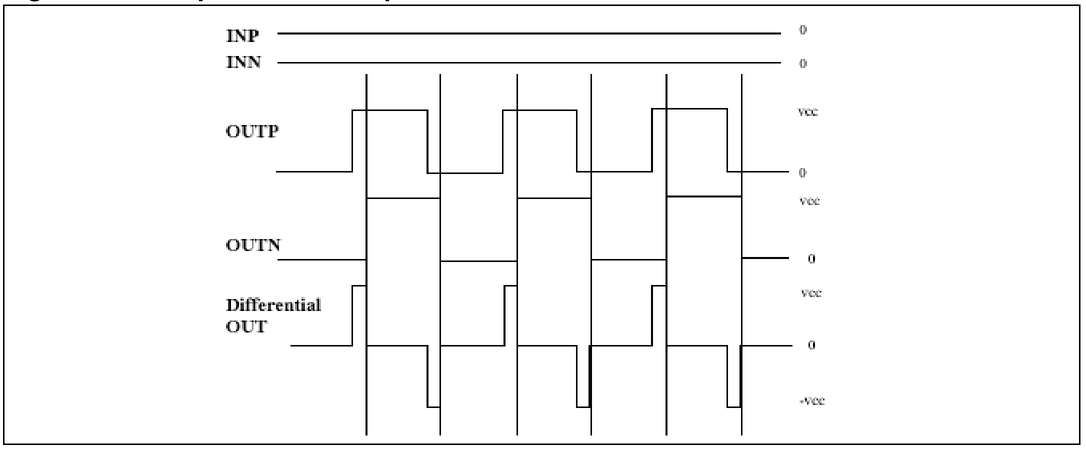


5.4 Filterless modulation

The modulation scheme of BTL is called unipolar PWM output. The differential output voltage changes between zero and $+V_{CC}$ or between zero and $-V_{CC}$, as opposed to the traditional bipolar PWM output between $+V_{CC}$ and $-V_{CC}$. The other advantage of this scheme effectively doubles the switching frequency of the differential output waveform. Signals on OUTP and OUTN are in the same phase when the input is zero, thus the current is greatly reduced and the loss in the load is small. A tiny delay between OUTP and OUTN is introduced to avoid high transient currents which could occur if both outputs switch simultaneously.

TDA7493 can be used without a filter between the PWM output and the speaker since the switching frequency of the output is beyond the audible range. The audio signal can be recovered by the inherent inductance of the speaker and natural filter of the human ear.

Figure 6. Unipolar PWM output



The filterless configuration is usable in applications where the speaker connections to the amplifier are shorter than 50 cm. In comparison to the low-pass Butterworth filter configuration, the filterless configuration gives rise to higher EMI. This can be reduced, if necessary, by inserting a ferrite bead filters close to the device.

Use a ferrite which exhibits high impedance at around 1 MHz and negligible impedance in the audio band.

It is recommended to use an EMI filter if the speaker cable is longer than 50 cm.

Figure 7. Schematic for the filterless configuration

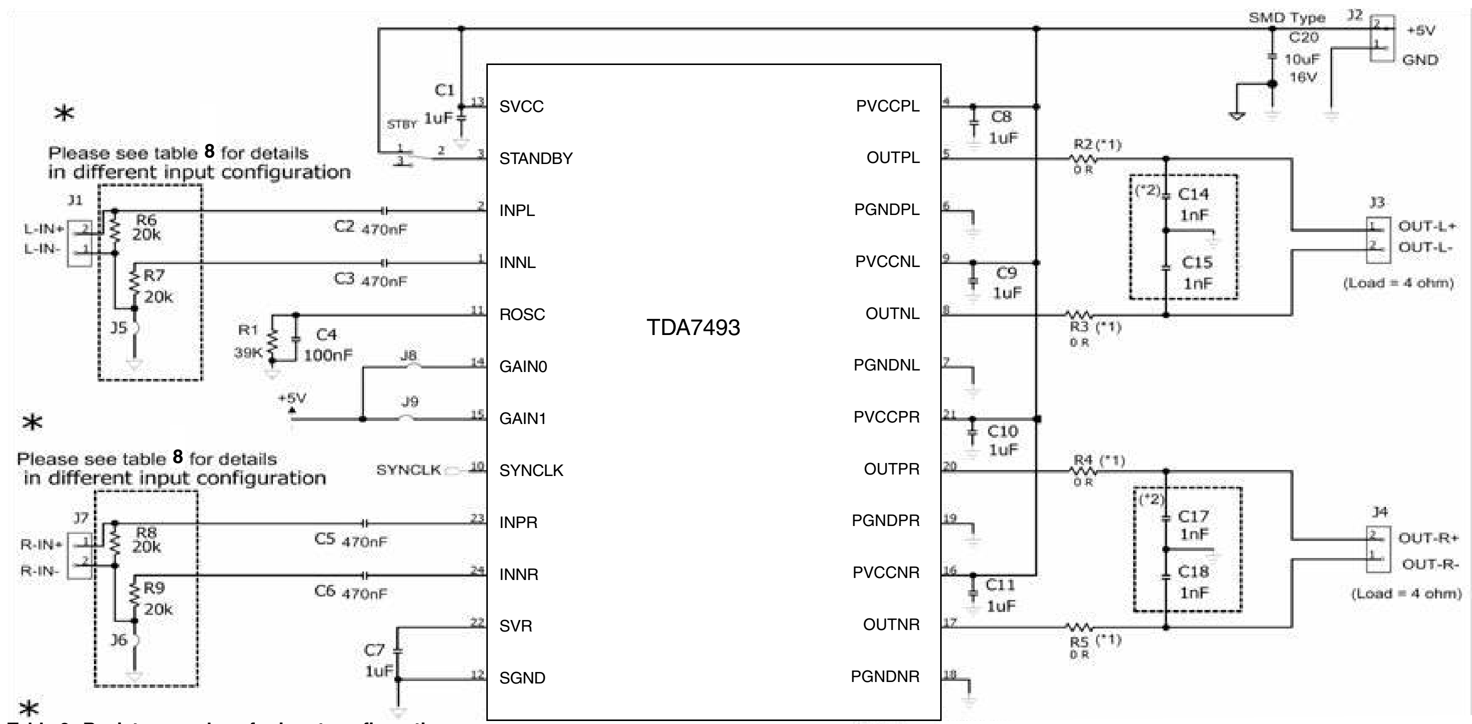


Table 8. Resistance values for input configuration

	R6	R7	J5	R8	R9	J6
Differential-end Input	open	0ohm	open	open	0ohm	open
Single-end Input	20K	20K	0ohm	20K	20K	0ohm

(*1) R2, R3, R4 and R5 are 0-Ω resistors which can be replaced by ferrite beads if EMI optimization is required

(*2) C14, C15, C17, and C18 are 1-nF capacitors which are needed when ferrite beads are used for EMI optimization

TDA7493 amplifier (filterless)

5.5 Internal clock and external clock

The clock of the class-D amplifier can be generated internally or it can be synchronous with the external clock. If two or more class-D amplifiers are used in the same system, it is better to have all devices working at the same frequency. This is realized by using one TDA7493 as clock master and the others as slaves. All SYNCLK pins are connected together as shown in *Figure 8*.

In master mode or with a single TDA7493, the output switching frequency is controlled by the resistor connected to pin ROSC. The switching frequency is:

$$f_{SW} = 10^6 / (R_{OSC} * 64 + 840)$$

where R_{OSC} is in kΩ and f_{SW} is in kHz.

In this configuration pin SYNCLK is an output whose frequency is also determined by R_{OSC}:

$$f_{SYNCLK} = 10^6 / (R_{OSC} * 32 + 420) = 2 * f_{SW}$$

Note: R_{OSC} should be lower than 60 kΩ in master mode to avoid operating in error mode.

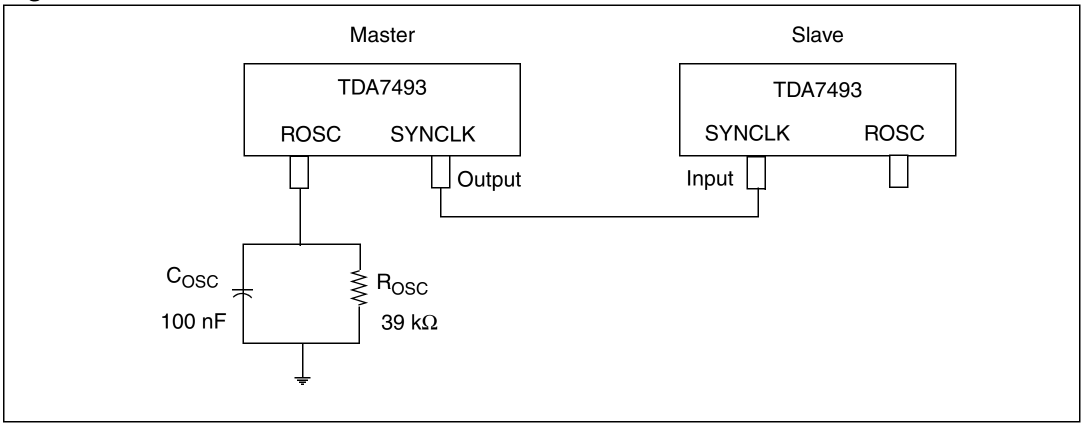
In slave mode, pin ROSC can be floating to force pin SYNCLK as input in order to accept the master clock. The switching frequency in this mode is:

$$f_{SW} = f_{SYNCLK} / 2$$

Table 9. Master and slave mode

Mode	Pin ROSC	Pin SYNCLK
Master	R_{OSC} < 60 kΩ	Output
Slave	Floating	Input

Figure 8. Master and slave modes



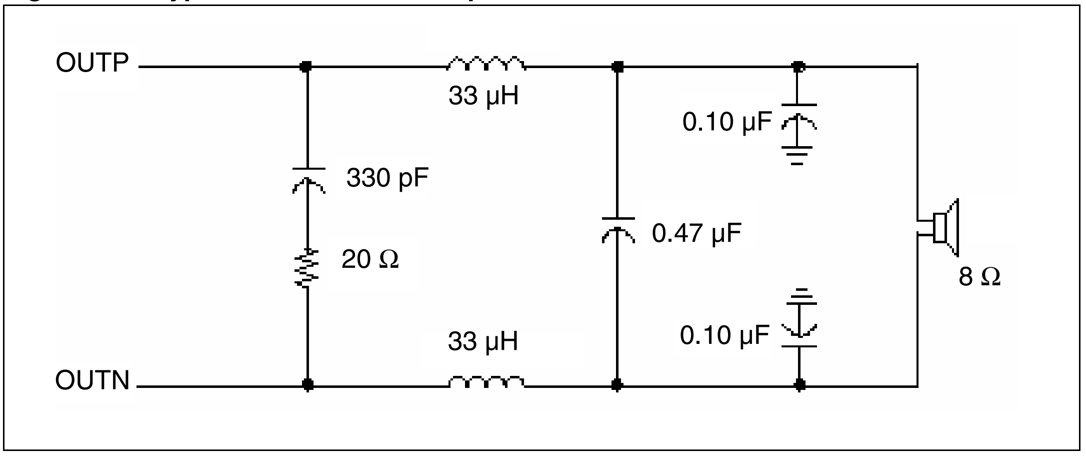
5.6 Output low-pass filter

To avoid EMI problems, a low-pass filter can be inserted before the speaker. The cut-off frequency of the filter should be higher than 22 kHz and much lower than the switching frequency.

The component values of the filter vary according to the speaker impedance.

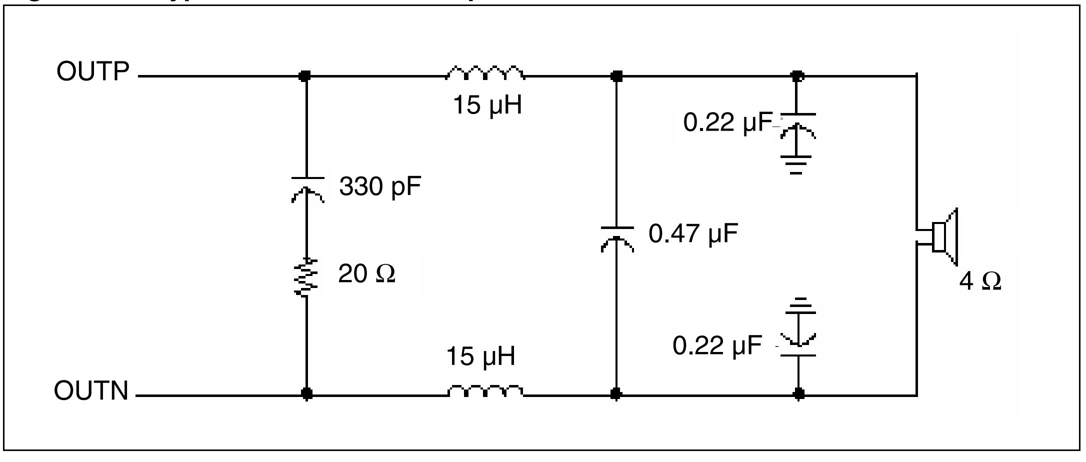
A typical LC output filter for a speaker impedance of 8 Ω and with a cut-off frequency of 27 kHz is shown in *Figure 9*.

Figure 9. Typical LC filter for 8 Ω speaker



A similar filter for a speaker impedance of 4 Ω and also with a cut-off frequency of 27 kHz is shown in *Figure 10*:

Figure 10. Typical LC filter for 4 Ω speaker



5.7 Protection function

The TDA7493 has four types of protection: overvoltage (OV), undervoltage (UV), thermal (OT) and short circuit (SC):

- overvoltage protection (OVP) for the supply $V_{CC} > 6$ V
- undervoltage protection (UVP) for the supply $V_{CC} < 3$ V
- thermal protection (OTP) for the junction temperature Tj > 155 °C
- short-circuit protection (SCP) across the load (tested at $V_{CC} = 5.0$ V).

When any of the above protection becomes active, the output goes to a high-impedance state. The device remains in this state until the condition is cleared or rectified, when the circuit restarts again.

5.8 Differential input

The TDA7493 can be used with either differential or single-ended inputs. In either case, the device must be AC coupled to the audio source.

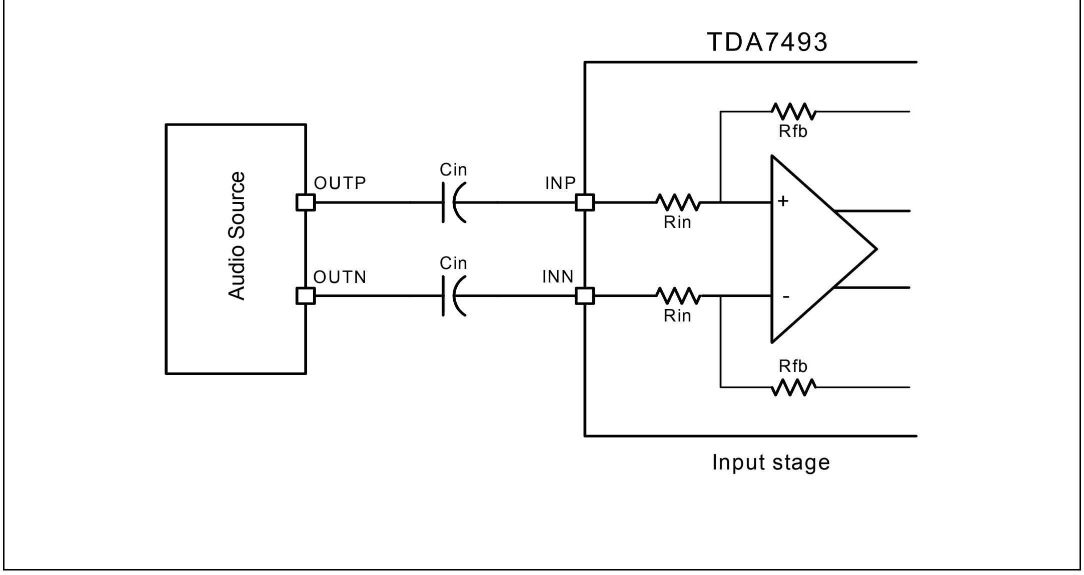
To use the device with a differential source, connect the positive lead from the audio source to the INP input and the negative lead to the INN input as shown in *Figure 11*. The differential input stage of the amplifier minimizes the common mode noise effectively.

In the differential input application:

- input impedance is given by 2 * Rin,
- cut-off frequency of the input filter is given by
  $f_c = 1 / (2 * \pi * Cin / 2 * 2 * Rin) = 1 / (2 * \pi * Cin * Rin)$.

Typically, Rin = 30 kΩ and Cin > 330 nF to get a cut-off frequency less than 20 Hz.

Figure 11. Differential input application

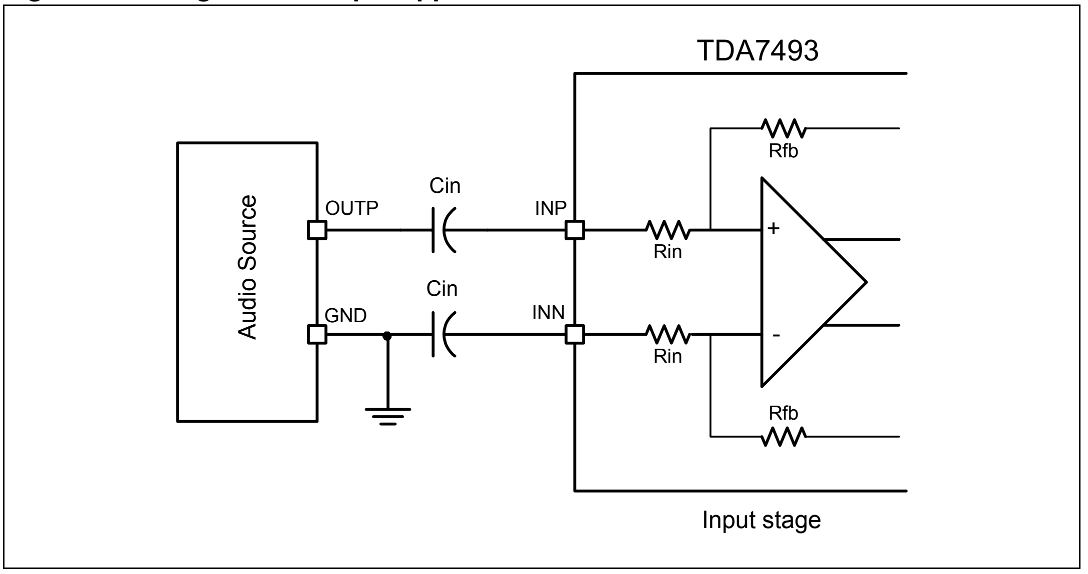


5.8.1 Single-ended input application

To use the device with a single-ended source, one input is AC connected to ground (via a capacitor) and the other input is connected to the audio source. This is designed as a fully differential input. The input scheme is shown in *Figure 12*.

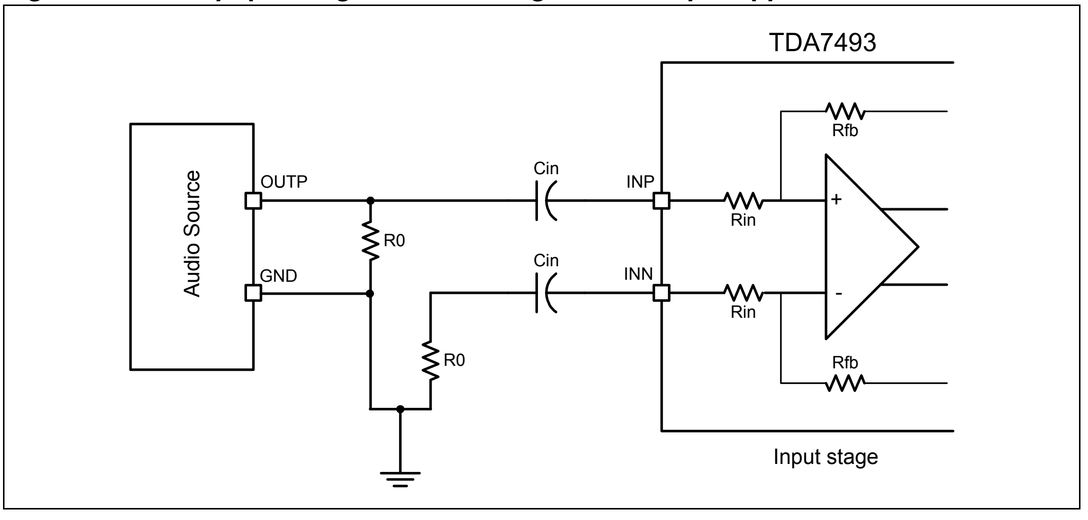
However, to avoid the start-up pop noise, it is important to equalize, as much as possible, the charging currents in the positive and negative inputs. Any imbalance in these charging currents will be amplified and result in the familiar turn-on pop.

Figure 12. Single-ended input application



Since the input charging currents in the circuit of *Figure 12* can be different it is necessary to add two resistors, R0, as shown in the circuit of *Figure 13*. In this way the currents in the two branches of the differential input are better balanced and this can lead to the elimination of the turn-on pop noise.

Figure 13. Anti-pop configuration for single-ended input application



The disadvantages of the anti-pop configuration are given below:

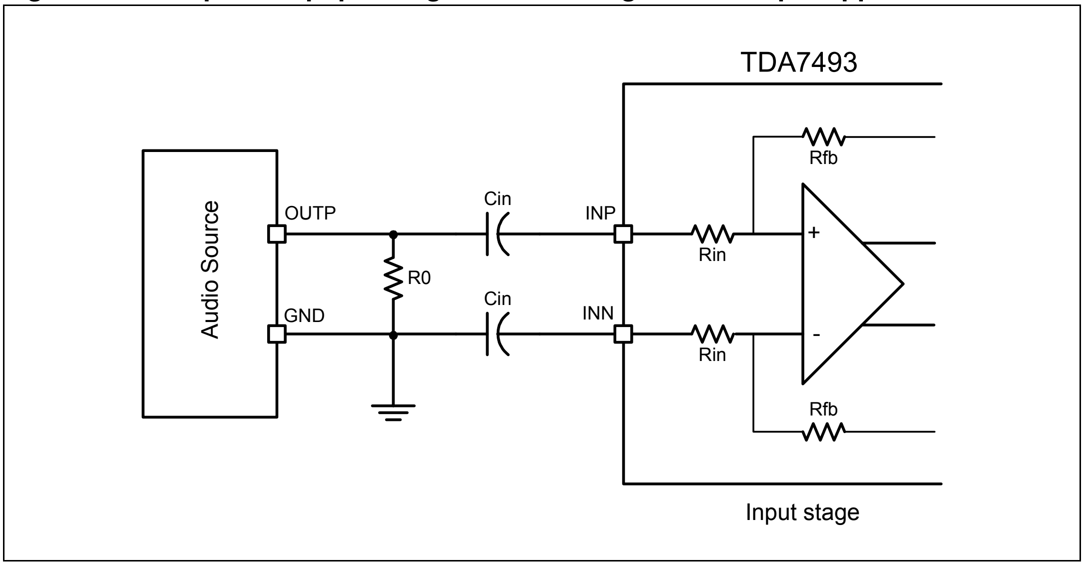
- The input impedance or the load of audio source is no longer 2 * Rin as in the case of differential input configuration but R0. It means the load effect should be considered during the application design. At this point, bigger R0 is better because of the lower load effect.
- The input signal is also equivalent to
  $V_{in\_actual} = V_{in} * 2 * Rin * (Rin + Rfb + R0) / (2 * Rin * (Rin + Rfb + R0) + Rfb * R0)$, not the original V_{in} which means the actual gain is reduced.

  When Rin = 30 kΩ, Rfb = 30 kΩ and R0 = 20 kΩ, the gain is reduced by 1 dB.

  When Rin = 30 kΩ, Rfb = 120 kΩ and R0 = 20 kΩ, the gain is reduced by 1.84 dB. In this case, smaller R0 is better.

If the pop noise is not critical, the anti-pop configuration can be simplified as shown in *Figure 14*. The suggested value of the resistor R0 is 20 kΩ.

Figure 14. Simple anti-pop configuration for single-ended input application



6 Electrical characterization curves

6.1 For the configuration with LC filter

- Test setup as given in *Figure 3 on page 8*
- Test conditions V_{CC} = 5 V, C20 = 10 µF, R_L = 4 Ω, LC filter 15 µH, 470 nF

Figure 15. THD vs output power at 1 kHz

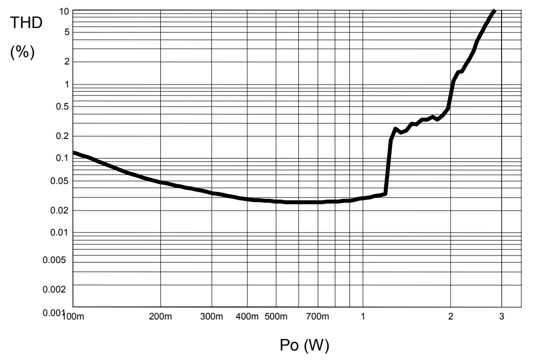


Figure 16. THD vs output power at 100 Hz

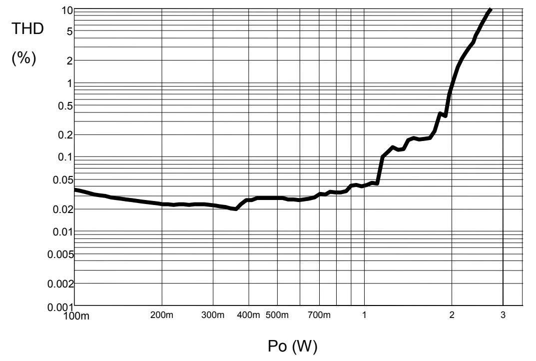


Figure 17. THD vs frequency at 100 mW

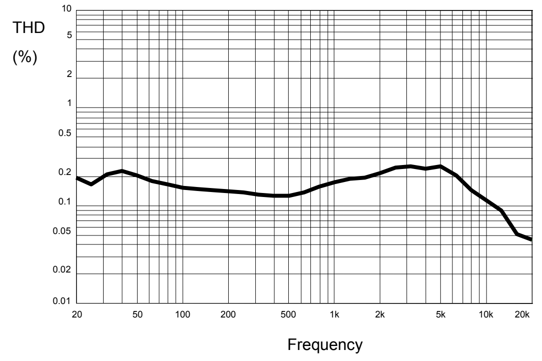


Figure 18. THD vs frequency at 1 W

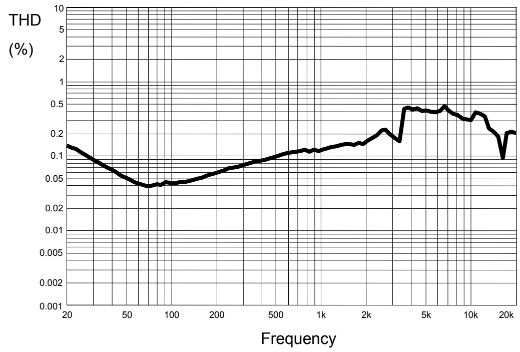


Figure 19. Output frequency response at 1 W

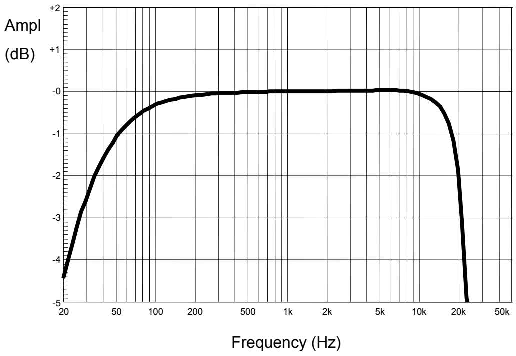


Figure 20. Crosstalk vs frequency at 1 W

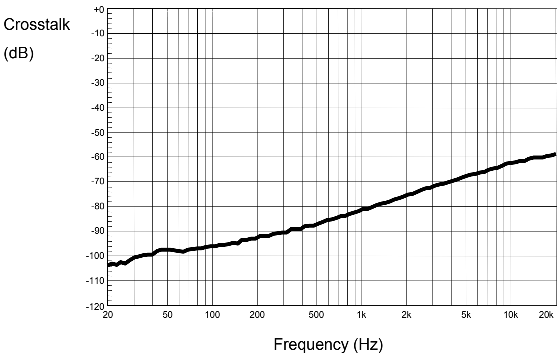


Figure 21. FFT (0 dB)

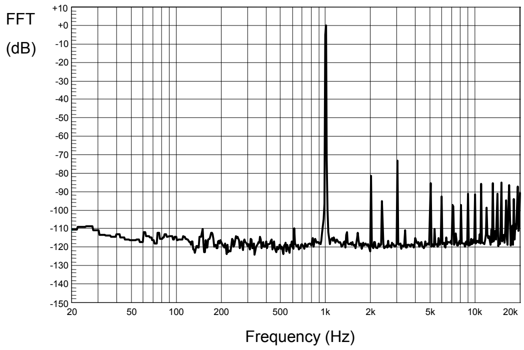
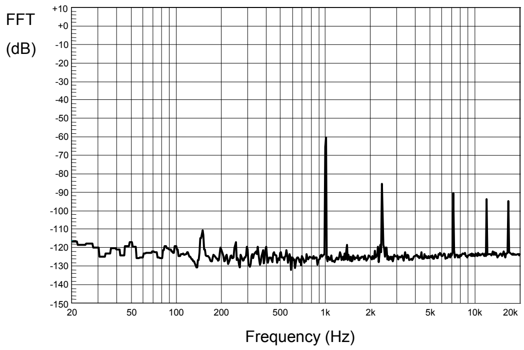


Figure 22. FFT (-60 dB)



6.2 For the configuration without filter

- Test setup as given in *Figure 7 on page 14*
- Test conditions V_{CC} = 5 V, C20 = 10 μF, R_L = 4 Ω + 270 μH, no LC filter

Figure 23. THD vs output power at 1 kHz

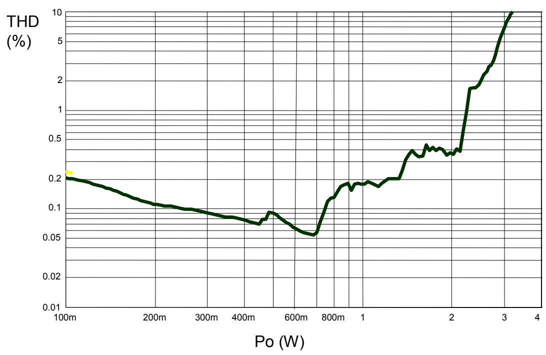


Figure 24. THD vs output power at 100 Hz

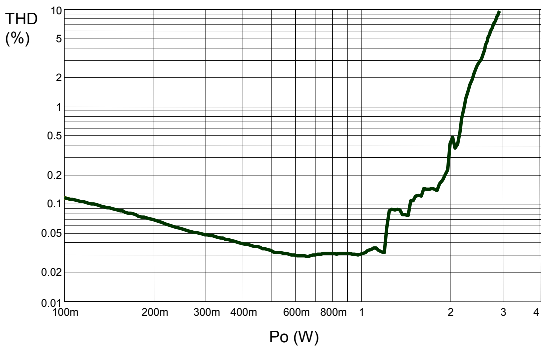


Figure 25. THD vs frequency at 100 mW

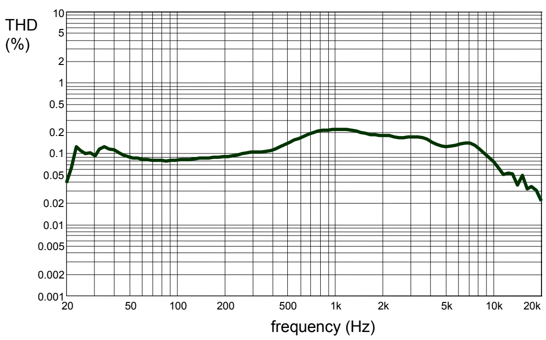


Figure 26. THD vs frequency at 1 W

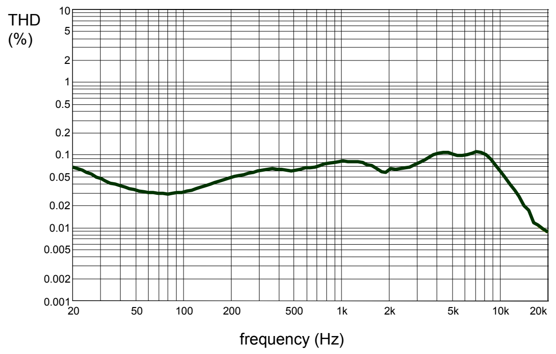


Figure 27. Frequency response at 1 W

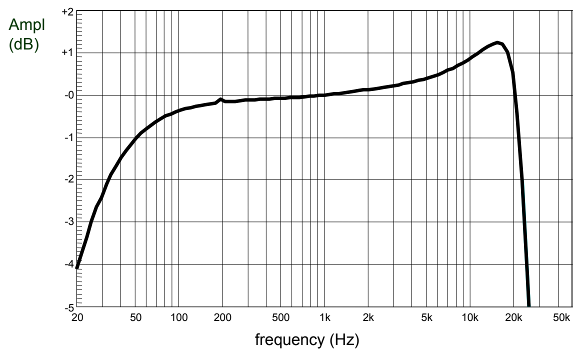


Figure 28. Crosstalk vs frequency at 1 W

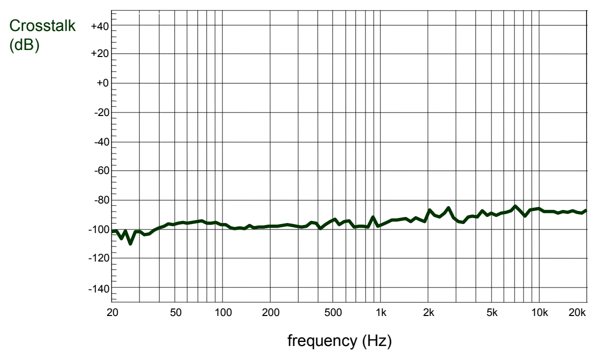


Figure 29. FFT (0 dB)

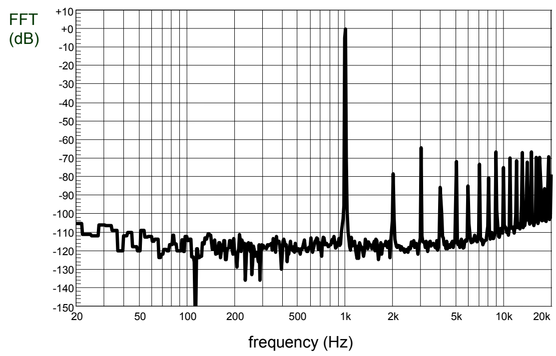


Figure 30. FFT (-60 dB)