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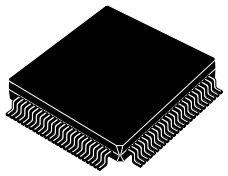
TDA7500A

DIGITAL AM/FM SIGNAL PROCESSOR

- FULL SOFTWARE FLEXIBILITY WITH TWO 24X24 BIT DSP CORES
- SOFTWARE AM/FM, AUDIO AND SOUND-PROCESSING
- HARDWARE RDS FILTER, DEMODULATOR & DECODER
- INTEGRATED CODEC (4ADCs, 6DACs)
- IIC AND SPI CONTROL INTERFACES
- SPI DEDICATED TO DISPLAY MICRO
- 6 CHANNEL SERIAL AUDIO INTERFACE (SAI)
- SPDIF RECEIVER WITH SAMPLE RATE CONVERTER
- EXTERNAL MEMORY INTERFACE (EMI)
- DOUBLE DEBUG INTERFACE
- ON-CHIP PLL
- 5V-TOLERANT 3V I/O INTERFACE
- 12x2 MULTIFUNCTION GENERAL PURPOSE I/O PORTS

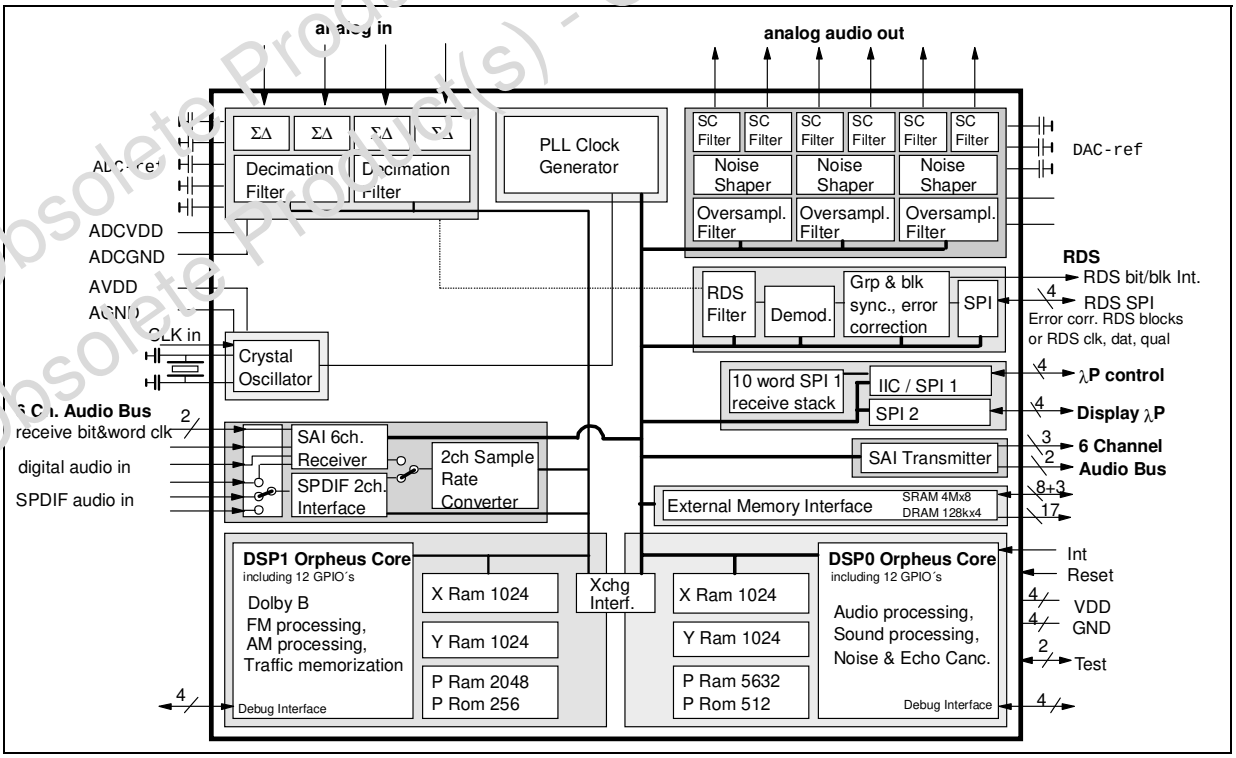


TQFP100 (with slug down)
ORDERING NUMBER: TDA7500A

DESCRIPTION

The TDA7500A is an integrated circuit implementing a fully digital, integrated and advanced solution to perform the signal processing in front of the power amplifier and behind the AM/FM tuner or any other audio source. The chip integrates two 45 MIPs DSP cores: one for stereo decoding, noise blanking, weak signal processing and multipath detection and one for sound processing, Dolby B, echo and noise cancelling for the telephone.

BLOCK DIAGRAM



DESCRIPTION (continued)

An I^2C/SPI interface is implemented for control and communication with the main micro. A separate SPI is available to interface the display micro.The DSP cores are integrated with their associated data and program memories. The peripherals and interfaces I^2C, SPI, Serial Audio Interface (SAI), PLL Oscillator, External Memory Interface, (EMI), General Purpose I/O register (Port A) and the D/A registers are connected to and controlled by DSP0, whereas the A/D registers, the SPDIF and the General Purpose I/O register (Port B) are connected to and controlled by DSP1. An hardware RDS filter , demodulator and decoder block is also embedded. No support is needed from the DSPs but at initialisation so that RDS can work in background and in parallel with other DSP processing. Separated Debug and Test Interfaces are connected to both DSP cores.

The TDA7500A is supposed to be used in kit with the TDA7501 or any other device of the same family. Thanks to the serial audio interface also digital sources can be processed and a direct output to a digital bus is also available.

The flexibility allowed by the wide memory space and by the two powerfull DSP cores make the TDA7500A usable for different applications. In example, inside the main radio as an audio co-processor or to perform the signal processing and equalisation associated to a digital power amplifier.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD} V_{CC}	Power supplies Digital Analog	-0.5 to +4.6 -0.5 to +4.6	V V
V_{aio}	Analog Input and Output Voltage	-0.5 to (V_{CC}+0.5)	V
V_{dio}	Digital Input and Output Voltage	-0.5 to (V_{DD}+0.5)	V
V_{di5}	Digital Input Voltage (5V tolerant)	-0.5 to 6.5	V
T_j	Operating Junction Temperature Range	-40 to 125	°C
T_{stg}	Storage Temperature	-55 to 150	°C

Warning: Operation at or beyond these limit may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient (1)	45	°C/W
	Thermal resistance junction to ambient (2)	20	°C/W
$R_{th\ j\text{-}case}$	Thermal junction to case (3)	5	°C/W

Note: 1. In still air
2. On 4 layers board with soldered slug
3. Measured on top side of the package

PIN DESCRIPTION

N°	Name	Type	Description
1	GND1		Ground pin dedicated to the digital circuitry.
2	VDD1		Supply pin dedicated to the digital circuitry.
3	TESTEN	I	Test Enable (Input). When low, puts the chip into test mode and muxes the XTI clock to all flip-flops. When TEST_SE is also active, the scan chain shifting is enabled. To be connected to Vdd in operating mode.
4	TESTSE	I	SCAN Enable (Input). When high with TESTEN also active, controls the shifting of the internal scan chains. When active with TESTEN not active, sets all tri-state outputs into hi-impedance mode. To be connected to GND in operating mode.
5	NRESET	I	System Reset (Input). A low level applied to NRESET input initializes the IC.
6	SCKM/DSP0_GPIO0	I/O	I^2C Serial Clock Line (Input/Output)/SPI Bit Clock (Input)/ General Purpose I/O (Input/Output). Clock line for I^2C bus. If SPI interface is enabled, behaves as SPI bit clock. Optionally it can be used as general purpose I/O controlled by DSP0.
7	MISOM/DSP0_GPIO1	I/O	I^2C Serial Data Line (Input/Output)/SPI Master Input Slave Output Serial Data (Input/Output)/General Purpose I/O (Input/ Output). Data line for I^2C bus. If SPI is enabled, behaves as Serial Data Input when in SPI Master Mode and Serial Data Output when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
8	MOSIM/DSP0_GPIO2	I/O	SPI Master Output Slave Input Serial Data (Input/Output)/ General Purpose I/O (Input/Output). Serial Data Output when in SPI Master Mode and Serial Data Input when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
9	SSM/DSP0_GPIO3	I	SPI Slave Select (Input)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Slave Select line for SPI bus. Optionally it can be used as general purpose I/O controlled by DSP0.
10	SCKD/DSP0_GPIO4	I	SPI Bit Clock (Input)/General Purpose I/O (Input/Output). SPI bit clock. Optionally it can be used as general purpose I/O controlled by DSP0.
11	MISOD/DSP0_GPIO5	I/O	SPI Master Input Slave Output Serial Data (Input/Output)/ General Purpose I/O (Input/Output). Behaves as Serial Data Input when in SPI Master Mode and Serial Data Output when in SPI Slave Mode. Optionally it can be used as general purpose I/ O controlled by DSP0.
12	MISOD/DSP0_GPIO6	I/O	SPI Master Output Slave Input Serial Data (Input/Output)/ General Purpose I/O (Input/Output). Serial Data Output when in SPI Master Mode and Serial Data Input when in SPI Slave Mode. Optionally it can be used as general purpose I/O controlled by DSP0.
13	SSD/DSP0_GPIO7	I	SPI Slave Select (Input)/General Purpose I/O (Input/Output). Behaves as Slave Select line for SPI bus. Optionally it can be used as general purpose I/O controlled by DSP0.

PIN DESCRIPTION (continued)

N°	Name	Type	Description
14	CLKIN	I	Clock Input pin (Input). Clock from external digital audio source to synchronize the internal PLL.
15	AVDD		Supply pin dedicated to the PLL.
16	XTI	I	Crystal Oscillator Input (Input). External Clock Input or crystal Oscillator input.
17	XTO	O	Crystal Oscillator Output (Output). Crystal Oscillator output drive.
18	AGND		Ground pin dedicated to the PLL.
19	RDSINT/DSP1_GPIO4	O	RDS bit/block interrupt (Output)/General Purpose I/O (Input/Output). Provides an interrupt to the main micro. Optionally it can be used as general purpose I/O controlled by DSP1.
20	RDSARI_SCK/DSP1_GPIO3	O	SPI Bit Clock (Input)/ARI indicator (Output)/General Purpose I/O (Input/Output). If SPI interface is enabled, behaves as SPI bit clock. Optionally it provides the ARI indication bit. Optionally it can be used as general purpose I/O controlled by DSP1.
21	RDSQAL_SO/DSP1_GPIO2	O	SPI Slave Output Serial Data (Output)/RDS Bit Quality (Output)/ General Purpose I/O (Input/Output). If SPI is enabled, behaves as Serial Data Output. Optionally it provides the RDS serial data quality information. Optionally it can be used as general purpose I/O controlled by DSP1.
22	RDSDAT_SI/DSP1_GPIO1	I	SPI Slave Input Serial Data (Input)/RDS Bit Data (Output)/ General Purpose I/O (Input/Output). If SPI is enabled, behaves as Serial Data Input. Optionally it provides the RDS serial data stream. Optionally it can be used as general purpose I/O controlled by DSP1.
23	RDSCLK_SS/DSP1_GPIO0	I	SPI Chip Select (Input)/RDS Bit Clock (Output)/General Purpose I/O (Input/Output). If SPI is enabled, behaves as Chip Select line for SPI bus. Optionally it provides the 1187.5Hz RDS Bit Clock. Optionally it can be used as general purpose I/O controlled by DSP1.
24	INT	I	External interrupt line (Input). When this line is asserted low, the DSP may be interrupted. Acts as IRQA line of DSP0 core.
25	CGND1		Ground pin dedicated to the digital circuitry.
26	CVDD1		Supply pin dedicated to the digital circuitry.
27	SCRCCD	I	SPDIF Input 1 (Input). Stereo SPDIF input to connect a digital audio source like a CD.
28	SCRMD	I	SPDIF Input 2 (Input). Stereo SPDIF input to connect a digital audio source like a MD.
29	DSRA<7>	I/O	DSP SRAM Data Lines<7> (Input/Output). When in SRAM Mode this pin act as the EMI data line 7.
30	DSRA<6>	I/O	DSP SRAM Data Lines<6> (Input/Output). When in SRAM Mode this pin act as the EMI data line 6.

PIN DESCRIPTION (continued)

N°	Name	Type	Description
31	DSRA<5>	I/O	DSP SRAM Data Lines<5> (Input/Output). When in SRAM Mode this pin act as the EMI data line 5.
32	DSRA<4>	I/O	DSP SRAM Data Lines<4> (Input/Output). When in SRAM Mode this pin act as the EMI data line 4.
33	DSRA<3>	I/O	DSP SRAM Data Lines<3> (Input/Output)/DSP DRAM Data Line<3>(Input/Output). This pin act as the EMI data line 3 in both SRAM Mode and DRAM Mode.
34	DSRA<2>	I/O	DSP SRAM Data Lines<2> (Input/Output)/DSP DRAM Data Line<2>(Input/Output). This pin act as the EMI data line 2 in both SRAM Mode and DRAM Mode.
35	DSRA<1>	I/O	DSP SRAM Data Lines<1> (Input/Output)/DSP DRAM Data Line<1>(Input/Output). This pin act as the EMI data line 1 in both SRAM Mode and DRAM Mode.
36	DSRA<0>	I/O	DSP SRAM Data Lines<0> (Input/Output)/DSP DRAM Data Line<0>(Input/Output). This pin act as the EMI data line 0 in both SRAM Mode and DRAM Mode.
37	SRA<0>	O	DSP SRAM Address Line<0> (Output)/DSP DRAM Address Line<0> (Output). This pin acts as the EMI address line 0 in both SRAM Mode and DRAM Mode
38	SRA<1>	O	DSP SRAM Address Line<1> (Output)/DSP DRAM Address Line<1> (Output). This pin acts as the EMI address line 1 in both SRAM Mode and DRAM Mode
39	SRA<2>	O	DSP SRAM Address Line<2> (Output)/DSP DRAM Address Line<2> (Output). This pin acts as the EMI address line 2 in both SRAM Mode and DRAM Mode
40	SRA<3>	O	DSP SRAM Address Line<3> (Output)/DSP DRAM Address Line<3> (Output). This pin acts as the EMI address line 3 in both SRAM Mode and DRAM Mode
41	SRA<4>	O	DSP SRAM Address Line<4> (Output)/DSP DRAM Address Line<4> (Output). This pin acts as the EMI address line 4 in both SRAM Mode and DRAM Mode
42	SRA<5>	O	DSP SRAM Address Line<5> (Output)/DSP DRAM Address Line<5> (Output). This pin acts as the EMI address line 5 in both SRAM Mode and DRAM Mode
43	SRA<6>	O	DSP SRAM Address Line<6> (Output)/DSP DRAM Address Line<6> (Output). This pin acts as the EMI address line 6 in both SRAM Mode and DRAM Mode
44	SRA<7>	O	DSP SRAM Address Line<7> (Output)/DSP DRAM Address Line<7> (Output). This pin acts as the EMI address line 7 in both SRAM Mode and DRAM Mode
45	SRA<8>	O	DSP SRAM Address Line<8> (Output)/DSP DRAM Address Line<8> (Output). This pin acts as the EMI address line 8 in both SRAM Mode and DRAM Mode

PIN DESCRIPTION (continued)

N°	Name	Type	Description
46	SRA<9>	O	DSP SRAM Address Line<9> (Output)/DSP DRAM Address Line<9> (Output). This pin acts as the EMI address line 9 in both SRAM Mode and DRAM Mode
47	SRA<10>	O	DSP SRAM Address Line<10> (Output)/DSP DRAM Address Line<10> (Output). This pin acts as the EMI address line 10 in both SRAM Mode and DRAM Mode
48	SRA<11>	O	DSP SRAM Address Line<11> (Output)/DSP DRAM Address Line<11> (Output). This pin acts as the EMI address line 11 in both SRAM Mode and DRAM Mode
49	SRA<12>	O	DSP SRAM Address Line<12> (Output)/DSP DRAM Address Line<12> (Output). This pin acts as the EMI address line 12 in both SRAM Mode and DRAM Mode
50	CGND2		Ground pin dedicated to the digital circuitry.
51	CVDD2		Supply pin dedicated to the digital circuitry.
52	SRA<13>	O	DSP SRAM Address Line<13> (Output)/DSP DRAM Address Line<13> (Output). This pin act as the EMI address line 13 in both SRAM Mode and DRAM Mode.
53	SRA<14>	O	DSP SRAM Address Line<14> (Output)/DSP DRAM Address Line<14> (Output). This pin act as the EMI address line 14 in both SRAM Mode and DRAM Mode.
54	SRA<15>	O	DSP SRAM Address Line<15> (Output)/DSP DRAM Address Line<15> (Output). This pin act as the EMI address line 15 in both SRAM Mode and DRAM Mode.
55	SRA<16>/DSP0_GPIO3	O	DSP SRAM Address Line<16> (Output)/DSP DRAM Address Line<16> (Output)/General Purpose I/O (Input/Output). This pin acts as the EMI address line 16 in both SRAM Mode and DRAM Mode. Optionally it can be used as general purpose I/O controlled by DSP0. After reset the state of this pin is read by the boot SW to select the boot mode (Refer to HW/SW maual).
56	DWR	O	DSP SRAM Write Enable (Output)/DRAM Write Enable (Output). This pin serves as the write enable for the EMI in both DRAM and SRAM Mode (active low). To be connected to R/W of the RAM.
57	DRD	O	DSP SRAM Read Enable(Output)/DRAM Read Enable (Output). This pin serves as the read enable for the EMI in both DRAM and SRAM Mode (active low). To be connected to R/W of the RAM.
58	CASALE	O	DSP DRAM Column Address Strobe (Output). When in DRAM Mode this pin acts as the column address strobe.
59	SDO<2>/SRA<17>/DSP1_GPIO<8>	O	SAI Outputs (Output)/EMI SRAM Address Line<17> (Output)/ General Purpose I/O (Input/Output). One stereo channel SAI data output in SAI mode. EMI address line 17 in SRAM Mode. Optionally it can be used as a general purpose I/O.

PIN DESCRIPTION (continued)

N°	Name	Type	Description
60	SDO<2>/SRA<18>/DSP1_GPIO<7>	O	SAI Outputs (Output)/EMI SRAM Address Line<18> (Output)/ General Purpose I/O (Input/Output). One stereo channel SAI data output in SAI mode. EMI address line 18 in SRAM Mode. Optionally it can be used as a general purpose I/O.
61	SDO<0>/SRA<19>	O	SAI Output (Output)/EMI SRAM Address Line<19> (Output). One stereo channel SAI data output in SAI mode. EMI address line 19 in SRAM Mode.
62	SDI<2>/SRA<20>/DSP1_GPIO<6>	I	SAI Input (Input)/EMI SRAM Address Line<20> (Output)/ General Purpose I/O (Input/Output). One stereo channel SAI data input in SAI mode. EMI address line 20 in SRAM Mode. Optionally it can be used as a general purpose I/O.
63	SDI<1>/SRA<21>/RAS/DSP1_GPIO<5>	I	SAI Input (Input)/EMI SRAM Address Line<21> (Output)/DRAM Row Address Strobe (Output)/General Purpose I/O (Input/ Output). One stereo channel SAI data input in SAI mode. EMI address line 21 in SRAM Mode. When in DRAM Mode this pin acts as the row address strobe. Optionally it can be used as a general purpose I/O.
64	SDI<0>/SRCCDC	I	SAI Input (Input)/SPDIF Input 3 (Input). One stereo channel SAI data input in SAI mode. Stereo SPDIF input intended to connect a digital audio source like a CD changer in SPDIF mode.
65	SCKT	I/O	SAI transmitter Bit Clock (Input/Output). SAI transmitter bit clock. Master or slave.
66	LRCKT	I/O	SAI transmitter Left-Right Clock (Input/Output). SAI transmitter Left-Right clock. Can be master or slave mode.
67	SCKR	I	SAI receiver Bit Clock (Input). SAI receiver bit clock. Slave only.
68	LRCKR	I	SAI receiver Left-Right Clock (Input/Output). SAI receiver Left-Right clock. Slave only.
69	DBOUT1/DSP1_GPIO10	I/O	Debug Port Serial Output (Input/Output)/ General Purpose I/O (Input/Output). The serial data output for the Debug Port. Optionally it can be used as a general purpose I/O.
70	DBIN1/OS10/DSP1_GPIO11	I/O	Debug Port Serial Input/Chip Status 0 (Input/Output)/ General Purpose I/O (Input/Output). The serial data input for the Debug Port is provided when an input. When an output, together with OS1 provides information about the chip status. Optionally it can be used as a general purpose I/O.
71	DBCK1/OS11/DSP1_GPIO9	I/O	Debug Port Bit Clock/Chip Status 1 (Input/Output)/General Purpose I/O (Input/Output). The serial clock for the Debug Port is provided when an input. When an output, together with OS0 provides information about the chip status. Optionally it can be used as a general purpose I/O.
72	DBRQN1	I	Debug Port Request Input (Input). Means of entering the Debug mode of operation.
73	DBOUT0/DSP0_GPIO10	I/O	Debug Port Serial Output (Input/Output)/ General Purpose I/O (Input/Output). The serial data output for the Debug Port. Optionally it can be used as a general purpose I/O.

PIN DESCRIPTION (continued)

N°	Name	Type	Description
74	DBIN0/OS00/DSP0_GPIO11	I/O	Debug Port Serial Input/Chip Status 0 (Input/Output)/ General Purpose I/O (Input/Output). The serial data input for the Debug Port is provided when an input. When an output, together with OS1 provides information about the chip status. Optionally it can be used as a general purpose I/O.
75	DBCK0/OS01/DSP0_GPIO9	I/O	Debug Port Bit Clock/Chip Status 1 (Input/Output)/General Purpose I/O (Input/Output). The serial clock for the Debug Port is provided when an input. When an output, together with OS0 provides information about the chip status. Optionally it can be used as a general purpose I/O.
76	DBRQN0	I	Debug Port Request Input (Input). Means of entering the Debug mode of operation.
77	VDD2		Supply pin dedicated to the digital circuitry.
78	GND2		Ground pin dedicated to the digital circuitry.
79	ADC<0>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
80	ADC<1>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
81	ADC<2>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
82	ADC<3>	I	Analog Inputs (Input). Single ended analog signal inputs to the ADC.
83	S2DREF	I	To be connected to ADCGND
84	ADCVDDREF	I	Voltage Reference (Input). Analog voltage reference input. Signal is supplied by A354. (typical 3.3V).
85	ADCREF<2>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
86	ADCREF<1>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
87	ADCREF<0>	I	Voltage Reference (Input). External decoupling of the analog references used for the sigma delta modulator.
88	ADCVDD		Analog Supply pin dedicated to the A/D converter.
89	ADCGND		Analog Ground pin dedicated to the A/D converter.
90	DAC<0>	O	Analog Outputs (Output). Analog signal outputs of the DAC
91	DAC<1>	O	Analog Outputs (Output). Analog signal outputs of the DAC
92	DAC<2>	O	Analog Outputs (Output). Analog signal outputs of the DAC
93	DAC<3>	O	Analog Outputs (Output). Analog signal outputs of the DAC
94	DAC<4>	O	Analog Outputs (Output). Analog signal outputs of the DAC
95	DAC<5>	O	Analog Outputs (Output). Analog signal outputs of the DAC

PIN DESCRIPTION (continued)

N°	Name	Type	Description
96	DACREF<2>	I	Voltage Reference (Input). External decoupling of the analog references of the CODEC and voltage biasing.
97	DACREF<1>	I	Voltage Reference (Input). It can be connected to pin 100.
98	DACREF<0>	I	Voltage Reference (Input). External decoupling of the analog references of the CODEC and voltage biasing.
99	DACGND		Analog Ground pin dedicated to the D/A converter.
100	DACVDD		Analog Supply pin dedicated to the D/A converter.

I/O DEFINITION AND STATUS
O: logic low output
X: undefined input/output
Z: high impedance
1: logic input output

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
1	GND1					supply	
2	VDD1					supply	To be connected to VDD
3	TESTEN	X	X	X	X	input	To be connected to GND
4	TESTSE	X	X	X	X	input	Ext. Pulldown
5	NRESET	X	X	X	X	input 5VT	
6	MSPI: SCKM input MSPI: SCKM output I2C: SCL bi-direct DSP0: GPIO0 input DSP0: GPIO0 output	X	X	(1)	(1)	input 5VT output 4mA PP input 5VT/output 4mA OD input 5VT output 4mA OD	(1) undefined input
7	MSPI: MISOM input MSPI: MISOM output I2C: SDA bi-direct DSP0: GPIO1 input DSP0: GPIO1 output	X	0 or 1	X X	X X	input 5VT output 4mA OD input 5VT/output 4mA OD input 5VT output 4mA PP	
8	MSPI: MOSIM input MSPI: MOSIM output DSP0: GPIO2 input DSP0: GPIO2 output	X	X	X	X	input 5VT output 4mA OD input 5VT output 4mA OD	
9	MSPI: SSM input DSP0: GPIO3 input DSP0: GPIO3 output	X	X	X	X	input 5VT input 5VT output 4mA PP	
10	DSPI: SCKD input DSPI: SCKD output DSP0: GPIO4 input DSP0: GPIO4 output	X	X	X	X	input 5VT output 4mA PP input 5VT output 4mA PP	

I/O DEFINITION AND STATUS (continued)

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
11	DSPI: MISOD input DSPI: MISOD output DSP0: GPIO5 input DSP0: GPIO5 output	X	X	X	X	input 5VT output 4mA OD input 5VT output 4mA OD	
12	DSPI: MOSID input DSPI: MOSID output DSP0: GPIO6 input DSP0: GPIO6 output	X	X	X	X	input 5VT output 4mA OD input 5VT output 4mA OD	
13	DSPI: SSD input DSP0 : GPIO7 input DSP0 : GPIO7 output		X	X	X	input 5VT input 5VT output 4mA PP	
14	PLL: CLKIN input	X	X	X	X	input	
15	PLL: AVDD					supply	
16	PLL: XTI input	X	X	X	X	analog input	max. 20 MHz
17	PLL: XTO output	X	X	X	X	analog output	
18	PLL: AGND					supply	
19	RDS: RDSINT output DSP1: GPIO4 input DSP1: GPIO4 output	X	X	X	X	output 4mA PP onput 5VT output 4mA PP	
20	RDS: RDSARI output RDS SPI: SCK input DSP1: GPIO3 input DSP1: GPIO3 output	X	X	X	X	output 4mA PP input 5VT input 5VT output 4mA PP	
21	RDS: RDSQAL output RDS SPI: SO input DSP1: GPIO2 input DSP1: GPIO2 output	X	X	X	X	output 4mA OD output 4mA OD input 5VT output 4mA OD	
22	RDS: RDSDAT output RDS SPI: SI input DSP1: GPIO1 input DSP1: GPIO1 output	X	X	X	X	output 4mA PP input 5VT input 5VT output 4mA PP	
23	RDS: RDSCLK output RDS SPI: SS input DSP1: GPIO0 input DSP1: GPIO0 output	X	X	X	X	output 4mA PP input 5VT input 5VT output 4mA PP	
24	INT input	X	X	X	X	input 5VT	Ext. Pullup
25	CGND1					supply	
26	CVDD1					supply	
27	SCRCCD input	X	X	X	X	input 5VT	
28	SCRCMD input	X	X	X	X	input 5VT	
29	EMI SRAM: Data<7> bi-direct	1	1	1	Z	input/output 2mA PP	

I/O DEFINITION AND STATUS (continued)

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
30	EMI SRAM: Data<6> bi-direct	1	1	1	Z	input/output 2mA PP	
31	EMI SRAM: Data<5> bi-direct	1	1	1	Z	input/output 2mA PP	
32	EMI SRAM: Data<4> bi-direct	1	1	1	Z	input/output 2mA PP	
33	EMI SRAM: Data<3> bi-direct EMI SRAM: Data<3> bi-direct	1	1	1	Z	input/output 2mA PP	
34	EMI SRAM: Data<2> bi-direct EMI SRAM: Data<2> bi-direct	1	1	1	Z	input/output 2mA PP	
35	EMI SRAM: Data<1> bi-direct EMI SRAM: Data<1> bi-direct	1	1	1	Z	input/output 2mA PP	
36	EMI SRAM: Data<0> bi-direct EMI SRAM: Data<0> bi-direct	1	1	1	Z	input/output 2mA PP	
37	EMI SRAM: Add<0> output EMI SRAM: Add<0> output	1	1	1	0/1	output 2mA PP output 2mA PP	
38	EMI SRAM: Add<1> output EMI SRAM: Add<1> output	1	1	1	0/1	output 2mA PP output 2mA PP	
39	EMI SRAM: Add<2> output EMI SRAM: Add<2> output	1	1	1	0/1	output 2mA PP output 2mA PP	
40	EMI SRAM: Add<3> output EMI SRAM: Add<3> output	1	1	1	0/1	output 2mA PP output 2mA PP	
41	EMI SRAM: Add<4> output EMI SRAM: Add<4> output	1	1	1	0/1	output 2mA PP output 2mA PP	
42	EMI SRAM: Add<5> output EMI SRAM: Add<5> output	1	1	1	0/1	output 2mA PP output 2mA PP	
43	EMI SRAM: Add<6> output EMI SRAM: Add<6> output	1	1	1	0/1	output 2mA PP output 2mA PP	
44	EMI SRAM: Add<7> output EMI SRAM: Add<7> output	1	1	1	0/1	output 2mA PP output 2mA PP	
45	EMI SRAM: Add<8> output EMI SRAM: Add<8> output	1	1	1	0/1	output 2mA PP output 2mA PP	
46	EMI SRAM: Add<9> output EMI SRAM: Add<9> output	1	1	1	0/1	output 2mA PP output 2mA PP	
47	EMI SRAM: Add<10> output EMI SRAM: Add<10> output	1	1	1	0/1	output 2mA PP output 2mA PP	
48	EMI SRAM: Add<11> output EMI SRAM: Add<11> output	1	1	1	0/1	output 2mA PP output 2mA PP	
49	EMI SRAM: Add<12> output EMI SRAM: Add<12> output	1	1	1	0/1	output 2mA PP output 2mA PP	
50	CGND2					supply	
51	CVDD2					supply	

I/O DEFINITION AND STATUS (continued)

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
52	EMI SRAM: Add<13> output EMI SRAM: Add<13> output	1	1	1	0/1	output 2mA PP output 2mA PP	
53	EMI SRAM: Add<14> output EMI SRAM: Add<14> output	1	1	1	0/1	output 2mA PP output 2mA PP	
54	EMI SRAM: Add<15> output EMI SRAM: Add<15> output	1	1	1	0/1	output 2mA PP output 2mA PP	
55	EMI SRAM: Add<16> output EMI SRAM: Add<16> output DSP0:GPIO8 input DSP0: GPIO8 output	X	X	X	X	output 2mA PP output 2mA PP input output 2mA PP	
56	EMI SRAM: WR output EMI DRAM: WR output	1	1	1	1	output 2mA PP output 2mA PP	
57	EMI SRAM: RD output EMI DRAM: RD output	1	1	1	1	output 2mA PP output 2mA PP	
58	EMI SRAM: ALE output EMI DRAM: CAS output	1	1	1	0	output 2mA PP output 2mA PP	
59	SAI: SDO2 output EMI SRAM: Add<17>output DSP1: GPIO8 input DSP1: GPIO8 output	X	X	X	X	output 2mA PP output 2mA PP input output 2mA PP	
60	SAI: SDO1 output EMI SRAM: Add<18>output DSP1: GPIO7 input DSP1: GPIO7 output	X	X	X	X	output 2mA PP output 2mA PP input output 2mA PP	
61	SAI: SDO0 output EMI SRAM: Add<19> output	1	1	1	1	output 2mA PP output 2mA PP	
62	SAI:SDI2 input EMI SRAM: Add<20> output DSP1: GPIO6 input DSP1: GPIO6 output	X	X	X	X	input output 2mA PP input output 2mA PP	
63	SAI:SDI2 input EMI SRAM: Add<21> output EMI DRAM: RAS output DSP1: GPIO5 input DSP1: GPIO5 output	X	X	X	X	input output 2mA PP output 2mA PP input output 2mA PP	
64	SAI: SDI0 input SPDIF: CD input	X	X	X	X	input input	
65	SAI: SCKT input SAI: SCKT output	X	X	X	X	input output 2mA PP	
66	SAI: LRCKT input SAI: LRCKT output	X	X	X	X	input output 2mA PP	
67	SAI: SCKR input	X	X	X	X	input	
68	SAI: LRCKR input	X	X	X	X	input	

I/O DEFINITION AND STATUS (continued)

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
69	DSP1 Debug: DBOUT output DSP1: GPIO10 input DSP1: GPIO10 output	X	1	1	1	output 4mA PP input 5VT output 4mA PP	After boot in debug mode
70	DSP1 Debug: DBIN input DSP1 : OS10 output DSP1: GPIO11 input DSP1: GPIO11 output	X	X	X	X	input 5VT output 4mA PP input 5VT output 4mA PP	After boot in debug mode
71	DSP1 Debug: DBCK input DSP1 : OS11 output DSP1: GPIO9 input DSP1: GPIO9 output	X	X	X	X	input 5VT output 4mA PP input 5VT output 4mA PP	After boot in debug mode
72	DSP1 Debug: DBRQN input	X	X	X	X	input 5VT	After boot in debug mode
73	DSP0 Debug: DBOUT output DSP0: GPIO10 input DSP0: GPIO10 output	X	1	1	1	output 4mA PP input 5VT output 4mA PP	After boot in debug mode
74	DSP0 Debug: DBIN input DSP0 : OS00 output DSP0: GPIO11 input DSP0: GPIO11 output	X	X	X	X	input 5VT output 4mA PP input 5VT output 4mA PP	After boot in debug mode
75	DSP0 Debug: DBCK input DSP0 : OS01 output DSP0: GPIO9 input DSP0: GPIO9 output	X	X	X	X	input 5VT output 4mA PP input 5VT output 4mA PP	After boot in debug mode
76	DSP0 Debug: DBRQN input	X	X	X	X	input 5VT	
77	GND2					supply	
78	VDD2					supply	
79	ADC<0>input	X	X	X	X	analog input	
80	ADC<1>input	X	X	X	X	analog input	
81	ADC<2>input	X	X	X	X	analog input	
82	ADC<3>input	X	X	X	X	analog input	
83	ADC: S2DREF input					Substrate biasing	connected to GND
84	ADC: ADCVDDREF input					voltage reference	connect 47µF electolytic and 100nF Ceramic parallel to ADCGND
85	ADC: REF<2> input					voltage reference	connect 100µF electolytic and 100nF Ceramic parallel to ADCGND

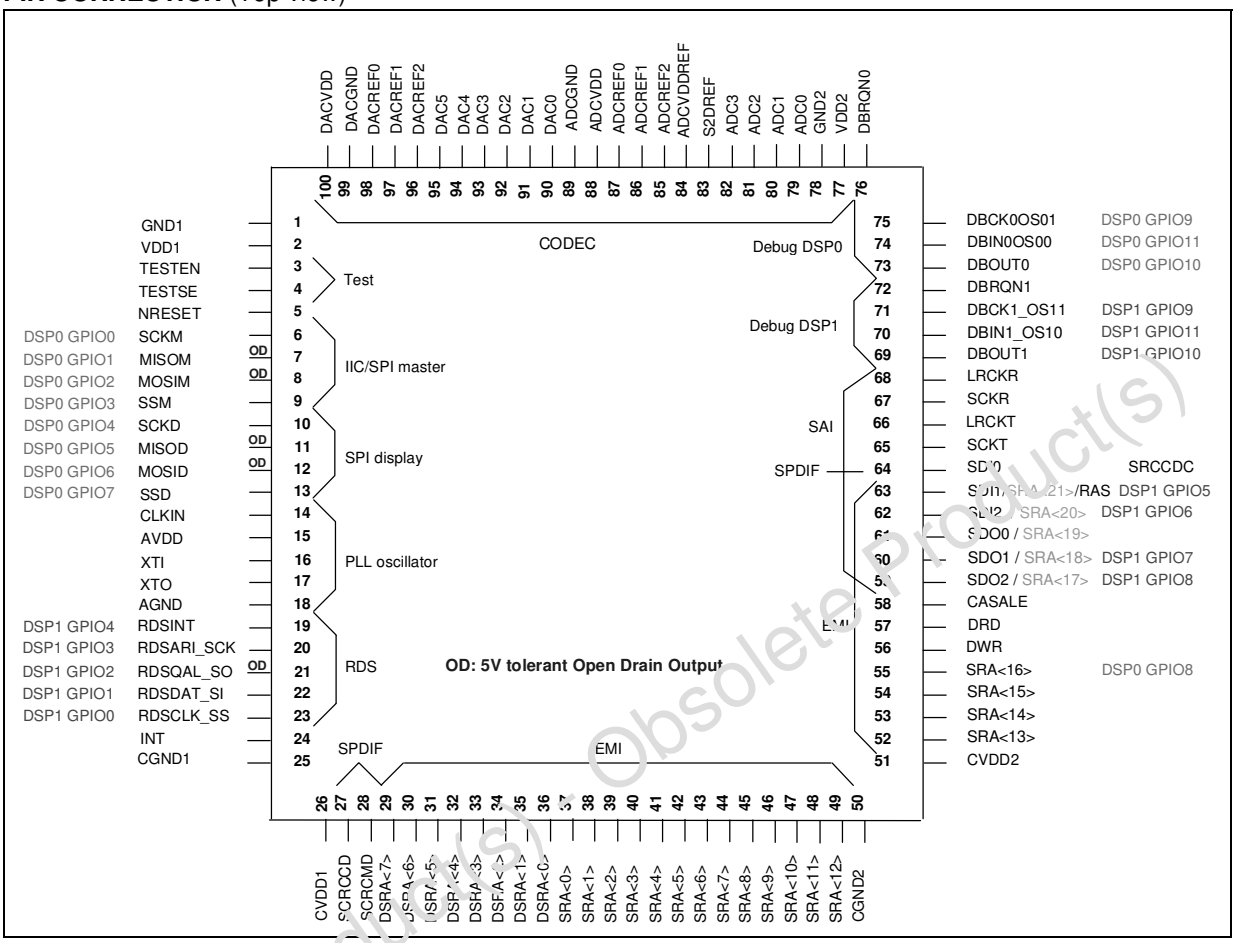
I/O DEFINITION AND STATUS (continued)

Pin #	Function	Reset State	After Boot			I/O	Comments
			SPI	I^2C	EMI		
86	ADC: REF<1> input					voltage reference	connect 47µF electolytic and 100nF Ceramic parallel to ADCGND
87	ADC: REF<0> input					voltage reference	connect 47µF electolytic and 100nF Ceramic parallel to ADCGND
88	ADCVDD					ADC power supply	
89	ADCGND					ADC ground	
90	DAC<0> output	X	X	X	X	analog output	
91	DAC<1> output	X	X	X	X	analog output	
92	DAC<2> output	X	X	X	X	analog output	
93	DAC<3> output	X	X	X	X	analog output	
94	DAC<4> output	X	X	X	X	analog output	
95	DAC<5> output	X	X	X	X	analog output	
96	DAC: REF<2> input					voltage reference	connect 47µF electolytic and 100nF Ceramic parallel to DACGND
97	DAC: REF<1> input					voltage reference	connect 47µF electolytic and 100nF Ceramic parallel to DACGND (It can be connected to Pin100)
98	DAC: REF<0> input					voltage reference	connect to DACGND (It can be connected to Pin99)
99	DACGND					DAC ground	
100	DACVDD					DAC power supply	

Output **PP**: Push-Pull/ **OD**: Open-Drain

5VT input: TTL Five Volt Tolerant Input - Schmitt-trigger for all inputs.

PIN CONNECTION (Top view)



RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DD}	3.3V Digital Power Supply Voltage		3.15	3.3	3.45	V
V_{CC}	3.3V Analog Power Supply Voltage		3.15	3.3	3.45	V

POWER CONSUMPTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{dd}	Total Maximum Current	power supply @ 3.3V and T_j = 125°C		450	490	mA

Note: 45MHz internal DSP clock, 4ADC and 6DAC enabled.

PLL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Lock Time (note1)	power supply @ 3.3V and T_j = 125°C			3	ms
F_{VCO}	VCO Frequency (note 2)		70		140	MHz

Note: 1. Depending on VCO output frequency.

2. $F_{dsp} = F_{vco}/2$ when PLL is running

OSCILLATOR CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{OSC}	Max Oscillator Frequency (XTI)	power supply @ 3.3V and T_j = 125°C			20	MHz

GENERAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{il}	Low Level Input Current without pullup device	V_i = 0V (note 1)			1	µA
I_{ih}	High Level Input Current without pullup device	$V_i = V_{dd}$ (note 1)			1	µA
I_{oz}	Tri-state Output leakage without pull up/down device	V_o = 0V or V_{dd} (note 1)			1	µA
I_{ozFT}	5V Tolerant Tri-state Output leakage without pull up/down device	V_o = 0V or V_{dd} (note 1)			1	µA
		V_o = 5.5V		1	3	µA
$I_{latchup}$	I/O latch-up current	V < 0V, V > V_{dd}	200			mA
V_{esd}	Electrostatic Protection	Leakage , 1µA (note 2)	2000			V

Note: 1. The leakage currents are generally very small, <1nA. The value given here, 1µA, is a maximum that can occur after an Electrostatic Stress on the pin.
2. Human Body Model.

LOW VOLTAGE CMOS INTERFACE DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage				0.2*V_{dd}	V
V_{ih}	High Level Input Voltage		0.8*V_{dd}			V
V_{hyst}	Schmitt trigger hysteresis		0.8			V
V_{ol}	Low level output Voltage	I_{ol} = XmA (notes 1, 2)			0.4	V
V_{oh}	High level output Voltage		0.85*V_{dd}			V

Note: 1. Takes into account 200mV voltage drop in both supply lines.
2. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

LOW VOLTAGE TTL INTERFACE DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{il}	Low Level Input Voltage	(note 1)			0.8	V
V_{ih}	High Level Input Voltage	(note 1)	2			V
V_{ilhyst}	Low level threshold input falling	(note 1)	0.9		1.35	V
V_{ihhyst}	Low level threshold input falling	(note 1)	1.3		1.9	V
V_{hyst}	Schmitt trigger hysteresis	(note 1)	0.4		0.7	V
V_{ol}	Low level output Voltage	I_{ol} = XmA (notes 1, 2 & 3)			0.4	V
V_{oh}	High level output Voltage		2.4			V

Note: 1. TTL specifications only apply to the supply voltage range Vdd = 3.0V to 3.6V
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

DSP CORE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{dsp}	Maximum DSP clock frequency	power supply @ 3.3V and T_j = 125°C	48			MHz

FM Stereo Decoder

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
a_ch	Channel Separation			>50		dB
THD	Total Harmonic Distortion			0.02		%
(S+N)/N	Signal plus Noise to Noise ratio			86		dB

ADC ELECTRICAL CHARACTERISTCS (T_{amb} = 25°C, V_{CC} = 3.3V, measurement bandwidth 10Hz to 20KHz, A-Weighted Filter.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Input Voltage Dynamic Range			0.75	0.8	Vrms
	Sampling rate	Audio mode			48	KHz
	Attenuation @ 20KHz	@ fs = 44.1KHz		-0.6		dB
	Dynamic Range	-60dB analog input	84	88		dB
	SNR	1KHz; -3dB analog input	84	88		dB
	(THD + N)	-3dB analog input (note 1)		-85	-80	dB
	Input Impedance	@ fs = 44.1KHz	40	55	75	kΩ
	Crosstalk	1Vrms input @ 1KHz			-85	dB
	Gain mismatch between four input	@ 1KHz	-0.5		0.5	dB

Note1: 0dB reference at $0.75V_{rms}$ input

ADC ELECTRICAL CHARACTERISTCS (T_{amb} = 25°C, V_{CC} = 3.3V, measurement bandwidth 10Hz to 53KHz.)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Input Voltage Dynamic Range			0.75	0.8	Vrms
	Sampling rate	AM-Mode			192	KHz
	Dynamic Range	-60dB analog input	80			dB
	SNR	1KHz; -3dB analog input	80			dB
	(THD +N)	-3dB analog input			-80	dB

ADC ELECTRICAL CHARACTERISTCS (T_{amb} = 25°C, V_{CC} = 3.3V, measurement bandwidth 10Hz to 160KHz.)

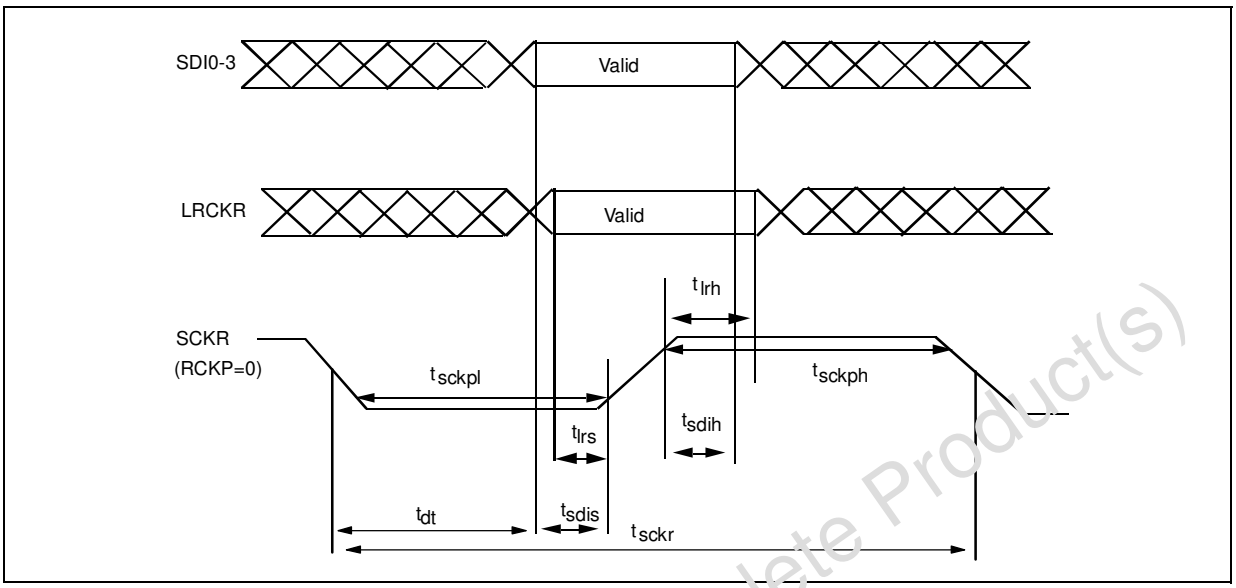
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Input Voltage Dynamic Range			0.75	0.8	Vrms
	Sampling rate	FM-Mode			390	KHz
	Dynamic Range	-60dB analog input	60			dB
	SNR	1KHz; -3dB analog input	60			dB

DAC PERFORMANCE (T_{amb} = 25°C, V_{CC} = 3.3V, measurement bandwidth 10Hz to 20KHz, A-Weighted Filter 0dB gain, output load 30kΩ)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
	Output voltage dynamic range		0.87	0.9	0.93	Vrms
	Sampling rate				48	KHz
	Attenuation @ 20kHz	@ 20KHz with f_s = 44.1KHz	-0.3	-0.2		dB
	Dynamic Range	-60dB analog input	90	93		dB
	SNR	1KHz -3dB analog output	90	93		dB
	Digital Silence	0000hex digital input		93		dB
	(THD + N)/S	@ digital full scale		-85	-83	dB
	Output Impedance			25	50	Ω
	Crosstalk	1Vrms output @ 1KHz		-90	-86	dB
	Gain mismatch between six outputs	@ 1KHz	-0.5		0.5	dB

SAI INTERFACE

Figure 1. SAI Timings



Timing	Description	Value	Unit
t_{sckr}	Minimum Clock Cycle	$4T_{DSP}$	ns
t_{dt}	SCKR active edge to data out valid	10	ns
t_{lrs}	LRCK setup time	5	ns
t_{lrh}	LRCK hold time	5	ns
t_{sdid}	SDI setup time	15	ns
t_{sdih}	SDI hold time	15	ns
t_{sckph}	Minimum SCK high time	0.35 t_{sckr}	ns
t_{sckpl}	Minimum SCK low time	0.35 t_{sckr}	ns

Note T_{DSP} = dsp master clock cycle time = $1/F_{DSP}$

Figure 2. SAI protocol when RLRS=0; RREL=0; RCKP=1; RDIR=0

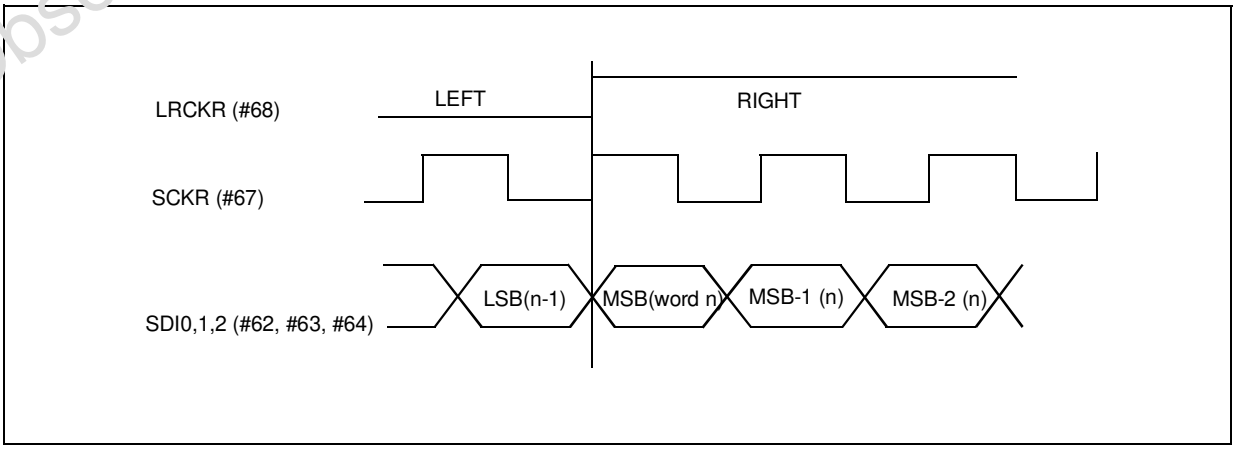


Figure 3. SAI protocol when RLRS=1; RREL=0; RCKP=1; RDIR=1.

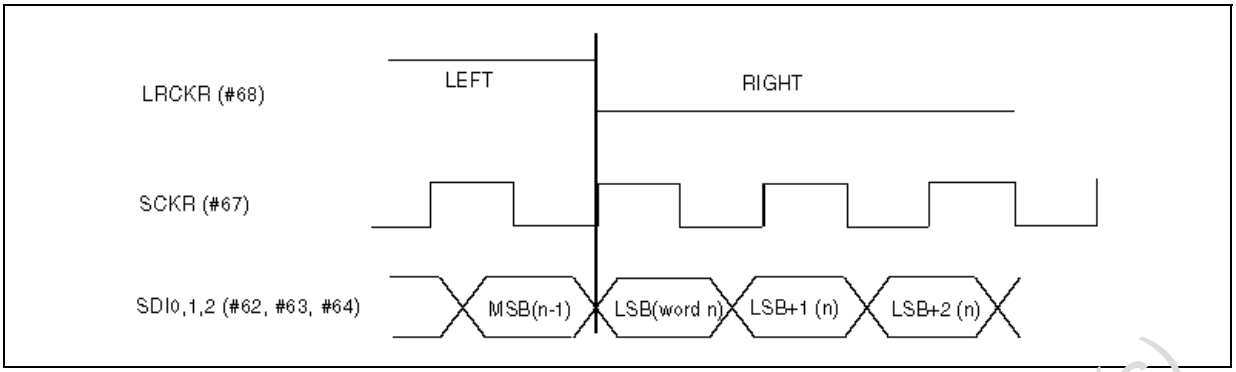


Figure 4. SAI protocol when RLRS=0; RREL=0; RCKP=0; RDIR=0.

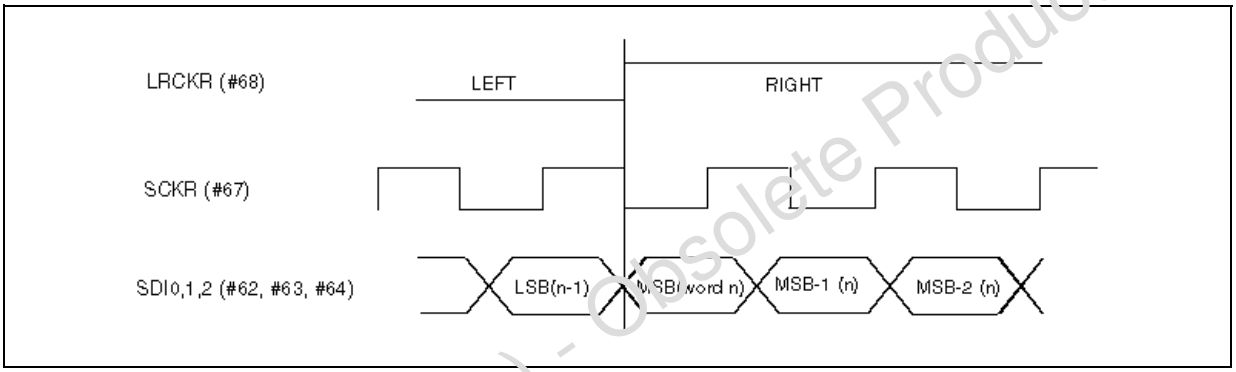
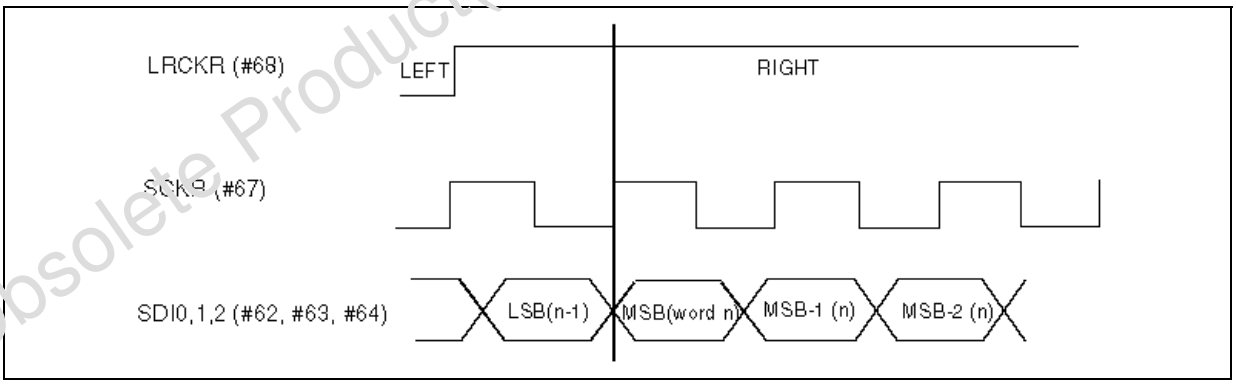


Figure 5. SAI protocol when RLRS=0; RREL=1; RCKP=1; RDIR=0.



SPI INTERFACES

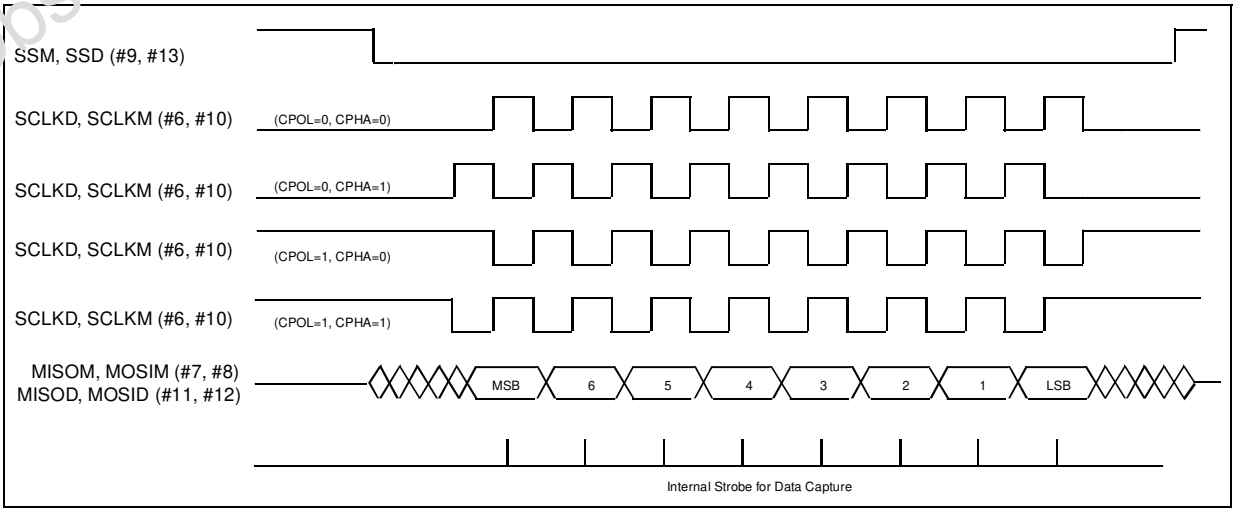
10 WORDS MAIN MICRO SPI

Symbol	Description	Min Value	Unit
	MASTER		
t_{sclk}	Clock Cycle	$12T_{DSP}$	ns
t_{dtr}	Sclk edge to MOSI valid	40	ns
$t_{misosetup}$	MISO setup time	16	ns
$t_{misohold}$	MISO hold time	4	ns
t_{sclkh}	SCK high time	$0.5t_{sclk}$	ns
t_{sclkl}	SCK high low	$0.5t_{sclk}$	ns
	SLAVE		
t_{sclk}	Clock Cycle	$12T_{DSP}$	ns
t_{dtr}	Sclk edge to MOSI valid	40	ns
$t_{mosisetup}$	MOSI setup time	16	ns
$t_{mosihold}$	MOSI hold time	4	ns
t_{sclkh}	SCK high time	$0.5t_{sclk}$	ns
t_{sclkl}	SCK high low	$0.5t_{sclk}$	ns

DISPLAY SPI (different timings)

	MASTER		
t_{sclk}	Clock Cycle	$6T_{DSP}$	ns
	SLAVE		
t_{sclk}	Clock Cycle	$6T_{DSP}$	ns

Figure 6. SPI Clocking scheme.



Debug Port Interface

No.	Characteristics	dclk = 40MHz		Unit
		Min.	Max.	
1	DBCK rise time	--	3	ns
2	DBCK fall time	--	3	ns
3	DBCK Low	40	--	ns
4	DBCK High	40	--	ns
5	DBCK Cycle Time	200	--	ns
6	DBRQN Asserted to DBOUT (ACK) Asserted	5 TDSP	--	ns
7	DBCK High to DBOUT Valid	--	42	ns
8	DBCK High to DBOUT Invalid	3	--	ns
9	DBIN Valid to DBCK Low (Set-up)	15	--	ns
10	DBCK Low to DBIN Invalid (Hold)	3	--	ns
	DBOUT (ACK) Asserted to First DBCK High	2 Tc	--	ns
	DBOUT (ACK) Assertion Width	4.5 TDSP - 3	5 TDSP + 7	ns
11	Last DBCK Low of Read Register to First DBCK High of Next Command	7 TDSP + 10	--	ns
12	Last DBCK Low to DBOUT Invalid (Hold)	3	--	ns
	DBSEL setup to DBCK	TDSP		ns

Figure 7. Debug Port Serial Clock Timing.

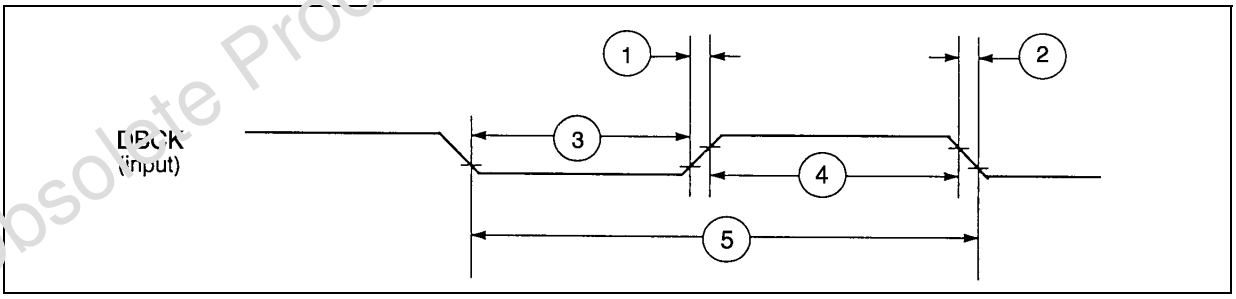


Figure 8. Debug Port Acknowledge Timing.

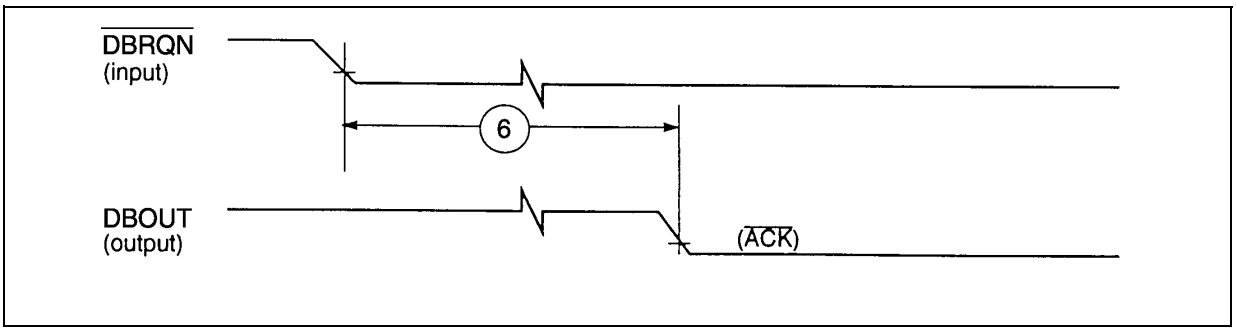


Figure 9. Debug Port Data I/O to Status Timing.

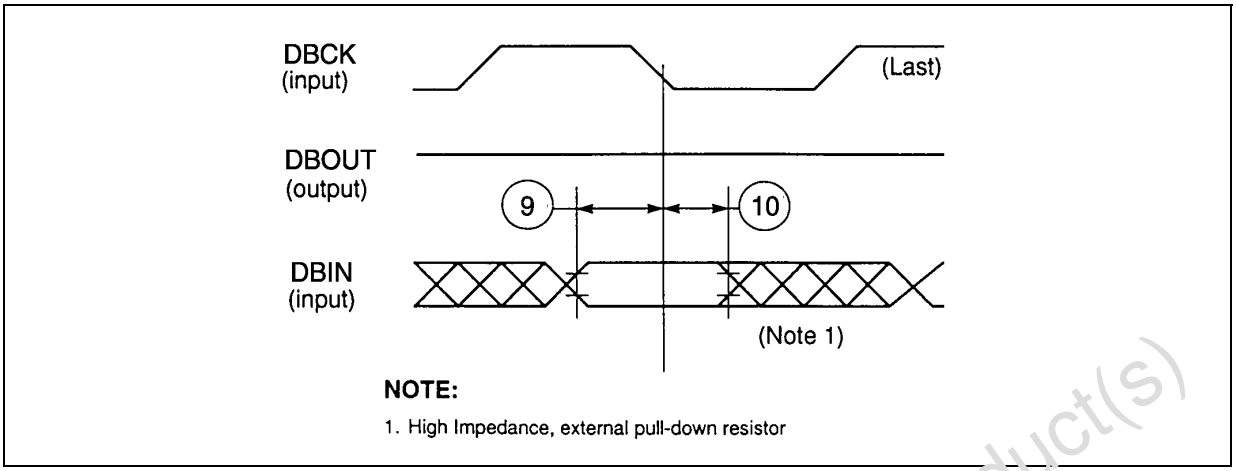


Figure 10. Debug Port Read Timing.

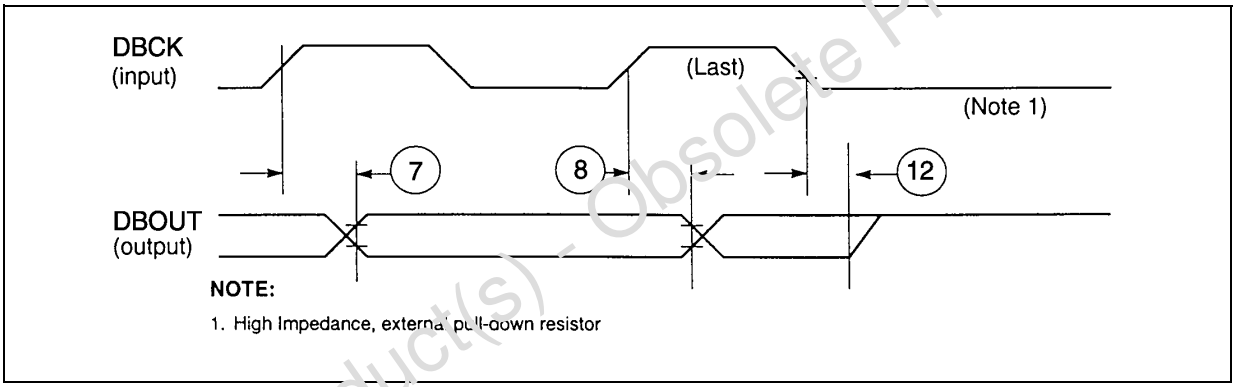
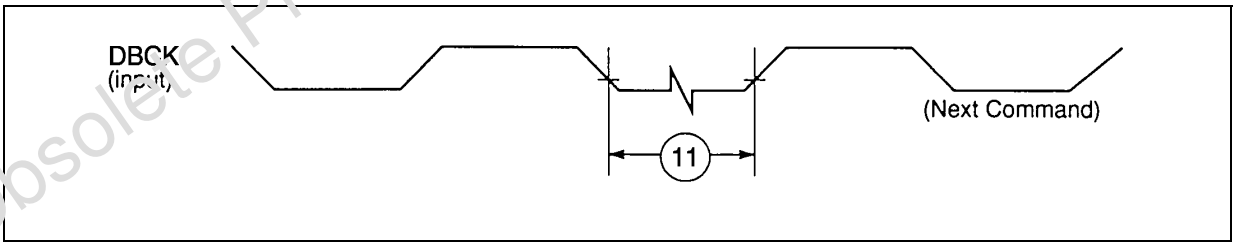


Figure 11. Debug Port DBCK Next Command After Read Register Timing.



EXTERNAL MEMORY INTERFACE (EMI) DRAM MODE

Characteristics	Timing Mode	40MHz		Unit
		Min.	Max.	
Page Mode Cycle Time	slow fast	10075	----	ns ns
$\overline{RAS}$ or $\overline{RD}$ Assertion to Data Valid	slow fast	-- --	159 109	ns ns
$\overline{CAS}$ Assertion to Data Valid	slow fast	-- --	65 40	ns ns
Column Address Valid to Data Valid	slow fast	-- --	80 55	ns ns
$\overline{CAS}$ Assertion to Data Active		0	--	ns
$\overline{RAS}$ Assertion Pulse Width (Note 1) (Page Mode Access Only)	slow fast	264 189	-- --	ns ns
$\overline{RAS}$ Assertion Pulse Width (Single Access Only)	slow fast	164 114	-- --	ns ns
$\overline{RAS}$ or $\overline{CAS}$ Negation to $\overline{RAS}$ Assertion	slow fast	120 70	-- --	ns ns
$\overline{CAS}$ Assertion Pulse Width	slow fast	65 40	-- --	ns ns
Last $\overline{CAS}$ Assertion to $\overline{RAS}$ Negation (Page Mode Access Only)	slow fast	60 35	-- --	ns ns

Note: 1. n is the number of successive accesses. n = 2, 3, 4, or 6.

DRAM Refresh Timing

Characteristics	Timing Mode	40MHz		Unit
		Min.	Max.	
$\overline{RAS}$ Negation to $\overline{RAS}$ Assertion	slow fast	143 93	-- --	ns ns
$\overline{CAS}$ Negation to $\overline{CAS}$ Assertion	slow fast	118 68	-- --	ns ns
Refresh Cycle Time	slow fast	325 225	-- --	ns ns
$\overline{RAS}$ Assertion Pulse Width	slowf ast	166 116	-- --	ns ns
$\overline{RAS}$ Negation to $\overline{RAS}$ Assertion for Refresh Cycle (Note 1)	slow fast	120 70	-- --	ns ns
$\overline{CAS}$ Assertion to $\overline{RAS}$ Assertion on Refresh Cycle		18	--	ns
$\overline{RAS}$ Assertion to $\overline{CAS}$ Negation on Refresh Cycle	slow fast	160 110	-- --	ns ns
$\overline{RAS}$ Negation to $\overline{CAS}$ Assertion on a Refresh Cycle	slow fast	114 64	-- --	ns ns
$\overline{CAS}$ Negation to Data Not Valid		0	--	ns

Note: 1. Happens when a Refresh Cycle is followed by an Access Cycle.

EXTERNAL MEMORY INTERFACE (EMI) SRAM MODE

Characteristics	40MHz		Unit
	Min.	Max.	
Address Valid and $\overline{CS}$ Assertion Pulse Width	89	--	ns
Address Valid to $\overline{RD}$ or $\overline{WR}$ Assertion	23	--	ns
$\overline{RD}$ or $\overline{WR}$ Assertion Pulse Width	45	--	ns
$\overline{RD}$ or $\overline{WR}$ Negation to $\overline{RD}$ or $\overline{WR}$ Assertion	39	--	ns
$\overline{RD}$ or $\overline{WR}$ Negation to Address not Valid	5	--	ns
Address Valid to Input Data Valid	--	72	ns
$\overline{RD}$ Assertion to Input Data Valid	--	35	ns
$\overline{RD}$ Negation to Data Not Valid (Data Hold Time)	0	--	ns
Address Valid to $\overline{WR}$ Negation	73	--	ns
Data Setup Time to $\overline{WR}$ Negation	32	--	ns
Data Hold Time from $\overline{WR}$ Negation	5	--	ns
$\overline{WR}$ Assertion to Data Valid	--	18	ns
$\overline{WR}$ Negation to Data High-Z (Note 1)	--	23	ns
$\overline{WR}$ Assertion to Data Active	5	--	ns

Figure 12. External Memory Interface SRAM Read Cycle.

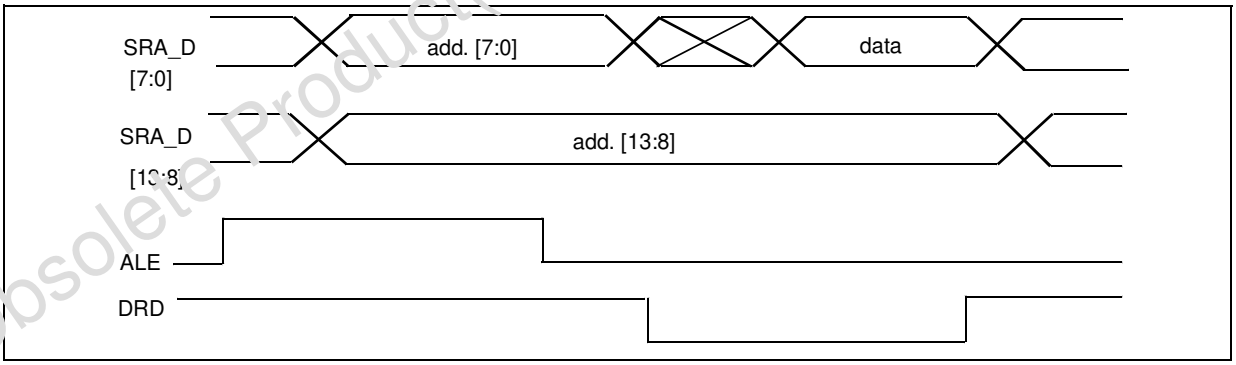


Figure 13. External Memory Interface SRAM Write Cycle.