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TDA7511

AM/FM TUNER FOR CAR RADIO AND HIFI APPLICATIONS

FM-PART

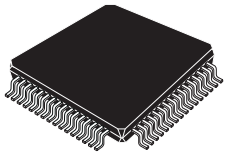
- RF AGC GENERATION BY RF AND IF DETECTION FOR PIN DIODES AND MOSFET (PRESTAGE)
- 1ST MIXER FOR 1ST FM IF 10.7MHz WITH PROGRAMMABLE IF TANK ADJUST FOR FM AND AM UPCONVERSION
- 2 PROGRAMMABLE IF-GAIN STAGES
- 2ND MIXER FOR 2ND IF 450KHz
- INTERNAL IF BANDPASS FILTER WITH THREE BANDWIDTHS CONTROLLED BY ISS (INCLUDING WEATHER BAND)
- FULLY INTEGRATED FM-DEMODULATOR

AM-PART

- WIDE AND NARROW AGC GENERATION
- PREAMPLIFIER AND MIXER FOR 1ST IF 10.7MHZ, AM UPCONVERSION
- 2ND MIXER FOR 2ND IF 450 KHZ
- INTEGRATED AM-DEMODULATOR
- OUTPUT FOR AM-STEREO-DECODER

ADDITIONAL FEATURES

- HIGH PERFORMANCE FAST PLL FOR RDS-SYSTEM
- IF COUNTER FOR FM AND AM UPCONVERSION WITH SEARCH STOP SIGNAL
- QUALITY DETECTOR FOR LEVEL, DEVIATION, ADJACENT CHANNEL AND MULTIPATH
- QUALITY DETECTION INFORMATIONS AS ANALOG SIGNALS EXTERNAL AVAILABLE
- ISS (INTELLIGENT SELECTIVITY SYSTEM) FOR CANCELLATION OF ADJACENT CHANNEL AND NOISE INFLUENCES
- ADJACENT CHANNEL MUTE
- FULLY ELECTRONIC ALIGNMENT
- ALL FUNCTIONS I^2C-BUS CONTROLLED
- ISS FILTER STATUS INFORMATION I^2C-BUS READABLE



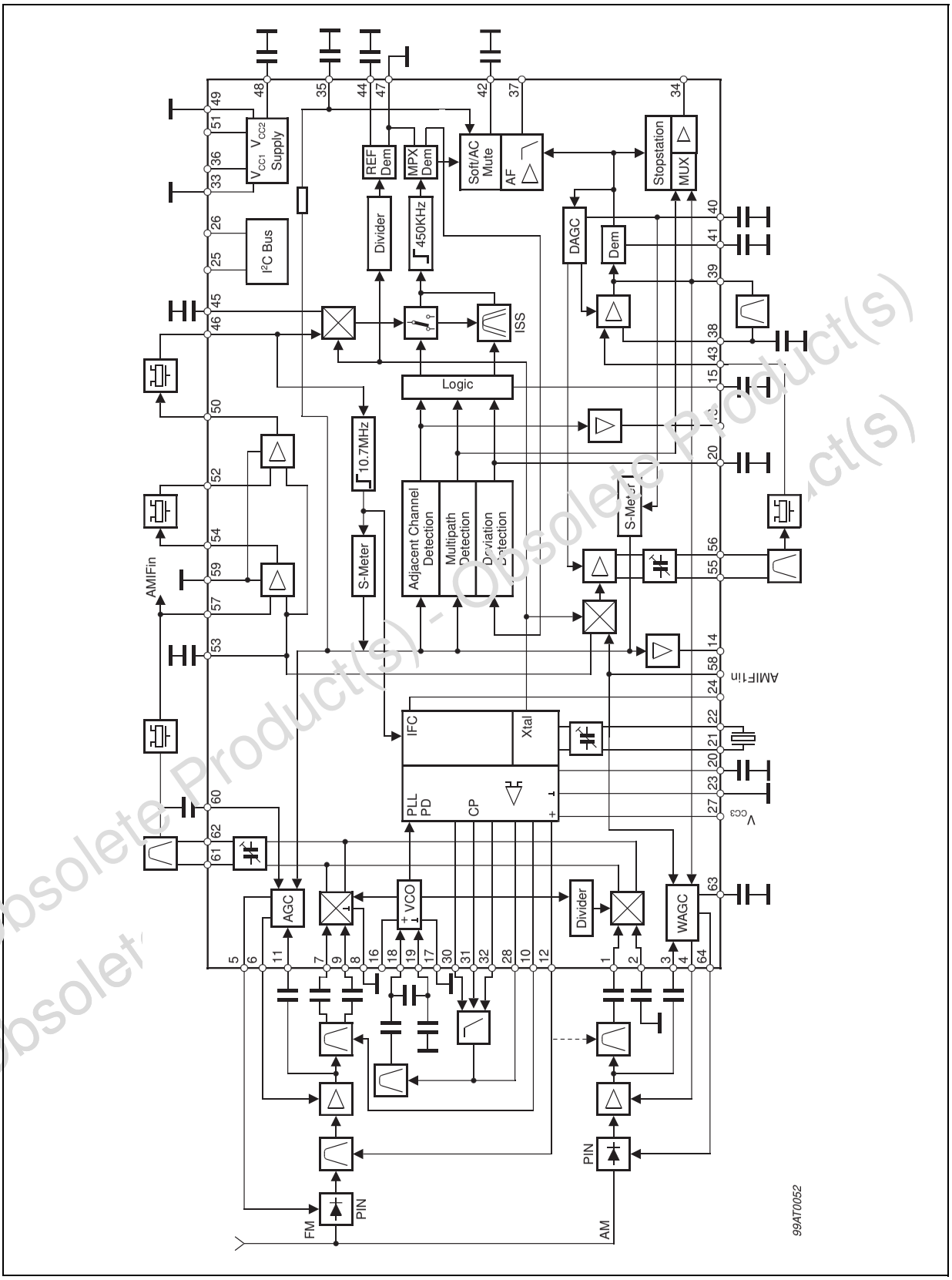
TQFP64
ORDERING NUMBER: TDA7511

DESCRIPTION

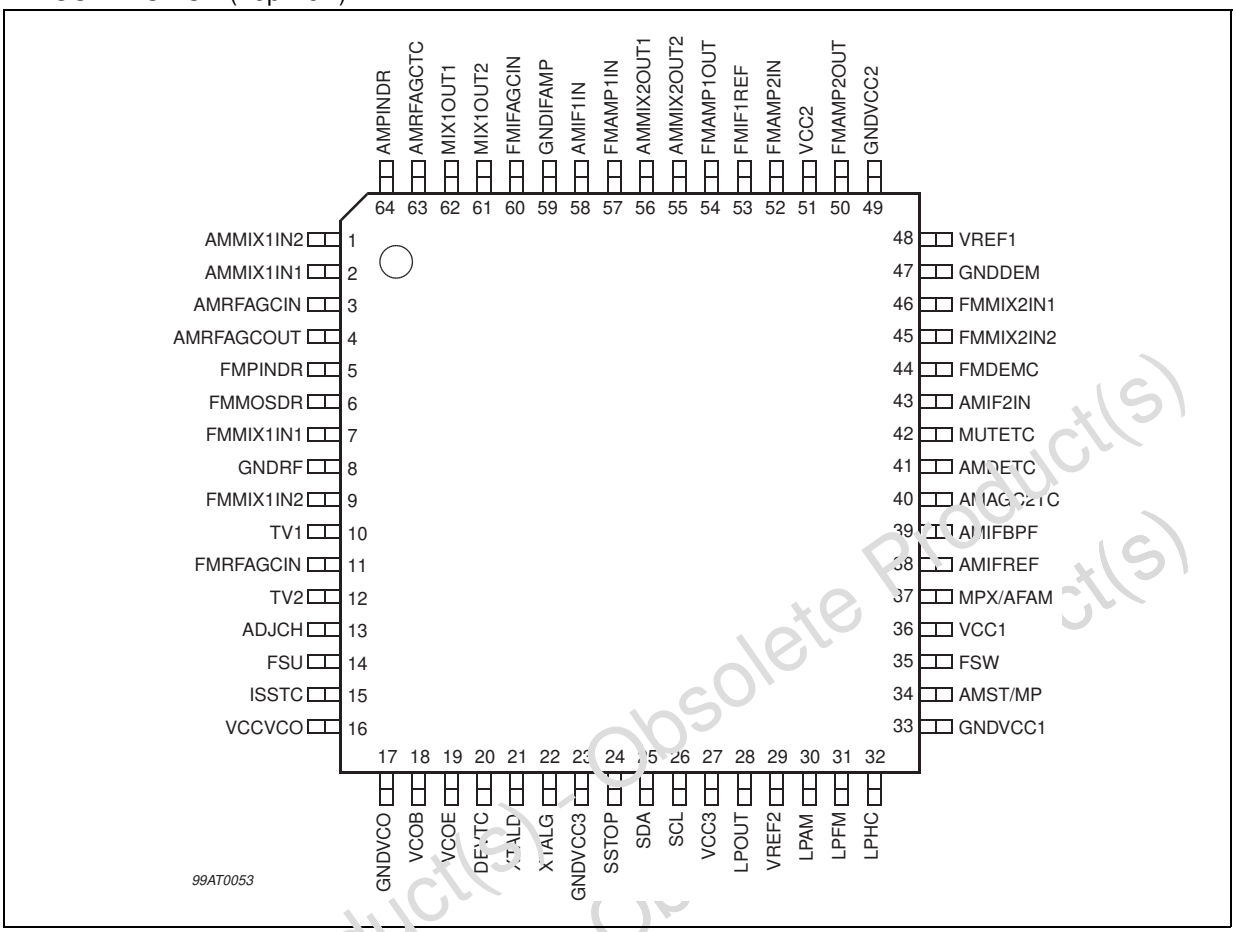
The TDA 7511 is a high performance tuner circuit for AM/FM car radio. It contains mixers, IF amplifiers, demodulators for AM and FM, quality detection, ISS filter and PLL synthesizer with IF counter on a single chip.

Use of BICMOS technology allows the implementation of several tuning functions and a minimum of external components.

BLOCK DIAGRAM



PIN CONNECTION (Top view)



PIN DESCRIPTION (continued)

N°	Pin	Function
1	AMMIX1IN2	AM Input2 Mixer1
2	AMMIX1IN1	AM Input1 Mixer1 Reference
3	AMRFAGCIN	Input AM RF AGC
4	AMRFAGCOUT	Output AM RF AGC
5	FMPINDR	FM PIN Diode Driver Output
6	FMMOSDR	FM MOS Driver Output
7	FMMIX1IN1	FM Input1 Mixer1
8	GNDRF	RF Ground
9	FMMIX1IN2	FM Input2 Mixer1
10	TV1	Tuning Voltage 1
11	FMRFAGCIN	FM RF AGC Input
12	TV2	Tuning Voltage 2
13	ADJCH	Ident. Adjacent Channel Output
14	FSU	Unweighted Fieldstrength Output

PIN DESCRIPTION (continued)

N°	Pin	Function
15	ISSTC	Time Constant for ISS Filter Switch
16	VCCVCO	VCO Supply
17	GNDVCO	VCO Ground
18	VCOB	VCO Input Base
19	VCOE	VCO Output Emitter
20	DEVTC	Deviation Detector Time Constant
21	XTALD	Xtal Oscillator to MOS Drain
22	XTALG	Xtal Oscillator to MOS Gate
23	GNDVCC3	VCC3 Ground
24	SSTOP	Search Stop Output
25	SDA	I^2C-Bus Data
26	SCL	I^2C-Bus Clock
27	VCC3	Supply Tuning Voltage
28	LPOUT	Op Amp Output to PLL Loop Filters
29	VREF2	Voltage Reference for PLL Op Amp
30	LPAM	Op Amp Input to PLL Loop Filters AM
31	LPFM	Op Amp Input to PLL Loop Filters FM
32	LPHC	High Current PLL Loop Filter Input
33	GNDVCC1	Digital Ground
34	AMST/MP	AM Stereo Out / Ident. Multipath Output
35	FSW	Weighted Fieldstrength Output
36	VCC1	Digital Supply
37	MPX/AFAM	MPX Output / AM AF Output
38	AMIFREF	Reference Voltage AM IF Amp
39	AMIFBPF	AM IF Filter
40	AMAGC2TC	AM AGC2 Time Constant
41	AMDETC	AM Detector Capacitor
42	MUTETC	Softmute Time Constant
43	AMIF2IN	Input AM IF2
44	FMDEMC	FM Demodulator Reference
45	FMMIX2IN2	FM IF1 MIX2 Input1
46	FMMIX2IN1	FM IF1 MIX2 Input2
47	GNDDEM	Ground FM Demodulator
48	VREF1	Reference 5V
49	GNDVCC2	Analog Ground
50	FMAMP2OUT	FM IF1 Amplifier2 Output

PIN DESCRIPTION (continued)

N°	Pin	Function
51	VCC2	Analog Supply
52	FMAMP2IN	FM IF1 Amplifier2 Input
53	FMIF1REF	FM IF1 Amplifier Reference
54	FMAMP1OUT	FM IF1 Amplifier1 Output
55	AMMIX2OUT2	AM Tank 450kHz
56	AMMIX2OUT1	AM Tank 450kHz
57	FMAMP1IN	FM IF1 Amplifier1 Input
58	AMIF1IN	AM IF1 Input
59	GNDIF1AMP	FM IF1 Amplifier Ground
60	FMIF1AGCIN	FM IF1 AGC Input
61	MIX1OUT2	MIX Tank 10.7MHz
62	MIX1OUT1	MIX Tank 10.7MHz
63	AMRFAGCTC	AM RF AGC Time Constant
64	AMPINDR	AM PIN Diode Driver Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	10.5	V
T_{amb}	Ambient Temperature	-40 to 85	°C
T_{stg}	Storage Temperature	-55 to +150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{Th(j-amb)}$	Thermal resistance	68	°C/W

ELECTRICAL CHARACTERISTCS

T_{amb} = +25°C, V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Supply						
V_{CC1}	Digital supply voltage		7.5	8.5	10	V
V_{CC2}	Analog supply voltage		7.5	8.5	10	V
V_{CC3}	Analog tuning voltage		7.5	8.5	10	V
V_{CCVCO}	VCO supply voltage		7.5	8.5	10	V

ELECTRICAL CHARACTERISTCS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1}$ = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CCMIX1}	MIX1 supply voltage		7.5	8.5	10	V
V_{CCMIX2}	MIX2 supply voltage		7.5	8.5	10	V
I_{CC1}	Supply current	FM ON		7.5		mA
I_{CC1}	Supply current	AM ON		10		mA
I_{CC2}	Supply current	FM ON		50		mA
I_{CC2}	Supply current	AM ON		60		mA
I_{CC3}	Supply current			2		mA
I_{CCVCO}	Supply current			2.5		mA
I_{CCMIX1}	Supply current	FM ON		6		mA
I_{CCMIX1}	Supply current	AM ON		5		mA
I_{CCMIX2}	Supply current	AM ON		5		mA
Reference Voltages						
V_{REF1}	Internal reference voltage	I_{REF1} = 0mA		5		V
V_{REF2}	Internal reference voltage	I_{REF2} = 0 mA		2.5		V
Wide Band RF AGC						
V_{11}	Threshold AGC start	$V_6 = V_{CC2}/2$		80		dBµV
R_{IN}	Input resistance			500		Ω
C_{IN}	Input capacitance			2.5		pF
Narrow Band RF & Keying AGC						
V_{60}	Lower threshold	FMAGC, V_{11} = 0mV$_{RMS}$		82		dBµV
V_{60}	Upper threshold	FMAGC, V_{11} = 0mV$_{RMS}$		92		dBµV
R_{IN}	Input resistance			10		kΩ
C_{IN}	Input capacitance			2.5		pF
AGC MOSFET Driver Output						
V_6	Max. AGC output voltage	V_{11} = 0mV$_{RMS}$	V_{CC2} -0.5V			V
V_6	Min. AGC output voltage	V_{11} = 50mV$_{RMS}$			0.5	V
I_6	Min. AGC charge current	V_{11} = 0mV$_{RMS}$, $V_6 = V_{CC2}/2$		-12.5		µA
I_6	Max. AGC discharge current	V_{11} = 50mV$_{RMS}$, $V_6 = V_{CC2}/2$		1.25		mA
AGC PIN Diode Driver Output						
I_5	AGC OUT, current min.	V_{11} = 0mV$_{RMS}$, V_5 = 2V		50		µA
I_5	AGC OUT, current max.	V_{11} = 50 mV$_{RMS}$, V_5 = 2V		-6		mA
Mixer1 (10.7MHz)						
R_{IN}	Input impedance	Balanced, f = 98MHz		9		Ω

ELECTRICAL CHARACTERISTCS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1}$ = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
IP3	3rd order intercept point			122		dBµV
F	Noise figure			6		dB
A_C	Conversion gain			120		mS
IF1 Amplifier1 & 2 (10.7MHz)						
A_{min}	Min. gain	IFG		9		dB
A_{max}	Max. gain	IFG		15		dB
R_{IN}	Input resistance			330		Ω
R_{OUT}	Output resistance			330		Ω
P_{1dB}	1dB compression point	Output referred		120		dBµV
IP3	3rd order Intercept Point	Output referred		132		dBµV
Mixer2 (450kHz)						
R_{IN}	Input impedance			330		Ω
V_{46}	Max. input voltage			900		mV_{RMS}
V_{48}	Limiting sensitivity	S/N = 20dB		25		µV
A	Mixer gain			18		dB
Limiter 1 (450kHz)						
$G_{Limiter}$	Gain			80		dB
Demodulator, Audio Output						
THD		Dev.= 75kHz, V_{46} = 10mV_{RMS}			0.1	%
V_{MPX}	MPX output signal	Dev.= 75kHz		500		mV_{RMS}
R_{OUT}	Output resistance			350		Ω
$\|\Delta V\|_{min}$	DC offset fine adjust	DEM, MENA=1		6		mV
$\|\Delta V\|_{max}$	DC offset fine adjust	DEM, MENA=1		186		mV
S/N		Dev.= 40kHz,V_{46} = 10mV_{RMS}		75		dB
Quality Detection						
S-meter, Unweighted Fieldstrength						
V_{46}	Min. input voltage MIX2			10		µV
ΔV	Per decade	SMSL = 0		1		V
ΔV	Per decade	SMSL = 1		1.5		V
V_{14}	Fieldstrength output	V_{46} = 0V_{RMS}		0.1		V
V_{14}	Fieldstrength output	V_{46} = 1V_{RMS}		4.9		V
R_{OUT}	Output resistance			4		kΩ

ELECTRICAL CHARACTERISTCS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1}$ = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ΔV_{14}	S-meter shift voltage	SL	-1.8		1.8	V
TK	Temp coeff.			0		ppm/K
S-meter, Weighted Fieldstrength						
V_{35}	Fieldstrength output	$V_{46} = 0V_{RMS}$		2.5		V
V_{35}	Fieldstrength output	$V_{46} = 1V_{RMS}$		4.9		V
R_{OUT}	Output resistance			12		kΩ
Adjacent Channel Gain						
A_{min}	Gain minimum	ACG		32		dB
A_{max}	Gain maximum	ACG		56		dB
Adjacent Channel Filter						
f_{HP}	-3dB frequency highpass	ACF		100		kHz
f_{BP}	Centre frequency	ACF		100		kHz
f_{-20dB}	Attenuation 20dB			70		kHz
Adjacent Channel Output						
V_{13}	Output voltage low			0.1		V
V_{13}	Output voltage high			4.9		V
R_{OUT}	Output resistance			4		kΩ
Multipath Channel Gain						
A_{min}	Gain minimum	MPG		12		dB
A_{max}	Gain maximum	MPG		23		dB
Multipath Bandpass Filter						
f_{Lower}	Centre frequency low	MPF		19		kHz
f_{Upper}	Centre frequency up	MPF		31		kHz
Q	Quality factor		5		10	
Multipath Output						
V_{34}	Output voltage low			0.1		V
V_{34}	Output voltage high			4.9		V
R_{OUT}	Output resistance			2.5		kΩ
ISS (intelligent Selectivity System)						
Filter 450kHz						
f_{centre}	Centre frequency	f_{REF_intern} = 450kHz		450		kHz
BW 3dB	Bandwidth, -3dB	ISS80 = 1		80		kHz
BW 20dB	Bandwidth, -20dB	ISS80 = 1		150		kHz

ELECTRICAL CHARACTERISTCS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1}$ = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BW 3dB	Bandwidth, -3dB	ISS80 = 0		120		kHz
BW 20dB	Bandwidth, -20dB	ISS80 = 0		250		kHz
BW 3dB	Bandwidth weather band	ISS30 = 1		30		kHz
BW 20dB	-20dB weather band	ISS30 = 1		80		kHz
Δf_{min}	Fine adjust	AISS		-20		kHz
Δf_{max}	Fine adjust	AISS		10		kHz
Adjacent Channel ISS Filter Threshold						
V_{NTH}	Internal low threshold	ACNTH		0		V
V_{NTH}	Internal high threshold	ACNTH		0.3		V
V_{WTH}	Internal low threshold	ACWTH		0.25		V
V_{WTH}	Internal high threshold	ACWTH		0.95		V
Multipath Threshold						
V_{THMP}	Internal low threshold	MPTH		0.50		V
V_{THMP}	Internal high threshold	MPTH		1.25		V
ISS Filter Time Constant						
I_{15}	Charge current low mid	TISS, ISSCTL = 1		-74		µA
I_{15}	Charge current high mid	TISS, ISSCTL = 1		-60		µA
I_{15}	Charge current low narrow	TISS, ISSCTL = 1		-124		µA
I_{15}	Charge current high narrow	TISS, ISSCTL = 1		-110		µA
I_{15}	Discharge current low	TISS, ISSCTL = 0		1		µA
I_{15}	Discharge current high	TISS, ISSCTL = 0		15		µA
V_{15}	Low voltage	ISSCTL = 0		0.1		V
V_{15}	High voltage	ISSCTL = 1		4.9		V
ISS Filter Switch Threshold						
V_{15}	Threshold ISS on	ISSCTL = 0		3		V
V_{15}	Threshold ISS off	ISSCTL = 0		1		V
V_{15}	Threshold ISS narrow on	ISSCTL = 0		4		V
V_{15}	Threshold ISS narrow off	ISSCTL = 0		2		V
I_{20}	Charge current low	TDEV		-20		µA
I_{20}	Charge current high	TDEV		-34		µA
I_{20}	Discharge current low	TDEV		6		µA
I_{20}	Discharge current high	TDEV		20		µA

ELECTRICAL CHARACTERISTCS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1}$ = 8.5V, f_{RF} = 98MHz, dev. = 40kHz, f_{MOD} = 1kHz, f_{IF1} = 10.7MHz, f_{IF2} = 450KHz, f_{Xtal} = 10.25MHz, in test or application circuit, unless otherwise specified.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DEV_{WTH}	Internal low threshold	DWTH		30		kHz
DEV_{WTH}	Internal high threshold	DWTH		75		kHz
$RATIO_{min}$	Referred to threshold	DTH		1		
$RATIO_{max}$	Referred to threshold	DTH		1.5		
Softmute						
V_{ANT}	Upper startpoint	SMTH, SMD, SLOPE = 0		16		dBµV
V_{ANT}	lower startpoint	SMTH, SMD, SLOPE = 0		[illegible]		dBµV
a_{SMmin}	Min. softmute depth	SMD, SLOPE = 0, $SMTH_{Upper}$		[illegible]		dB
a_{SMmax}	Max. softmute depth	SMD, SLOPE = 0, $SMTH_{Upper}$		36		dB
$a_{SMTHISS}$	Mute depth threshold for ISS filter on	SMCTH	0.2		2	dB
V_{ACTH}	Internal AC mute threshold	ACM	60		220	mV
a_{SMAC}	AC mute depth			6		dB
I_{42}	Charge current			-47.5		µA
I_{42}	Discharge current			2.5		µA
S/N Over All						
S/N		V_{IN_min} = 60dBµV, dev.= 40kHz,LP=15KHz deemphasis t = 50µs		66		dB

ELECTRICAL CHARACTERISTICS
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCMIX2}$ = 8.5V, f_{RF} = 1MHz, f_{MOD} = 400Hz at 30% AM f_{IF1} = 10.7MHz, f_{IF2} = 450kHz, f_{xtal} = 10.25MHz, in test or application circuit, (unless otherwise noted, V_{inRF} antenna input).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
AM SECTION						
Global						
V_{INRF} min	Max. sensitivity	Ref.: V_{INRF} = 74dBµV, ΔV_{37} = -10dB		19		dBµV
V_{INRF} us	Usable sensitivity	(S+N)/N = 20 dB	30	26		dBµV
ΔV_{INRF}	AGC Range	Ref.: V_{INRF} = 74dBµV, ΔV_{37} = -10dB	51			dB
(S+N)/N	Signal to Noise Ratio	Ref.: V_{INRF} = 74dBµV	49	56		dB

ELECTRICAL CHARACTERISTICS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCMIX2}$ = 8.5V, f_{RF} = 1MHz, f_{MOD} = 400Hz at 30% AMf_{IF1} = 10.7MHz, f_{IF2} = 450kHz, f_{xtal} = 10.25MHz, in test or application circuit, (unless otherwise noted, V_{inRF} antenna input).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
a_{IF}	IF rejection	Ref: V_{INRF} = 74dBµV, IF1 = 10.7MHz IF2 = 450kHz ΔV_{37} = -10dB	 100 100			 dB dB
a_{TW}	Tweet	C_{28} = 22µF	-3	-0.7		dB
f_{AF}	Frequency response	Ref.: V_{INRF} = 74dBµV, ΔV_{AF} = -3 dB		3.6		kHz
V_{INRFSS}	Seek Stop Sensitivity	AMSS	20	35	45	dBµV
THD	Total Harmonic Distortion	V_{INRF} = 74 dBµV, m = 0.8 m = 0.3 V_{INRF} = 120 dbµV, m = 0.8 m = 0.3		0.5 0.3 1.0 0.3		%
V_{37}	Output level	V_{INRF} = 74 dBµV		220		mV_{RMS}
V_{34}	Output level	V_{INRF} = 74 dBµ, m = 0.8		190		mV_{RMS}
V_3	Min. RF AGC threshold Max. RF AGC threshold	AMAGC Wide		82 98.8		dBµV dBµV
V_{58}	Min. IF AGC threshold Max. IF AGC threshold	AMAGC Middle		80.1 96.8		dBµV dBµV
V_3	Min. IF AGC threshold Max. IF AGC threshold	DAGC Narrow		32.6 80.7		dBµV dBµV
R_{63OUT}	Output impedance			100		kΩ
R_{40OUT}	Output impedance	AMSEEK = 0		150		kΩ
R_{40OUT}	Output impedance	AMSEEK = 1		5		kΩ
AGC Voltage Driver Output						
V_4	Max. AGC output voltage		3.5			V
V_4	Min. AGC output voltage				0.5	V
$\|I_4\|$	AGC current			100		µA
AGC PIN Diode Driver Output						
I_{64}	AGC driver current			1.5		mA
AM Mixer1 (10.7MHz)						
R_{IN}	Input impedance			1.2		kΩ
IP3	3rd order intercept point			140		dBµV
F	Noise figure			7		dB

ELECTRICAL CHARACTERISTICS (continued)
T_{amb} = +25°C, $V_{CC1} = V_{CC2} = V_{CC3} = V_{CCVCO} = V_{CCMIX1} = V_{CCMIX2}$ = 8.5V, f_{RF} = 1MHz, f_{MOD} = 400Hz at 30% AMf_{IF1} = 10.7MHz, f_{IF2} = 450kHz, f_{xtal} = 10.25MHz, in test or application circuit, (unless otherwise noted, V_{inRF} antenna input).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
A	Gain			6		dB
C_{min}	Min. capacitance step	IF1T		0.55		pF
C_{max}	Max. capacitance	IF1T		8.25		pF
C_{61-62}		IF1T		2		pF
AM Mixer2 (450kHz)						
R_{IN}	Input impedance	Dependent on application		5		kΩ
IP3	3rd order intercept point			110		dBµV
F	Noise figure			12		dB
A	Max. gain	Mixer2 tank output		15		dB
ΔA	Gain control range			20		dB
C_{min}	Min. cap step	IF2T		1.6		pF
C_{max}	Max. cap	IF2T		24		pF
C_{55-56}		IF2T		2		pF

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ADDITIONAL PARAMETERS						
Outputs of Tuning Voltage(TV1, TV2)						
V_{OUT}	Output voltage	TVR,TVO	1		VCC3-1V	V
R_{OUT}	Output impedance			20		kΩ
Xtal Reference Oscillator						
f_{LO}	Reference frequency	C_{Load} = 15pF		10.25		MHz
C_{Step}	Min. cap step	XTAL		0.6		pF
C_{max}	Max. cap	XTAL		19.4		pF
Δf/f	Freq. deviation versus VCC2	ΔV_{CC2} = 1V		1.5		ppm/V
Δf/f	Freq. deviation versus temp	-40°C < T < +85°C		0.2		ppm/K
I²C-Bus interface						
f_{SCL}	Clock frequency				400	kHz
V_{IL}	Input low voltage				1	V

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage		3			V
I_{IN}	Input current		-5		5	µA
V_O	Output voltage SDA acknowledge	I_O = 1.6mA			0.4	V
Loop Filter Input/Output						
$-I_{IN}$	Input leakage current	V_{IN} = GND, PD_{OUT} = Tristate	-0.1		0.1	µA
I_{IN}	Input leakage current	V_{IN} = VREF1 PD_{OUT} = Tristate	-0.1		0.1	µA
V_{OL}	Output voltage Low	I_{OUT} = -0.2mA		0.05	0.5	V
V_{OH}	Output voltage High	I_{OUT} = 0.2mA	VCC3 -0.5	VCC3 -0.05		V
I_{OUT}	Output current, sink	V_{OUT} = 1V to V_{CC3}-1V			10	mA
I_{OUT}	Output current, source	V_{OUT} = 1V to V_{CC3}-1V	-10			mA
Voltage Controlled Oscillator (VCO)						
f_{VCOmin}	Minimum VCO frequency		50			MHz
f_{VCOmax}	Maximum VCO frequency				200	MHz
C/N	Carrier to Noise	1KHz offset		85		dBc
SSTOP Output						
V_{24}	Output voltage low	I_{24} = -20µA			0.2	V
V_{24}	Output voltage high	I_{24} = 20µA	3			V
V_{46}	IF counter sensitivity	Antenna input		6		dBµV

1 FUNCTIONAL DESCRIPTION

1.1 FM Section

1.2 Mixer1, AGC and 1.IF

Mixer1 is a wide dynamic range stage with low noise and large input signal performance. The mixer1 tank can be adjusted by software (IF1T). The AGC operates on different sensitivities and bandwidths (FMAGC) in order to improve the input sensitivity and dynamic range (keying AGC). The output signals of AGC are controlled voltage and current for preamplifier and prestage pin diode attenuator. (look at Figure 4)

Two 10.7MHz programmable amplifiers (IFG1, IFG2) correct the IF ceramic insertion loss and the costumer level plan application.

1.3 Mixer2, Limiter and Demodulator

In this 2. mixer stage the first 10.7MHz IF is converted into the second 450kHz IF. A multi-stage limiter generates signals for the complete integrated demodulator without external tank. MPX output DC offset compensation is possible by software (DEM).

1.4 Quality Detection and ISS (look at Figure 2)

Fieldstrength

Parallel to mixer2 input a 10.7MHz limiter generates a signal for digital IF counter and a fieldstrength output signal. This internal unweighted fieldstrength is used for keying AGC, adjacent channel and multipath detection and is available at PIN14 (FSU) after +6dB buffer stage. The behaviour of this output signal can be corrected for DC offset (SL) and slope (SMSL). The internal generated unweighted fieldstrength is filtered at PIN35 and used for softmute function and generation of ISS filter switching signal for weak input level (sm).

Adjacent Channel Detector

The input of the adjacent channel detector is AC coupled from internal unweighted fieldstrength. A programmable highpass or bandpass (ACF) and amplifier (ACG) as well as rectifier determines the influences. This voltage is compared with adjustable comparator1 thresholds (ACWTH, ACNTH). The output signal of this comparator generates a DC level at PIN15 by programmable time constant. Time control (TISS) for a present adjacent channel is made by charge and discharge current after comparator1 in an external capacitance. The charge current is fixed and the discharge current is controlled by I^2C Bus. This level produces digital signals (ac, ac+) in an additional comparator4. The adjacent channel information is available as analog output signal after rectifier and +8dB output buffer.

Multipath Detector

The input of the multipath detector is AC coupled from internal unweighted fieldstrength. A programmable bandpass (MPF) and amplifier (MPG) as well as rectifier determines the influences. This voltage is compared with an adjustable comparator2 thresholds (MPTH). The output signal of this comparator2 is used for the "Milano" effect. In this case the adjacent channel detection is switched off. The "Milano" effect is selectable by I^2C Bus (MPOFF). The multipath information is available as analog output signal after rectifier and +8dB output buffer.

450kHz IF Narrow Bandpass Filter (ISS filter)

The device gets an additional second IF narrow bandpass filter for suppression noise and adjacent channel signal influences. This narrow filter has three switchable bandwidthes, narrow range of 80kHz, mid range of 120kHz and 30KHz for weather band information. Without ISS filter the IF bandwidth (wide range) is defined only by ceramic filter chain. The filter is switched in after mixer2 before 450kHz limiter stage. The centre frequency and matching to the demodulator center frequency can be fine adjusted (AISS) by software..

Deviation Detector

In order to avoid distortion in audio output signal the narrow ISS filter is switched OFF for present overdeviation.

Hence the demodulator output signal is detected. A lowpass filtering and peak rectifier generates a signal that is defined by software controlled current (TDEV) in an external capacitance. This value is compared with a programmable comparator3 thresholds (DWTH, DTH) and generates two digital signals (dev, dev+).

ISS Switch Logic

All digital signals coming from adjacent channel detector, deviation detector and softmute are acting via switching matrix on ISS filter switch. The IF bandpass switch mode is controlled by software (ISSON, ISS30, ISS80, ISSCTL). The switch ON of the IF bandpass is also available by manipulation of the voltage at PIN15. Two application modes are available (APPM). The conditions are described in table 37.

1.5 Soft Mute Control

The external fieldstrength signal at PIN 35 is the reference for mute control. The startpoint, mute depth and slope are programmable (SMTH, SMD, SLOPE) in a wide range. The time constant is defined by external capacitance. Additional adjacent channel mute function is supported. A highpass filter with -3dB threshold frequency of 100kHz, amplifier and peak rectifier generates an adjacent noise signal from MPX output with the same time constant for softmute. This value is compared with comparator5 thresholds (ACM). For present strong adjacent channel the MPX signal is attenuated typical 6dB.

1.6 AM Section

The upconversion mixer1 is combined with a gain control circuit 1 sensing three input signals, narrow band information at PIN 39, upconversion signal at PIN 58 and wide band information at PIN 3.This gain control circuit gives two output signals. The first one is a current for pin diode attenuator and the second one is a voltage for preamplifier. It is possible to put in a separate narrow bandpass filter before mixer2 at PIN 58. The intervention point for first AGC (AMAGC) is programmable by software.

The oscillator frequency for mixer1 is generated by dividing the FM VCO frequency (AMD).

In mixer2 the IF1 is downconverted into the IF2 450kHz. Before the output signal reaches the 450kHz tank an attenuator for IF gain control 2 is passed. Mixer1 and mixer2 tanks are software controlled adjustable (IF1T, IF2T).

After filtering by ceramic filter a 450kHz amplifier with a gain control 3 is included. The gain control 2 and 3 are the second AGC and programmable too by software (DAGC). In order to avoid an oscillation in intervention point it is important to know that the DAGC threshold has to be smaller than AMAGC! .

The demodulator is a peak detector. A further time constant with capacitor at pin40 produces a DC AGC reference voltage dependent on input signal. The time constant is switchable by ratio of 30. This is necessary for the station search function. The switching is software controlled (AMSEEK).

An internal comparator compares the AGC voltage with a programmable reference (AMSS). Consequently it is possible to generate a seekstop impulse over a defined range.

A separate output is available for AMIF stereo or a permanent seek stop signal(SSTSEL).

1.7 PLL and IF Counter Section

PLL Frequency Synthesizer Block

This part contains a frequency synthesizer and a loop filter for the radio tuning system. Only one VCO is required to build a complete PLL system for FM and AM upconversion. For auto search stop operation an IF counter system is available.

The counter works in a two stages configuration. The first stage is a swallow counter with a two modulus (32/33) precounter. The second stage is an 11-bit programmable counter.

The circuit receives the scaling factors for the programmable counters and the values of the reference frequencies via an I^2C-Bus interface.The reference frequency is generated by an adjustable internal (XTAL) oscillator followed by the reference divider. The reference and step-frequencies are free selectable (RC, PC).

Output signals of the phase detector are switching the programmable current sources. The loop filter integrates

their currents to a DC voltage.

The values of the current sources are programmable by 6 bits also received via the I^2C Bus (A, B, CURRH, LPF).

To minimize the noise induced by the digital part of the system, a special guard area is implemented.

The loop gain can be set for different conditions by setting the current values of the chargepump generator.

Frequency Generation for Phase Comparison

The RF signals applies a two modulus counter (32/33) pre-scaler, which is controlled by a 5-bit divider(A). The 5-bit register (PC0 to PC4) controls this divider. In parallel the output of the prescaler connects to an 11-bit divider(B). The 11-bit PC register (PC5 to PC15) controls this divider

Dividing range:

$f_{OSC} = (R+1) \times f_{REF}$

$f_{VCO} = [33 \times A + (B + 1 - A) \times 32] \times f_{REF}$

$f_{VCO} = (32 \times B + A + 32) \times f_{REF}$

Important: For correct operation: $A \leq 32$; $B \geq A$

Three State Phase Comparator

The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

Charge Pump Current Generator

This system generators signed pulses of current. The phase error signal decides the duration and polarity of those pulses. The current absolute values are programmable by A register for high current and B register for low current.

Inlock Detector

Switching the chargepump in low current mode can be done either via software or automatically by the inlock detector, by setting bit LDENA to "1"

After reaching a phase difference of 10 - 40nsec and a delay of some times $1/f_{REF}$, the chargepump is forced in low current mode. A new PLL divider alternation by I^2C-Bus will switch the chargepump in the high current mode.

Few programmable phase errors (D0, D1) are available for inlock detection

The count of detected inlock informations, to release the inlock signal is adjustable (D2, D3), to avoid a switching to low current during a frequency jump.

Low Noise CMOS Op-amp

An internal voltage divider at pin VREF2 connects the positive input of the low noise op-amp. The charge pump output connects the negative input. This internal amplifier in cooperation with external components can provide an active filter. The negative input is switchable to three input pins, to increase the flexibility in application. This feature allows two separate active filters for different applications.

A logical "0" in the LPF register activates PIN LPFM, otherwise PIN LPAM is active. While the high current mode is activated LPHC is switched on.

IF Counter Block

The input signal for FM and AM upconversion is the same 10.7MHz IF level after limiter. The grade of integration is adjustable by eight different measuring cycle times. The tolerance of the accepted count value is adjustable, to reach an optimum compromise for search speed and precision of the evaluation.

For the FM range the center frequency of the measured count value is adjustable in 32 steps, to get the possibility of fitting the IF-filter tolerance. In the AM upconversion range an IF frequency of 10.689MHz to 10.720MHz with 1kHz steps is available.

The IF-Counter Mode

The IF counter works in 2 modes controlled by IFCM register.

Sampling Timer

A sampling timer to generate the gate signal for the main counter is build with a 14-bit programmable counter (IRC). In FM mode a 6.25kHz, in AM mode a 1kHz basically signal is generated. This is followed by an asynchronous divider to generate several sampling times.

Intermediate Frequency Main Counter

This counter is a 11 - 21-bit synchronous autoreload down counter. Five bits (CF) are programmable to have the possibility for an adjust to the frequency of the IF-filter. The counter length is automatic adjusted to the chosen sampling time and the counter mode (FM, AM-UPC).

At the start the counter will be loaded with a defined value which is an equivalent to the divider value (t_{Sample} x f_{IF}).

If a correct frequency is applied to the IF counter frequency input at the end of the sampling time the main counter is changing its state from 0h to 1FFFFFh.

This is detected by a control logic and an external search stop output is changing from LOW to HIGH. The frequency range inside which a successful count result is adjustable by the EW bits.

$t_{TIM} = (IRC + 1) / f_{OSC}$

$t_{CNT} = (CF + 1697) / f_{IF}$ FM mode

$t_{CNT} = (CF + 10689) / f_{IF}$ AM up conversion mode

Counter result succeeded:

$t_{TIM} \geq t_{CNT} - t_{ERR}$

$t_{TIM} \leq t_{CNT} + t_{ERR}$

Counter result failed:

$t_{TIM} > t_{CNT} + t_{ERR}$

$t_{TIM} < t_{CNT} - t_{ERR}$

t_{TIM} = IF timer cycle time
t_{CNT} = IF counter cycle time
t_{ERR} = discrimination window (controlled by the EW registers)

The IF counter is only started by inlock information from the PLL part. It is enabled by software (IFENA).

Adjustment of the Measurement Sequence Time

The precision of the measurements is adjustable by controlling the discrimination window. This is adjustable by programming the control registers EW0 to EW2.

The measurement time per cycle is adjustable by setting the Register IFS0 - IFS2.

Adjust of the Frequency Value

The center frequency of the discrimination window is adjustable by the control register CF0 to CF4.

1.8 I²C-Bus Interface

The TDA 7511 supports the I²C-Bus protocol. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and device being controlled is the slave. The master will always initiate data transfer and provide the clock to transmit or receive operations.

Data Transition

Data transition on the SDA line must only occur when the clock SCL is LOW. SDA transitions while SCL is HIGH will be interpreted as START or STOP condition.

Start Condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This "START" condition must precede any command and initiate a data transfer onto the bus. The TDA 7511 continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

Stop Condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus-interface of the TDA 7511 into the initial condition.

Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it receive the eight bits of data.

Data Transfer

During data transfer the TDA 7511 samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

Device Addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device it is addressing.

The most significant 6 bits of the slave address are the device type identifier.

The TDA 7511 device type is fixed as "110001".

The next significant bit is used to address a particular device of the previous defined type connected to the bus.

The state of the hardwired PIN 41 defines the state of this address bit. So up to two devices could be connected on the same bus. When PIN 41 is connected to VCC2 the address bit “1” is selected. In this case the AM part doesn’t work. Otherwise the address bit “0” is selected (FM and AM is working). Therefor a double FM tuner concept is possible.

The last bit of the start instruction defines the type of operation to be performed:

- When set to "1", a read operation is selected
- When set to "0", a write operation is selected

The TDA 7511 connected to the bus will compare their own hardwired address with the slave address being transmitted, after detecting a START condition. After this comparison, the TDA 7511 will generate an "acknowledge" on the SDA line and will do either a read or a write operation according to the state of R/W bit.

Write Operation

Following a START condition the master sends a slave address word with the R/W bit set to "0". The TDA 7511 will generate an "acknowledge" after this first transmission and will wait for a second word (the word address field). This 8-bit address field provides an access to any of the 32 internal addresses. Upon receipt of the word address the TDA 7511 slave device will respond with an "acknowledge". At this time, all the following words transmitted to the TDA 7511 will be considered as Data. The internal address will be automatically incremented. After each word receipt the TDA 7511 will answer with an "acknowledge".

Read Operation

IF the master sends a slave address word with the R/W bit set to "1", the TDA 7511 will transit one 8-bit data word. This data word includes the following informations:

bit0 (ISS filter, 1 = ON, 0 = OFF)

bit1 (ISS filter bandwidth, 1 = 80kHz, 0 = 120kHz)

bit2 (MPOUT,1 = multipath present, 0 = no multipath)

bit3 (1 = PLL is locked in , 0 = PLL is locked out).

bit4 (fieldstrength indicator, 1 = lower as softmute threshold, 0 = higher as softmute threshold)

bit5 (adjacent channel indicator, 1 = adjacent channel present, 0 = no adjacent channel)

bit6 (deviation indicator, 1 = strong overdeviation present, 0 = no strong overdeviation)

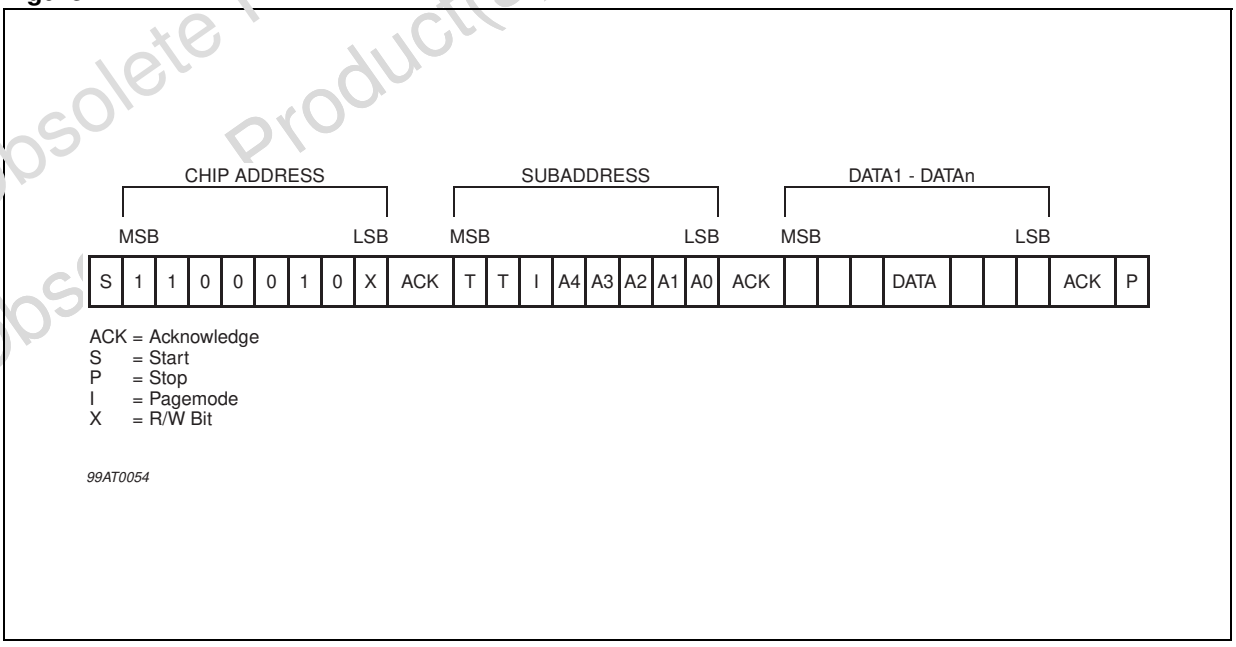
bit7 (deviation indicator, 1 = overdeviation present, 0 = no overdeviation)

2 Software Specification

The interface protocol comprises:

- start condition (S)
- chip address byte
- subaddress byte
- sequence of data (N bytes + Acknowledge)
- stop condition (P)

Figure 1.



2.1 Address Organization

Table 1.

Function	Addr	7	6	5	4	3	2	1	0
CHARGEPUMP	0	LPF	CURRH	B1	B0	A3	A2	A1	A0
LOCKDET	1	LDENA	D3	D2	D1	D0	AMON	TEST3	RES2
PLL COUNTER	2	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
	3	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
PLL REF COUNTER	4	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
	5	RC15	RC14	RC13	RC12	RC11	RC10	RC9	RC8
TV1	6	TV011	TV010	TVR15	TVR14	TVR13	TVR12	TVR11	TVR10
TV2	7	TV021	TV020	TVR25	TVR24	TVR23	TVR22	TVR21	TVR20
IFC CTRL 1	8	TV013	TV012	TV023	TV022	IFENA	EW2	EW1	EW0
IFC CTRL 2	9	IFS2	IFS1	IFS0	CF4	CF3	CF2	CF1	CF0
IF REF CNT1	10	IRC7	IRC6	IRC5	IRC4	IRC3	IRC2	IRC1	IRC0
IF REF CNT2	11	IFCM1	IFCM0	IRC13	IRC12	IRC11	IRC10	IRC9	IRC8
IF1/FMAGC	12	-	FMAGC2	FMAGC1	FMAGC0	IFG21	IFG20	IFG11	IFG10
DEM ADJ	13	DNB1	DNB0	DEM5	DEM4	DEM3	DEM2	DEM1	DEM0
QUALITY AC	14	ACNTH1	ACNTH0	ACWTH2	ACWTH1	ACWTH0	ACG	ACF	ISS30
QUALITY MP	15	MPAC	APPM2	APPM1	MPTH1	MPTH0	MPG	MPF	MPOFF
QUALITYDEV	16	-	DTH1	DTH0	DWTH1	DWTH0	TDEV2	TDEV1	TDEV0
QUALITYISS	17	AISS1	AISS0	TISS2	TISS1	TISS0	ISS80	ISSON	ISSCTL
AM CTL1	18	DAGC3	DAGC2	DAGC1	DAGC0	AMD1	AMD0	AMST	AMSEEK
AM CTL2	19	AMSS3	AMSS2	AMSS1	AMSS0	AMAGC3	AMAGC2	AMAGC1	AMAGC0
MUTE1	20	SMCTH1	SMCTH0	SLOPE	MENA	SMD3	SMD2	SMD1	SMD0
MUTE2	21	ACM3	ACM2	ACM1	ACM0	SMTH3	SMTH2	SMTH1	SMTH0
SLIDER	22	-	-	SL5	SL4	SL3	SL2	SL1	SL0
TANK ADJ	23	IF1T3	IF1T2	IF1T1	IF1T0	IF2T3	IF2T2	IF2T1	IF2T0
XTAL ADJ	24	-	-	CLKSEP	XTAL4	XTAL3	XTAL2	XTAL1	XTAL0
TESTCNTRL	25	ISSIN	SMSL	SSTSEL	ISSCOFF	DEMOFF	450LOFF	TESTOUT	TESTIN
TEST	26	-	-	-	-	-	DIV2	DIV1	DIV0
TEST MODE1	27	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
TEST MODE2	28	-	-	TINMP	TINAC	OUT11	OUT10	OUT9	OUT8

2.2 Control Register Function

Table 2.

Register Name	Function
A	Charge pump high current
ACF	Adjacent channel filter select
ACG	Adjacent channel filter gain
ACM	Threshold for startpoint adjacent channel mute
ACNTH	Adjacent channel narrow band threshold
ACWTH	Adjacent channel wide band threshold
AISS	ISS filter fine adjust

Table 2. (continued)

Register Name	Function
AMAGC	AM wide band AGC threshold
AMD	AM prescaler
AMON	AM-FM switch
AMSEEK	Switch time constant for AM seek
AMSS	AM seek stop threshold
AMST	AM stereo select
APPM	Application mode quality detection
B	Charge pump low current
CF	Center frequency IF counter
CLKSEP	Clock separation (only for testing)
CURRH	Set current high charge pump
D	Inlock phase error and delay time for lock detector
DAGC	AM narrow band AGC threshold
DEM	Demodulator offset
DEMOFF	Demodulator clock “OFF” (only for testing)
DNB	Demodulator noise blanking
DIV	Divider ratio for reference frequency (only for testing)
DTH	Deviation detector threshold for ISS filter “OFF”
DWTH	Deviation detector threshold for ISS filter narrow/wide
EW	Frequency error window IF counter
FMAGC	FM AGC threshold
IF1T	FM/AM mixer1 tank adjust
IF2T	AM mixer2 tank adjust
IFCM	IF counter mode
IFENA	IF counter enable
IFG	IF amplifier gain (10.7MHz)
IFS	IF counter sampling time
IRC	IF reference counter
ISSCOFF	ISS filter clock “OFF” (only for testing)
ISSCTL	ISS filter control
ISSIN	Test input for ISS filter
ISSON	ISS filter “ON”
ISS30	ISS filter 30KHz weather band
ISS80	ISS filter narrow/mid switch
LDENA	Lock detector enable
LPF	Loop filter input select
MENA	Softmute enable
MPAC	Adjacent channel control by multipath
MPOFF	Multipath control “OFF”
MPF	Multipath filter frequency
MPG	Multipath filter gain
MPTH	Multipath threshold
OUT	Test output (only for testing)

Table 2. (continued)

Register Name	Function
PC	Counter for PLL (VCO frequency)
RC	Reference counter PLL
RES	Reservation
SL	S meter slider threshold
SLOPE	Softmute slope select
SMCTH	Softmute capacitor threshold for ISS “ON”
SMD	Softmute depth threshold
SMSL	S meter slope
SMTH	Softmute startpoint threshold
SSTSEL	Search stop select for continuous signal
TEST3	Testing PLL/IFC (only for testing)
TESTOUT	Switch FSW output to TEST output (only for testing)
TESTIN	Switch FSU input to TEST input (only for testing)
TDEV	Time constant for deviation detector
TINAC	Test input adjacent channel (only for testing)
TINMP	Test input multipath(only for testing)
TISS	Time constant for ISS filter “ON”/”OFF”
TVR	Tuning voltage for prestage proportional referred to PLL
TVO	Tuning voltage offset for prestage
XTAL	Xtal frequency adjust
450LOFF	450kHz limiter “OFF” (only for testing)

Subaddress

Table 3.

MSB							LSB	Function
T2	T1	I	A4	A3	A2	A1	A0	
			0	0	0	0	0	Charge pump control
			0	0	0	0	1	PLL lock detector
			-	-	-	-	-	-
			1	1	1	0	0	Test mode 2
		0						Page mode “OFF”
		1						Page mode enable

Note: 1. T1, T2 used for testing, in application mode they have to be "0".

2.3 Data Byte Specification

Addr 0 Charge Pump Control

Table 4.

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1mA
				0	0	1	1	High current = 1.5mA
				-	-	-	-	-
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0µA
		0	1					Low current = 50µA
		1	0					Low current = 100µA
		1	1					Low current = 150µA
	0							Select low current
	1							Select high current
0								Select LPFM
1								Select LPAM

Addr 1 PLL Lock Detector

Table 5.

MSB							LSB	Function	
d7	d6	d5	d4	d3	d2	d1	d0		
						0	0	Not used, have to be 0, d1 only for testing	
					0			Select FM mode	
					1			Select AM mode	
			0	0				PD phase difference threshold	10ns
			0	1					20ns
			1	0					30ns
			1	1					40ns
	0	0						Not valid	
	0	1						Activation delay	4 x $1/f_{REF}$
	1	0							6 x $1/f_{REF}$
	1	1							8 x $1/f_{REF}$
0								Lock detector doesn't control charge pump	
1								Lock detector controls charge pump	

Addr 2 PLL Counter 1 (LSB)

Table 6.

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Addr 3 PLL Counter 2 (MSB)

Table 7.

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536

Note: 1. Swallow mode: f_{VCO}/f_{SYN} = LSB + MSB + 32

Addr 4 PLL Reference Counter 1 (LSB)

Table 8.

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

Addr 5 PLL Reference Counter 2 (MSB)

Table 9.

MSB							LSB	Function
d7	d6	d5	d4	d3	d2	d1	d0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536

Note: 1. f_{OSC}/f_{REF} = LSB + MSB + 1

Addr 6, Addr7, Addr 8 TV1,2 (proportional and offset control referred to tuning voltage V28)

Table 10.

addr8		addr6								Function TV1
d7	d6	d7	d6	d5	d4	d3	d2	d1	d0	
addr8		addr7								Function TV2
d5	d4	d7	d6	d5	d4	d3	d2	d1	d0	
				0	0	0	0	0	0	TVR = 0
				0	0	0	0	0	1	TVR = -1
				0	0	0	0	1	0	TVR = -2
-	-	-	-	-	-	-			-	-
				0	1	1	1	1	1	TVR = -31
				1	0	0	0	0	1	TVR = +1
				1	0	0	0	1	0	TVR = +2
-	-	-	-	-	-	-	-	-	-	-
				1	1	1	1	1	1	TVR = +31
0	0	0	0							TVO = 0
0	0	0	1							TVO = -1
0	0	1	0							TVO = -2
-	-	-	-	-	-	-	-	-	-	-
0	1	1	1							TVO = -7
1	0	0	1							TVO = +1
1	0	1	0							TVO = +2
-	-	-	-	-		-	-	-	-	-
1	1	1	1							TVO = +7

Note: 1. TV1,2 = V28 + V28 * TVR/128 + TVO * 50mV
TVR: -31, -30, ... 0 ... 30, 31
TVO: -7, -6, ... 0 ... 6, 7