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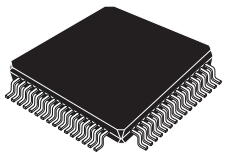
TDA7529

RF front-end for AM/FM DSP car-radio with IF sampling

Features

- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- I/Q mixer for FM IF 10.7 MHz with image rejection and integrated LNA
- I/Q mixer for AM IF 10.7 MHz up conversion with high dynamic range
- Integrated balun, which allows saving of external mixer tank
- RF AGC, IF AGC, DAGC
- Low noise IF amplifier with switched wide dynamic AGC range
- IF switch for FM / AM / IBOC
- Electronic alignment for the preselection stages
- I^2C/SPI controlled
- Single 5 V supply
- Alternative frequency control signals to DSP



LQFP64

Description

The front-end is a high performance tuner circuit for AM/FM - DSP car radios with 10.7 MHz IF sampling. It contains mixer and IF amplifiers for AM and FM, fully integrated VCO and PLL synthesizer on a single chip. Use of BiCMOS technology allows the implementation of several tuning functions and a minimum of external components.

Table 1. Device summary

Order code	Package	Packing
TDA7529	LQFP64 exposed pad (10x10x1.4)	Tray
TDA7529TR	LQFP64 exposed pad (10x10x1.4)	Tape and reel

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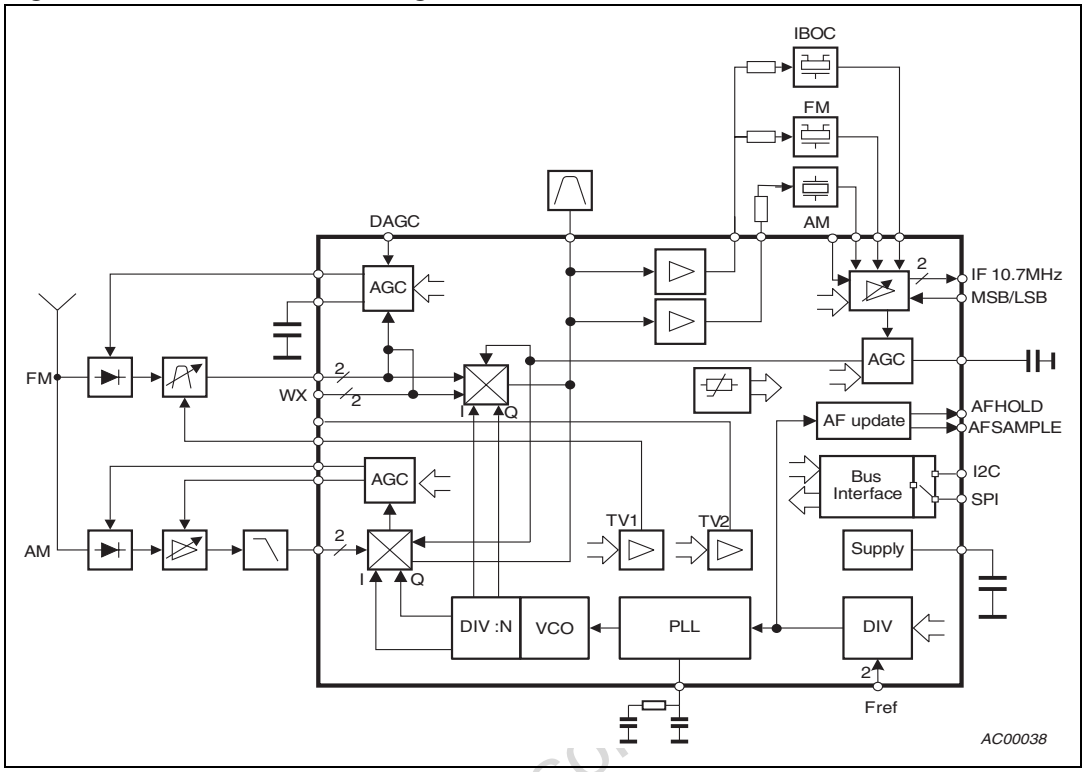
1 Functional block diagram

Figure 1. Functional block diagram



2 Pin description

Figure 2. Pin connection

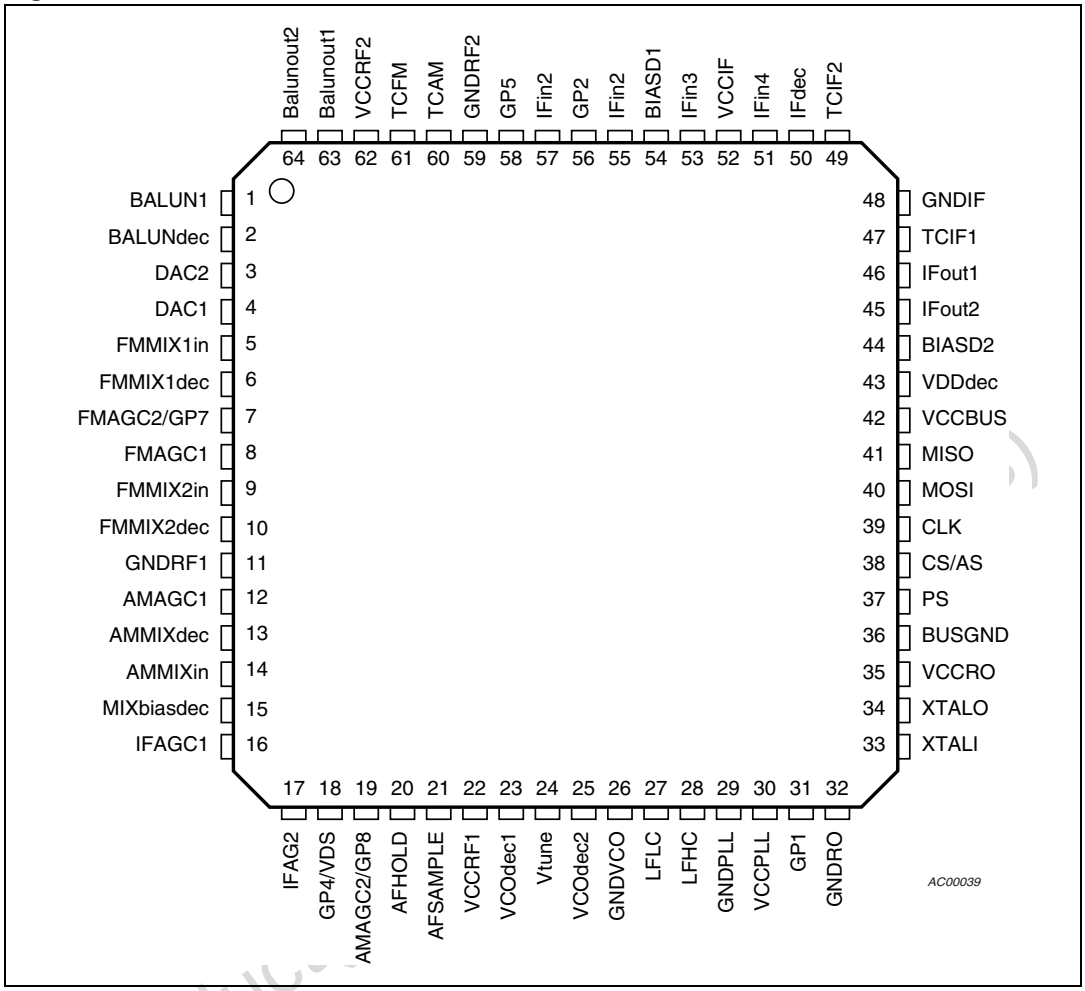


Table 2. Pin assignment

Pin #	Pin Name	Description
1	BALUN1	Active balun input 1
2	BALUNdec	Active balun input 2 (de coupling)
3	DAC2	Tuning DAC 2 output
4	DAC1	Tuning DAC 1 output
5	FMMIX1in	FM mixer input – high gain stage = mode 1
6	FMMIX1dec	FM mixer de couple
7	FMAGC2/GP7	FM AGC voltage output / alternative GP7 output
8	FMAGC1	FM PIN diode driver output
9	FMMIX2in	FM Mixer input – low gain stage = mode2

Table 2. Pin assignment (continued)

Pin #	Pin Name	Description
10	FMMIX2dec	FM Mixer de couple
11	GNDRF1	GND RF1 section
12	AMAGC1	AMAGC PIN diode driver output
13	AMMIXdec	AM mixer de couple
14	AMMIXin	AM mixer input
15	MIXbiasdec	Mixer bias de coupling
16	IFAGC1	IFAMP gain control via IFAGC - LSB
17	IFAGC2	IFAMP gain control via IFAGC - MSB
18	GP4/VDS	GPIO 4 / VDS input
19	AMAGC2 / GP8	AMAGC voltage output / alternative GP8 output
20	AFHOLD	AF state machine hold output
21	AFSAMPLE	AF state machine sample output
22	VCCRF1	Supply RF1 section
23	VCOdec1	BIAS de couple for VCO
24	Vtune	VCO tuning voltage
25	VCOdec2	BIAS de couple for VCO
26	GNDVCO	VCO Ground
27	LFLC	Loop filter low current output
28	LFHC	Loop filter high current output
29	GNDPLL	PLL Ground
30	VCCPLL	Supply PLL
31	GP1	GPIO 1
32	GNDRO	Ground PLL digital part
33	XTALI	Reference oscillator input
34	XTALO	Reference oscillator output
35	VCCRO	Supply PLL digital part
36	BUSGND	BUSinterface Ground
37	PS	Protocol Select
38	CS/AS	Chip select / Address select
39	CLK	SPI / I2C clodk
40	MOSI	SPIdata input / I2C Data
41	MISO	SPI Data Output
42	VCCBUS	Supply of BUSinterface
43	VDDdec	De couple of internal 3.3V (=3,3V + Vbe)

Table 2. Pin assignment (continued)

Pin #	Pin Name	Description
44	BIASD2	De coupling for Biasing
45	IFout2	Differential IF output 2
46	IFout1	Differential IF output 1
47	TCIF1	time constant IF AGC for AM
48	GNDIF	ground IF section
49	TCIF2	time constant IF AGC for FM
50	IFdec	De couple of IF amplifier
51	IFin4	IF input 4
52	VCCIF	Supply IF section
53	IFin3	IF input 3
54	BIASD1	De coupling for Biasing
55	IFin2	IF input 2
56	GP2	GPIO 2
57	IFin1	IF input 1
58	GP5	GPIO 5
59	GNDRF2	GND RF2 section = active balun GND
60	TCAM	AM AGC time constant
61	TCFM	FM AGC time constant
62	VCCRF2	Supply voltage RF2 section
63	Balunout1	Active balun output 2 = FM output
64	Balunout2	Active balun output 1 = AM output

3 Function description

3.1 IMR mixer and active balun output

The IMR mixer has two FM inputs (referred as mode 1 / mode 2) and one AM input selectable by software. The FM inputs differ by their gains, noise figures, IIP3 and maximum signal handling capability. The mode 1 FM input (with the higher gain, lower IIP3 and lower noise figure) is normally coupled with passive antenna input stages; the mode 2 FM input is normally used for input stages featuring an external preamplifier.

There are two single ended outputs of the IMR mixer: Balunout1 has a 4 dB higher gain than Balunout2. It is not recommended to use both outputs in parallel.

The Balun1 pin is the current mixer output over an internal resistor. The LC filter at Balun1 can be realized with a low cost SMD-coil (Q ~ 4).

3.2 FM RF-AGC

The FM AGC system is controlled by a peak detector, whose gain can be varied by the keyed AGC. The latter function is meant to be controlled by a D/A converter in the back-end part of the system.

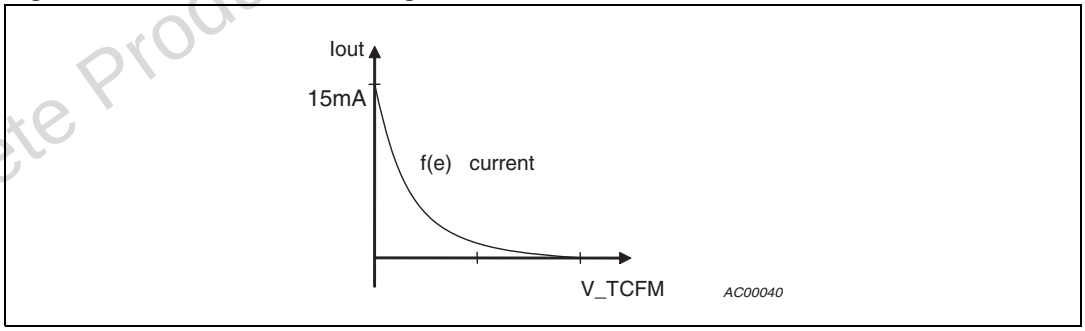
The time constant of the FM RF-AGC is defined by an external capacitor connected to TCFM and programmable internal currents. The currents can be selected independently for AGC attack and decay. By this the ratio between the attack and the decay time can be programmed between 0.4 and 250.

The FM RF-AGC has two output pins to drive one PIN diode attenuator and the external preamplifier gain control.

The AGC outputs can be programmed to the following modes:

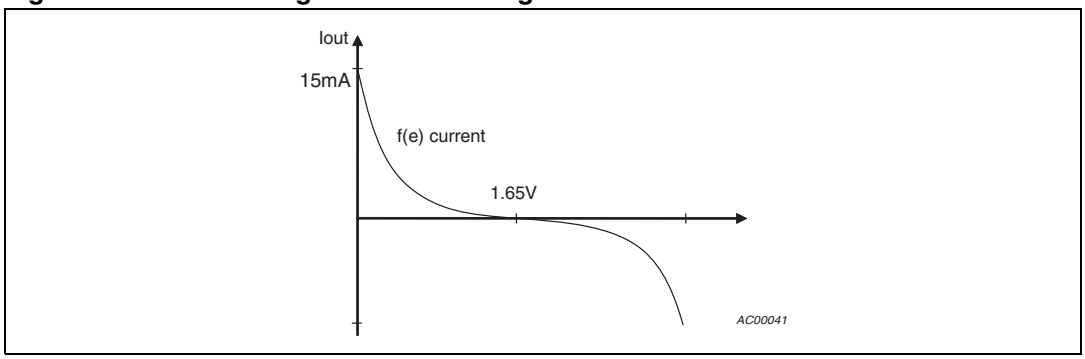
1. Positive current I=f(e): after reaching the AGC threshold voltage, the current output delivers a current I=f(e) up to 15mA in a voltage range from 0.1V (@10µA sink current) up to V_{CC}-1.2V with a quasi-exponential characteristic referred to the voltage at TCFM.

Figure 3. Positive current diagram



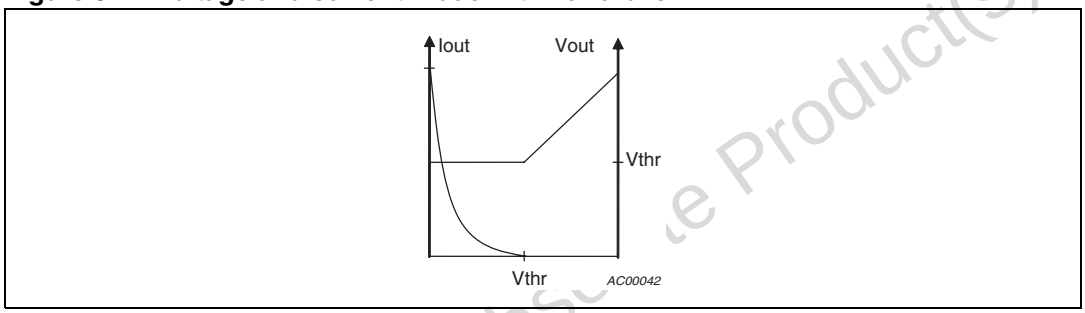
2. Pos/neg current I = f(e): below the AGC threshold voltage the AGC output sinks a constant current of -5 mA. When the RF input level crosses the AGC threshold voltage, the current is reduced down to 0 mA with a quasi-logarithmic behavior. At half control voltage the current becomes positive and reaches up to 15mA following an exponential function.

Figure 4. Positive/negative current diagram



3. Constant current mode: the output current can be set to 2 mA source current. The AGC detector is in power -down mode and only the PIN diode driver is active.
4. Voltage and current mode with hand-over: the Vthr level is programmable with 6 bit in the range of 0.2V to 2.56V. The voltage Vthr is the internal reference voltage of an external cascode transistor emitter feedback loop.

Figure 5. Voltage and current mode with hand-over



The voltage output swing is comprised between 0V and 3.3V (VDD).

The microcontroller can read the voltage at the AGC capacitor via the serial control interface.

3.3 AM RF-AGC

The AM AGC system is controlled by an average detector. The time constant of the AM RF-AGC is defined by an external capacitor connected to TCAM and programmable internal currents with symmetrical attack/decay behavior.

The AM RF-AGC has two output pins to drive one PIN diode attenuator and the external preamplifier gain control.

The AGC outputs can be programmed to the same modes as the FM RF-AGC with the exception of pos/neg current.

The microcontroller can read the voltage at the AGC capacitor via the serial control interface.

3.4 IF AGC and IF amplifier

The IF AGC system is controlled in AM with an average detector and in FM with a peak detector, and reduces the mixer gain. The time constant is defined by two external capacitors connected to TCIF1 and TCIF2 respectively, and programmable internal currents.

The microcontroller can read the voltage at the AGC capacitors via the serial control interface.

The IF amplifier gain is not affected by the on-chip IF-AGC but is meant to be controlled by the back-end part of the system through pins IFAGC1 and IFAGC2. The gain is reduced in 6 dB steps starting from the programmed value "G" according to the following table:

Table 3. IF AGC and IF amplifier

IFAGC2	IFAGC1	Gain
0	0	G
0	1	G - 6 dB
1	1	G - 12 dB
1	0	G - 18 dB

3.5 Dividers

The mixer divider V is followed by a divide-by-4-stage that generates 0°/90°/-90° LO signals for the IMR mixer (90°/-90° mode to switch between upper or lower side-band suppression in the IMR mixer).
The main divider N can be operated in integer mode.

3.6 D/A converters

The front-end contains two D/A-converters for tuning the filters of the FM pre-stage. The converters have a resolution of 9 bit.

3.7 VCO

The 3.7 GHz VCO has an internal switch that allows extending the oscillation frequency range. This is required by the fact that each of the two resulting VCO sub-bands (upper/lower) cannot individually cover the complete required frequency range versus temperature and process; for this reason a calibration procedure is needed to determine the process type (typical, slow, fast) and select the transition frequency between the two VCO sub-bands.

To run the procedure the VCO range 2 must be selected, the synthesized frequency needs to be set to 4GHz; then if Vtuning > 2.6V then the process is 'slow', if Vtuning < 1.7V then is 'fast' and otherwise is 'typical'. The switching frequency as a function of the process is reported in the following table:

Table 4. Switching frequency as a function of the process

Slow	Typ.	Fast
3.635 GHz	3.72 GHz	3.794 GHz

3.8 FREF

The reference frequency for the PLL can be derived by a XTAL directly connected to the device or by means of an LVDS signal. In the latter case an external matching resistor must be used to obtain the desired input signal level.

3.9 A/D converter

The front-end contains a 6 bit SAR A/D-converter for sensing several analog values of the tuner. The following analog sources can be switched to the ADC input by software command:

- FM RF AGC capacitor voltage
- AM RF AGC capacitor voltage
- IF AGC capacitor voltage (automatically connected to the FM or AM IF AGC filtering capacitor)
- PLL tuning voltage
- Temperature sensor
- GPIO 1 voltage
- GPIO 2 voltage
- ADC reference generated from VCC.

The ADC can be clocked by an integrated RC-oscillator, in which case the oscillation frequency is programmable, or by the PLL reference frequency.

3.10 GPIO - general purpose IO interface pins

The front-end has seven GPIO - general purpose control pins to switch external stages (output), e.g amplifiers, or to read the status of external stages (input), e.g. control voltages. Some control pins are multiplexed with other functions that are not necessary in every tuner design (FM AGC keying, AM cascode control). All the GPIOs may put in tristate or in enable mode. When in enable the GPIOs can be configured as shown in the following table.

All GPIOs are short-circuit protected by current limiter and voltage-tolerant up to 3.5 V.

Table 5. GPIO - general purpose IO interface pins

GPIO ports	Function	Note
GPIO1	Selects function of GPIO1: if input, connects GPIO1 to ADC (ADC must then be configured to use GPIO1 as input); if output, level depends on GPIO Out Lev Ctrl → GPIO1	– AnlgIn to AD – DigOut
GPIO2	Selects function of GPIO2: if input, connects GPIO2 to ADC (ADC must then be configured to use GPIO2 as input) and to KAGC (FM KAGC must then be enabled); if output, level depends on GPIO Out Lev Ctr → GPIO2	– AnlgIn to AD – Kagc In – DigOut
GPIO4	Selects function of GPIO4: if input, configures GPIO4 as AM Cascode V_{DS} input; if output, level depends on GPIO Out Lev Ctrl → GPIO4	– AnlgIn – DigOut
GPIO5	Selects function of GPIO5: if input, it is directly connected to read-only register byte 48 bit 4; if output, level depends on GPIO Out Lev Ctrl → GPIO5. When set to input, it is necessary to set IF AMP → GPIO5 out mode to “ON GPIO5 out En” (labels are wrong). Also used for production testing as analog output (not relevant for application).	– DigIn – Out (Dig or Anlg)
GPIO6	Selects function of GPIO6 if device is configured in I^2C mode: if input, it is directly connected to read-only register byte 48 bit 5; if output, level depends on GPIO Out Lev Ctrl → GPIO5. When the device is configured in SPI mode, program GPIO Out Lev Ctr → GPIO5 to “Low”. The value of GPIO mode → GPIO5 does not matter	– Din (spi MISO out) – Dout (spi MISO out)
GPIO7	Selects function of GPIO7: if digital output is selected, level depends on GPIO Out Lev Ctrl → GPIO7; otherwise, configures GPIO7 as FM AGC Vout	– Digital Out – FM agc Vout
GPIO8	Selects function of GPIO8: if output, level depends on GPIO Out Lev Ctrl → GPIO8; otherwise, configures GPIO8 as AM AGC Vout	– Digital Out – AM agc Vout

3.11 AFSAMPLE/AFHOLD

On the TDA7529 there are two dedicated open drain pins (AFSAMPLE and AFHOLD), that allow the control of the DSP (mute and quality controls) during AF update.

Details are given in *Chapter 5*.

3.12 Serial bus interface

The TDA7529 has a serial data port for communication with the microcontroller. It is used for programming the device and for reading out its detectors. This port supports data communication using the SPI and the I^2C protocol. The data transfer of several consecutive bytes is supported by the auto increment feature.

Table 6. Supports data communication using the SPI and the I^2C protocol

Name	Pin	SPI signal	Pin	I^2C signal
Signal 1	PS	Protocol Select SPI/I^2C	PS	Protocol Select SPI/I^2C
Signal 2	CS	Chip Select	AS	Address Select
Signal 3	CLK	Clock	CLK	Clock
Signal 4	MOSI	Master Out – Slave In	DATA	bidirectional Data
Signal 5	MISO	Master In – Slave Out	GP6	General Purpose Out

The "PS"- pin (protocol select) determines which communication protocol is used. The information is not latched, so any level change at this pin immediately affects the protocol used by the TDA7529.

The SPI protocol is selected by setting PS = 0 while, during the I^2C operation, PS needs to be open (internally set to 1).

SPI-Protocol: CPOL=1, CPHA=1.

The CS pin performs the Chip Select function during the SPI operation; it has to be reset to 0 during transmission or reception, otherwise set to 1 (the CS pin is set to 1 by leaving it open).

Both the CS and the AS functions are performed by the CS pin.

When the I^2C mode is used, the "AS" pin determines which I^2C address or group of addresses (see below) is used. Three different external connections are defined to represent three groups of addresses (refer to the following table for details). The information is not latched, so any level change at this pin immediately affects the address used by the TDA7529.

First the IC address is transmitted including the R/W bit for setting the direction of the following data transfer

Table 7. I²C addresses

Tuner:	Tuner 3	Tuner 2	Tuner 1
level at pin AS	2.2V – 3.5V	1.1V – 1.7V	0.0V – 0.6V
address:	1100 1xxd	1100 x1xd	1100 xx1d
MSB ... LSB	-	-	-
1100 000d	-	-	-
1100 001d	-	-	R / W
1100 010d	-	R / W	-
1100 011d	-	W	W
1100 100d	R / W	-	-
1100 101d	W	-	W
1100 110d	W	W	-
1100 111d	W	W	W

x = must be "0" for reading, can be "1" or "0" for writing to the TDA7529

d = determinates the direction of data transfer, reading or writing

R / W = indicates the address to read to and/or to write from a single TDA7529

W = indicates those addresses that can be used to transmit equal data to several TDA7529 frontends. A read out has no purpose for these addresses (data collision), but must be possible without damaging the tuner IC.

The two serial bus protocols, I²C and SPI, are as follows:

Figure 6. I²C (sub address mode)

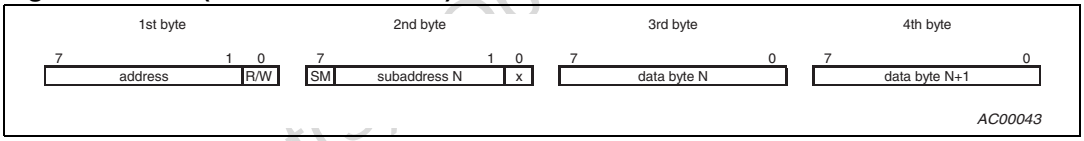
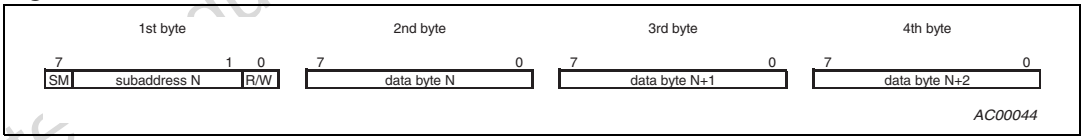


Figure 7. SPI



Data auto increment mode is always active regardless of the serial bus mode chosen.

4 Electrical specifications

Electrical parameters are guaranteed if F_{ref} = 100kHz, with frequency stability of +/- 20ppm max.

4.1 Absolute maximum ratings

Table 8. Absolute maximum ratings

Symbol	Parameter	Test condition	Min	Typ	Max	Units
V_{CC}	Abs. supply voltage	-	-	-	5.5	V
T_{amb}	Ambient temperature range	-	-40	-	105	°C
T_{stg}	Storage temperature	-	-55	-	150	°C
T_j	Junction temperature	-	-	-	150	°C

4.2 Thermal data

Table 9. Thermal data

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
$R_{thj-amb}$	Thermal resistance junction to ambient	2s2p std Jedec board with thermal via underneath the component (36 board via: diameter = 0.5mm / pitch = 1.5mm), max 30% missing soldering	-	-	33	°C/W

4.3 General key parameters

Table 10. General key parameters

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
V_{CC}	5V supply voltage	-	4.7	5	5.35	V
I_{CC}	Supply current @ 5V	-	-	145	175	mA
I_{CC_pwd}	Supply current @ 5V in power down mode	-	-	9	14	mA
T_{amb}	Ambient temperature range	-	-40	-	105	°C

4.4 FM - section

Refer to application circuit in figure 3. V_{CC} = 4.7V to 5.35V; T_{amb} = -40 to +105°C; f_c = 76 to 108 MHz; 60dBµV antenna level; mono signal, unless otherwise specified. Antenna level equivalence: 0dBµV = 1µV_{rms}, all RF levels are intended as PD.

Table 11. FM - section

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
FM IMR Mixer and active balun						
G_{mix1}	Mixer conversion gain	mode 1 (unloaded)	20	22	24	dB
		mode 2 (unloaded)	14	16	18	
-	Gain attenuation range	controlled by IF-AGC	18	20	-	dB
R_{in}	Input impedance	mode 1	30	50	-	kΩ
		mode 2	5	6.5	9.5	
R_{out}	Output impedance	active balun	15	20	30	Ω
V_{out_max}	Max. output voltage	without clipping (unloaded)	122	-	-	dBµV
v_{noise}	Input noise voltage	Mode1, Rsource=1.5kΩ, noiseless	-	3	3.7	nV/√Hz
		Mode 2, Rsource=800, noiseless	-	5	6	
IIP3	3rd order intercept point(1)	mode 1 up to Vin/tone = 90 dBµV	123	125	-	dBµV
		mode 2 up to Vin/tone = 98 dBµV	132	134		
IIP2	2nd order intercept point	mode 1	144	-	-	dBµV
		mode 2	152			
IRR	Image rejection ratio	without gain/phase adjust	30	-	-	dB
		with gain/phase adjust	40	45	-	
FM RF AGC						
L_{thr}	Mixer input referred RF level threshold	mode 1, min. setting	82	85	88	dBµV
		mode 1, max setting	97	100	103	
		mode 2, min. setting	90	93	96	
		mode 2, max setting	105	108	111	
-	Threshold steps	4 bit control	0.5	1	1.5	dB
-	Pin diode source current	AGC control pin 1 Logarithmic current	10	-	-	mA
-	Pin diode sink current	AGC control pin 1 Logarithmic current	-	-	-3	mA
-	Pin diode source current in constant current mode	-	1	2	-	mA
-	Threshold shift keyed AGC	Control input = 1V	10.5	12.5	13.5	dB/V

1. parameter guaranteed by correlation.

4.5 AM - section

Refer to application circuit in figure 3. V_{CC} = 4.7V to 5.35V; T_{amb} = -40 to +105°C; LW, MW and SW bands; 74dBµV antenna level, unless otherwise specified. Antenna level equivalence: 0dBµV = 1µVrms, all RF levels are intended as EMF.

Table 12. AM - section

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
AM IMR Mixer and active balun						
Gmix1	Mixer conversion gain	-	7.2	9	10.5	dB
∆gmix1	Gain attenuation range	controlled by IF-AGC	18	20	-	dB
Rin	Input impedance	-	5	6.5	9.5	kΩ
Rout	Output impedance	-	15	20	30	Ω
-	Min. external load	-	400	-	-	Ω
Vin_max	Max. output voltage	without clipping (unloaded)	122	-	-	dBµV
Vnoise	Input noise voltage	-	-	6	8.3	nV/√Hz
IIP3	3rd order intercept point	-	130	134	-	dBµV
IIP2	2nd order intercept point	-	159	-	-	dBµV
IRR	Image rejection ratio	without gain/phase adjust	30	-	-	dB
IRR	Image rejection ratio	with gain/phase adjust	40	45	-	dB
AM RF AGC External capacitance for time constant from 1nF to 4700nF – time constant values are directly proportional to the external capacitor value						
Lthr	Mixer input referred RF level threshold	min. setting	83	86	89	dBµV
		max setting	98	101	104	
-	threshold steps	4 bit control	0.5	1	1.5	dB
-	Pin diode source current	AGC control pin 1 Logarithmic current	10	-	-	mA
-	Min. voltage	AGC control pin 1 with 5µA sink current	-	-	0.1	V
-	Isink	5µA sink current	5	10	-	µA
-	Pin diode source current in constant current mode	-	1	-	-	mA
-	Max. voltage	AGC control pin 1	V_{CC}-1.4	V_{CC}-1.2	-	V
-	Max. output voltage in GPO mode	AGC control pin 2	V_{DD}-0.3	-	V_{DD}	V
-	Min. output voltage	AGC control pin 2	-	-	0.3	V

Table 12. AM - section (continued)

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
-	Fast attack time constant	active in case of overdrive (more than 7dB)	0.05	0.5	5	ms
-	Time constant	Range, mode T1 Range, mode T2 Range, mode T3	-	0.5-50 2.5-250 12.5-1250	-	ms ms ms

4.6 IF - section

Table 13. IF - section

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
IF AMPLIFIER						
Grange	Gain range	Input 1-3 (FM,HD,AM), min.	23	25	27	dB
		Input 1-3 (FM,HD,AM), max	36	38	40	
		Input 4 (HD-Radio AM), min.	15	17	19	
		Input 4 (HD-Radio AM), max	29	31	33	
Gstep	Gain step	3 bit control	1.5	2	2.5	dB
ΔAGC	AGC range	-	16.5	18	19	dB
	AGC steps	2-bit control	5.2	6	6.6	
Rin_input1	Input impedance input 1	FM –input @ 10.7MHz	230	330	450	Ω
Rin_input2	Input impedance input 2	HD-Radio FM input @ 10.7MHz	2.2	2.9	3.6	kΩ
Rin_input3	Input impedance input 3	AM input @ 10.7MHz	7	8.2	10	kΩ
Rin_input4	Input impedance input 4	HD-Radio AM input @ 10.7MHz	7	8.7	11	kΩ
Rout	Differential output impedance	-	-	15	-	Ω
Vout_max	Max. output voltage	-	115	-	117	dBµV
Gain, load	Gain variation in loaded conditions	10pF between each IFAMP outputs and GND, 10kΩ differential load	-	-	0.5	dB
IIP3,load	IIP3 decrease in loaded conditions	10pF between each IFAMP outputs and GND, 10kΩ differential load	-	-	1	dB
IIP3	3rd order intercept point	input stage 1-3, @ 25dB gain	119	122	-	dBµV
		input stage 4, @ 17dB gain	130	133	-	
IIP2	2nd order intercept point	input stage 1-3	142	-	-	dBµV
		input stage 4	154	-	-	

Table 13. IF - section (continued)

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
Vnoise_input 1	IN1 input noise voltage	@ source impedance 330Ω · noiseless, @31dB gain	-	3.5	4.2	nV/√Hz
Vnoise_input 2	IN2 input noise voltage	@ source impedance 470Ω · noiseless, @ 31dB gain, with external 560Ω input termination resistor	-	3.8	4.6	nV/√Hz
Vnoise_input 3	IN3 input noise voltage	@ source impedance 2.2kΩ · noiseless, @ 29dB gain, with external 2.7kΩ input termination resistor	-	5	6.5	nV/√Hz
Vnoise_input 4	IN4 input noise voltage	@ source impedance 2.2kΩ · noiseless, @ 24dB gain, with external 2.7kΩ input termination resistor	-	7	8.5	nV/√Hz
IF AGC External capacitance for time constant from 10nF to 500nF in FM (asym. mode), from 100nF to 4700nF in AM (sym. mode) – time constant values are directly proportional to the external capacitor value						
Lthr	IFAmp input referred	FM, min. setting	88.5	91	93.5	dBµV
		FM, max setting	99.5	101	103.5	
		AM, min. setting	86.5	89	91.5	
		AM, max setting	96.5	99	101.5	
-	Threshold steps	-	1	1.5	2	dB
-	Fast attack mode in AM-mode, range	active in case of overdrive	0.05	0.5	5	ms
-	Time constant attack, range	FM: asym. mode U1 FM: asym. mode U2 AM: sym. mode S1 AM: sym. mode S2	-	10-500 0.05-2.5 2.0-100 20-1000	-	µs ms ms ms
-	Time constant decay, range	FM: asym. mode U1 / U2 AM: sym. mode S1 AM: sym. mode S2	-	2-100 2-100 20-1000	-	ms ms ms

4.7 VCO

Table 14. VCO

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
-	Frequency range VCO	±8% tuning range	3430		4010	MHz
-	Phase Noise of LO	Free running VCO; values referred @ 100MHz @ 10 Hz @ 100 Hz @ 1 kHz @ 10 kHz	 -46 -76 -103	 -40 -60 -86 -106	-	dBc/Hz
-	Deviation error	FM reception, de-emphasis 50µs, fNF=20Hz...20kHz @ min. VCO frequency	-	8	-	Hz

4.8 Reference frequency input buffer

Table 15. Reference frequency input buffer

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
Reference frequency input buffer mode						
-	Max input voltage high	-	-	-	1475	mV
-	Min. input voltage low	-	925	-	-	mV
-	Input differential voltage	-	200	-	400	mV
-	Input impedance (xtal mode)	-	150	-	-	kΩ
-	Input impedance (lvds mode)	-	10	-	-	kΩ
-	Input voltage range	Single ended mode	200	-	1000	mV_{PP}

4.9 Dividers

Table 16. Dividers

Symbol	Parameter	Test condition, comments	Min	Typ	Max	Units
Mixer divider V – integer values						
N_V	divider value divider_V	7 bit	5	-	131	-
Divide by 4 – generation of 0°/90°/-90° LO signal for IMR						
-	I/Q phase error of divider	phase calibration in IMR	-0.5	-	0.5	DEG
Main divider N – integer divider						
N_N	divider value divider_N	21bit (32/33 pre scaler)	992	-	2097151	-
Reference divider R – integer values						
N_R	divider value divider_R	8 bit	1	-	255	-

4.10 Phase locked loop

Table 17. Phase Locked Loop

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
-	Settling time AM/FM	$\Delta f < 0,01\%$ @ f_{PFD} = 100 kHz	-	800	1200	µs
-	Spurious suppression	@ divided VCO signal	70	-	-	dB

4.11 Phase frequency detector and charge pump

Table 18. Phase frequency detector and charge pump

Symbol	Parameter	Test Condition, Comments	Min	Typ	Max	Units
PFD						
f_{PFD}	PFD input frequency	-	2	-	3000	kHz
Charge pump						
-	Sink current	high current mode bit1	-0.4	-0.65	-0.9	mA
		high current mode bit2	-0.8	-1.3	-1.7	mA
		high current mode bit3	-1.7	-2.4	-3.1	mA
		high current mode bit4	-3.1	-4.5	-5.8	mA
		low current mode bit5	-40	-60	-80	µA
		low current mode bit6	-80	-120	-160	µA
		low current mode bit7	-160	-240	-320	µA
		low current mode bit8	-320	-480	-640	µA
		low current mode bit9	-640	-960	-1280	µA
-	Source current	high current mode bit1	0.4	0.65	0.9	mA
		high current mode bit2	0.8	1.3	1.7	mA
		high current mode bit3	1.7	2.4	3.1	mA
		high current mode bit4	3.1	4.5	5.8	mA
		low current mode bit5	40	60	80	µA
		low current mode bit6	80	120	160	µA
		low current mode bit7	160	240	320	µA
		low current mode bit8	320	480	640	µA
		low current mode bit9	640	960	1280	µA