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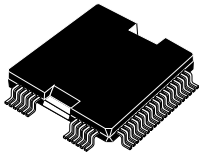
TDA7572

200 W mono bridge PWM amplifier with built-in step-up converter

Features

- Input stage and gain compressor
- Over-modulation protection and current limiting
- Modulator
- DAC
- Step-up
- Mode control
- Diagnostics / safety
- Power control



HiQUAD-64

Description

TDA7572 is a highly integrated, highly versatile, semi-custom IC switch mode audio amplifier. It integrates audio signal processing and power amplification tailored for standalone remote bass box applications, while providing versatility for full bandwidth operation in either automotive or consumer audio environments. It's configured as one full bridge channel, using two clocked PWM modulators driving external, complementary FET's.

Broad operating voltage is supported, allowing operation from both 14 V and 42 V automotive power buses, as well as from split supplies for consumer electronics use.

A current mode control boost converter controller is provided to allow high power operation in a 14 V environment. Turn-on and turn-off transients are minimized by soft muting/unmuting and careful control of offsets within the IC.

Digital Audio input is supported by an integrated one channel DAC. Sophisticated diagnostics and protection provide fault reporting via I^2C and power shutdown for safety related faults.

TDA7572 is packaged in a HiQUAD-64 package.

Table 1. Device summary

Order code	Package	Packing
TDA7572	HiQUAD-64	Tray

Contents

List of tables

List of figures

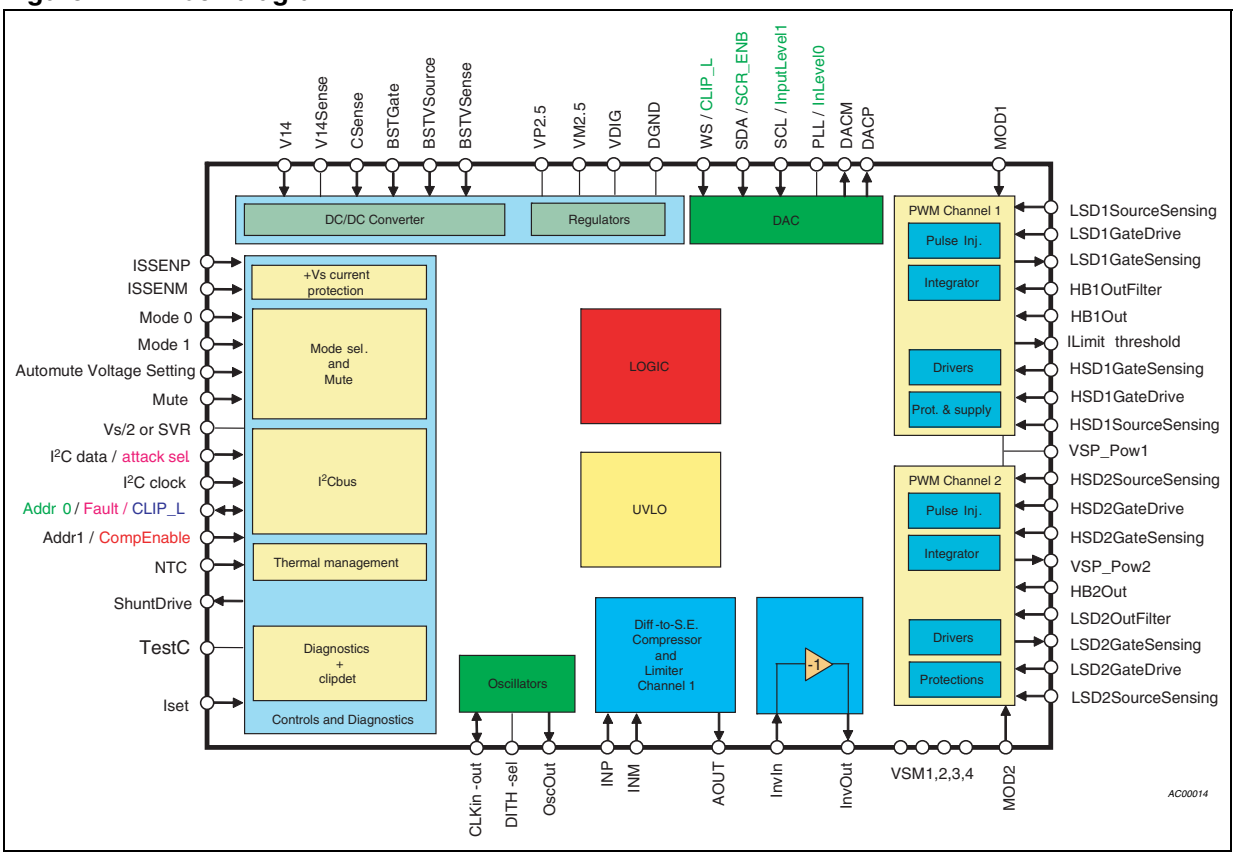
1 Detailed features

- Input Stage and Gain Compressor
  - Differential, high CMRR, analog input
  - Programmable input attenuation/gain to support up to four drive levels
  - Noiseless Gain compression of up to 16 dB with programmable attack and decay.
  - Compressor controlled by monitoring estimated THD
  - Soft mute / un-mute for pop control
- Over-modulation Protection and Current Limiting
  - Adaptive pulse injection prevents missing pulses due to over modulation which maximizes useful output swing.
  - Programmable current limiting based on FET VDS
- Modulator
  - Optimized for low distortion at low switching frequency (approximation 110 kHz)
  - Dual Clocked PWM modulators for 3 state switching
  - External gain control / internal integrator components
  - Controls 4 external FETS with switching optimized for low EMI
  - Oscillation frequency selectable by I^2C
  - Anti-pop shunt driver
- DAC
  - 18bit, mono
  - I^2S inputs 38-48 kHz, 96 kHz, 192 kHz
  - Hybrid architecture, area optimized for Bass
  - Full bandwidth supported by off loading the interpolator function
  - Synchronization with modulator
- Step-Up
  - On board STEP-UP step up converter, synchronized to the modulator frequency
  - Drives external NFET switch
  - Externally compensated
  - Soft start and current limiting
- Mode Control
  - Critical modes controllable by mode pins for bus-less operation
  - I^2C provides additional mode control
- Diagnostics / Safety
  - Offset, short, open, overcurrent, over temperature
  - I^2C used to report errors, and for configuration control
  - Faults pin used to report errors in bus-less environment
  - Clipping reported at a separate pin
  - Abnormal supply current detection disables input power for fail safe operation
  - Output current limiting
  - Power control
  - Latching control of an external PMOS power switch for safety related faults.
  - Power is switched off for safety related faults of abnormal supply current, excessive internal or external temperature, or persistent output stage over-current that fails to be controlled by the pulse-by-pulse current limiting method

2 Interface description

I²C bus and mode control pins are use to control operation. Default values of all the operating modes are deterministic, some of these values are intrinsic to the IC and some are determined by configurations pins. The configuration pins are read at power-up and copied into registers, which may later be modified using the I²C bus, if one is present. This allows varied operation in an environment where NO I²C bus is present, while allowing full control and override of pin programmed modes when used with I²C.

Figure 1. Block diagram



3 Pins description

Figure 2. Pins connection (top view)

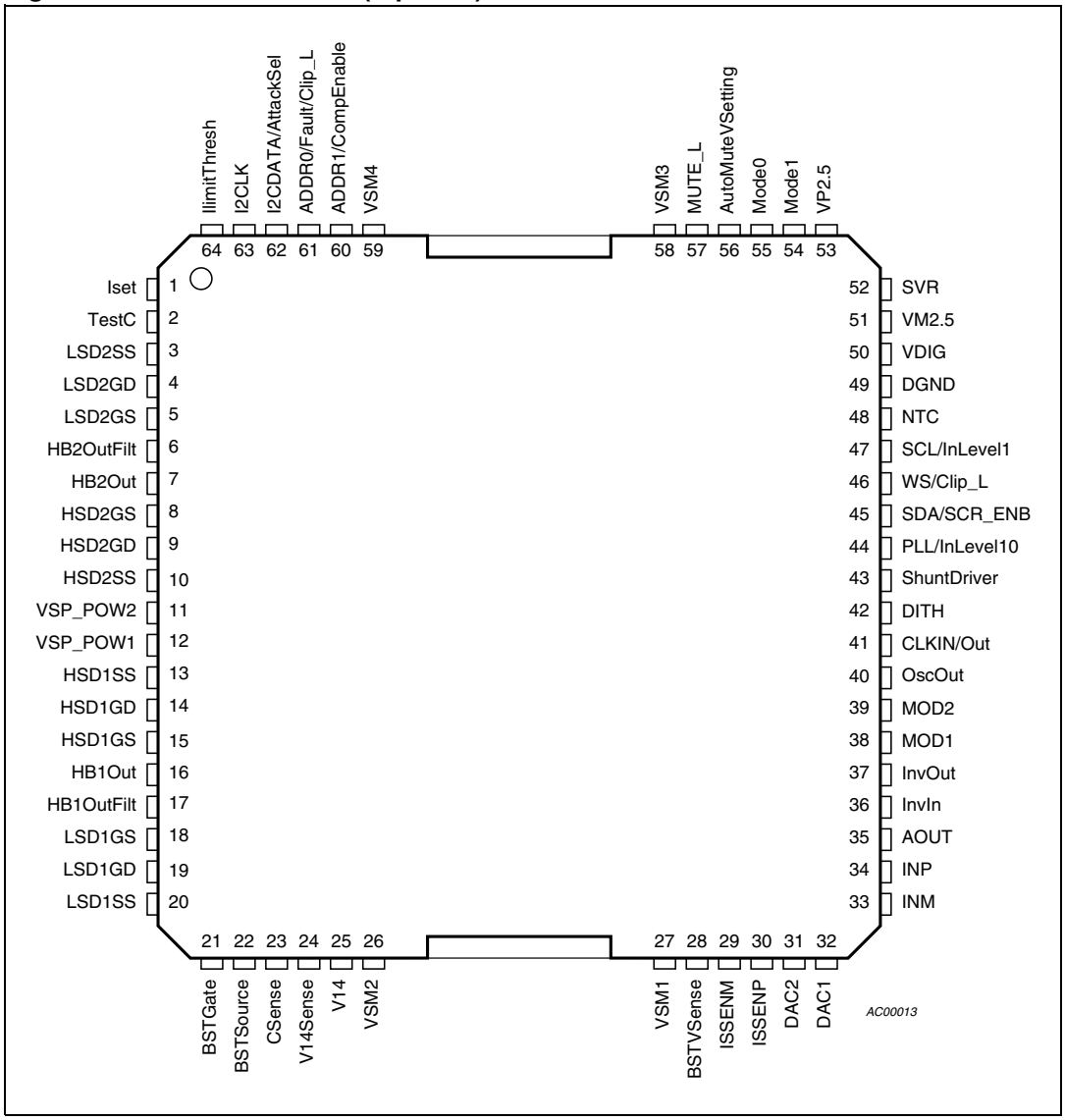


Table 2. Pin list by argument

Pin #	Pin name	Description
On/off circuitry		
11	VSP_POW2	Positive supply power for low power, non gate-drive functions with a separate bonding to power the gate drive of modulator two
53	VP2.5	+2.5 V analog supply output
51	VM2.5	-2.5 V analog supply output
50	VDIG	5 V logic supply decoupling
49	DGND	Digital gnd
52	SVR	Vs/2 analog reference filter capacitor. Reference for input stage.
55	Mode0	Mode control bit0, selects standby/normal/ I^2C/diagnostic operation
54	Mode1	Mode control bit1, selects standby/normal/ I^2C/diagnostic operation
57	MUTE_L	Mute input and / or timing cap, assertion level low
56	AutoMuteVSetting	Auto-mute voltage setting
Input/gain compressor		
34	INP	Non inverting audio input
33	INM	Inverting audio input
35	AOUT	Compressed audio output
-	-	Input stage gain selection – see PLL pin in DAC *Section 8*
-	-	Compressor attack/decay select – see I^2C data pin in DAC *Section 8*
Inverter		
36	InvIn	Inverter input
37	InvOut	Inverter output
Modulator		
64	IlimitThresh	Output stage current limiting trip voltage set point
32	LVLSFT	Gain program pin for SVR to HVCC level shifting
38	MOD1	Modulator1 Inverting / Summing node
20	LSD1SS	Low-side1 Source Sensing
19	LSD1GD	Low-side1 Gate Drive
18	LSD1GS	Low-side1 Gate sense
17	HB1OutFilt	Half bridge1 post-LC filter – for diagnostics
16	HB1Out	Half-bridge1 output, HSD 1 drain sense, LSD1 Drain Sense
15	HSD1GS	High-side1 Gate sense
14	HSD1GD	High-side1 Gate Drive
13	HSD1SS	High-side1 Source sense
12	VSP_POW1	Positive supply voltage connection for gate drive circuitry

Table 2. Pin list by argument (continued)

Pin #	Pin name	Description
39	MOD2	Modulator2 Inverting / Summing node
10	HSD2SS	Highside2 Source sense
9	HSD2GD	Highside2 Gate Drive
8	HSD2GS	Highside2 Gate sense
7	HB2Out	Half-bridge2 output, HSD 1 drain sense, LSD1 Drain Sense
6	HB2OutFilt	Half bridge2 post-LC filter – for diagnostics
5	LSD2GS	Lowside2 Gate sense
4	LSD2GD	Lowside2 Gate Drive
3	LSD2SS	Lowside2 Source Sense
27	VSM1	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
26	VSM2	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
58	VSM3	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
59	VSM4	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
43	ShuntDriver	Shunt driver
DC-DC		
28	BSTVSense	Voltage feedback input for voltage booster
22	BSTSource	Boost converter NFET source
21	BSTGate	Boost converter NFET gate drive
23	CSense	Inverting input for booster current sensing and digital test enable (operating when is more then about 3V under the V14 pin level)
24	V14Sense	Non-inverting input for booster current sensing
25	V14	Power for boost converter gate drive and Output LSD's
Oscillator		
41	CLKIN/Out	Clock input
42	DITH	Dither capacitor
40	OscOut	Oscillator output
Diagnostics / Bus		
62	I^2CDATA/AttackSel	I^2C data (I^2C mode) Compressor aggressiveness selection (non-bus mode)
63	I^2CCLK	I^2C clock

Table 2. Pin list by argument (continued)

Pin #	Pin name	Description
61	ADDR0/Fault/Clip_L	I^2C address set (I^2C mode) Fault output in non bus mode (non-bus mode) Clipping indicator, assertion level low, (when DAC is enabled)
60	ADDR1/CompEnable	I^2C address set (I^2C mode) Compressor Enable/disable (non-bus mode)
48	NTC	Connection for NTC thermistor
2	TestC	Test cap used to generate the slow current pulses
1	ISet	Program pin for current level used in Short/Open test
30	ISSENP	Supply non-inverting current sense
29	ISSENM	Supply inverting current sense
DAC		
46	WS / Clip_L	I^2S Word select / Clipping indicator, assertion level low (non-DAC mode)
45	SDA/SCR_ENB	I^2C serial data / SCR ENABLE (non DAC mode)
47	SCL/ InLevel1	I^2C serial data bit clock/ Input Level selection bit1 (non-DAC mode)
44	PLL/InLevel0	DAC clock PLL filter/ Input Level selection bit 0 (non-DAC mode)
31	DAC2	DAC output voltage p
32	DAC1	DAC output voltage n

Table 3. Pin list

Pin #	Pin name	Description
1	Iset	Program pin for current level used in Short/Open test
2	TestC	Test cap used to generate the slow current pulses
3	LSD2SS	Lowside2 source sense
4	LSD2GD	Lowside2 Gate Drive
5	LSD2GS	Lowside2 Gate sense
6	HB2OutFilt	Half bridge2 post-LC filter – for diagnostics
7	HB2Out	Half-bridge2 output, HSD 1 drain sense, LSD1 Drain Sense
8	HSD2GS	Highside2 Gate sense
9	HSD2GD	Highside2 Gate Drive
10	HSD2SS	Highside2 Source sense
11	VSP_POW2	Positive supply power for low power, non gate-drive functions with a separate bonding to power the gate drive of modulator two
12	VSP_POW1	Positive supply voltage connection for gate drive circuitry
13	HSD1SS	Highside1 Source sense
14	HSD1GD	Highside1 Gate Drive
15	HSD1GS	Highside1 Gate sense

Table 3. Pin list (continued)

Pin #	Pin name	Description
16	HB1Out	Half-bridge1 output, HSD 1 drain sense, LSD1 Drain Sense
17	HB1OutFilt	Half bridge1 post-LC filter – for diagnostics
18	LSD1GS	Low-side1 Gate sense
19	LSD1GD	Low-side1 Gate Drive
20	LSD1SS	Low-side1 Source Sensing
21	BSTGate	Boost Converter NFET gate drive
22	BSTSource	Boost Converter NFET Source
23	CSense	Inverting input for Booster Current Sensing and Digital Test Enable (operating when is more then about 3V under the V14 pin level)
24	V14Sense	Non-inverting input for Booster Current Sensing
25	V14	Power for Boost converter gate drive and Output LSD's
26	VSM2	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
27	VSM1	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
28	BSTVSense	Voltage feedback input for Voltage Booster
29	ISSENM	Supply inverting current sense
30	ISSENP	Supply non-inverting current sense
31	DAC2	Half VCC (VSP- VSM)/2 Used for output stage reference.
32	DAC1	Gain program pin for SVR to HVCC level shifting
33	INM	Inverting audio input
34	INP	Non inverting audio input
35	AOUT	Compressed Audio Output
36	InvIn	Inverter input
37	InvOut	Inverter Output
38	MOD1	Modulator1 Inverting / Summing node
39	MOD2	Modulator2 Inverting / Summing node
40	OscOut	Oscillator output
41	CLKIN/Out	Clock input
42	DITH	Dither capacitor
43	ShuntDriver	Shunt Driver
44	PLL/InLevel0	DAC clock PLL filter/ Input Level selection bit 0 (non-DAC mode)
45	SDA/SCR_ENB	I^2C serial data / SCR ENABLE (non DAC mode)
46	WS / Clip_L	I^2S Word select / Clipping indicator, assertion level low (non-DAC mode)
47	SCL/ InLevel1	I^2C serial data bit clock/ Input Level selection bit1 (non-DAC mode)
48	NTC	Connection for NTC thermistor

Table 3. Pin list (continued)

Pin #	Pin name	Description
49	DGND	GND logic supply decoupling
50	VDIG	5V logic supply decoupling
51	VM2.5	-2.5 V analog supply output
52	SVR	Vs/2 analog reference filter capacitor. Reference for input stage.
53	VP2.5	+2.5 V analog supply output
54	Mode1	Mode control bit1, selects standby/normal/I^2C/diagnostic operation
55	Mode0	Mode control bit0, selects standby/normal/ I^2C/diagnostic operation
56	AutoMuteVSetting	Auto-Mute Voltage Setting
57	MUTE_L	Mute input and / or timing cap, assertion level low
58	VSM3	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
59	VSM4	Die tab connection to lowest supply voltage – gnd for single ended supplies, negative supply for split supplies
60	ADDR1/CompEnable	I^2C address set (I^2C mode) Compressor Enable/disable (non-bus mode)
61	ADDR0/Fault/Clip_L	I^2C address set (I^2C mode) Fault output in non bus mode (non-bus mode) Clipping indicator, assertion level low, (when DAC is enabled)
62	I^2CDATA/AttackSel	I^2C data (I^2C mode) Compressor aggressiveness selection (non-bus mode)
63	I^2CCLK	I^2C Clock
64	IlimitThresh	Output stage Current Limiting trip voltage setpoint

4 Electrical specifications

4.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameters	Test conditions	Min.	Max.	Units
V_{SP}	Supply voltage	-	V_{SM} -0.6	V_{SM} +58	V
V_{peak}	Peak supply voltage	(V_{S+} - V_{S-}) time ≤ 50 ms	-	68	V
V_{DATA}	Data pin voltage	w.r.t Dgnd	V_{S}—0.6	6V	V
T_J	Junction temperature	-	-40	150	C
T_{Stg}	Storage temperature	-	-55	150	C
P_{DMAX}	Power dissipation	Any operating condition For thermal budgeting	-	2.5	W

4.2 Thermal data

Table 5. Thermal data

Symbol	Parameters	Value	Units
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	3	°C/W

4.3 Electrical characteristics

Unless otherwise specified, all ratings below are for -40 °C < T_J < 125 °C, V_{SP} = 42 V, V_{SM} = 0V and the application circuit of *Figure 12*. Operation of the IC above this junction temperature will continue without audible artifacts until thermal shutdown, but these parameters are not guaranteed to be within the specifications below. F_{PWM} =110 kHz, Booster not enabled.

4.3.1 Operating voltage and current

Table 6. Operating voltage and current

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{SP42}	Operating voltage 42 V automotive range	Normal operation without audible defects required Single ended supply 42 V configuration, V_{SM}=0	30	42	58	V
V_{SP14}	Operating voltage 14.4 V automotive range	Normal operation without audible defects required Single ended supply 14 V configuration, V_{SM}=0	9	14.4	-	

Table 6. Operating voltage and current (continued)

Symbol	Parameters	Test conditions		Min.	Typ.	Max.	Units
V_{SPLIT}	Operating voltage V_{SP} - V_{SM} split supply rails	Normal operation required Split supply application configuration, $V_{SM}<V_{SVR}-4$, $V_{SP}>V_{SVR}+4$		8	48	58	V
I_{stdby}	Stand-by current	IC in standby, Mode 0, and Mode 1 low V_s = 42 V		-	-	50 at T = 85 °C 10 at T = 25 °C	µA
$I_{tristate}$	Tristate current	Outputs tristated Booster not running, F_{pwm} = nominal	V14	-	13	20	mA
			VSP	-	15	25	
I_{MUTE}	Mute mode current	MUTE asserted,	V14	-	15	-	mA
			VSP	-	20	-	

4.3.2 Under voltage lockout

Table 7. Under voltage lockout

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{LimAM}	AutomuteVSetting pin voltage limit	Voltage limit respect to the SVR pin Allowed voltage range on Automute pin	0.5	-	2.1	V
VSP UVLO						
V_{AM}	Auto-mute supply voltage VSP	Mute is forced if VSP-VSVR or VSVR-VSM is less than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	VVSVR* 7	+15 %	V
VPO-	Auto-tristate supply voltage VSP negative slope	The IC is set in tristate if VSP-VSM is less than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	VVSVR *12	+15 %	V
VPO+	Auto-tristate supply voltage VSP positive slope	The IC is set out from tristate if VSP-VSM is higher than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	VVSVR *13	+15 %	V
V_U	Auto-tristate supply voltage VSP Relative maximum value	The IC is set in tristate if VSP-VSM is more than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	VVSVR* 48	+15 %	V
V_{UC}	Auto-tristate supply voltage VSP Absolute maximum value	The IC is set in tristate if VSP-VSM is higher than this value	60	63	66	V
V14 – UVLO						
V14-	Auto-tristate supply voltage V14 negative slope	The IC is kept in tristate if 14 V VSM become lower than this value	5.5	-	7	V

Table 7. Under voltage lockout (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V14+	Auto-tristate supply voltage V14 positive slope	The IC is goes out from tristate if 14 V-VSM become higher than this value	6.5	-	8	V
V14h	Auto-tristate 14V voltage hysteresis	Comparator hysteresis for auto-tristate threshold	0.8	-	-	V
V14su	Step-up tristate	The step-up is in tristate when voltage lower than this threshold	5	-	8	V
V14mute-	Auto-mute supply voltage V14 negative slope	The IC goes in mute if 14 V-VSM become lower than this value	V14- + 0.7 V	-	V14- + 1.2 V	V
V14mute+	Auto-mute supply voltage V14 positive slope	The IC goes in play if 14 V-VSM become higher than this value	V14V+ + 40 mV	-	V14V+ + 170 mV	V
SVR – UVLO						
Vsvr-	Auto-tristate SVR voltage negative slope	The IC is kept in tristate if VSvr - VSM become less than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	5.2 x VVSVR	+15 %	V
Vsvr+	Auto-tristate SVR voltage positive slope	The IC is goes out from tristate if VSvr - VSM become higher than this value Vautomute VSetting-V_{SVR}=VVSVR	-15 %	6 x VVSVR	+15 %	V
VPOH	Auto-tristate SVR voltage hysteresis	Comparator hysteresis for auto-tristate threshold Vautomute VSetting-V_{SVR}=VVSVR	0.40 x VVSVR	-	1.2V x VVSVR	V

4.3.3 Input stage

Table 8. Input stage

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Input differential amplifier/ gain attenuator						
R_{IN}, No compression	Input resistance	INLEVEL1=0, INLEVEL0=0	-30%	22	+30%	kΩ
		INLEVEL1=0, INLEVEL0=1	-30%	12	+30%	
		INLEVEL1=1, INLEVEL0=0	-30%	24	+30%	
		INLEVEL1=1, INLEVEL0=1	-30%	12	+30%	
R_{IN} max compression		INLEVEL1=0, INLEVEL0=0	-30%	17	+30%	
		INLEVEL1=0, INLEVEL0=1	-30%	12	+30%	
		INLEVEL1=1, INLEVEL0=0	-30%	17	+30%	
		INLEVEL1=1, INLEVEL0=1	-30%	12	+30%	

Table 8. Input stage (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{InMax}	Input clipping level Voltage level of the input that trespassed cause clipping in the preamplifier	INLEVEL1=0, INLEVEL0=0	2	-	-	V_{RMS}
		INLEVEL1=0, INLEVEL0=1	7	-	-	V_{RMS}
		INLEVEL1=1, INLEVEL0=0	2.6	-	-	V_{RMS}
		INLEVEL1=1, INLEVEL0=1	9.5	-	-	V_{RMS}
A_{IN_0}	Input stage gain	(V_{AOUT}-V_{SVR}) / (VInP-VinM) INLEVEL1=0, INLEVEL0=0, no compression	-4	-3	-2	dB
A_{IN_2}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=0, INLEVEL0=1, no compression	-15	-14	-13	dB
A_{IN_1}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=1, INLEVEL0=0 no compression	-6.3	-5.3	-4.3	dB
A_{IN_3}		(V_{AOUT}- V_{SVR}) / (VInP-VinM) INLEVEL1=1, INLEVEL0=1, no compression	-17.6	-16.6	-15.6	dB
V_{outH}	AOUT output voltage swing	With respect to SVR, 10 K loading to a buffered version of SVR	2	-	-	V
V_{outL}	AOUT output swing	With respect to SVR, 10 K loading to a buffered version of SVR	-	-	-2	V
$AOUT_{THD}$	THD	Vin=1 Vrms, f=20-20 kHz, INLEVEL1=0, INLEVEL0=0, no compression	-	0.01	0.05	%
-	Output slew rate	Vin=1KHz square wave, 2 Vpp, INLEVEL1=0, INLEVEL0=0, no compression Time to transition from 10 % to 90 %	-	-	8	µs
-	AOUT clip detector	Duty cycle of the Clipping signal when there is 5 % distortion at the output of AOUT, f=1 kHz, R_L =10 kohm	15	-	25	%
f_{-3dB}	Frequency response	Vin=1Vrms, INLEVEL1=0, INLEVEL0=0	20	-	-	kHz
CMRR	Common mode rejection ratio	V_{CM}=1 V_{RMS} @1 kHz CMRR= A_{VDIFF}/A_{VCM} INLEVEL1=0, INLEVEL0=0 No compressor	47	-	-	dB

Table 8. Input stage (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
CG	Common gain	V_{CM}=1V_{RMS} @1 kHz INLEVEL1=0, INLEVEL0=0 No compressor	51	-	-	dB
		V_{CM}=1 V_{RMS} @1 kHz INLEVEL1=1, INLEVEL0=0 No compressor	51	-	-	dB
		V_{CM}=1 V_{RMS} @1 kHz INLEVEL1=0, INLEVEL0=1 No compressor	51	-	-	dB
		V_{CM}=1 V_{RMS} @1 kHz INLEVEL1=1, INLEVEL0=1 No compressor	51	-	-	dB
PSRR	Power supply rejection, Vsp supply	freq < 10 kHz	60	80		dB
V_{offset}	Output offset	V_{Offset} with respect to SVR Rin=100 ohms, Mute state	-4	0	+4	mV
Eno	Noise	Noise at output of this stage f = 20-20 kHz, R_{input} = 100 ohm A weighting	-	7	10	μV_{RMS}
Gain compressor						
-	Maximum attenuation	INLEVEL1 = 0, INLEVEL0 = 0	-21	-19	-17	dB
		INLEVEL1 = 0, INLEVEL0 = 1	-30	-28	-26	
		INLEVEL1 = 1, INLEVEL0 = 0	-25	-23	-21	
		INLEVEL1 = 1, INLEVEL0 = 1	-34	-32	-30	
-	Attenuation step size	INLEVEL1 = 0, INLEVEL0 = 0	0.5-0.25	0.5	0.5+ 0.25	dB
-		INLEVEL1 = 0, INLEVEL0 = 1	0.44- 0.25	0.44	0.44+ 0.25	
-		INLEVEL1 = 1, INLEVEL0 = 0	0.55- 0.25	0.55	0.55+ 0.25	
-		INLEVEL1 = 1, INLEVEL0 = 1	0.48- 0.25	0.48	0.48+ 0.25	
-	Gain Change ZC comparator offset (in the diff. – S.E. block) offset	Observed at AOUT pin ZC crossing must be detected within 50mV of the actual zero crossing,	-80	-	80	mV
-	Gain Change ZC comparator offset (in the diff. – S.E. block) offset	Observed at InvOut pin ZC crossing must be detected	-220	-	+220	mV

Table 8. Input stage (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Mute						
-	Mute attenuation	Mute pin voltage = Dgnd Vin=1 Vrms	90	-	-	dB
-	Charge current	Mute Pin Voltage(57) = 1.5 V	-30%	100	+30%	µA
-	Discharge current	Mute Pin Voltage(57) = 1.5 V	-30%	100	+30%	µA
-	Mute threshold	Maximum voltage where we must be in complete mute	-	-	1.5	V
-	Unmute threshold	-	2.5	-	-	V
-	Mute to unmute transition voltage	-	0.2	0.3	0.44	V
-	Vol	IC in mute mode, FastMute=1 Iout=0	-	-	Digital GND + 0.1	V
-	Voh	IC in unmute, Iout=0	$V_{DIGITAL}$-0.1	-	-	V
-	Fast mute Resistance	FASTMUTE =1 Vmutepin =1.5 V	420	550	680	Ohm

4.3.4 Oscillator

Table 9. Oscillator

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Internal oscillator						
F_{PWM_NOM}	Switching frequency	PWMCLOCK=[0 1]	100K	120	140K	kHz
		PWMCLOCK=[1 0]	-	F_{PWM_NOM} *2	-	
		PWMCLOCK=[0 0]	-	F_{PWM_NOM} /2	-	
CLK_{DC}	Duty cycle	-	48	50	52	%
V_{CLK_High}	Maximum voltage level	Clock output high value Load = 20 kohm and 100 pF to buffered SVR	V_{P25}-0.1	-	V_{P25}	V
V_{CLK_Low}	Minimum voltage level	Clock output low value Load = 20 kohm and 100 pF to buffered SVR	V_{M25}-0.1	-	V_{M25}	V
$V_{CLK-P-P}$	Peak-peak voltage	Load = 20 kohm and 100 pF to SVR	-10%	4.7	+10%	V
-	Dither cap charge current	Dither pin voltage = 2.5 V	±30%	100	±30%	µA
-	Dither cap discharge current	-	±30%	100	±30%	µA
-	Peak-peak dither voltage swing	-	1.4	1.6	1.7	V
-	Dither external clock determination	Voltage at the dither pin at to select external clock function	VDIG-0.2	-	-	V
-	No dither	Voltage at the dither pin at which no dither will occur	-	-	VDGND +0.2	V
-	Peak F_{PWM} increase due to dither	Cdither = 100 nF	+8	+10	+12	%
-	Peak F_{PWM} decrease due to dither	Cdither = 100 nF	-8	-10	-12	%
-	Triangular peak value	-	VGND+ 1 V	-	VDIG- 1 V	-

4.3.5 Modulator

Table 10. Modulator

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Integrator operational amplifier						
Int_Voff	Input offset voltage	-	-2.5	-	+2.5	mV
Int_ibias	Input bias current	Guaranteed by design	-	-	500	nA
T_{off}	Maximum duty cycle	V_{sp} =1 4.4V	-	-	1.1	µs

4.3.6 Gate drive and output stage control

Table 11. Gate drive and output stage control

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{OL_LSD}	LSG low voltage	I_{sink} = 0.5 A I_{sink} = 20 mA	-	-	1.75 0.080	V
V_{OH_LSD}	LSG high voltage	I_{source} = 0.5 A I_{source} = 20 mA	7 9.2	-	-	V
V_{OL_HSD}	HSG low voltage	I_{sink} = 0.5 A I_{sink} = 20 mA	-	-	VSP-7 VSP-9.2	V
V_{OH_HSD}	HSG high voltage	I_{source} = 0.5 A I_{source} = 20 mA	VSP-1.75 VSP-0.080	-	-	V
-	HSG low Z drive t_{delay}	After a commutation	2	-	10	µs
-	LSG low Z drive t_{delay}	After a commutation	2	-	10	µs
-	HSG HiZ sink current	V_{HSG}=V_{SP} t > 10 µs	-	-	150	mA
-	LSG HiZ source current	V_{LSG}=V_{SM}, t > 10 µs	-	-	150	mA
Overcurrent sensing						
$I_{limThresh}$	Range of $I_{lim\ Trthresh}$	-	0.3	-	1.1	V
Vilim	Vilim	Engagement of the current limiting $V_{limitTreshold}$ = 1 V w.r.t. VM2p5	Vlim* 3.0	-	Vlim* 5.0	V
	Vitrip	Start of cycle by cycle current limiting	-15%	Vlim * 6.0	+15%	V
Anti-shoo through						
PV_{GS_ON}	PFET gate voltage that will block NFET enhancement	-	-2.5	-	-	V
PV_{GS_OFF}	PFET gate voltage that will allow NFET enhancement	-	-	-	-3.5	V

Table 11. Gate drive and output stage control (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
NV_{GS_ON}	NFET gate voltage that will block PFET enhancement	-	2.5	-	-	V
NV_{GS_OFF}	NFET gate voltage that will allow PFET enhancement	-	-	-	3.5	V

4.3.7 Diagnostics

Table 12. Diagnostics

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Turn-on diagnostics/ Power-up diagnostics						
I_{TEST}	Test current for short/open	-	-15 %	2.45/ (3*Riset)	+15 %	mA
		R_i set = 56ohm	-15 %	15	+15 %	
-	R_{ISET} allowed range	-	5.6	-	-	ohm
V_{LSSHRT}	Short threshold to lower supply rail	-	-	-	-Vs +1	V
V_{NOP}	Normal operation thresholds	-	-Vs+2	-	-Vs+5.5	V
-	Short to supply	-	-Vs+8	-	-	V
-	Shorted load	-		-	6	mV
-	Normal load	-	0.025	-	1	V
-	Open load	-	2	-	-	V
-	Test charge current	-	-30 %	10 µA	+30 %	µA
t_{TEST}	Test time	-	60	80	100	ms
Permanent diagnostics						
V_{offACT}	DC offset detected	-	±3	-	-	V
V_{offACT}	DC offset not detected, normal operation allowed	-	-	-	±1.2	V
Temperature						
T_{WARN}	Chip thermal warning	-	135	150	165	°C
T_{WH}	Chip thermal warning hysteresis	-	3	5	7	-
T_{SH}	Chip thermal shutdown	-	155	160	175	°C
-	Shutdown hysteresis	-	3	5	7	°C
T_{EW}	External thermal warning	-	-10 %	V_{DIG} *.4	+10 %	V
T_{EWH}	External thermal warning hysteresis	-	Vdig*0.030	-	Vdig*0.044	V

Table 12. Diagnostics (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
T_{ES}	External thermal shutdown	-	-15 %	V_{DIG} *0.36	+15 %	V
T_{ESH}	External thermal shutdown hysteresis	-	Vdig* 0.032	-	Vdig* 0.046	V
Supply current sense						
V_{SSenT}	Supply sense trip voltage	-	16	20	25	mV
-	AOUT levels that allow sensing of supply current	-	-	-	3	V
-	Duration of AOUT under threshold to allow supply current sensing	-	-25 %	80	+25 %	ms
I_{ssenp}	Input bias current	-	200	-	700	µA
I_{ssenM}	Input bias current	-	-500	-	500	nA

4.4 Voltage booster

Table 13. Voltage booster

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
Current mode control topology						
BST_{DCMAX}	Max duty cycle	-	-	-	88	%
BST_{DCMIN}	Min duty cycle	-	0	-	-	%
BSTREF	Vref	-	-8 %	2.5	+8 %	V
$IBIAS_{BSTREF}$	V_{sense} input bias current	-	-200	-	200	nA
V_{SENSE_UL}	V_{sense} pin allowed voltage range	-	-0.6	-	58	V
BSTVGain	Voltage-error gain ΔDuty cycle/ΔBSTVSense	-	0.4	0.8	1.2	% D.C. per mV
$BSTDC_{NOM}$	Nominal duty cycle	-	55	-	65	% D.C.
C_{sense_UL}	C_{sense} pin allowed voltage range	-	-0.6	-	58	V
$C_{sense\ gain}$	C_{sense} gain ΔDuty cycle / ΔC_{sense}	-	0.120	-	0.350	% D.C. per mV
$Csense_{Trip}$	limit trip point	-	0.220	-	0.440	V
T_{SS}	Soft-start step period not yet tested (to be confirmed)	-	-	3	-	ms
-	Soft start steps	-	-	16	-	-

Table 13. Voltage booster (continued)

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
V_{OH_BST}	BST gate high voltage	I_{source} = 0.5 A I_{source} = 20 mA	7 9.2	-	-	V
V_{OL_BST}	BST gate low voltage	I_{sink} = 0.5 A I_{sink} = 20 mA	-	-	1.75 V 0.080	V

4.4.1 Digital to analog converter

Table 14. Digital to analog converter

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Units
-	Dynamic range at -60 dBFS	At output of analog filter -60dBFS input 1KHz sine tone	80	90	-	dB
-	Noise floor	At output of analog filter after > 25 ms of –97dBFS input 20-20 kHz flat	-	-	20	µV
-	THD+N at maximum useful input level	Input = -1.5 dBFS The DAC output is limited to prevent operation in regions of degraded DAC performance. This spec represents the performance at this maximum practical value	-	-	-60	dB
-	Silent Mute	Must engage after 25 mS of <- 96 dbFS input signal	20		30	ms
-	Differential output voltage	Magnitude of –1.5 dBFS sine, 1 kHz	-10 %	2.1	+10 %	Vrms
-	Output resistance	-	1.8	2.5	3.0	kΩ