



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

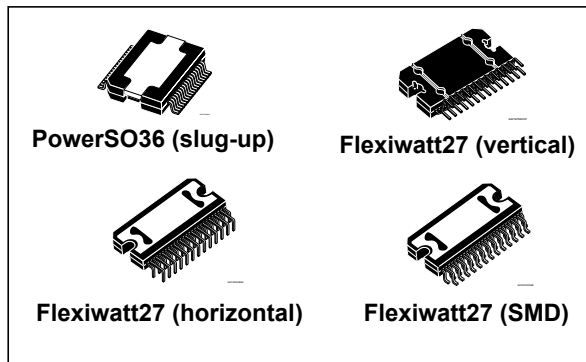
Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



2 x 75 W dual-bridge power amplifier with I²C complete diagnostics and "start-stop" profile (6 V operation)

Datasheet - production data



Features

- MOSFET (DMOS) output power stage
- High-efficiency (class SB)
- Single-channel 1 Ω driving capability
 - 84 W undistorted power
- High output power capability 2 x 28 W / 4 Ω @ 14.4 V, 1 kHz, 10 % THD
- Max. output power 2 x 75 W / 2 Ω, 1 x 150 W / 1 Ω
- Full I²C bus driving with 4 addresses
- Low voltage (6 V) operation (i.e. 'start-stop')
- Gain 16/26 dB
- Full digital diagnostic (AC and DC loads)
- Legacy mode (operation without I²C)
- Differential inputs
- Fault detection through integrated diagnostics
- DC offset detection
- Two independent short circuit protections
- Diagnostic on clipping detector with selectable threshold (2 % / 10 %)
- Clipping detector pin
- ST-BY and MUTE pins
- ESD protection
- Very robust against misconnections

Description

The TDA7577BLV is a new MOSFET dual bridge amplifier specially intended for car radio applications. Thanks to the DMOS output stage the TDA7577BLV has a very low distortion allowing a clear powerful sound, together with high output power capability.

It is a very flexible device capable to support the most demanding specifications in terms of power dissipation and battery transitions: its superior efficiency performance, coming from the internal exclusive structure, can reduce the dissipated output power up to the 50 % (when compared to conventional class AB solutions). Moreover it is compliant to the recent OEM specifications thanks to the capability to work down to 6 V ('start-stop' compatibility).

This device is also equipped with a full diagnostic array that communicates the status of each speaker through the I²C bus. TDA7577BLV can also drive 1 Ω loads (with parallel connection of the outputs).

It is possible also to exclude the I²C bus interface, controlling the device by means of the usual ST-BY and MUTE pins.

Table 1. Device summary

Order code	Package	Packing
TDA7577BLV	Flexiwatt 27 (vertical)	Tube
TDA7577BLVPD	PowerSO36	Tube
TDA7577BLVPDTR	PowerSO36	Tape and reel
TDA7577BLVH	Flexiwatt 27 (horizontal)	Tube
TDA7577BLVSM	Flexiwatt 27 (SMD)	Tube

Contents

- 1 Block and pins diagrams 6**
- 2 Application circuit 7**
- 3 Electrical specifications 8**
 - 3.1 Absolute maximum ratings 8
 - 3.2 Thermal data 8
 - 3.3 Electrical characteristics 8
 - 3.4 Electrical characteristics typical curves 13
- 4 Diagnostics functional description 17**
 - 4.1 Turn-on diagnostic 17
 - 4.2 Permanent diagnostics 19
 - 4.3 Output DC offset detection 20
 - 4.4 AC diagnostic 20
 - 4.5 Multiple faults 22
 - 4.6 Fault presence information availability on I²C 22
- 5 1 Ω load capability setting 23**
- 6 Battery transitions management 24**
 - 6.1 Low voltage operation (“start stop”) 24
 - 6.2 Advanced battery management 25
- 7 I²C mode and legacy mode selection 26**
- 8 Application suggestions 27**
 - 8.1 High efficiency introduction 27
- 9 I²C bus interface 28**
 - 9.1 Data validity 28
 - 9.2 Start and stop conditions 28
 - 9.3 Byte format 28

9.4	Acknowledge	28
9.5	I2C programming/reading sequences	29
10	Software specifications	30
10.1	Examples of bytes sequence	33
11	Package information	34
11.1	PowerSO-36 (slug up) package mechanical data	34
11.2	Flexiwatt 27 (vertical) package mechanical data	36
11.3	Flexiwatt 27 (horizontal) package mechanical data	38
11.4	Flexiwatt 27 (SMD) package mechanical data	40
12	Revision history	42

List of tables

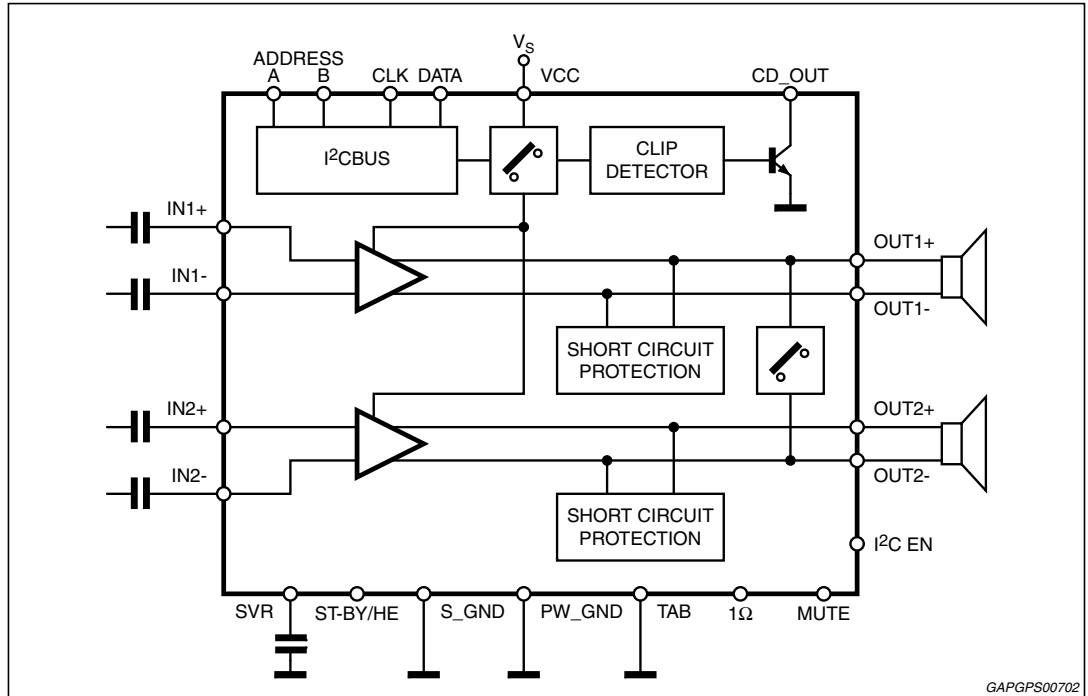
Table 1.	Device summary	1
Table 2.	Absolute maximum ratings	8
Table 3.	Thermal data	8
Table 4.	Electrical characteristics	8
Table 5.	Double fault table for turn on diagnostic	22
Table 6.	Address selection	30
Table 7.	IB1	30
Table 8.	IB2	31
Table 9.	DB1	31
Table 10.	DB2	32
Table 11.	PowerSO-36 (slug up) package mechanical data	34
Table 12.	Flexiwatt 27 (vertical) package mechanical data	36
Table 13.	Flexiwatt 27 (horizontal) package mechanical data	38
Table 14.	Flexiwatt 27 (SMD) package mechanical data	40
Table 15.	Document revision history	42

List of figures

Figure 1.	Block diagram	6
Figure 2.	Pin connections (top view)	6
Figure 3.	Application circuit (TDA7577BLVPD)	7
Figure 4.	Quiescent drain current vs. supply voltage	13
Figure 5.	Output power vs. supply voltage (4 Ω)	13
Figure 6.	Output power vs. supply voltage (2 Ω)	13
Figure 7.	Output power vs. supply voltage (1 Ω)	13
Figure 8.	Distortion vs. output power (4 Ω , STD mode)	13
Figure 9.	Distortion vs. output power (2 Ω , STD mode)	13
Figure 10.	Distortion vs. output power (2 Ω , HI-EFF mode)	14
Figure 11.	Distortion vs. output power (1 Ω , STD mode)	14
Figure 12.	Distortion vs. frequency (4 Ω load)	14
Figure 13.	Distortion vs. frequency (2 Ω load)	14
Figure 14.	Distortion vs. frequency (1 Ω load)	14
Figure 15.	Output attenuation vs. supply voltage	14
Figure 16.	CMRR vs. frequency	15
Figure 17.	Cross talk vs frequency	15
Figure 18.	Power dissipation vs. average Po (2 Ω , STD mode, sine wave)	15
Figure 19.	Power dissipation vs. Po (2 Ω , STD mode, audio program simulation)	15
Figure 20.	Power dissipation vs. average Po (2 Ω , HI-EFF mode)	15
Figure 21.	Power dissipation vs. Po (1 Ω , STD mode, audio program simulation)	15
Figure 22.	ITU R-ARM frequency response, weighting filter for transient pop	16
Figure 23.	Turn-on diagnostic: working principle	17
Figure 24.	SVR and output behavior - case 1: without turn-on diagnostic	17
Figure 25.	SVR and output pin behavior - case 2: with turn-on diagnostic	18
Figure 26.	Short circuit detection thresholds	18
Figure 27.	Load detection thresholds - high gain setting	18
Figure 28.	Load detection thresholds - high gain setting	18
Figure 29.	Restart timing without diagnostic enable (permanent) each 1ms time, a sampling of the fault is done	19
Figure 30.	Restart timing with diagnostic enable (permanent)	19
Figure 31.	Current detection high: load impedance Z vs. output peak voltage	21
Figure 32.	Current detection low: load impedance Z vs. output peak voltage	21
Figure 33.	Worst case battery cranking curve sample 1	24
Figure 34.	Worst case battery cranking curve sample 2	24
Figure 35.	Upwards fast battery transitions diagram	25
Figure 36.	High efficiency - basic structure	27
Figure 37.	Data validity on the I ² C bus	28
Figure 38.	Timing diagram on the I ² C bus	29
Figure 39.	Timing acknowledge clock pulse	29
Figure 40.	PowerSO-36 (slug up) package mechanical drawing	34
Figure 41.	Flexiwatt 27 (vertical) package mechanical drawing	36
Figure 42.	Flexiwatt 27 (horizontal) package mechanical drawing	38
Figure 43.	Flexiwatt 27 (SMD) package mechanical drawing	40

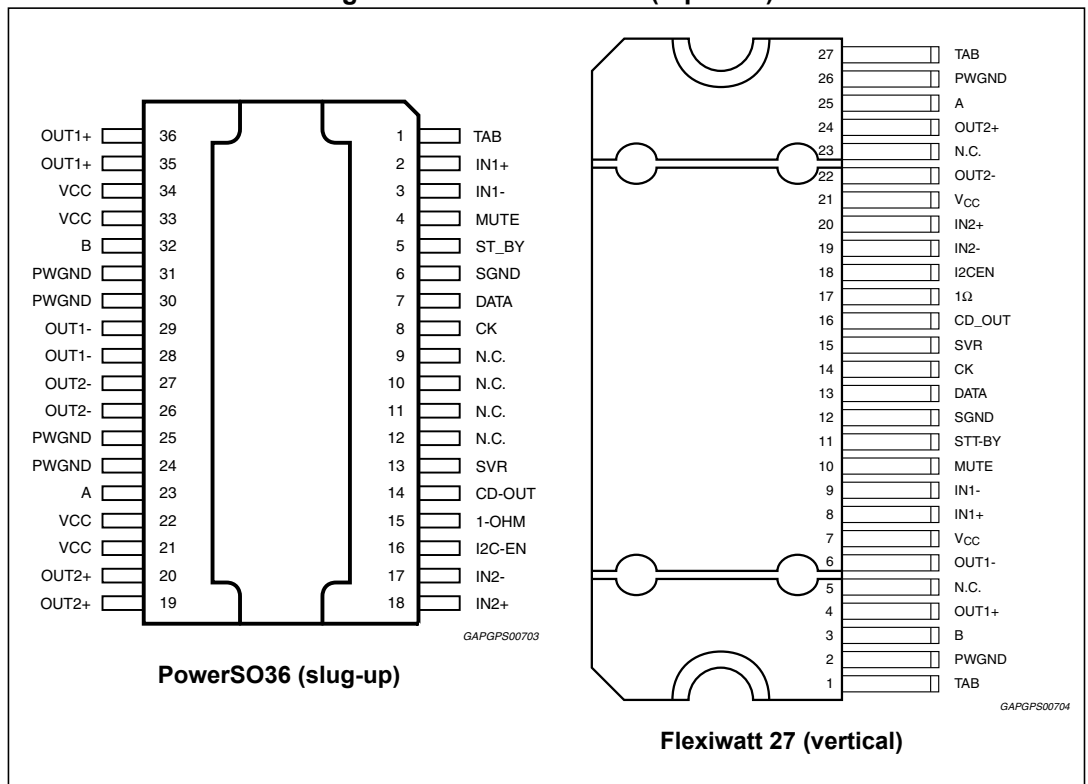
1 Block and pins diagrams

Figure 1. Block diagram



GAPGPS00702

Figure 2. Pin connections (top view)

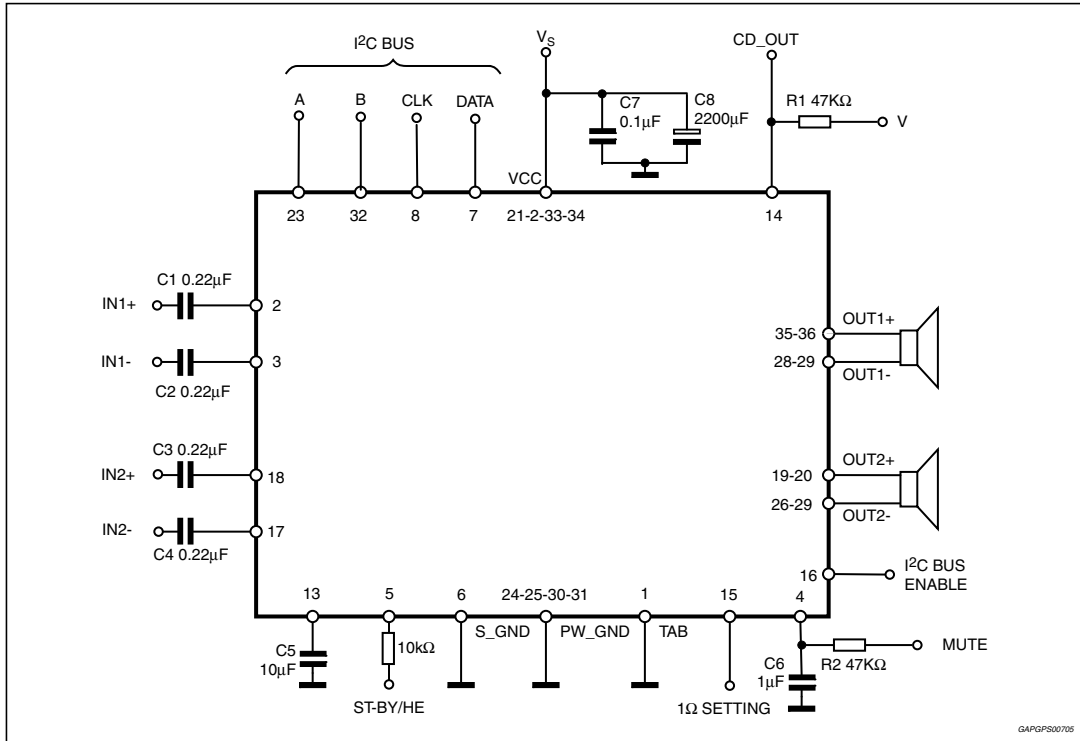


GAPGPS00703

GAPGPS00704

2 Application circuit

Figure 3. Application circuit (TDA7577BLVPD)



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{op}	Operating supply voltage	18	V
V _S	DC supply voltage	28	V
V _{peak}	Peak supply voltage (for t = 50 ms)	50	V
V _{CK} , V _{DATA}	I2C CK and DATA pin voltage	-0.3 to 6	V
GND _{max}	Ground pin voltage	-0.3 to 0.3	V
V _{st-by}	Standby pin voltage	-0.3 to V _{op}	V
V _{CP}	Clip detector voltage	-0.3 to V _{op}	V
V _{in max}	Input max voltage	-0.3 to V _{op}	V
I _O	Output peak current (not repetitive t = 100 ms)	8	A
I _O	Output peak current (repetitive f > 10 Hz)	6	A
P _{tot}	Power dissipation T _{case} = 70 °C ⁽¹⁾	86	W
T _{stg} , T _j	Storage and junction temperature ⁽²⁾	-55 to 150	°C
T _{amb}	Operative temperature range	-40 to 105	°C

1. This is maximum theoretical value; for power dissipation in real application conditions, please refer to curves reported in [Section 3.4: Electrical characteristics typical curves](#).
2. A suitable dissipation system should be used to keep T_j inside the specified limits.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	PowerSO36	Flexiwatt 27	Unit
R _{th j-case}	Thermal resistance junction-to-case Max	1	1	°C/W

3.3 Electrical characteristics

Refer to the test circuit, V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; G_V = 26 dB; T_{amb} = 25 °C; unless otherwise specified.

Tested at T_{amb} = 25 °C and T_{hot} = 105 °C; functionality guaranteed for T_j = -40 °C to 150 °C.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V _S	Supply voltage range	-	6	-	18	V
		R _L = 2 Ω	6	-	16	V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_d	Total quiescent drain current	-	-	140	200	mA
R_{IN}	Input impedance	-	100	115	140	k Ω
V_{AM}	Min supply mute threshold	Start-stop IB1(D7) = 0 (default)	5	-	6	V
		No start-stop IB1(D7) = 1	7	-	8	
V_{OS}	Offset voltage	Mute & play, standard bridge	-65	-	65	mV
I_{SB}	Standby current consumption	$V_{st-by} = 0$ V	-	1	5	μ A
PSRR	Power supply rejection ratio	$f = 100$ Hz to 10 kHz; $V_f = 1$ Vpk; $R_g = 600$ Ω	60	75	-	dB
T_{ON}	Turn on delay	D2 (IB1) 0 to 1	-	30	50	ms
T_{OFF}	Turn off delay	D2 (IB1) 1 to 0	-	30	50	ms
V_{MC}	Max. common mode input level	$f = 1$ kHz	-	-	1	V _{rms}
SR	Slew rate	-	2	4.5	-	V/ μ s
Audio performances						
P_o	Output power	Max. power ⁽¹⁾	40	45	-	W
		THD = 10 %	25	28	-	
		THD = 1 %	-	22	-	
		$R_L = 2$ Ω ; THD 10 %	45	50	-	W
		$R_L = 2$ Ω ; THD 1 %	-	40	-	
		$R_L = 2$ Ω ; Max. power ⁽¹⁾	70	78	-	
Single channel configuration (1 Ω pin >2.5 V); $R_L = 1$ Ω ; THD 3 %	Max. power ⁽¹⁾	80	85	-	W	
		140	155	-		
	Max. power ⁽¹⁾ , $V_s = 6$ V	-	6	-	W	
	Max. power ⁽¹⁾ , $V_s = 6$ V, $R_L = 1$ Ω ;	-	25	-	W	
THD	Total harmonic distortion	$P_O = 1-12$ W; STD MODE	-	0.04	0.1	%
		HE MODE; $P_O = 1-2$ W	-	0.03	0.1	
		HE MODE; $P_O = 4-8$ W	-	0.1	-	
		$P_O = 1-12$ W, $f = 10$ kHz, STD MODE	-	0.3	0.5	%
$R_L = 2$ Ω ; HE MODE; $P_o = 3$ W	-	0.05	0.5	%		
Single channel configuration (1 Ω pin > 2.5 V); $R_L = 1$ Ω ; $P_O = 4-30$ W	-	0.085	0.15	%		
C_T	Cross talk	$R_g = 600$ Ω ; $P_O = 1$ W	75	90	-	dB
G_{V1}	Voltage gain 1 (default)	-	25	26	27	dB
ΔG_{V1}	Voltage gain match 1	-	-1	-	1	dB
G_{V2}	Voltage gain 2	-	15	16	17	dB
ΔG_{V2}	Voltage gain match 2	-	-1	-	1	dB

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_{IN1}	Output noise voltage gain 1	$R_g = 600 \Omega$; $G_v = 26$ dB filter 20 to 22 kHz	-	45	60	μ V
E_{IN2}	Output noise voltage gain 2	$R_g = 600 \Omega$; $G_v = 16$ dB filter 20 to 22 kHz	-	20	30	μ V
BW	Power bandwidth	(-3 dB)	100	-	-	kHz
CMRR	Input CMRR	$V_{CM} = 1$ Vpk-pk; $R_g = 0 \Omega$	55	70	-	dB
ΔV_{OITU}	ITU Pop filter output voltage	Standby to Mute and Mute to Standby transition ITU-R 2K, $C_{svr} = 10 \mu$ F	-7.5	-	+7.5	mV
		Mute to Play transition: Low gain High gain ITU-R 2K ⁽²⁾	-7.5 -12	- -	+7.5 +12	mV mV
		Play to Mute transition Low gain High gain ITU-R 2K ⁽³⁾	-7.5 -12	- -	+7.5 +12	mV mV
Clip detector						
I_{CDH}	Clip pin high leakage current	CD off, $0 V < V_{CD} < 5.5 V$	-5	-	5	μ A
I_{CDL}	Clip pin low sink current	CD on; $V_{CD} < 300$ mV	1	-	-	mA
CD	Clip detect THD level	D0 (IB1) = 0	1	2	3	%
		D0 (IB1) = 1	5	10	15	%
Control pin characteristics						
V_{OFF}	ST-BY pin for standby ⁽⁴⁾	-	0	-	1.2	V
V_{SB}	ST-BY pin for standard bridge	-	2.6	-	5	V
V_{HE}	ST-BY pin for Hi-eff	-	7	-	18	V
$I_{O (ST-BY)}$	ST-BY pin current	$1.2 V < V_{st-by/HE} < 18 V$	-	150	200	μ A
	ST-BY pin current	$V_{stby} < 1.2 V$	-	1	5	μ A
V_m	Mute pin voltage for mute mode	-	0	-	1	V
	Mute pin voltage for play mode	-	2.6	-	18	V
I_m	Mute pin current (st_by)	$V_{mute} = 0 V, V_{st-by} < 1.2 V$	-5	-	5	μ A
	Mute pin current (operative)	$0 V < V_{mute} < 18 V, V_{st-by} > 2.6 V$	-	60	100	μ A
V_{I2C}	I ² C pin voltage for I ² C disabled	-	0	-	1.5	V
	I ² C pin voltage for I ² C enabled	-	2.5	-	18	V
I_{I2C}	I ² C pin current (standby)	$0 V < I^2C EN < 18 V, V_{stby} < 1.2 V$	-5	-	5	μ A
	I ² C pin current (operative)	$I^2C EN < 18 V, V_{st-by} > 2.6 V$	7	13	18	μ A

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{1\Omega}$	1 Ω pin voltage for 2ch mode	-	0	-	1.5	V
	1 Ω pin voltage for 1 Ω mode	-	2.5	-	18	V
$I_{1\Omega}$	1 Ω pin current (standby)	$0\text{ V} < 1\ \Omega < 18\text{ V}, V_{s\text{-tby}} < 1.2\text{ V}$	-5	-	5	μA
	1 Ω pin current (operative)	$1\ \Omega < 18\text{ V}, V_{s\text{-tby}} > 2.6\text{ V}$	7	13	18	μA
La	A pin voltage	Low logic level	0	-	1.5	V
Ha		High logic level	2.5	-	18	V
Ia	A pin current (ST-BY)	$0\text{ V} < A < 18\text{ V}, V_{s\text{-tby}} < 1.2\text{ V}$	-5	-	5	μA
	A pin current (operative)	$A < 18\text{ V}, V_{s\text{-tby}} > 2.6\text{ V}$	7	13	18	μA
Lb	B pin voltage	Low logic level	0	-	1.5	V
Hb		High logic level	2.5	-	18	V
Ib	B pin current (ST-BY)	$0\text{V} < B < 18\text{ V}, V_{s\text{tby}} < 1.2\text{ V}$	-5	-	5	μA
	B pin current (operative)	$B < 18\text{ V}, V_{s\text{-tby}} > 2.6\text{ V}$	7	13	18	μA
A_{SB}	Standby attenuation	-	90	100	-	dB
A_M	Mute attenuation	-	80	100	-	dB
Turn on diagnostics (Power amplifier mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in standby condition	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)	-	$V_s - 0.9$	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the Output is considered without faults).	-	1.8	-	$V_s - 1.5$	V
Lsc	Shorted load det.	-	-	-	0.5	Ω
Lop	Open load det.	-	85	-	-	Ω
Lnop	Normal load det.	-	1.5	-	45	Ω
Turn on diagnostics (Line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in standby	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)		$V_s - 0.9$	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the Output is considered without faults).		1.8	-	$V_s - 1.5$	V
Lsc	Shorted load det.		-	-	1.5	Ω
Lop	Open load det.		330	-	-	Ω

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Lnop	Normal load det.	Power amplifier in standby	4.5	-	180	Ω
Permanent diagnostics (Power amplifier mode or line driver mode)						
Pgnd	Short to GND det. (below this limit, the Output is considered in Short Circuit to GND)	Power amplifier in Mute or Play condition, one or more short circuits protection activated	-	-	1.2	V
Pvs	Short to Vs det. (above this limit, the Output is considered in Short Circuit to VS)	-	$V_s - 0.9$	-	-	V
Prop	Normal operation thresholds. (Within these limits, the Output is considered without faults).	-	1.8	-	$V_s - 1.5$	V
Lsc	Shorted load det.	Pow. amp. mode	-	-	0.5	Ω
		Line driver mode	-	-	1.5	Ω
VO	Offset detection	Power amplifier in play condition AC input signals = 0	±1.5	±2	±2.5	V
INLH	Normal load current detection	$V_O < (V_S - 5)\mu\text{k IB2 (D0) = 0}$	500	-	-	mA
INLL	Normal load current detection	$V_O < (V_S - 5)\mu\text{k IB2 (D0) = 1}$	250	-	-	mA
IOLH	Open load current detection	$V_O < (V_S - 5)\mu\text{k IB2 (D0) = 0}$	-	-	250	mA
IOLL	Open load current detection	$V_O < (V_S - 5)\mu\text{k IB2 (D0) = 1}$	-	-	125	mA
I²C bus interface						
f _{SCL}	Clock frequency	-	-	-	400	kHz
V _{IL}	Input low voltage	-	-	-	1.5	V
V _{IH}	Input high voltage	-	2.3	-	-	V

- Saturated square wave output.
- Voltage ramp on Mute pin: from 350 mV to 3.05 V in 40 ms. In case of I²C interface enabled command IB1(D2)=1 (Mute->Unmute) must be transmitted before to start the voltage ramp on Mute pin.
- Voltage ramp on Mute pin: from 2.8 V to 1.2 V in 40 ms. In case of I²C interface enabled the I²C command IB1(D2)=0 (Unmute->Mute) must be NOT transmitted before to start the voltage ramp on Mute pin.
- ST-BY pin high enables the I²C bus; ST-BY pin low enables ST-BY condition: detailed pin levels description is contained in paragraph 'I²C habilitation settings'.

3.4 Electrical characteristics typical curves

Figure 4. Quiescent drain current vs. supply voltage

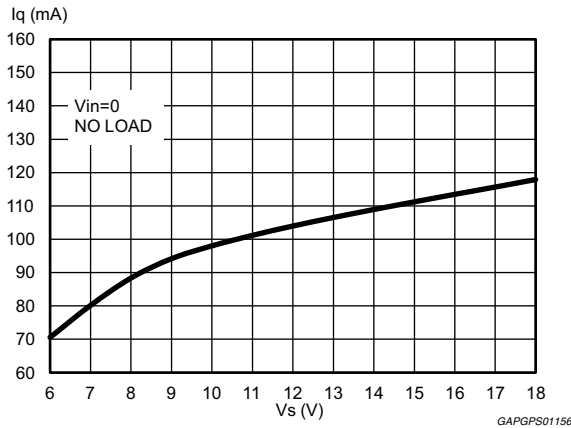


Figure 5. Output power vs. supply voltage (4 Ω)

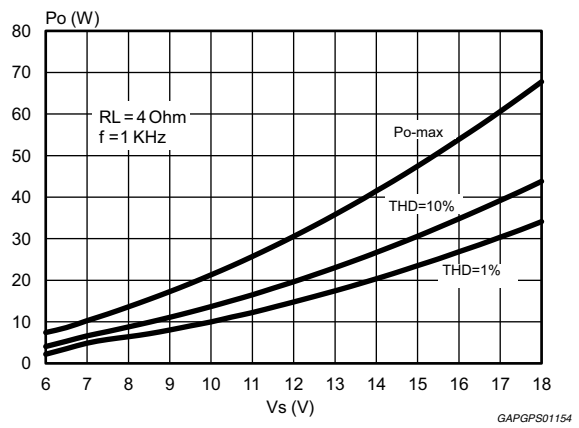


Figure 6. Output power vs. supply voltage (2 Ω)

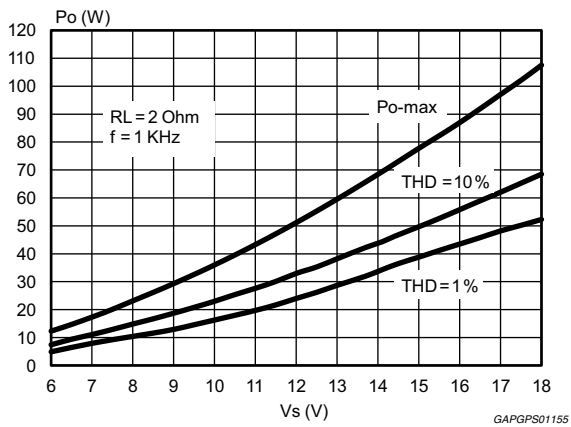


Figure 7. Output power vs. supply voltage (1 Ω)

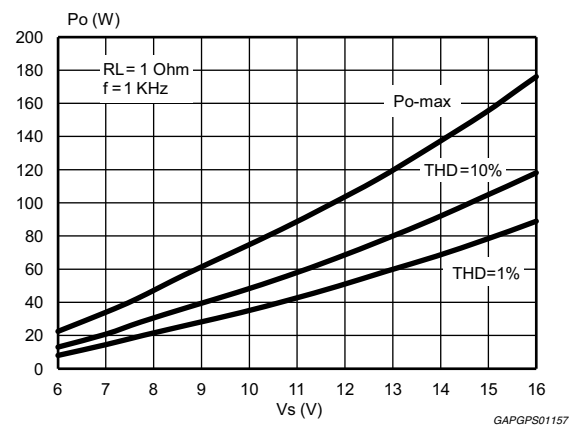


Figure 8. Distortion vs. output power (4 Ω , STD mode)

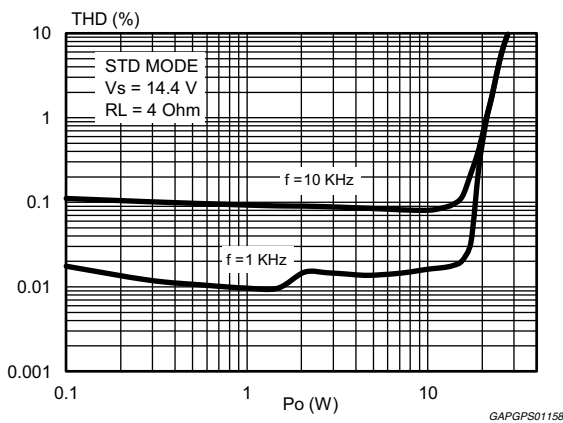


Figure 9. Distortion vs. output power (2 Ω , STD mode)

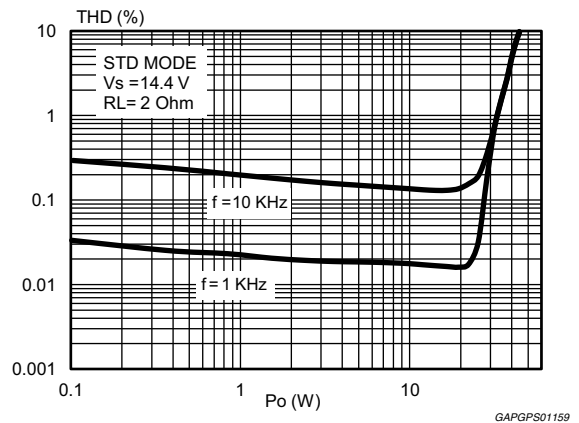


Figure 10. Distortion vs. output power (2 Ω, HI-EFF mode)

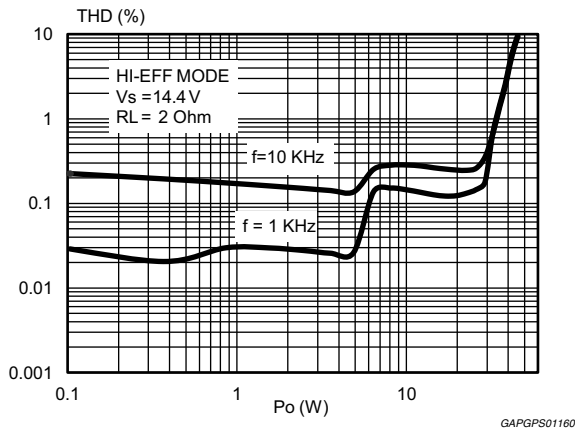


Figure 11. Distortion vs. output power (1 Ω, STD mode)

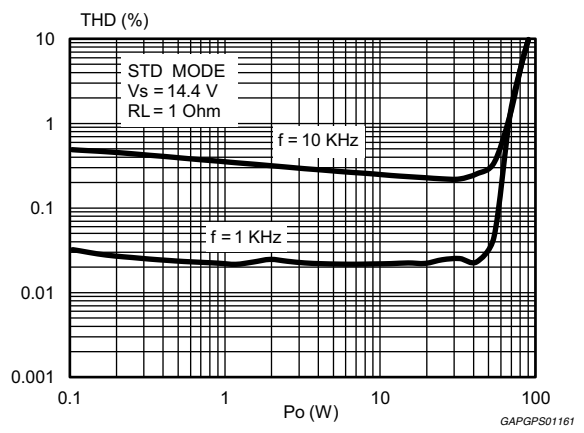


Figure 12. Distortion vs. frequency (4 Ω load)

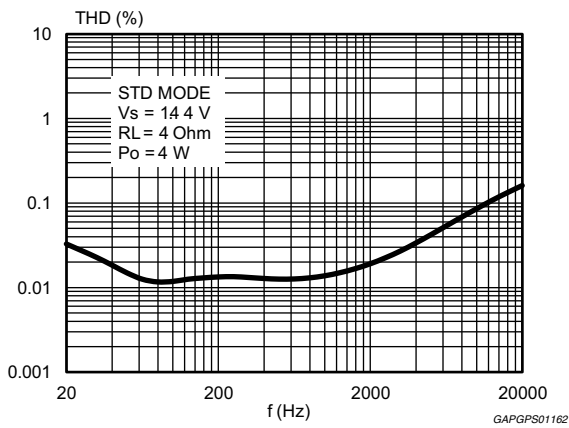


Figure 13. Distortion vs. frequency (2 Ω load)

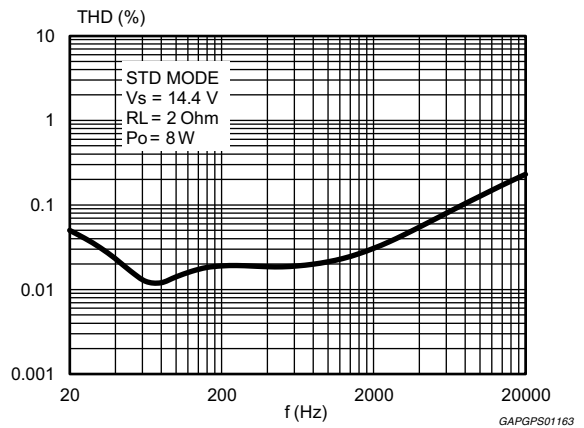


Figure 14. Distortion vs. frequency (1 Ω load)

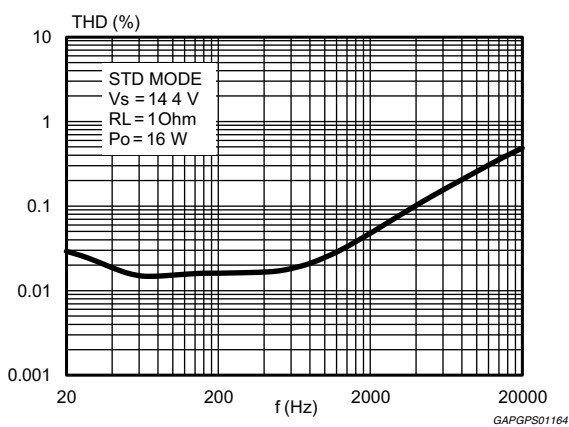


Figure 15. Output attenuation vs. supply voltage

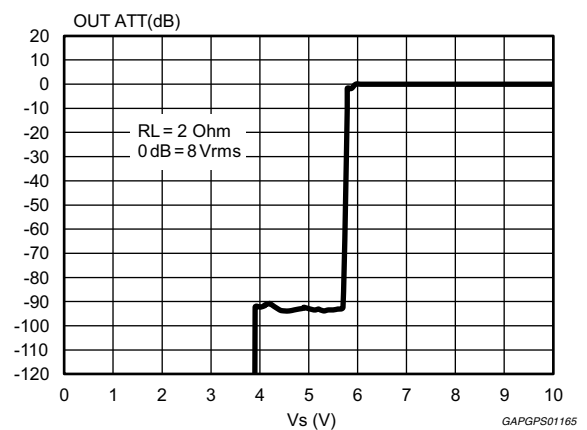


Figure 16. CMRR vs. frequency

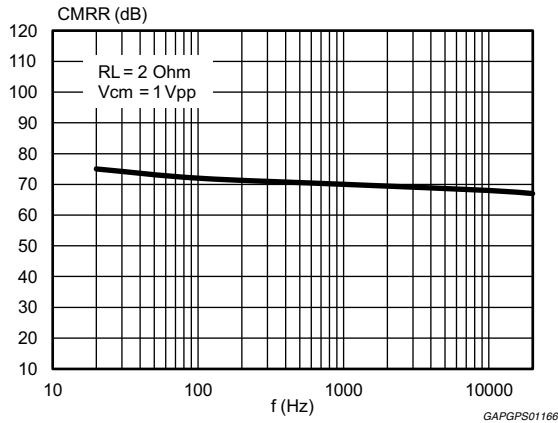


Figure 17. Cross talk vs frequency

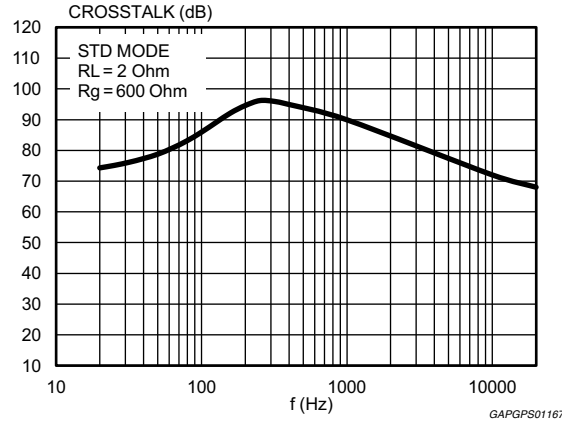


Figure 18. Power dissipation vs. average Po (2 Ω, STD mode, sine wave)

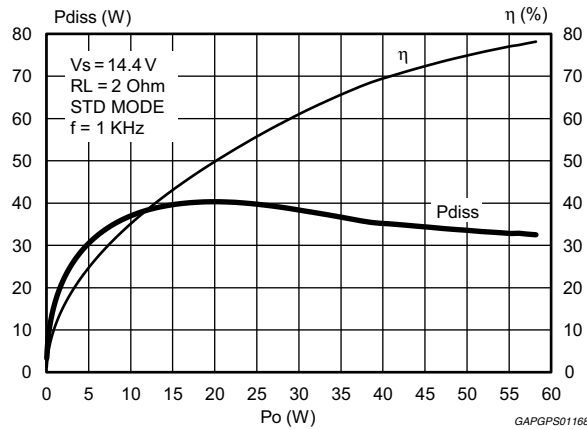


Figure 19. Power dissipation vs. Po (2 Ω, STD mode, audio program simulation)

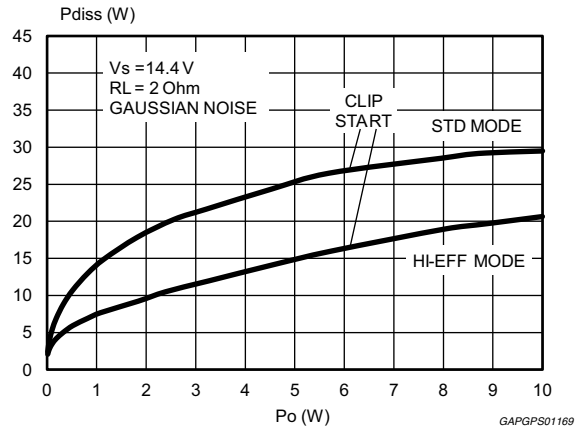


Figure 20. Power dissipation vs. average Po (2Ω, HI-EFF mode)

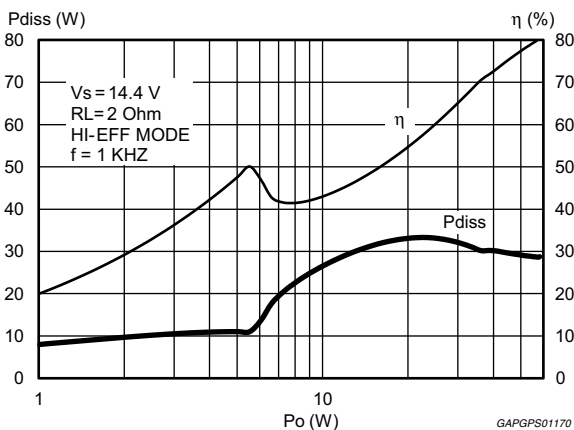


Figure 21. Power dissipation vs. Po (1 Ω, STD mode, audio program simulation)

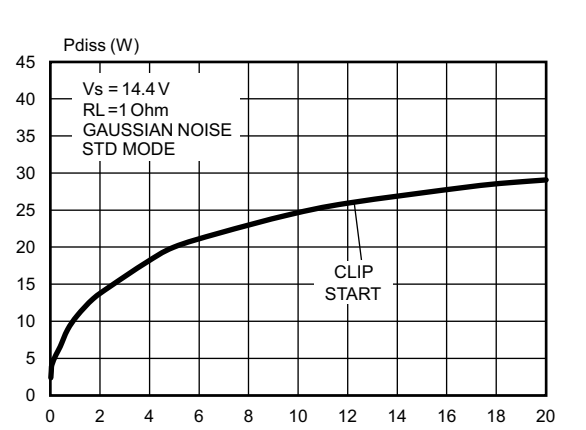
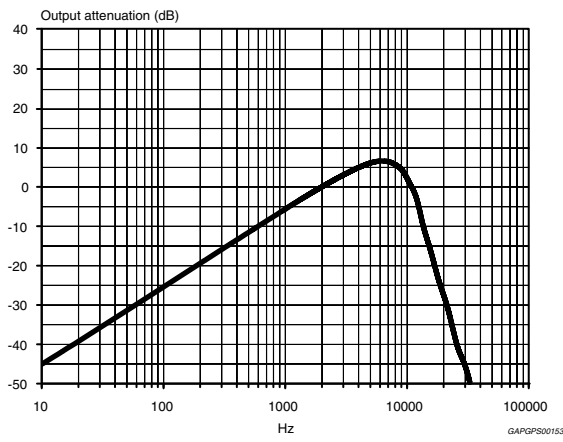


Figure 22. ITU R-ARM frequency response, weighting filter for transient pop



4 Diagnostics functional description

4.1 Turn-on diagnostic

It is strongly recommended to activate this function at the turn-on (standby out) through I²C bus request. Detectable output faults are:

- SHORT TO GND
- SHORT TO V_s
- SHORT ACROSS THE SPEAKER
- OPEN SPEAKER

To verify if any of the above misconnections is in place, a subsonic (inaudible) current pulse (Figure 23) is internally generated, sent through the speaker(s) and sunk back. The Turn-on diagnostic status is internally stored until a successive diagnostic pulse is requested (after a I²C reading).

If the "standby out" and "diag. enable" commands are both given through a single programming step, the pulse takes place first (during the pulse power stages stay off, showing high impedance at the outputs).

Afterwards, when the Amplifier is biased, the permanent diagnostic takes place. The previous turn-on state is kept until a short appears at the outputs.

Figure 23. Turn-on diagnostic: working principle

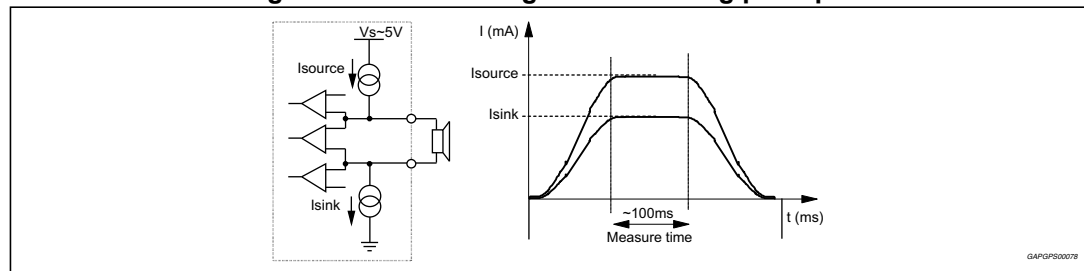


Fig. Figure 24 and Figure 25 show SVR and OUTPUT waveforms at the turn-on (standby out) with and without turn-on diagnostic.

Figure 24. SVR and output behavior - case 1: without turn-on diagnostic

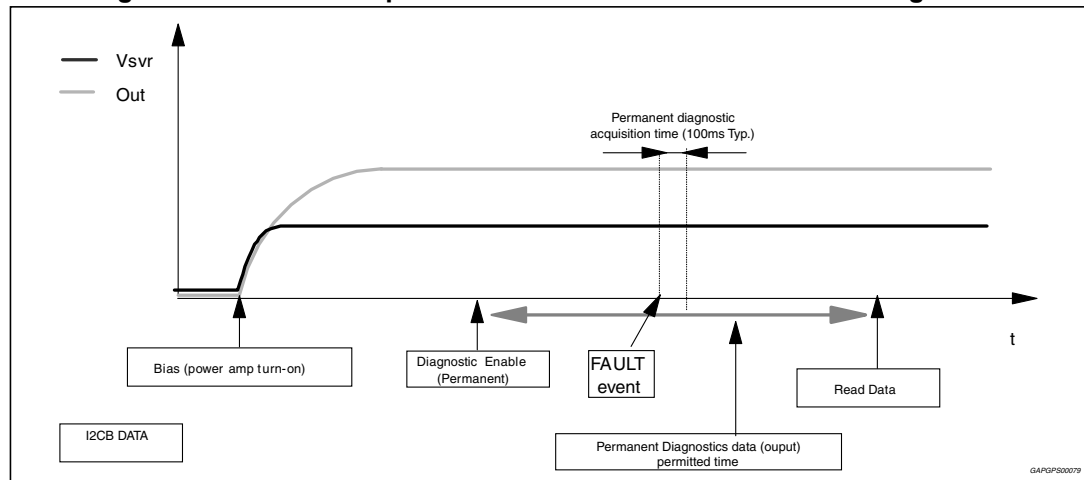
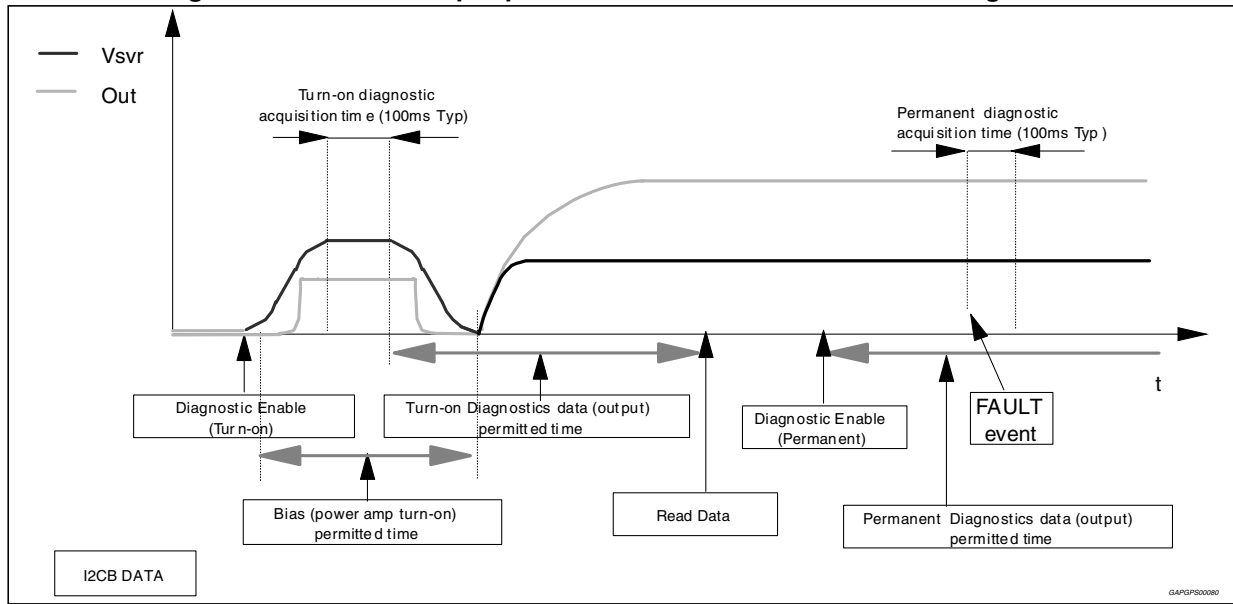
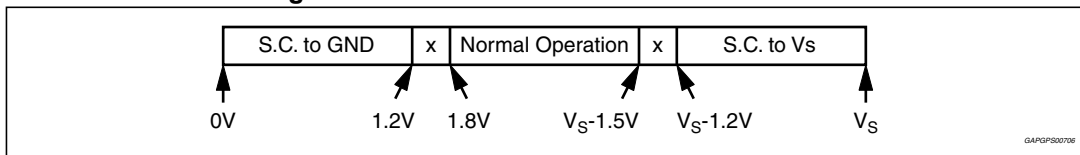


Figure 25. SVR and output pin behavior - case 2: with turn-on diagnostic



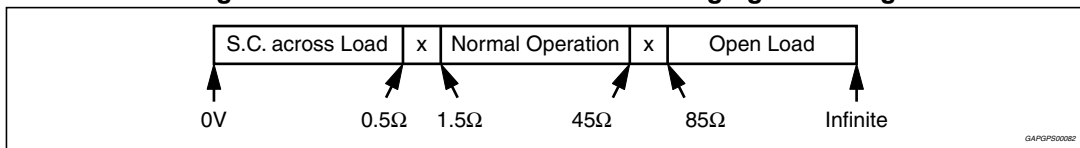
The information related to the outputs status is read and memorized at the end of the current pulse plateau. The acquisition time is 100 ms (typ.). No audible noise is generated in the process. As for SHORT TO GND / Vs the fault-detection thresholds remain unchanged from 26 dB to 16 dB gain setting. They are as follows:

Figure 26. Short circuit detection thresholds



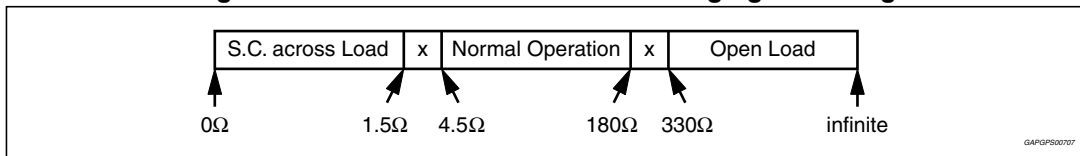
Concerning SHORT ACROSS THE SPEAKER / OPEN SPEAKER, the threshold varies from 26 dB to 16 dB gain setting, since different loads are expected (either normal speaker's impedance or high impedance). The values in case of 26 dB gain are as follows:

Figure 27. Load detection thresholds - high gain setting



If the Line-Driver mode (Gv = 16 dB and Line Driver Mode diagnostic = 1) is selected, the same thresholds will change as follows:

Figure 28. Load detection thresholds - high gain setting



4.2 Permanent diagnostics

Detectable conventional faults are:

- SHORT TO GND
- SHORT TO Vs
- SHORT ACROSS THE SPEAKER

The following additional feature is provided:

- OUTPUT OFFSET DETECTION

The TDA7577BLV has 2 operating status:

1. RESTART mode. The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the channel(s) interested is shut down. A check of the output status is made every 1 ms (*Figure 29*). Restart takes place when the overload is removed.
2. DIAGNOSTIC mode. It is enabled via I²C bus and it self activates if an output overload (such as to cause the intervention of the short-circuit protection) occurs to the speakers outputs. Once activated, the diagnostics procedure develops as follows (*Figure 30*):
 - To avoid momentary re-circulation spikes from giving erroneous diagnostics, a check of the output status is made after 1ms: if normal situation (no overloads) is detected, the diagnostic is not performed and the channel returns active.
 - Instead, if an overload is detected during the check after 1 ms, then a diagnostic cycle having a duration of about 100 ms is started.
 - After a diagnostic cycle, the audio channel interested by the fault is switched to RESTART mode. The relevant data are stored inside the device and can be read by the microprocessor. When one cycle has terminated, the next one is activated by an I²C reading. This is to ensure continuous diagnostics throughout the car-radio operating time.
 - To check the status of the device a sampling system is needed. The timing is chosen at microprocessor level (more than half a second is recommended).

Figure 29. Restart timing without diagnostic enable (permanent) each 1ms time, a sampling of the fault is done

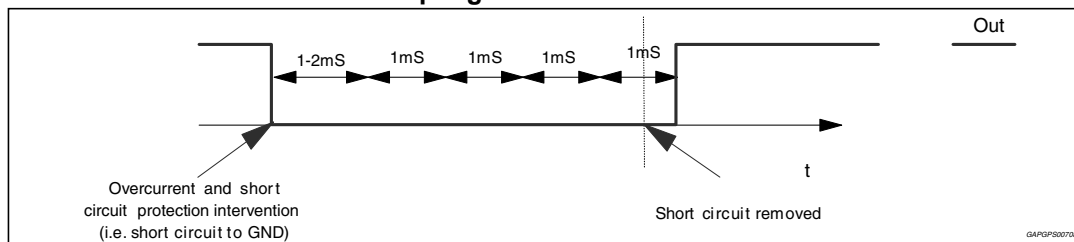
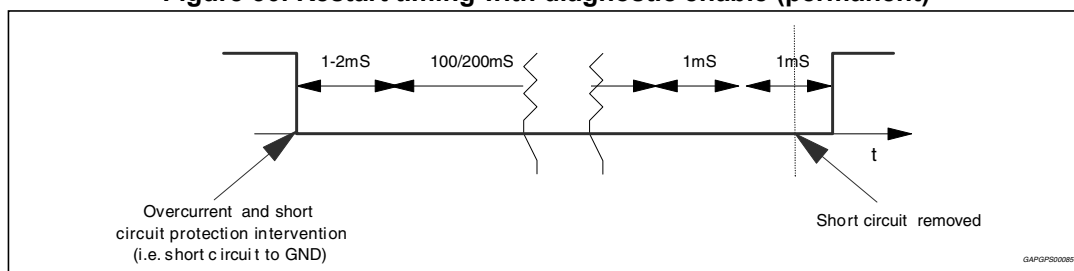


Figure 30. Restart timing with diagnostic enable (permanent)



4.3 Output DC offset detection

Any DC output offset exceeding ± 2 V is signalled out. This inconvenient might occur as a consequence of initially defective or aged and worn-out input capacitors feeding a DC component to the inputs, so putting the speakers at risk of overheating.

This diagnostic has to be performed with low-level output AC signal (or $V_{in} = 0$).

The test is run with selectable time duration by microprocessor (from a "start" to a "stop" command):

- START = Last reading operation or setting IB1 - D5 - (OFFSET enable) to 1
- STOP = Actual reading operation

Excess offset is signalled out if it is persistent for all the assigned testing time. This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

4.4 AC diagnostic

It is targeted at detecting accidental disconnection of tweeters in 2-way speaker and, more in general, presence of capacitively (AC) coupled loads.

This diagnostic is based on the notion that the overall speaker's impedance (woofer + parallel tweeter) will tend to increase towards high frequencies if the tweeter gets disconnected, because the remaining speaker (woofer) would be out of its operating range (high impedance). The diagnostic decision is made according to peak output current thresholds, and it is enabled by setting (IB2-D2) = 1. Two different detection levels are available:

- HIGH CURRENT THRESHOLD IB2 (D7) = 0
 $I_{out} > 500\text{mA}_{pk}$ = NORMAL STATUS
 $I_{out} < 250\text{mA}_{pk}$ = OPEN TWEETER
- LOW CURRENT THRESHOLD IB2 (D7) = 1
 $I_{out} > 250\text{mA}_{pk}$ = NORMAL STATUS
 $I_{out} < 125\text{mA}_{pk}$ = OPEN TWEETER

To correctly implement this feature, it is necessary to briefly provide a signal tone (with the amplifier in "play") whose frequency and magnitude are such as to determine an output current higher than 500 mA_{pk} with IB2(D7) = 0 (higher than 250 mA_{pk} with IB2(D7) = 1) in normal conditions and lower than 250 mA_{pk} with IB2(D7) = 0 (lower than 125 mA_{pk} with IB2(D7) = 1) should the parallel tweeter be missing.

The test has to last for a minimum number of 3 sine cycles starting from the activation of the AC diagnostic function IB2<D2> up to the I²C reading of the results (measuring period). To confirm presence of tweeter, it is necessary to find at least 3 current pulses exceeding the above threshold over all the measuring period, else an "open tweeter" message will be issued.

The frequency / magnitude setting of the test tone depends on the impedance characteristics of each specific speaker being used, with or without the tweeter connected (to be calculated case by case). High-frequency tones (> 10 kHz) or even ultrasonic signals are recommended for their negligible acoustic impact and also to maximize the impedance module's ratio between with tweeter-on and tweeter-off.

Figure 31 and 32 shows the load impedance as a function of the peak output voltage and the relevant diagnostic fields.

It is recommended to keep output voltage always below 8 V (high threshold) or 4 V (low threshold) to avoid circuit to saturate (causing wrong detection cases).

This feature is disabled if any overloads leading to activation of the short-circuit protection occurs in the process.

Figure 31. Current detection high: load impedance |Z| vs. output peak voltage

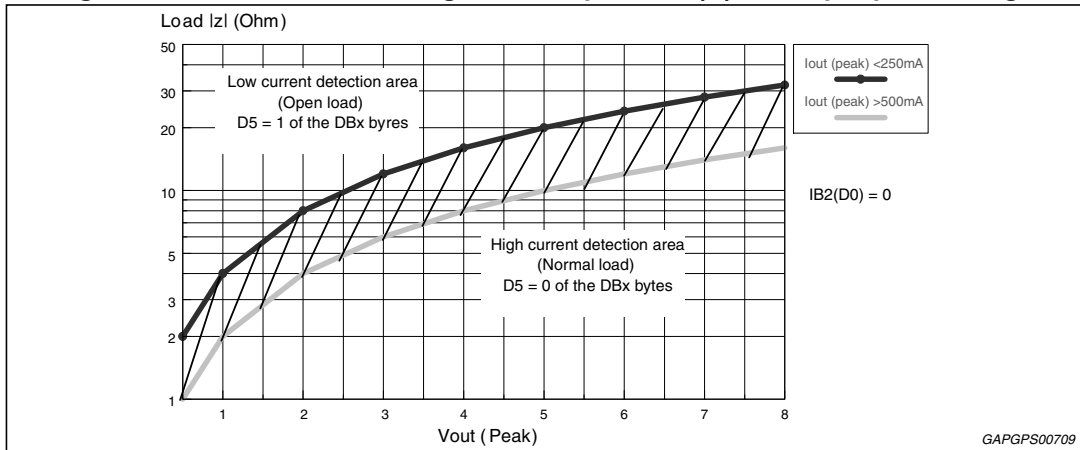
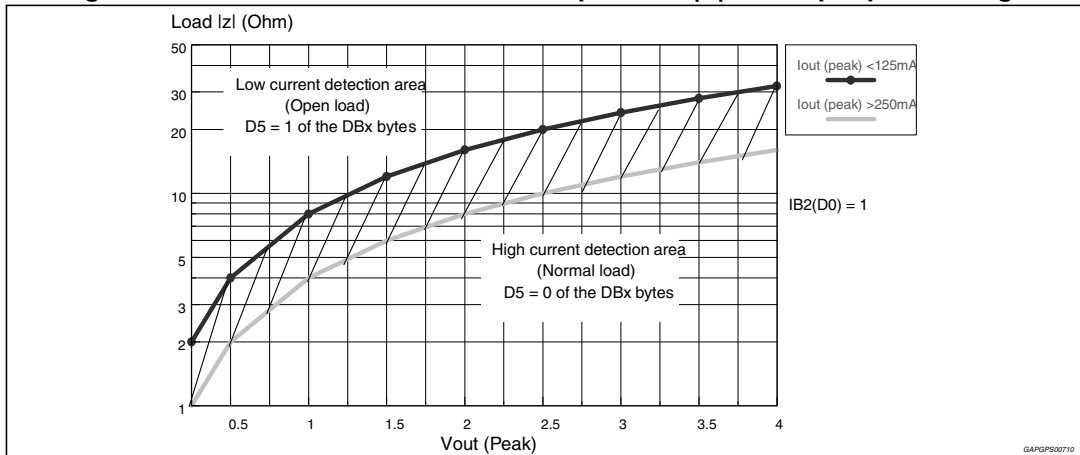


Figure 32. Current detection low: load impedance |Z| vs. output peak voltage



4.5 Multiple faults

When more misconnections are simultaneously in place at the audio outputs, it is guaranteed that at least one of them is initially read out. The others are notified after successive cycles of I²C reading and faults removal, provided that the diagnostic is enabled. This is true for both kinds of diagnostic (Turn on and Permanent).

The table below shows all the couples of double-fault possible. It should be taken into account that a short circuit with the 4 Ω speaker unconnected is considered as double fault.

Table 5. Double fault table for turn on diagnostic

	S. GND	S. Vs	S. Across L.	Open L.
S. GND	S. GND	S. Vs + S. GND	S. GND	S. GND
S. Vs	/	S. Vs	S. Vs	S. Vs
S. Across L.	/	/	S. Across L.	N.A.
Open L.	/	/	/	Open L. (*)

In Permanent Diagnostic the table is the same, with only a difference concerning Open Load(*), which is not among the recognizable faults. Should an Open Load be present during the device's normal working, it would be detected at a subsequent Turn on Diagnostic cycle (i.e. at the successive car radio turn-on).

4.6 Fault presence information availability on I²C

All the results coming from I²C bus, by read operations, are the consequence of measurements inside a defined period of time. If the fault is stable throughout the whole period, it will be sent out. This is true for DC diagnostic (Turn-on and Permanent), for offset detector.

To guarantee always resident functions, every kind of diagnostic cycles (turn-on, Permanent, Offset) will be reactivated after any I²C reading operation. Each I²C read-out done by the microcontroller will enable a new diagnostic cycle, but the read data will come from the previous diagnostic cycle (i.e. The device is in turn-on state, with a short to GND, then the short is removed and micro reads I²C. The short to GND is still present in bytes, because it is the result of the previous cycle. If another I²C reading operation occurs, the bytes do not show the short). In general to observe a change in diagnostic bytes, two I²C reading operations are necessary.

5 1 Ω load capability setting

It is possible to drive 1 Ω load paralleling the outputs into a single channel.

In order to implement this feature, outputs should be connected as follows:

OUT1+ shorted to OUT2+

OUT1- shorted to OUT2-.

It is recommended to minimize the impedance on the board between OUT2 and the load in order to minimize THD distortion. It is also recommended to control the maximum mismatch impedance between V_{CC} pins (PIN21/PIN22 respect to PIN33/PIN34) and between PWGND pins (PIN24/PIN25 respect to PIN30/PIN31), mismatch that must not exceed a value of 20 m Ω .

With 1 Ω feature settled the active input is IN2 (PIN17 and PIN18), therefore IN1 pins should be let floating.

It is possible to set the load capability acting on 1 Ω pin as follows:

1 Ω PIN < 1.2V: two channels mode (for a minimum load of 2 Ω)

1 Ω PIN > 2.6V: one channel mode (for 1 Ω load).

It is to remember that 1 Ω function is a hardware selection.

Therefore it is recommended to leave 1 Ω pin floating or shorted to GND to set the two channels mode configuration, or to short 1 Ω pin to V_{CC} to set the one channel (1 Ω) configuration.

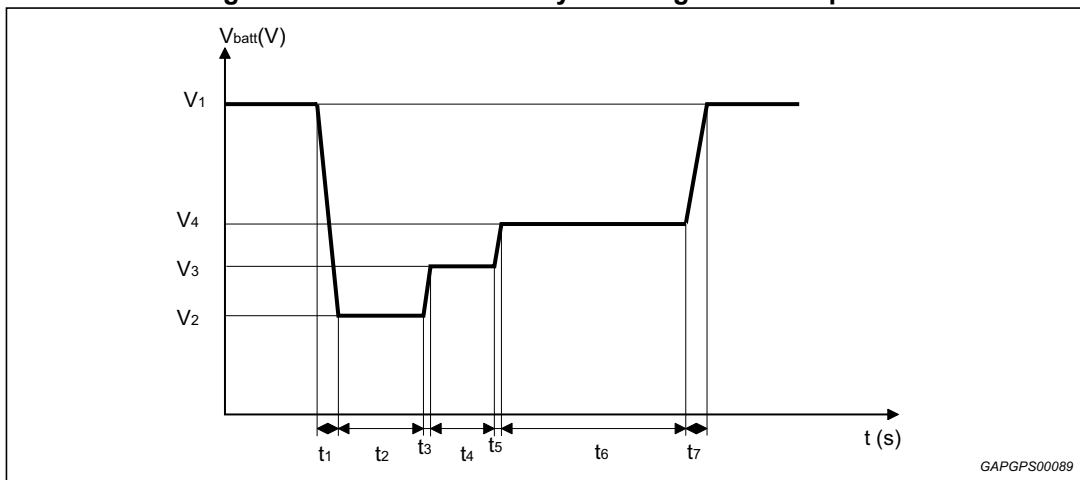
6 Battery transitions management

6.1 Low voltage operation (“start stop”)

The most recent OEM specifications require automatic stop of car engine at traffic light, in order to reduce emissions of polluting substances. The TDA7577BLV, thanks to its innovating design, is able to play when battery falls down to 6/7 V during such conditions, without producing audible pop noise. The maximum system power will be reduced accordingly.

Worst case battery cranking curves are shown below, indicating the shape and duration of allowed battery transitions.

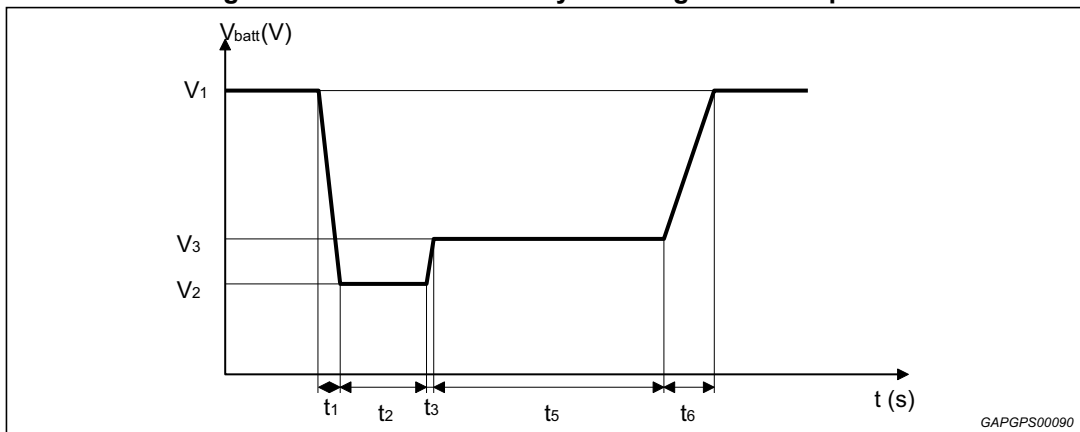
Figure 33. Worst case battery cranking curve sample 1



$V_1 = 12\text{ V}; V_2 = 6\text{ V}; V_3 = 7\text{ V}; V_4 = 8\text{ V}$

$t_1 = 2\text{ ms}; t_2 = 50\text{ ms}; t_3 = 5\text{ ms}; t_4 = 300\text{ ms}; t_5 = 10\text{ ms}; t_6 = 1\text{ s}; t_7 = 2\text{ ms}$

Figure 34. Worst case battery cranking curve sample 2



$V_1 = 12\text{ V}; V_2 = 6\text{ V}; V_3 = 7\text{ V}$

$t_1 = 2\text{ ms}; t_2 = 5\text{ ms}; t_3 = 15\text{ ms}; t_5 = 1\text{ s}; t_6 = 50\text{ ms}$

6.2 Advanced battery management

In addition to compatibility with low V_{batt} , the TDA7577BLV is able to sustain upwards fast battery transitions (like the one showed in [Figure 35](#)) without causing unwanted audible effect, thanks to the innovative circuit topology.

Figure 35. Upwards fast battery transitions diagram

