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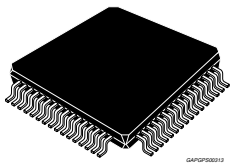
TDA7786
TDA7786M

ELITE automotive tuners for AM/FM car-radio

Datasheet - production data



LQFP64

Features

- AEC-Q100 qualified
- FM, AM and weather band reception
- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- Integrated AM LNA and PIN diodes
- Automatic self alignment for FM front-end pre-selection filter and image rejection
- Integrated IF filters with high selectivity, dynamic range and adaptive bandwidth control
- Drift-free Digital-IF signal processing with high performance
- RDS demodulation with group and block synchronization
- High performance stereo decoder with noise-blanker
- Digital interface for HD Radio™ reception with digital audio blending
- I^2C bus-controlled
- I^2S input/output digital audio interfaces
- Single 5 V supply
- LQFP64 package
- MuSICA (multipath noise reduction) algorithm available for premium version of the device

Description

The TDA7786x (ELITE) tuner is an optimized high-performance AM/FM tuner IC family for car-radio applications, suitable also (in combination with an external baseband decoder) for HD Radio™ reception.

Its members integrate mixers and IF amplifiers for AM, FM and WX, fully integrated VCO and PLL synthesizer, IF- processing including adaptive bandwidth control, stereo decoder, RDS decoder, and digital interfaces for external HD Radio™ decoding on a single IC.

AM/FM IBOC base band filtering is available in parallel to standard analog reception.

The utilization of digital signal processing results in numerous advantages: very low number of external components, very small space occupation and easy application, very high selectivity due to digital filters, high customization possibility through software control, automatic alignment and a powerful DSP for custom processing.

Two versions of the device cover different application/performance requirements:

TDA7786: entry-level, high-performance tuner;

TDA7786M: tuner with enhanced behavior in case of FM multipath, thanks to the proprietary MuSICA algorithm.

Both versions are HW- and SW-compatible.

Table 1. Device summary

Order code	Package	Packing
TDA7786	LQFP64 (10x10x1.4mm)	Tray
TDA7786M		

Contents

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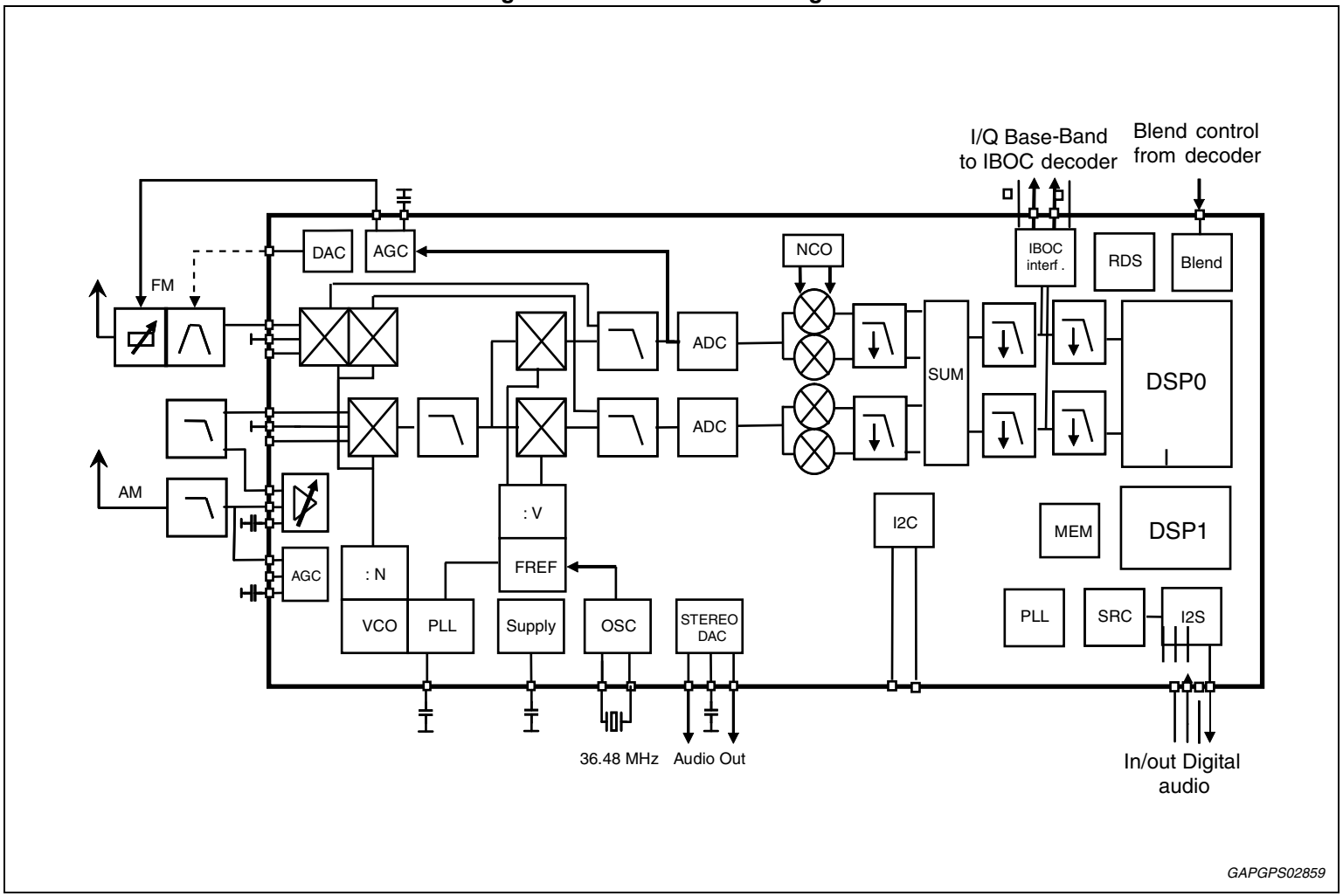
List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

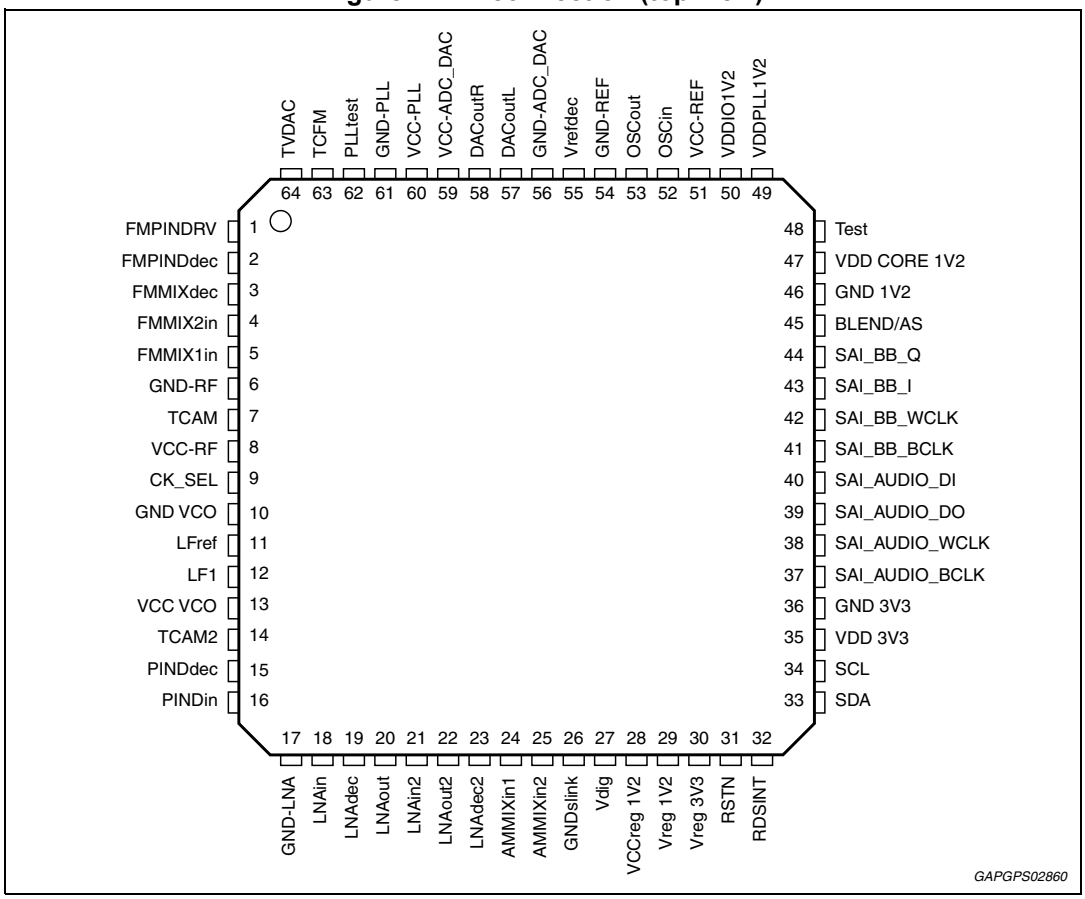


Table 2. Pin description

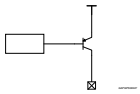
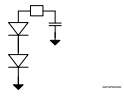
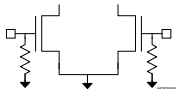
Pin	Pin name	I/O	Function	Description	Equivalent circuit
1	FMPINDRV	Out	FM	FM PIN diode driver output	
2	FMPINDdec	In		Integrated FM PINdiode decoupling	
3	FMMIXdec	-		FM RF signal ground	
4	FMMIXin2	In		FM mixer input 2	
5	FMMIXin1	In		FM mixer input 1	
6	GNDRF	-	-	RF power ground	-

Table 2. Pin description (continued)

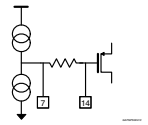
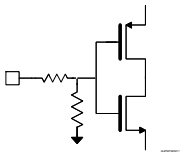
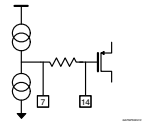
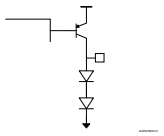
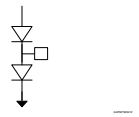
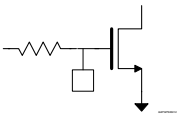
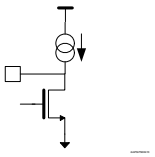
Pin	Pin name	I/O	Function	Description	Equivalent circuit
7	TCAM	-	-	AM AGC time constant	
8	VCCRF	In	-	RF 5 V supply	-
9	CK_SEL	In	-	Master/Slave clock operation select	
10	GNDVCO	-	VCO	VCO ground	-
11	LFref	-		Loop filter reference	-
12	LF1	-		Loop filter output	-
13	VCCVCO	In		VCO 5V supply	-
14	TCAM2	-		AM AGC 2nd order time constant	
15	PINDdec	-	AM pin diode	AM AGC internal PIN diode decoupling	
16	PINDin	-		AM AGC internal PIN diode input	
17	GNDLNA	-	AM LNA	AM LNA ground	-
18	LNAin	In		AM LNA input	
19	LNAdec	-		AM LNA decoupling	
20	LNAout	Out		AM LNA output	-
21	LNAin2	-		AM LNA input 2nd stage	-

Table 2. Pin description (continued)

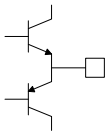
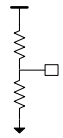
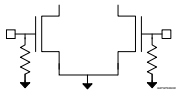
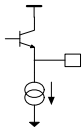
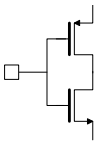
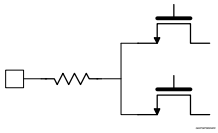
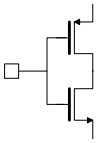
Pin	Pin name	I/O	Function	Description	Equivalent circuit
22	LNAout2	-	AM LNA	AM LNA output 2nd stage	
23	LNAdec2	-		AM LNA decoupling 2nd stage	
24	AMMIXin1	In	AM mixer inputs	AM mixer input 1	
25	AMMIXin2	In		AM mixer input 2	
26	GNDSLINK	-	Supply, ground and reset	Internal inter-IC communication bus ground	-
27	Vdig	In		Front-end digital 5 V supply	-
28	VCCreg1V2	In		Internal 1.2 V regulator 5 V supply	-
29	REG1V2	Out		Internal 1.2 V regulator output	
30	Vreg3v3	Out		Internal 3.3 V regulator output	
31	RSTN	In		Reset (low active) Pull-up 50 kΩ to 3.3 V IO supply	
32	RDSINT	Out		RDS interrupt output Pull-down 50 kΩ to ground	-
33	SDA	In/Out	I2C interface	I2C bus data Pull-up 50 kΩ to 3.3 V IO supply	
34	SCL	In		I2C bus clock Pull-up 50 kΩ to 3.3 V IO supply	
35	VDD3V3	In	-	IO ring (3.3 V) supply	-
36	GND3V3	-	-	IO ring (3.3 V) supply	-

Table 2. Pin description (continued)

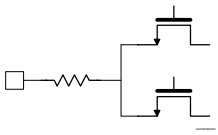
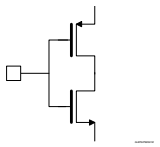
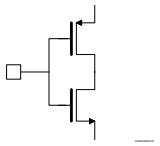
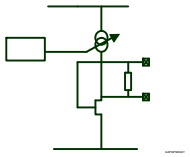
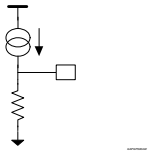
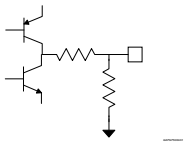
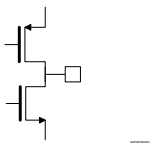
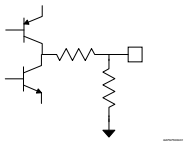
Pin	Pin name	I/O	Function	Description	Equivalent circuit
37	SAI_AUDIO_BCLK	In/Out	HD Radio™ connectivity/ Audio output I2S interface	SAI clk Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
38	SAI_AUDIO_WCLK	In/Out		Audio SAI word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
39	SAI_AUDIO_DO	Out		Audio SAI data output Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
40	SAI_AUDIO_DO	In		Audio SAI data-input Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
41	SAI_BB_BCLK	In/Out		SAI Base-Band clock Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
42	SA_BB_WCLK	In/Out		SAI Base-Band word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
43	SAI_BB_I	Out		SAI Base-Band I data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
44	SAI_BB_Q	Out		SAI Base-Band Q data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
45	BLEND/AS	In		HD blend input Pull-down 50 kΩ to ground	
46	GND1V2	-	-	DSP core ground	-
47	VDD core 1V2	In	-	DSP core 1.2 V supply	-
48	Test	In	-	Test Mode Pull-down 50 kΩ to ground	
49	VDDPLL1V2	In	-	Digital PLL 1.2 V supply	-
50	VDDIO1V2	In	-	Internal inter-IC communication 1.2 V supply	-
51	VCC-REF	In	-	Front-end reference frequency and regulator 5 V supply	-

Table 2. Pin description (continued)

Pin	Pin name	I/O	Function	Description	Equivalent circuit
52	OSCin	In	Oscillator	Crystal oscillator input	-
53	OSCout	Out		Crystal oscillator output	
54	GND-REF	-	-	Front-end reference frequency and regulator ground	-
55	Vrefdec	-	-	3.3 V Bias generation decoupling	
56	GND-ADC_DAC	-	DAC	IFADC and audio DAC ground	-
57	DACoutL	Out		Audio output left	
58	DACoutR	Out		Audio output right	
59	VCC-ADC_DAC	In		IFADC and audio DAC 5 V supply	-
60	VCC-PLL	In	PLL	Tuning PLL 5 V supply	-
61	GND-PLL	-		Tuning PLL ground	-
62	PLLtest	Out		PLL Test output	
63	TCFM	-	-	FM AGC time constant	
64	TVDAC	Out	-	Tuning voltage output	-

2 Function description

2.1 FM - mixers

The FM Image Rejection mixer has two single ended inputs, selectable through software. They are designed to achieve best performance both in case of a passive tuned preselection and of a passive fixed band-pass preselection without tuning for lower cost applications.

The input frequency is down-converted to very low IF with high image rejection.

The tuned application is supported by an 8-bit tuning DAC. The alignment of the DAC is performed automatically on-chip.

2.2 FM - AGC

The programmable RFAGC senses the mixer input to avoid overload.

When the RFAGC threshold is reached, the PIN diode output is activated in order to attenuate the incoming RF signal

The PIN diode driver is able to drive external PIN diodes with up to 15 mA current.

The time constant of the FM AGC is defined by the combination of an external capacitor and internal currents. There are two programmable attack and decay time constants.

2.3 AM - LNA

The integrated AM LNA feature is integrated with low-noise and high IIP2 and IIP3. The gain of the LNA is controlled by the AGC. The maximum gain is set with an external resistor, typically 26 dB with 470 Ω.

2.4 AM - AGC

The programmable AM RFAGC senses the mixer inputs and controls the internal PIN diodes and LNA gains.

Firstly the LNA gain is reduced by about 10 dB, and then the PIN diodes are activated to further attenuate the signal.

The time constant of the 2^{nd} order AM AGC LPF is defined by both external components and programmable internal currents.

2.5 AM - Mixers

The image rejection mixer has two AM inputs selectable via software. It easily supports low-cost applications for extended frequency bands like short-waves.

The input frequency is converted to low IF with high image rejection.

2.6 IF A/D converters

A high performance IQ-IFADC converts the IF signal to the digital domain for subsequent digital signal processing.

Two fully differential, continuous-time Sigma-Delta (ΣΔ) IF-ADCs are used for both the 'I' path and the 'Q' path. For each IFADC, two fully differential input nodes are fed with an input signal having a bandwidth up to 325 kHz. This fully differential design provides good suppression of even-order harmonics. For complex filtering, the input signals of the 'I' path and the 'Q' path have a 90 degree phase shift. The IFADC sampling frequency is 36.48 MHz.

2.7 Audio D/A converters

A CD-quality (>100dB DR) stereo DAC provides the left/right audio signals after IF processing and stereo-decoding by the DSP. In presence of an external HD Radio™ decoder the DAC delivers the high quality audio resulting from the decoding of the HD Radio™ transmissions.

2.8 VCO

The VCO is fully integrated without any external tuning component. It covers all the FM frequency bands including EU, US, Japan, East-Europe, Weather-Band and the AM bands including LW, MW and SW. Its center frequency is approximately 2.7 GHz.

2.9 PLL

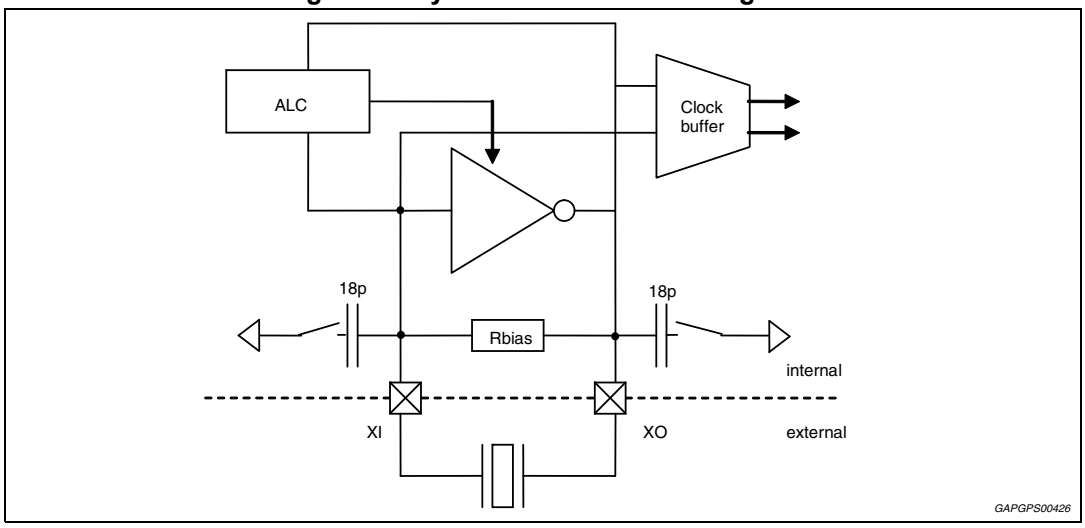
2.9.1 Tuner PLL

The very high-speed tuning PLL is able to settle within about 100 µs for fast RDS applications. The frequency step can be as low as 5 kHz in FM and 500 Hz in AM.

2.10 Crystal oscillator

The device works with a 36.48 MHz fundamental tone crystal. The oscillator block diagram is shown in *Figure 3*. On the PCB the crystal must be connected as close as possible to the chip oscillator input and output pins of the chip. The internal load capacitance together with pin and pad capacitance is optimized for fundamental tone crystal units at 36.48 MHz. It is not recommended to put any additional external load capacitors. By suitably configuring pin #9 (CK_SEL), the device can be operated as either a clock master or a clock slave. If pin 9 is left open or tied to GND, the device is configured as clock master (typical operation mode). In case the device is configured as clock slave, pin 9 needs to be connected to 5 V. Then the crystal oscillator is switched off and the device expects a crystal equivalent signal on the OSCout/OSCin pins.

Figure 3. Crystal oscillator block diagram



2.11 DSP and digital hardware accelerators

The TDA7786x embeds two DSP cores for high computational power and achievable customization. The DSP cores, in combination with the hardware accelerators, take care of all the tuner digital signal processing. The main program is fixed in ROM. Control parameters are copied to RAM and are accessible and modifiable there, thus allowing a parametric performance optimization. The operations performed by the DSP cores and HW accelerators are:

- digital down-conversion of IF
- bandwidth selection with variable controlled bandwidth
- FM and AM noise blanking
- FM/AM demodulation with soft-mute, high-cut, weak signal processing and quality detection
- FM stereo decoding with stereo-blend
- RDS demodulation including error correction and block synchronization with generation of an RDS interrupt for the main µP
- Autonomous control of RDS-AF tests
- Self-alignment of pre-selection tuning

2.12 Digital high speed IO interface pins

The IC has several IOs tasked for connectivity to an external HD Radio™ decoder and/or to I^2S audio sources and destinations (pins 37 to 44).

These pins are driven by a special buffer that has been developed to reduce disturbance originating from activity on the digital lines. This bidirectional buffer is based on a TTL Schmitt trigger receiver and a slew-rate controlled driver with programmable cut-off frequency and current capability.

Typical configurations of these IOs for both analog and digital-HD reception are indicated in *Table 3*; for the suggested configuration all the slew-rate controlled pads are programmed with a 10 MHz cut-off frequency:

Table 3. Suggested GPIO direction and driving capability

Pin	Use case: HD reception	Use case: digital audio out	Driving capability	
			10 pF	5 pF
37	IN	OUT		X
38	IN	OUT		X
39	OUT	OUT		X
40	IN	IN		X
41	OUT	-	X	
42	OUT	-		X
43	OUT	-	X	
44	OUT	-	X	

In case a different GPIO configuration is used, it is recommended to connect the TDA7786x to an externally regulated 3.3 V source.

2.13 Multipath reduction

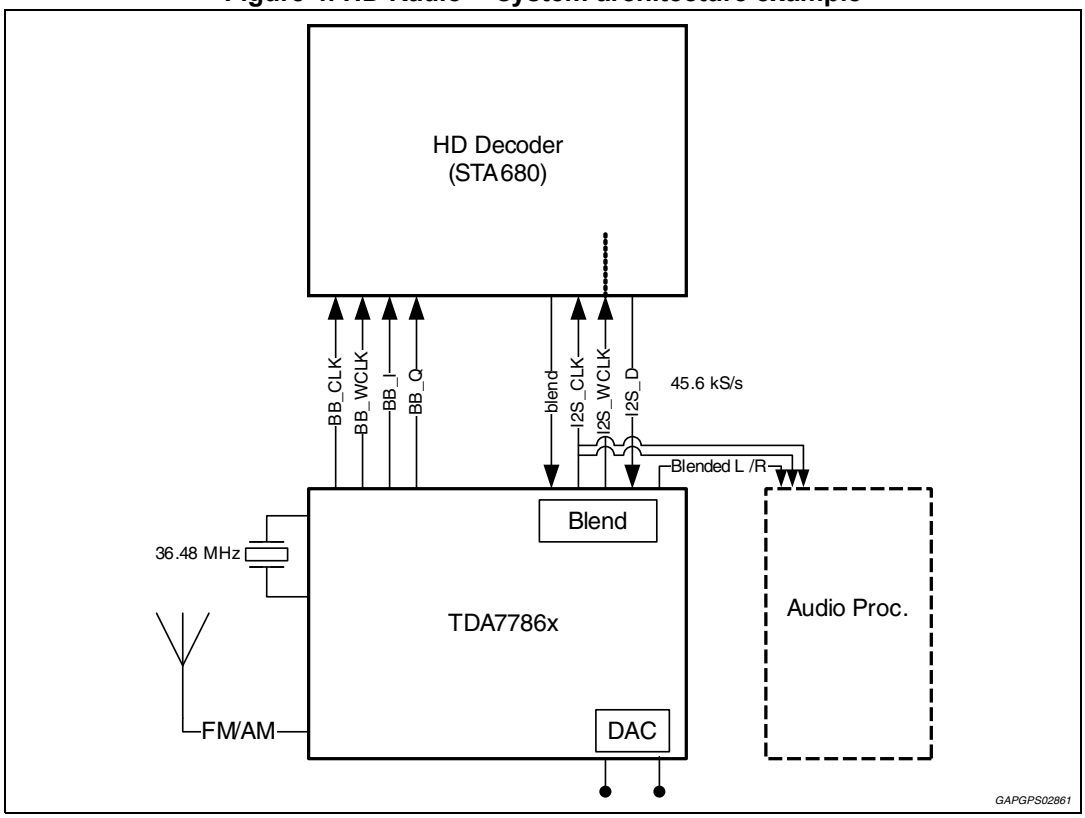
The TDA7786 is equipped with a basic FM multipath noise reduction system in addition to the traditional weak signal processing. The algorithm, called DANCE, assures an improved performance in presence of in-band interference (such as in case of multipath).

The premium version of the ELITE family, the TDA7786M is equipped with a superior algorithm, called MuSICA, to further enhance the reception quality even in presence of strong multipath.

2.14 HD Radio™ connectivity

The ELITE complies with HD Radio™ interface specifications as per Ibiquity's 'RX_SSS_1108 HD Radio™ power efficient RF-IF and peripheral processing (power RIPP) specification', thus providing an external HD Radio™ decoder with I/Q base-band signals and receiving the decoded digital audio from it, as shown in *Figure 4*.

Figure 4. HD Radio™ system architecture example



The complex baseband signal of an IBOC transmission is sent to the external decoder using the dedicated digital output interface SAI_BB. The SAI_BB supports the modes shown in both *Figure 5* and *Figure 6*. Timing information for the protocols shown is detailed in *Table 4* and *Table 5*.

Figure 5. SAI_BB waveforms (normal mode)

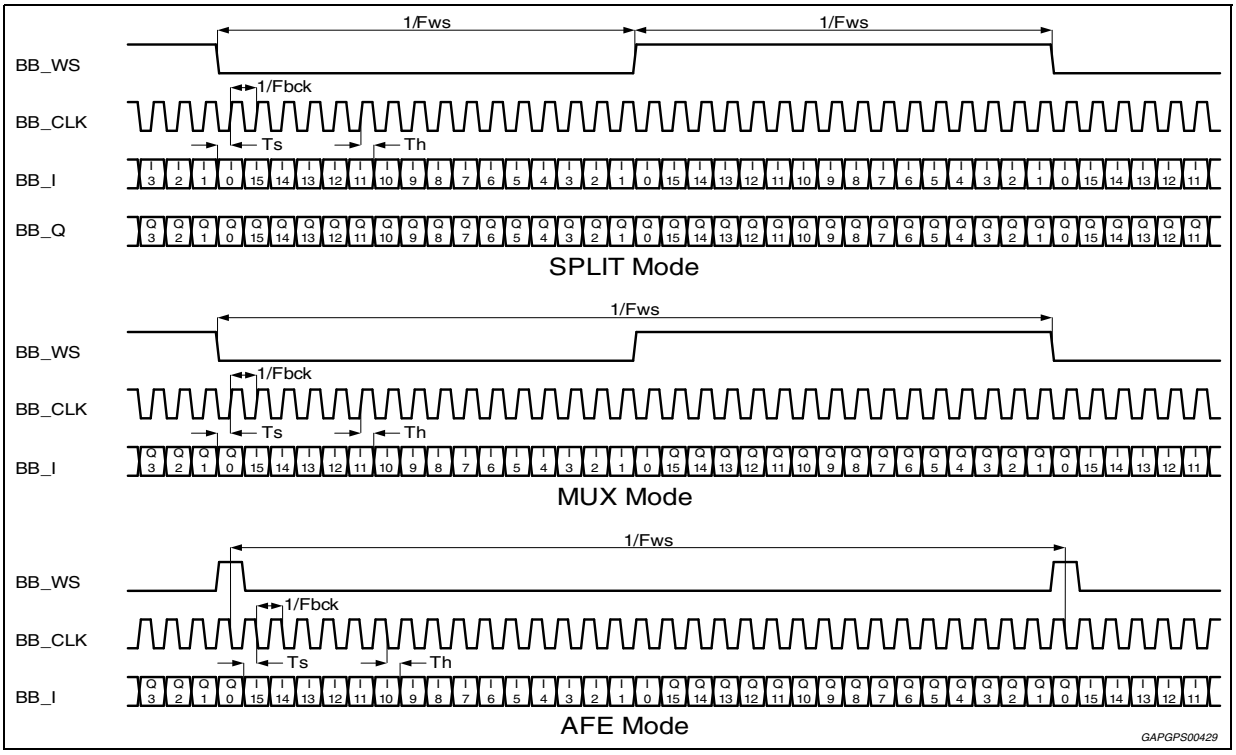


Table 4. SAI_BB timing values (normal mode)

Symbol	Parameter	Rate					Unit
Fpll	PLL clock	332.8	345.6	451.584	466.944	245.76	MHz
Fws	Word strobe	650 (332.8/512)	675 (345.6/512)	882 (451.582/512)	912 (466.944/512))	48 (245.76/5120)	KHz
Fbclk	Bit clock in SPLIT mode	10.4 (332.8/32)	10.8 (345.6/32)	14.112 (451.584/32)	14.592 (466.944/32)	0.768 (245.76/320)	MHz
Fbclk	Bit clock in MUX mode	20.8 (332.8/16)	21.6 (345.6/16)	28.224 (451.584/16)	29.184 (466.944/16)	1.536 (245.76/160)	MHz
Fbclk	Bit clock in AFE mode	20.8 (332.8/16)	21.6 (345.6/16)	28.224 (451.584/16)	29.184 (466.944/16)	1.536 (245.76/160)	MHz
Ts	Data setup time (min)	5	5	5	5	5	ns
Th	Data hold time (min)	5	5	5	5	5	ns

Figure 6. SAI_BB waveforms (burst mode)

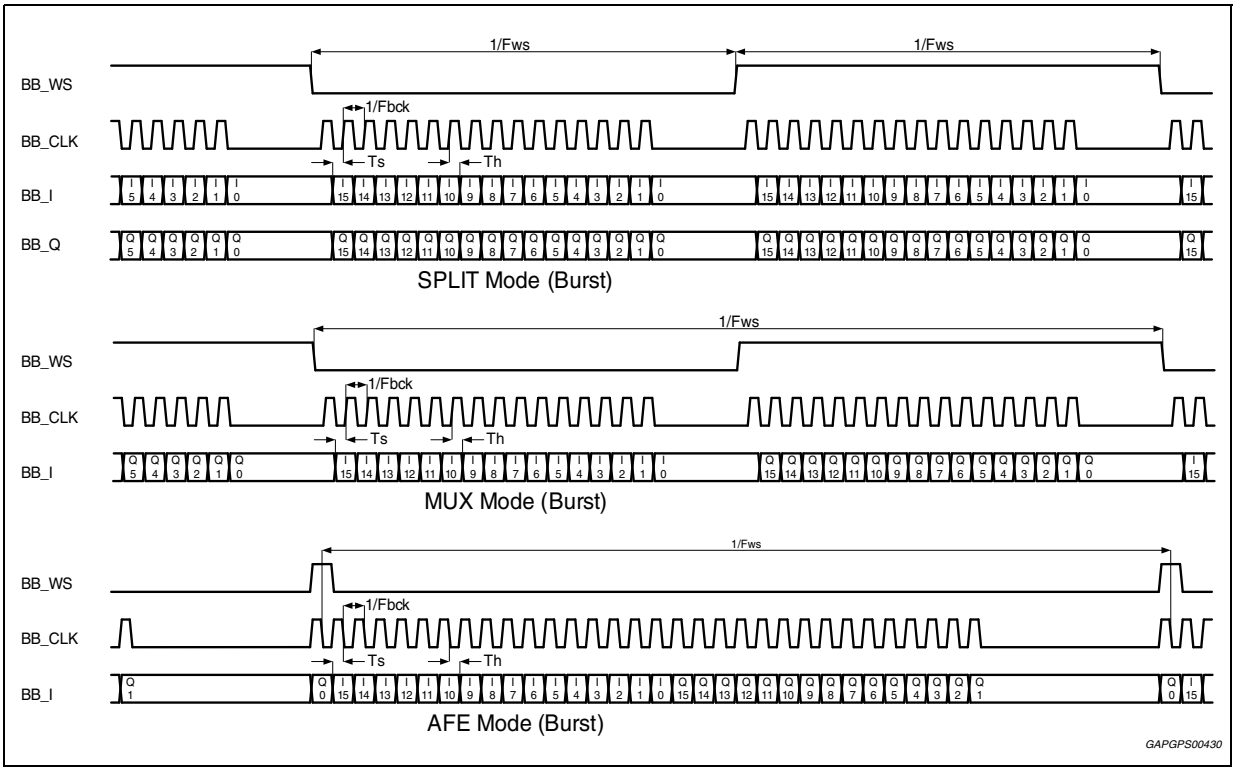


Table 5. SAI_BB timing values (burst mode)

Symbol	Parameter	Rate					Unit
Fpll	PLL clock	332.8	345.6	451.584	466.944	245.76	MHz
Fws	Word strobe	650 (332.8/512)	675 (345.6/512)	882 (451.582/512)	912 (466.944/512))	48 (245.76/5120)	KHz
Fbclk	Bit clock in SPLIT mode	332.8/n (n=16/32)	345.6/n (n=16/32)	451.584/n (n=16/32)	466.944/n (n=16/32)	245.76/n (n=160/320)	MHz
Fbclk	Bit clock in MUX mode	332.8/n (n=8/16)	345.6/n (n=8/16)	451.584/n (n=8/16)	466.944/n (n=8/16)	245.76/n (n=80/160)	MHz
Fbclk	Bit clock in AFE mode	332.8/n (n=8/16)	345.6/n (n=8/16)	451.584/n (n=8/16)	466.944/n (n=8/16)	245.76/n (n=80/160)	MHz
Ts	Data setup time (min)	5	5	5	5	5	ns
Th	Data hold time (min)	5	5	5	5	5	ns

2.15 I²S - serial audio interface

The audio SAI serves as stereo input/output audio bus interface (e.g. to an external audio processor, or from an external HD decoder) using the I²S protocol. The latter calls for a bit clock line, a word select line and data lines; the SAI interface on the TDA7786x has one input data line and one output data line.

The audio SAI lines are: SAI_AUDIO_CLK (pin 37, bit clock line), SAI_AUDIO_WCLK (pin 38, word select (frame) clock line), SAI_AUDIO_DO (pin 39, data output line), SAI_AUDIO_DI (pin 40, data input line). In master mode SAI_AUDIO_BCLK and SAI_AUDIO_WCLK are outputs, in slave mode these pins are inputs.

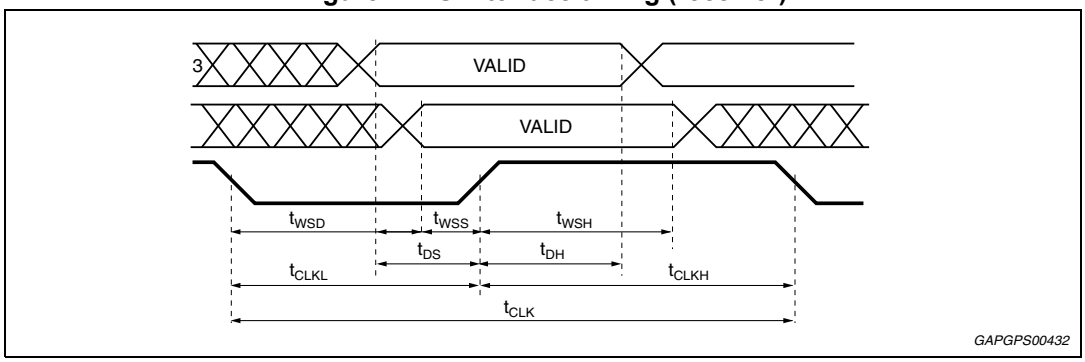
The input and output data lines are operated at the same sampling frequency.

The bit clock has one pulse for each discrete bit of data on the data lines. The bit clock operates at a frequency which is a multiple of the sample rate, and is equal to the sampling frequency times the number of bits per word times two.

Table 6. Audio I²S configuration overview

Name	Channels	World length	Valid Bits	Pins	Formats	Master/Slave mode	Input Rate/ksps	Output Rate /ksps	Max. bit clock frequency
SAI	1x2 In and 1x2 Out	16/32	16/24	4	I²S	M/S	32-48	32-48	12.288 MHz

Figure 7. I²S interface timing (receiver)

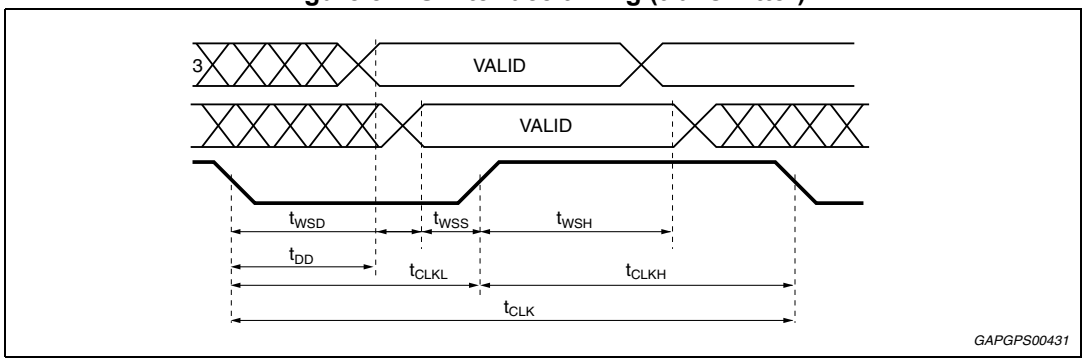


Note: The polarity of the signals and the data bit-shift direction can be selected by configuration bits.

Table 7. I²S interface timing (receiver)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	3	-	-	ns
t_{WSD}	Word-select delay	master mode	4	-	-	ns
t_{DS}	Data setup time	-	5	-	-	ns
t_{DH}	Data_hold time	-	5	-	-	ns

Figure 8. I²S interface timing (transmitter)



Note: The polarity of the signals and the data shift direction can be selected by configuration bits.

Table 8. I²S interface timing (transmitter)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{CLK}	Minimum Clock Cycle (CLK)	-	50	-	-	ns
t_{CLKH}	Minimum bit clock high time	-	25	-	-	ns
t_{CLKL}	Minimum bit clock low time	-	25	-	-	ns
t_{WSS}	Word-select setup time	slave mode	5	-	-	ns
t_{WSH}	Word-select hold time	slave mode	5	-	-	ns
t_{WSD}	Word-select delay	master mode	5	-	-	ns
t_{DD}	Data delay	-	5	-	-	ns

The audio SAI can be configured via software to be operating either in master or in slave mode. The frame length is selectable as 16/32 bits per word, with 16/24 valid bits. *Figure 9* shows the default setting of SAI for the 16-bit mode. Different settings of clock polarity, word clock polarity, transmission mode (I²S mode) and data direction (either MSB or LSB first transmission) are possible, and they can be changed through software. Supported configurations are shown in *Figure 10*. Timing information for the protocols is detailed in *Figure 10*.

Figure 9. I²S interface 16-bit

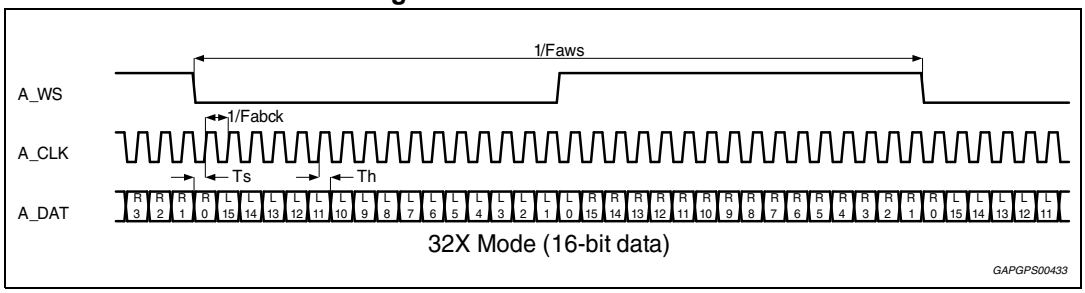
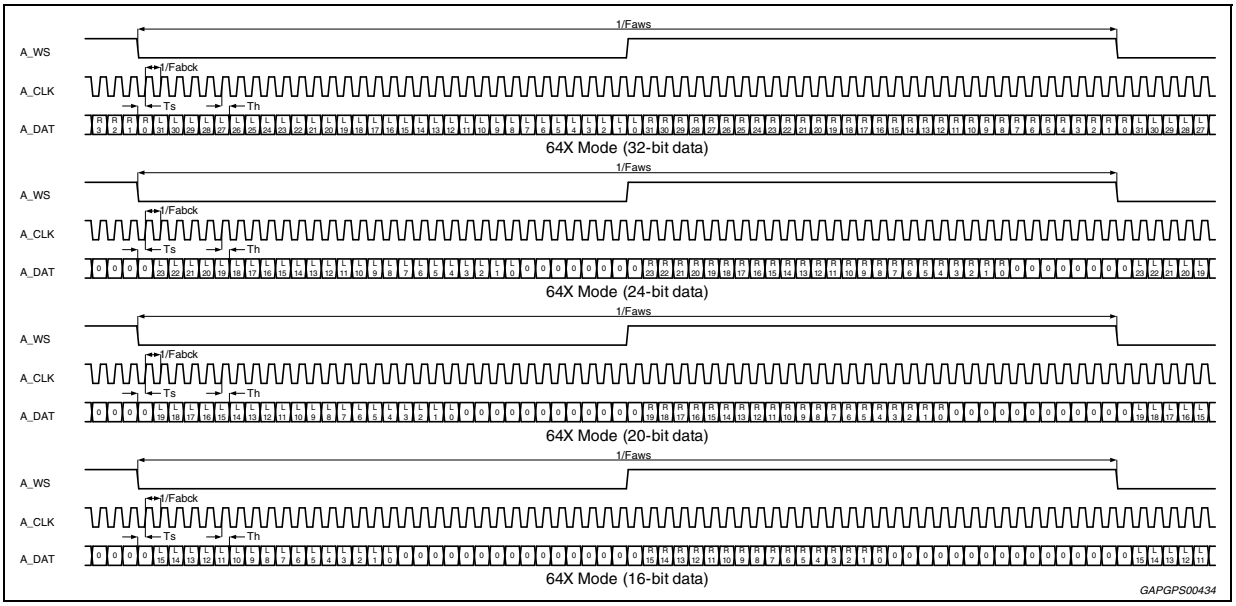


Figure 10. I²S interface 32/24/20/16-bit



2.16 Audio sample rate converter

The TDA7786x is equipped with internal sample rate converters (SRC) that can be configured to modify the sampling frequency of outgoing and incoming digital audio both in the master and in the slave SAI mode (the native audio sampling frequency of the TDA7786x is 45.6 kHz).

The SRC is able to automatically detect the input and output sampling rates and includes a sample clock jitter rejection function which can be enabled separately. The input signal word-width is 20 bits, while the output signal word width can be selected as 20 bits or 16 bits. In order to properly assist in the conversion, the SRC is coupled to self-adjusting low-pass filters.

2.17 Serial control interface

The device is controlled via I^2C.

Through serial bus the processing parameters can be modified and the signal quality parameters and the RDS information can be read out.

The operation of the device is handled mainly through high level commands sent by the car-radio microprocessor through the serial interface, which allows simplification of the operations carried out in the microprocessor itself. The high level commands include among others:

- change frequency (which allows to avoid computing the PLL divider factors)
- change band;
- start seek (the seek operation can be carried out by the TDA7786x in a completely autonomous fashion);
- RDS seek/search (jumps to AF and quality measurements are automatically sequenced).

2.17.1 Serial interface / boot mode

The device possesses two different I2C addresses: 0xC2/C3 and 0xC8/C9. The configuration is chosen by applying the proper voltage at the exit from reset to the pins indicated in *Table 9*. The configuration is latched (e.g. made effective) when the RSTN line transitions from low to high (when RSTN is low, the IC is in reset mode).

The voltage level forced to the boot pins must be released to start the system operation a suitable time after the RSTN line has gone high. The list of configurations is shown in the following table:

Table 9. 64-pin package boot mode configuration

SAI_AUDIO_DO pin 39	**RDS INT pin 32**	**BUS mode**
0	0	I^2C Address = 0xC2
0	1	I^2C Address = 0xC8

The status of these pins during the reset phase can be set to:

- High: through external <10 kΩ resistors tied to 3.3V
- Low: by not forcing any voltage on them from outside, as 50 kΩ internal pull-down resistors are present inside the device.

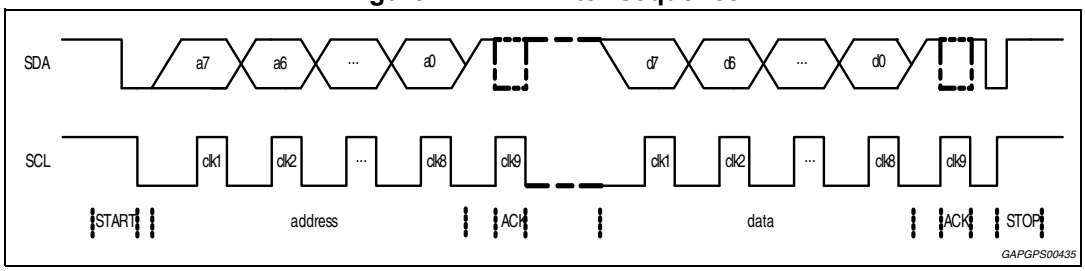
To make sure the I^2C address is correctly latched up at start-up, it is advisable to keep the RSTN line low until the IC supply pins have reached their steady state, and further keep it low for an additional time Treset.

2.17.2 I²C bus protocol

The I²C communication requires two signals: clock (SCL) and data (SDA - bidirectional). The protocol requires an acknowledge signal after any 8-bit transmission.

A "write" communication example is shown in the figure below, for an unspecified number of data bytes (see the relevant technical documentation for frame structure description):

Figure 11. I²C "write" sequence

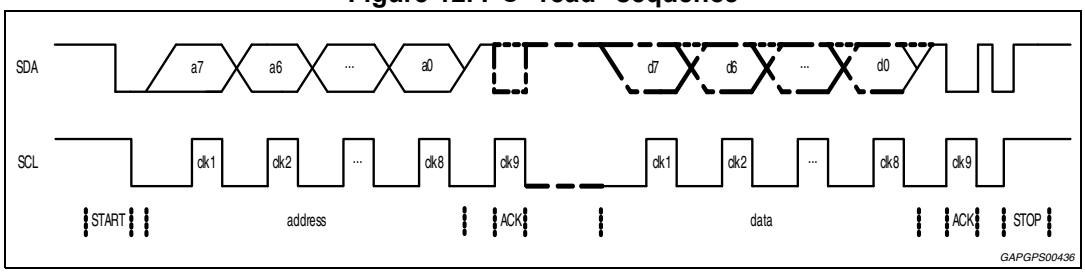


The sequence consists of the following phases:

1. START: SDA line transitioning from H to L with SCL fixed H. This indicates that a new transmission is starting;
2. DATA LATCHING: on the rising SCL edge. The SDA line can vary only when SCL is low (otherwise its transitions are interpreted as either a START or a STOP transition);
3. ACKNOWLEDGE: on the 9th SCL pulse the microprocessor keeps the SDA line H, and the TDA7786x pulls it down in case the communication has been successful. Lack of the acknowledge pulse generation from the TDA7786x indicates a communication failure; the chip-address byte must be sent at the beginning of the transmission. The value can be 0xC2 or 0xC8 (according to the mode chosen at start-up) for "write"; as many data bytes as needed can follow the address before the communication is terminated. See the next section for details on the frame format;
4. STOP: SDA line transitioning from L to H with SCL H. This signifies the end of the transmission.

Dashed lines represent transmissions from the TDA7786x to the microprocessor. A communication example is shown in the figure below, for an unspecified number of data bytes (see later on for frame structure description):

Figure 12. I²C "read" sequence



The "read" sequence is similar to the "write" and it has the same constraints for start, stop, data-latching and the following differences:

- the chip address must always be sent by the microprocessor to the TDA7786x; the address must be 0xC3 (if C2 had been selected at boot) or 0xC9 (if 0xC8 had been selected at boot);
- the header is transmitted after the chip address (the same happens for "write") before data are transferred from the TDA7786x to the microprocessor. See the relevant technical documentation for details on the frame format;
- when data are transmitted from the TDA7786x to the µP, the latter keeps the SDA line H;
- the acknowledge pulse is generated by the µP for those data bytes that are sent by the TDA7786x to the µP. Failure of the µP to generate an ACK pulse on the 9th CLK pulse has the same effect on the TDA7786x as a STOP.

The maximum clock speed is 500 kbit/s.

Warning: When the TDA7786x is not powered on, the internal ESD protection diodes act as a pull-down keeping the I^{2}C lines voltage below 2 V. This implies that the I^{2}C bus connected to the TDA7786x may not be used to drive other devices when the TDA7786x is powered off.

2.18 Digital-down-converter (DDC)

The complex digital mixer in the DDC performs mixing of the IF signal to zero IF. The internal sample rate for FM/AM processing is 456 kS/s and the sample rate for FM/AM IBOC is 912 kS/s. AM IBOC require additional filtering implemented in software.

Figure 13. Digital-down-converter simplified block diagram

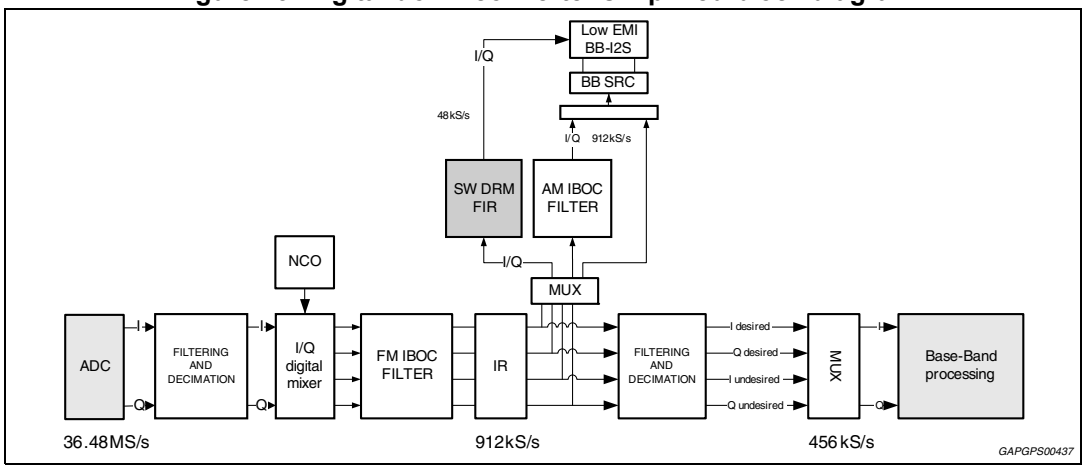


Figure 14. Cumulative transfer function at output of IBOC_FM filter

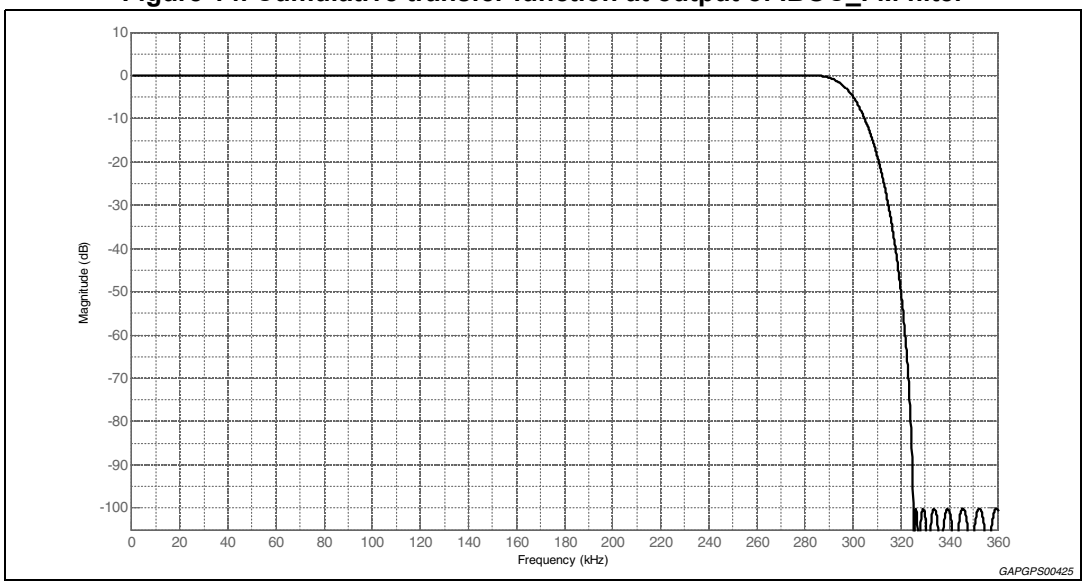


Table 10. Overall filter characteristics for IBOC_FM filter

Item	Value	Unit
Pass-band edge	282	kHz
Stop-band edge	325	kHz
In-band ripple (0 kHz to 282 kHz)	<0.002	dB
Anti-alias band range	[-500 +500]	kHz
Anti-alias Attenuation	100	dB