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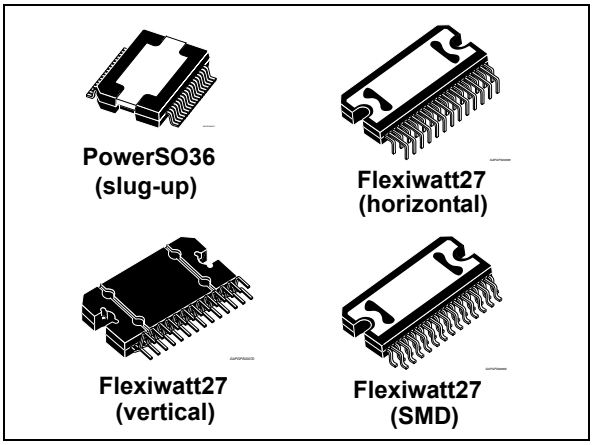
TDA7801

Digital input quad power amplifier with built-in diagnostics features

Datasheet - production data



Features

- Integrated 110 dB D/A conversion
- I^2S digital input (3.3/1.8 V) with TDM option
- Selectable input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- MOSFET power outputs
- High output power capability 4x28 W/ 4 Ω @ 14.4 V, 1 kHz, 10 % THD
- Max. output power 4x72 W/2 Ω
- Full I^2C bus driving (3.3/5 V):
  - Independent front/rear soft play/ mute
  - Selectable gain (four levels) for very low noise line-out function
  - I^2C bus digital diagnostics (including DC and AC load detection)
- Two I^2C bus addresses and 8-ch TDM mode (only in PowerSO package)
- Optional non I^2C bus mode
- Offset detector (play or mute mode)
- Clipping detector (selectable level) and diagnostics pin
- CMOS compatible enable pin (3.3/5 V)
- Full fault protection
- Four independent short circuit protections
- Linear thermal protection (four thermal warnings)
- ESD protection

Description

The TDA7801 is a new BCD technology quad bridge amplifier for car audio applications.

Thanks to the BCD6 technology it is possible to integrate a high performance D/A converter together with powerful MOSFET outputs.

The possibility of having the D/A conversion on board allows the performance to reach an outstanding 115 dB S/N ratio with more than 105 dB of dynamic range.

This device is equipped with a full diagnostics array that communicates the status of each speaker through the I^2C bus. The possibility to control the configuration and behavior of the device by means of the I^2C bus makes TDA7801 a very flexible machine.

Table 1. Device summary

Order code	Package	Packing
TDA7801PD	PowerSO36 (slug-up)	Tube
TDA7801PDTR	PowerSO36 (slug-up)	Tape and reel
TDA7801	Flexiwatt27 (vertical)	Tube
TDA7801H	Flexiwatt27 (horizontal)	Tube
TDA7801SM	Flexiwatt27 (SMD)	Tube

Contents

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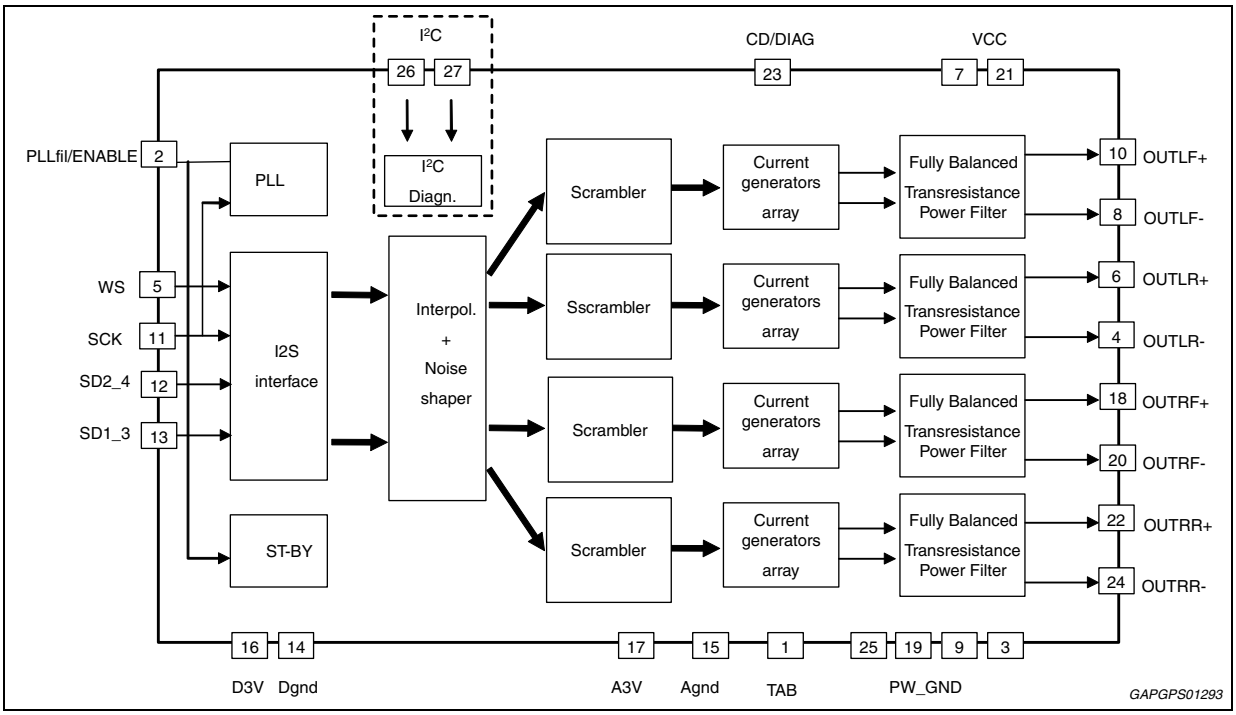
1 Block diagram and pins description

1.1 Block diagram

Figure 1. Block diagram (Flexiwatt27)



2 Application diagrams

Figure 2. I²C bus mode application diagram (TDA7801/H/SM)

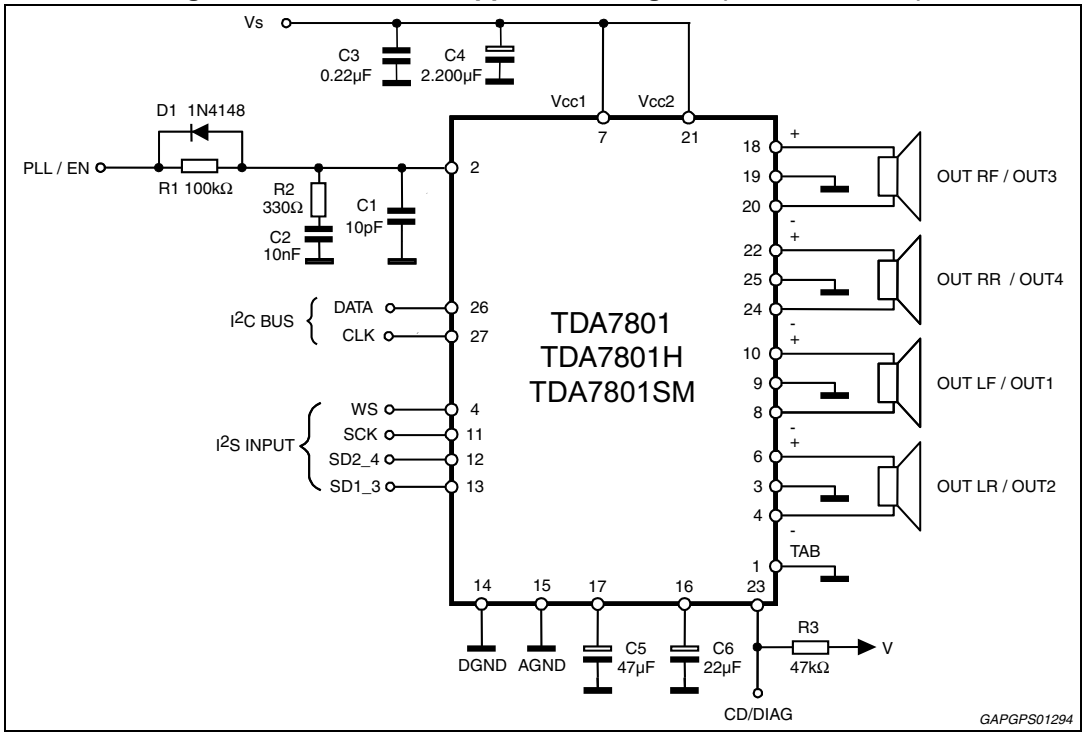


Figure 3. I²C bus mode application diagram (TDA7801PD)

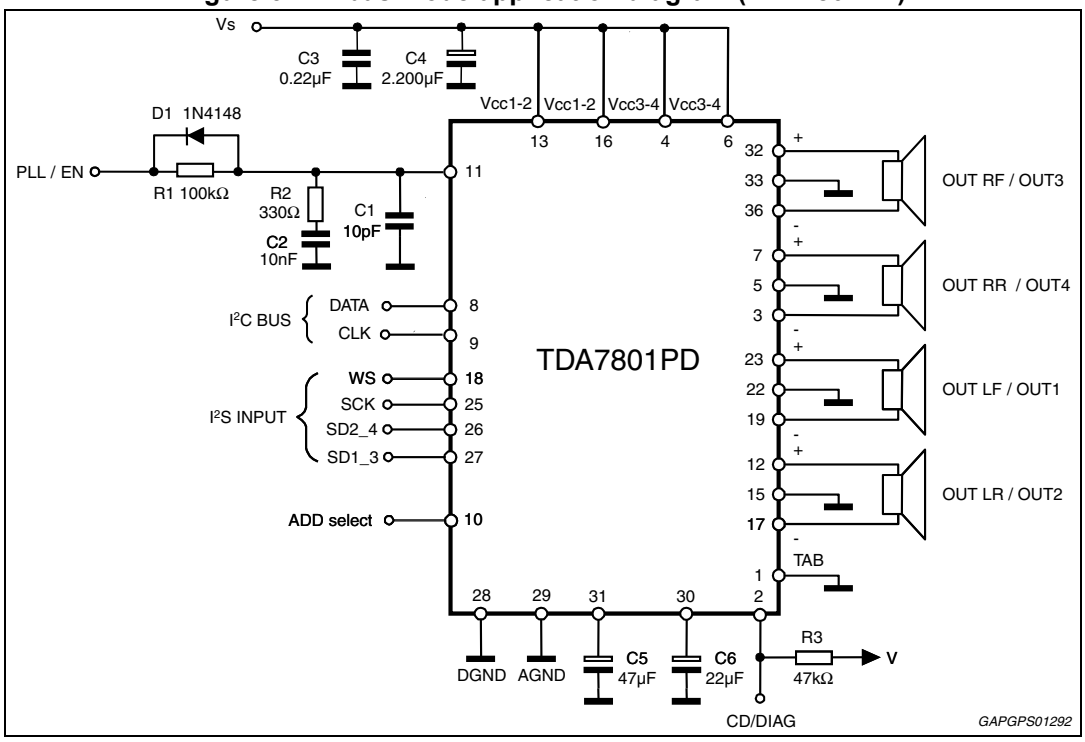


Figure 4. Legacy mode application diagram (TDA7801/H/SM)

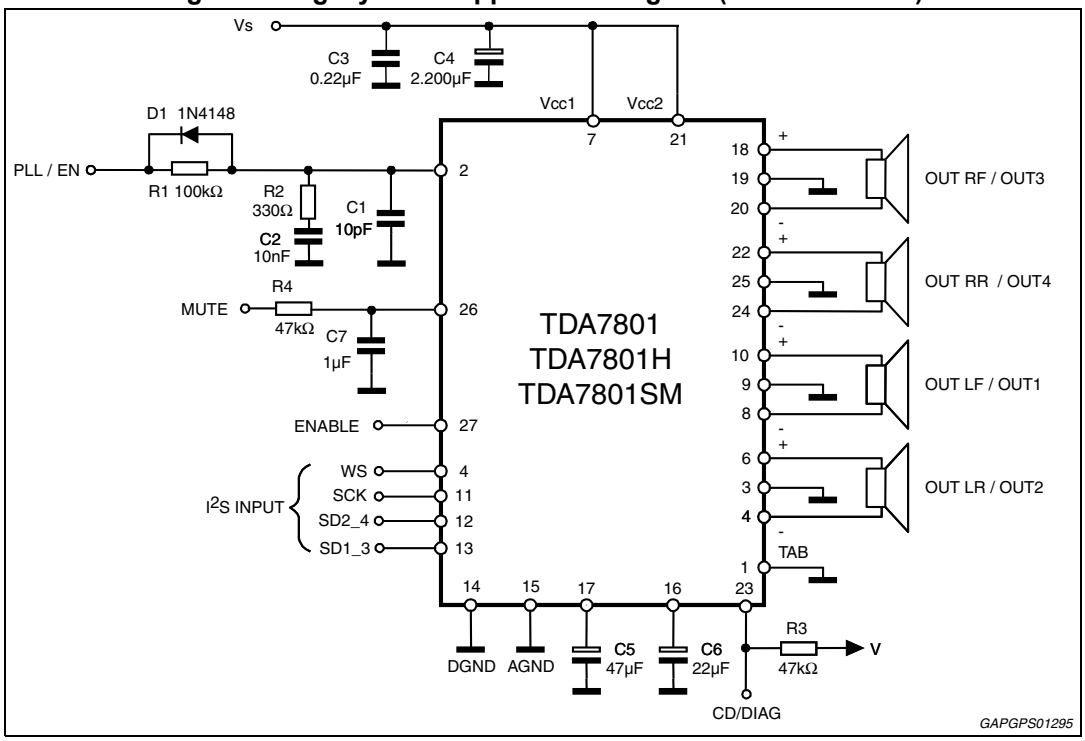
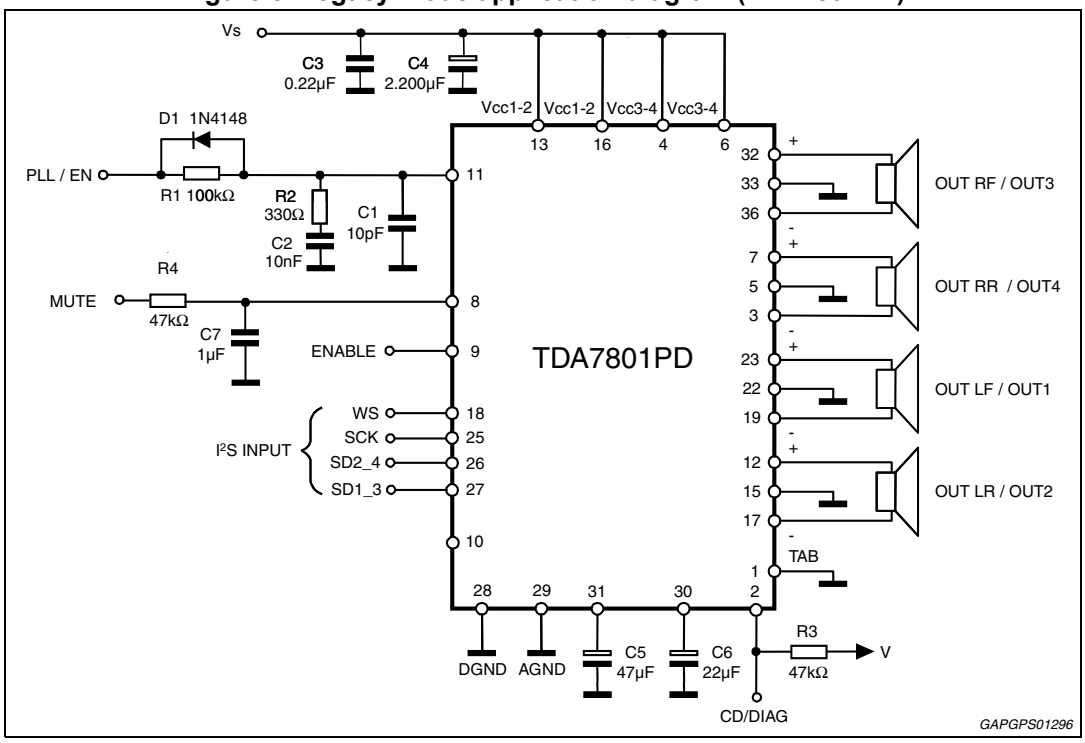


Figure 5. Legacy mode application diagram (TDA7801PD)



2.1 Pin description

Figure 6. Pin connection diagrams

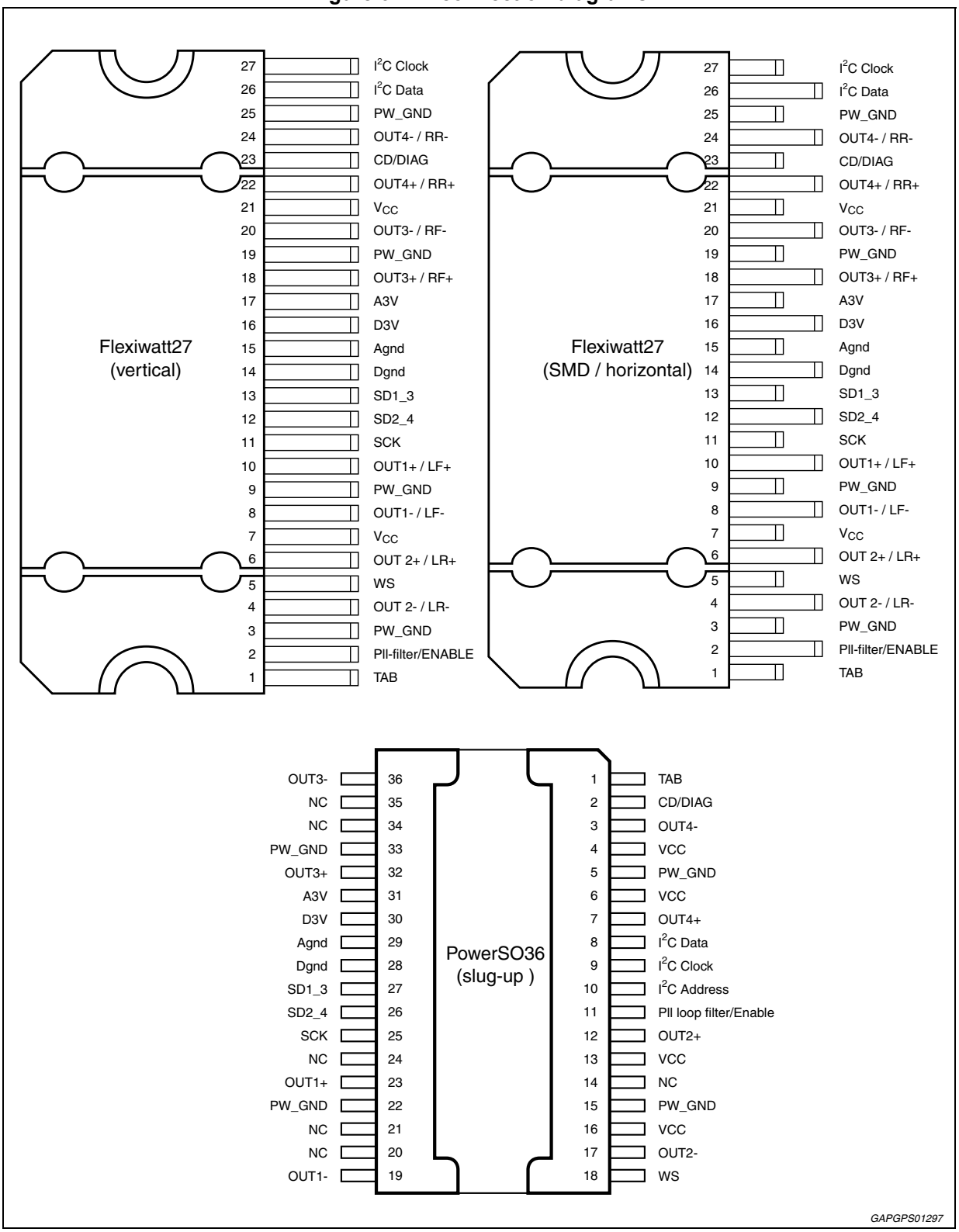


Table 2. Flexiwatt27 (vertical/SMD/horizontal) pin description

N°	Pin	Function
1	TAB	TAB connection (GND)
2	Pll-filter / ENABLE	Pll loop filter / ENABLE
3	PW_GND	Power ground channel 2
4	OUT 2- / LR-	Channel 2 (Left Rear) negative output
5	WS	Word select (I^2S bus, logic input)
6	OUT 2+ / LR+	Channel 2 (Left Rear) positive output
7	Vcc	Channel 1 and 2 positive supply
8	OUT 1- / LF-	Channel 1 (Left Front) negative output
9	PW_GND	Power ground channel 1
10	OUT 1+ / LF+	Channel 1 (Left Front) positive output
11	SCK	Serial clock (I^2S bus, logic input)
12	SD2_4	Serial data channels 2 and 4 (I^2S bus, logic input)
13	SD1_3	Serial data channels 1 and 3 (I^2S bus, logic input)
14	Dgnd	Digital ground
15	Agnd	Analog ground
16	D3V	Digital 3.3 V supply filter
17	A3V	Analog 3.3 V supply filter
18	OUT3+ / RF+	Channel 3 (right front) positive output
19	PW_GND	Power ground channel 3
20	OUT3- / RF-	Channel 3 (right front) negative output
21	Vcc	Channels 3 and 4 positive supply
22	OUT4+ / RR+	Channel 4 (right rear) positive output
23	CD/DIAG	Clip detector and diagnostic output: – Overcurrent protection intervention – Thermal warning – POR – (Open drain output)
24	OUT4- / RR-	Channel 4 (right rear) negative output
25	PW_GND	Power ground channel 4
26	I^2C Data	I^2C data/legacy mode mute
27	I^2C Clock	I^2C clock/enable legacy mode

Table 3. PowerSO36 pin description

N°	Pin	Function
1	TAB	TAB connection (GND)
2	CD/DIAG	Clip detector and diagnostic output: Overcurrent protection intervention Thermal warning Offset detection POR (Open drain output)
3	OUT4-	Channel 4 (right rear) negative output
4	VCC	Channels 3-4 positive supply
5	PW_GND	Power ground channel 4
6	VCC	Channels 3-4 positive supply
7	OUT4+	Channel 4 (right rear) positive output
8	I2C Data	I^2C Data / legacy mode mute
9	I2C Clock	I^2C Clock / enable legacy mode
10	I2C Address	I^2C Address
11	Pll loop filter/Enable	Pll loop filter / Enable
12	OUT2+	Channel 2 (left rear) positive output
13	VCC	Channel 1-2 positive supply
14	NC	Not connected
15	PW_GND	Power ground channel 2
16	VCC	Channel 1-2 positive supply
17	OUT2-	Channel 2 (left rear) negative output
18	WS	Word Select (I^2S bus, logic input)
19	OUT1-	Channel 1 (left front) negative output
20	NC	Not connected
21	NC	Not connected
22	PW_GND	Power ground channel 1
23	OUT1+	Channel 1 (left front) positive output
24	NC	Not connected
25	SCK	Serial clock (I^2S bus, logic input)
26	SD2_4	Serial data channels 2 and 4 (I^2S bus, logic input)
27	SD1_3	Serial data channels 1 and 3 (I^2S bus, logic input)
28	Dgnd	Digital ground
29	Agnd	Analog ground
30	D3V	Digital 3.3 V supply filter
31	A3V	Analog 3.3 V supply filter
32	OUT3+	Channel 3 (right front) positive output
33	PW_GND	Power ground channel 3
34	NC	Not connected
35	NC	Not connected
36	OUT3-	Channel 3 (right front) negative output

3 Electrical specifications

3.1 Absolute maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{op}	Operating supply voltage	18	V
V_S	DC supply voltage	28	V
V_{peak1}	Peak supply voltage (for t = 50 ms)	50	V
V_{peak2}	Peak supply voltage (for t = 500 ms)	34	V
$V_{i2cdata}$	I^2C bus data pin voltage / legacy mode mute	20	V
V_{i2ck}	I^2C bus clock pin voltage / enable legacy mode	50	V
V_{i2s}	I^2S bus pins voltage	3.6	V
I_O	Output peak current (not repetitive t = 100 µs)	8	A
I_O	Output peak current (repetitive f > 10 Hz)	6	A
P_{tot}	Power dissipation T_{case} = 70 °C	85	W
F_s max	Maximum input sample rate	200	kHz
T_{amb}	Operative temperature range(1)	-40 to 105	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C
C_{max}	Maximum capacitor vs. ground connected to the output	10	nF

1. A suitable heatsink/dissipation system should be used to keep T_j inside the specific limits.

3.2 Thermal data

Table 5. Thermal data

Symbol	Parameter		PowerSO36	Flexiwatt 27	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	Max	1	1	°C/W

3.3 Electrical characteristics

Refer to the test circuit, V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_S	Supply voltage range	-	8	-	18	V
I_d	Total quiescent drain current in amplifier mode	enable on amplifier mode muted	150	260	350	mA
I_t	Total quiescent drain current in tristate mode	enable on tristate mode	30	45	60	mA
P_O	Output power	R_L = 4 Ω; max power	41	45	-	W
		THD = 10 %	25	28	-	W
		THD = 1 %	20	22	-	W
		R_L = 2 Ω; max power	70	78	-	W
		R_L = 2 Ω; THD 10%	43	49	-	W
		R_L = 2 Ω; THD 1%	34	38	-	W
THD	Total harmonic distortion	P_O = 1 W to 10 W, f=1 kHz, G_{V1}	-	0.03	0.05	%
		P_O = 1 W to 10 W, f=10 kHz, G_{V1}	-	0.2	0.5	%
		R_L =100 Ω, input=-10 dBFS, f=1 kHz, $G_{V1,2,3,4}$	-	0.01	0.02	%
C_T	Cross talk	f = 1 kHz to 10 kHz	60	80	-	dB
G_{V1}	Voltage gain 1	Output voltage @ -10 dBFS	14.9	-	16.9	dB (Vp)
G_{V2}	Voltage gain 2		9.45	-	11.45	dB (Vp)
G_{V3}	Voltage gain 3		6.9	-	8.9	dB (Vp)
G_{V4}	Voltage gain 4		1.45	-	3.45	dB (Vp)
F_{SV1}	Full scale voltage G_{V1}	Output voltage @ 0 dBFS V_S=18 V; R_L = 100 Ω	12.7	-	-	Vrms
F_{SV2}	Full scale voltage G_{V2}	Output voltage @ 0 dBFS	6.65	-	8.35	Vrms
F_{SV3}	Full scale voltage G_{V3}		4.9	-	6.2	Vrms
F_{SV4}	Full scale voltage G_{V4}		2.65	-	3.35	Vrms
DG	Delta voltage gain 20 Hz – 20 kHz	P_o =1 W	-0.5	-	0.5	dB
DR	Dynamic range $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw=20 Hz to 20 kHz, un weighted	 105 100 100 98	 110 105 105 103	-	dB

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
E_{IN}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw =20 Hz to 20 kHz, un weighted	-	 25 25 19 19	 35 35 26 26	µV
SNR	Signal to noise ratio $G_V = G_{V1}$ $G_V = G_{V2}$ $G_V = G_{V3}$ $G_V = G_{V4}$	Bw=20 Hz to 20 kHz, un weighted	 111 105 105 100	 115 109 109 104	-	dB
G_B	Gain balance		-1	-	+1	dB
SVR	Supply voltage rejection	f = 1 kHz; V_r = 1 Vpk;	50	70	-	dB
I_{SB}	Stand-by current	$V_{pin\ ENABLE}$ = 0v	-	-	10	µA
A_M	Mute attenuation	-	80	-		dB
V_{OS}	Offset voltage	Mute & Play	-50	-	50	mV
V_{AM}	Supply automute range	Above this voltage the device is in play	7.8	-	-	V
		Below this voltage the device is in mute	-	-	6.8	V
$V_{POWONRESET}$	Supply voltage of power-on reset	-	-	4.5	5	V
$V_{OVERVOLTAGE}$	Over voltage shut-down	-	18		24	V
CD_{LK}	Clip det high Leakage current	CD off	-	0	5	µA
CD_{SAT}	Clip det sat. voltage	CD on; I_{CD} = 1 mA	-	150	300	mV
$CD1_{THD}$	Clip det THD level 1 %	-	-	1	2	%
$CD2_{THD}$	Clip det THD level 5 %	-	3	5	7	%
$CD3_{THD}$	Clip det THD level 10 %	-	7	10	13	%
T_{mute}	Mute and unmute commutation time	Programmable by I^2C bus register IB1(6:4) F_s =44.1 kHz	-	1.45	-	ms
			-	5.8	-	
			-	11.6	-	
			-	23.2	-	
			-	34.8	-	
			-	69.6	-	
			-	140	-	
			-	278	-	
N_{GL}	Noise gating input level	Under this level the device is in mute	-	-102	-	dB

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
N_{GT}	Noise gating time	Fs = 44100 Hz	-	92	-	ms
E_{IN2}	Output noise voltage GV=GV1 GV=GV2 GV=GV3 GV=GV4	Bw=20 Hz to 20 kHz, un weighted, noise gating off, No input signal	-	 44.2 42 31.2 21	 88 84 63 42	µV
Turn on diagnostics speaker mode						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
P_{vs}	Short to V_s det. (above this limit, the output is considered in short circuit to V_S)	-	V_s – 1	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).	-	2	-	V_s – 2	V
Lsc	Shorted load det.	-	-	-	0.5	Ω
Lop	Normal load det.	-	1.65	-	25	Ω
Lnop	Open load det.	-	75	-	-	Ω
Td	Max diagnostic time	Input sampling frequency Fs = 44100 Hz	-	-	190	ms
Turn on diagnostics booster mode						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to V_s det. (above this limit, the output is considered in short circuit to V_s)	-	V_s – 1	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults).	-	2	-	V_s – 2	V
Lsc	Shorted load det.	-	-	-	15	Ω
Lop	Normal load det.	-	0.065	-	1	kΩ
Lnop	Open load det.	-	3.5	-	-	kΩ
AC-diagnostic						
$I_{ACTRESH}$	AC diagnostic current threshold	IB4 – D6= ‘0’	250	375	500	mA
		IB4 – D6= ‘1’	125	187	250	mA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Permanent diagnostics						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to V_s det. (above this limit, the Output is considered in short circuit to V_s)	-	V_s – 1	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults)	-	2	-	V_s – 2	V
L_{SC}	Shorted load det.	Speaker mode	-	-	0.5	Ω
		Booster mode	-	-	15	Ω
Lop	Normal load det.	Speaker mode	1.65	-	-	Ω
		Booster mode	0.065	-	-	kΩ
V_O	Offset detection	Absolute value	1.5	-	2.5	V
T_{ph}	Thermal protection junction temperature	Gain attenuation of 60 dB	-	175	-	°C
T_{pl}		Gain attenuation of 0.5 dB	-	165	-	°C
T_{w1}	Thermal warning junction temperature	-	-	Tpl-10	-	°C
T_{w2}		-	-	Tpl-27	-	°C
T_{w3}		-	-	Tpl-45	-	°C
T_{w4}		-	-	Tpl-62	-	°C
Legacy mode						
V_{LM_MUTE}	Legacy mode mute threshold	Gain Attenuation of 80 dB	-	-	1.2	V
		Gain Attenuation of 0.1 dB	2.6	-	-	V
V_{LM_ON}	Legacy mode threshold	Device in legacy mode	Vs-2	-	Vs	V
I_{LKG_MUTE}	Mute pin leakage	-	-5	-	+5	µA
I^2C Bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	1.5	V
V_{IH}	Input high voltage	-	2.3	-	-	V
PII-filter /ENABLE pin						
V_{ILENB}	Input low voltage	-	-	-	1.5	V
V_{IHENB}	Input high voltage	-	2.3	-	-	V
I_{ILENB}(1)	Logic ‘0’ output current	V_{IN} = 0.45 V	-	-	2	mA
I_{IHENB}	Logic ‘1’ input current	V_{IN} = 2.3 V (IB0 D4=0)	-	-	2	µA

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I^2S pin						
V_{IL-I2S}	Input low voltage	-	-	-	0.8	V
V_{IH-I2S}	Input high voltage	-	1.3	-	-	V
I_{IH}	Input high current except WS pin	V_I = 3.3 V	-	-	5	µA
I_{IL}	Input low current	V_I = 0 V	-	-	5	µA
I_{IH_WS}	Input high current for WS	V_I = 3.3 V	-	70	150	µA

1. This has to be considered the maximum current value for a short time and not the standby current.

3.4 Electrical characteristics typical curves

Figure 7. Quiescent current vs. supply voltage

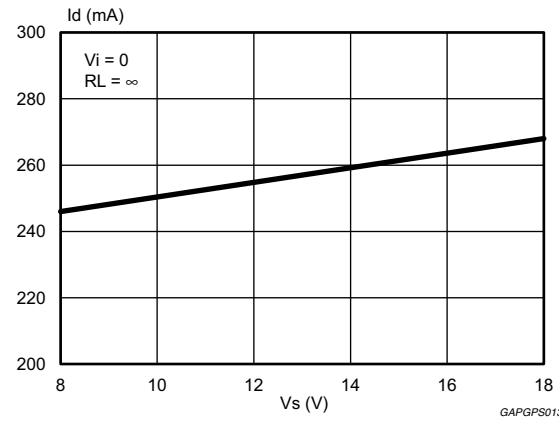


Figure 8. Output power vs. supply voltage (4 Ω)

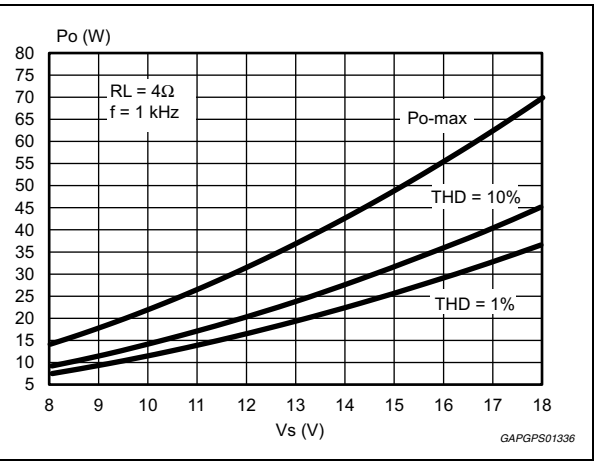


Figure 9. Output power vs. supply voltage (2 Ω)

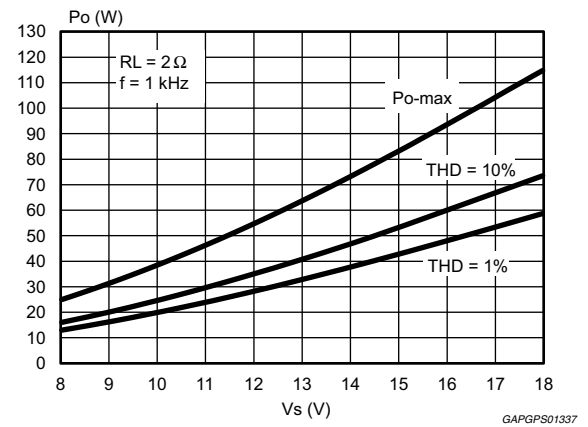


Figure 10. Distortion vs. output power (4 Ω)

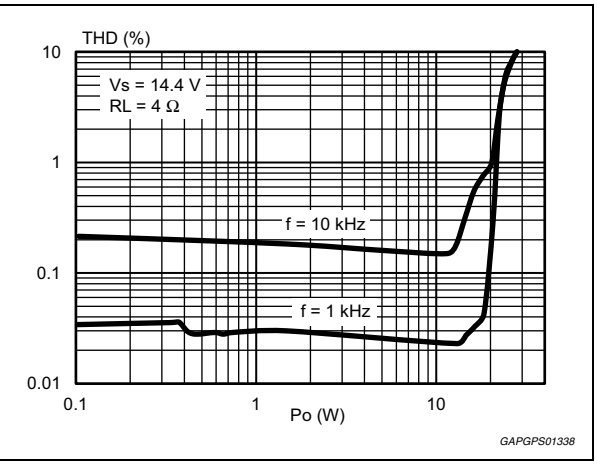


Figure 11. Distortion vs. output power (2 Ω)

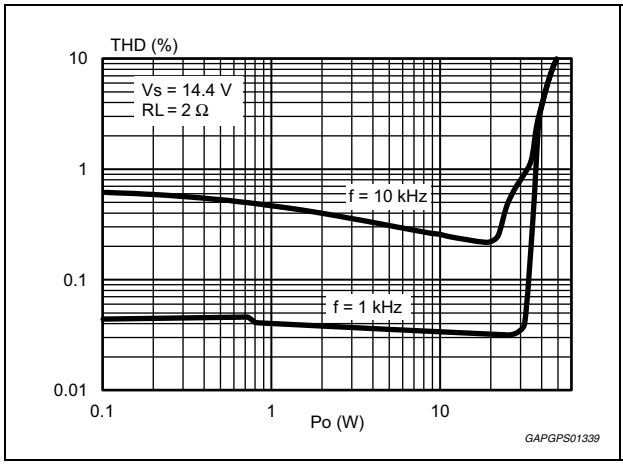


Figure 12. Distortion vs. frequency (4 Ω)

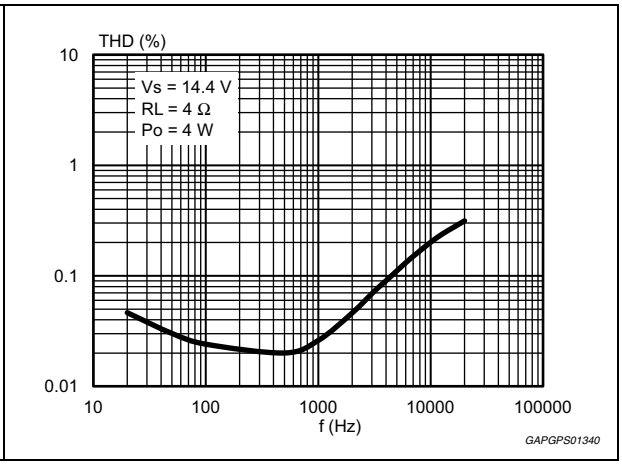


Figure 13. Distortion vs. frequency (2 Ω)

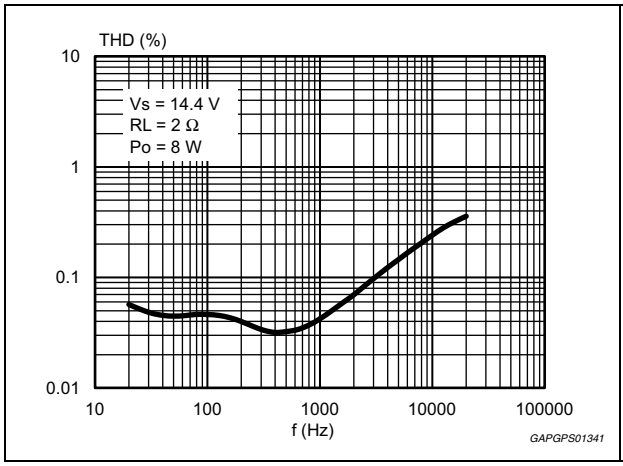


Figure 14. Vo vs. Vin (Gv1-2-3-4 settings)

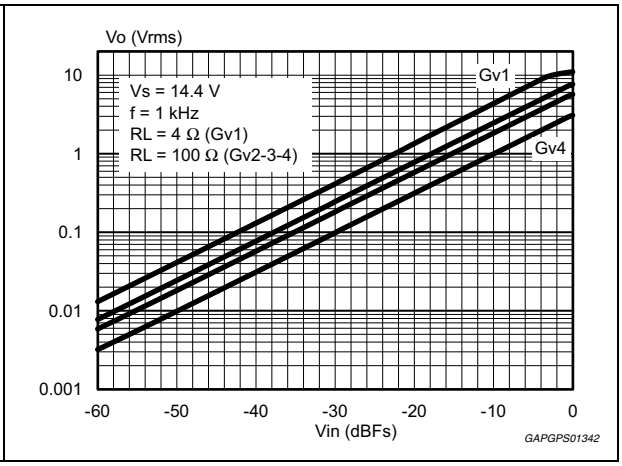


Figure 15. Vo vs. Vin (Gv1-2-3-4 settings + 6 dB dig. gain)

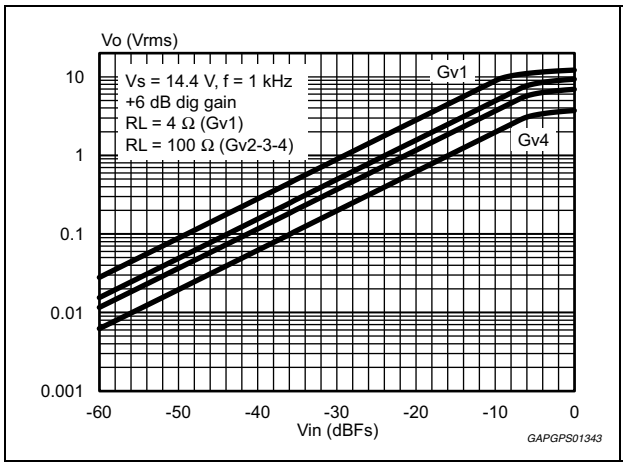


Figure 16. Distortion vs. output voltage (LD-Gv2)

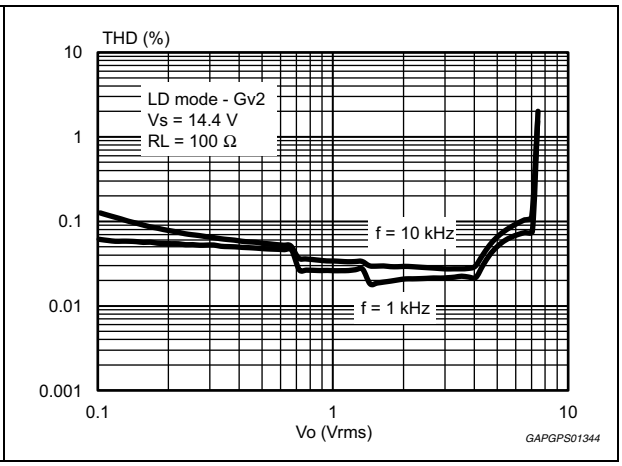


Figure 17. Distortion vs. output voltage (LD-Gv3)

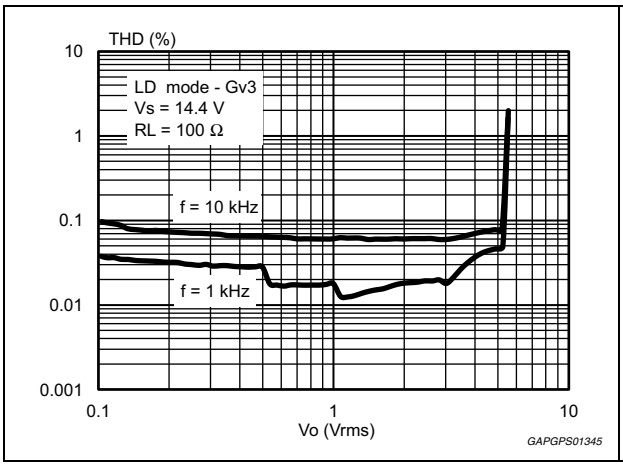


Figure 18. Distortion vs. output voltage (LD-Gv4)

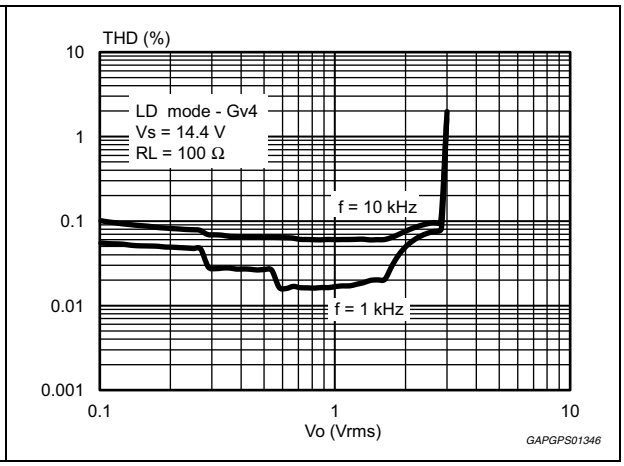


Figure 19. Output attenuation vs. Vs

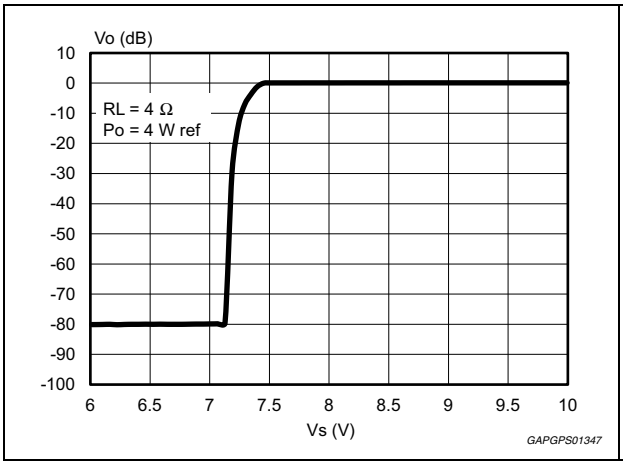


Figure 20. Crosstalk vs. frequency

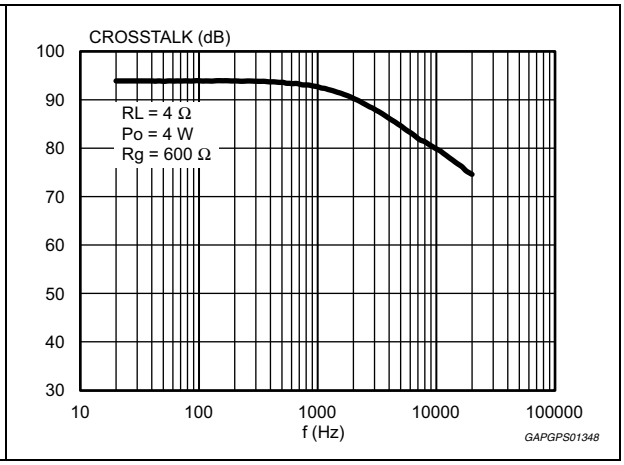


Figure 21. Supply voltage rejection vs. frequency

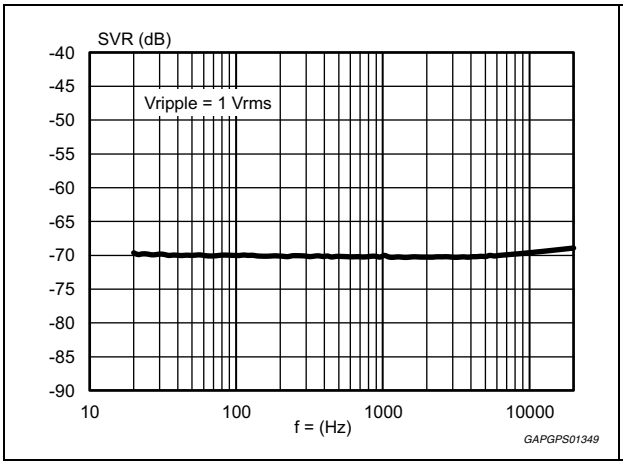


Figure 22. Total power dissipation & efficiency vs. Po (4 Ω)

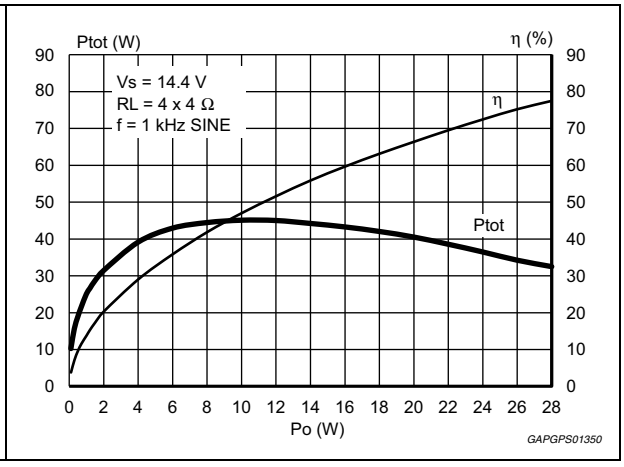


Figure 23. Power dissipation vs. average Po (audio program simulation, 4 Ω)

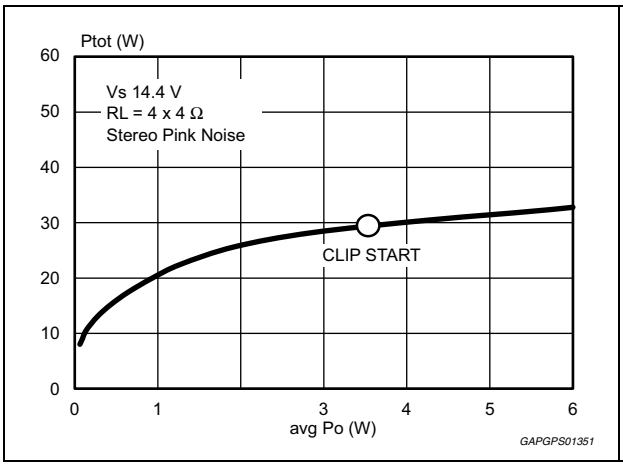


Figure 24. Power dissipation vs. average Po (audio program simulation, 2 Ω)

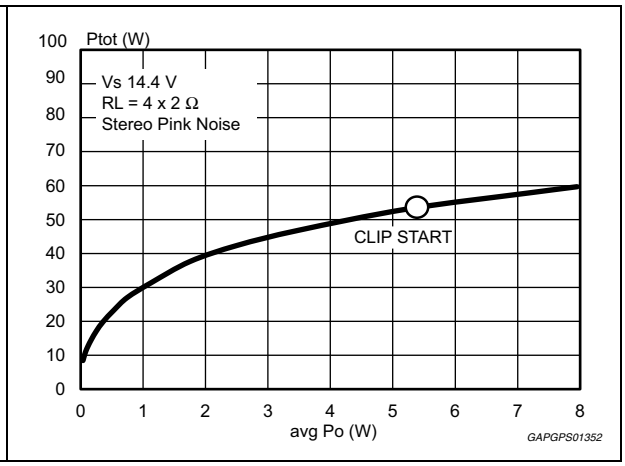
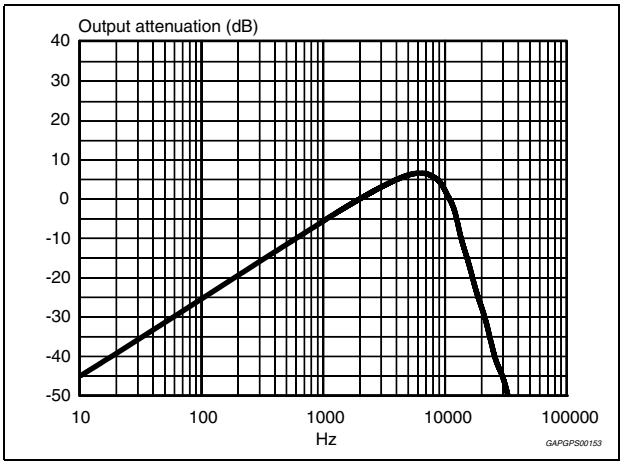


Figure 25. ITU R-ARM frequency response, weighting filter for transient pop



4 Operation mode

The device has three main operation modes:

- Standby mode
- Tristate mode
- Amplifier mode

4.1 Standby mode

When the ENABLE pin is low the device is in standby-mode. The current consumption is I_{SB}.

4.2 Tristate mode

When the ENABLE pin is high and the bit D7 of register DB0 is low the device is in tristate-mode. In that state the amplifier outputs are "high impedance", the I^2C bus is ready to receive command.

4.3 Amplifier mode

When the ENABLE pin is high and the bit D7 of register DB0 is high the device is in amplifier-mode ready to play. To move the device in that state it is enough to write '1' on bit D7 of register IB1 from tristate-mode. Note that the device starts with all channels muted by default (see I^2C registers description, *Section 9*).

5 "PLL-filter /enable" pin description

5.1 Functionality

The pin 2 has the functions to:

- ENABLE
- PLL filter

When the pin 2 is set to logic level low the TDA7801 is in standby-mode and the current consumption is ISB. The device is waked-up and put in tristate-mode setting the same pin to logic level high. In tristate-mode the TDA7801 is ready to receive I^2C bus instructions. The device is set in amplifier-mode writing '1' on bit D7 of byte IB1.

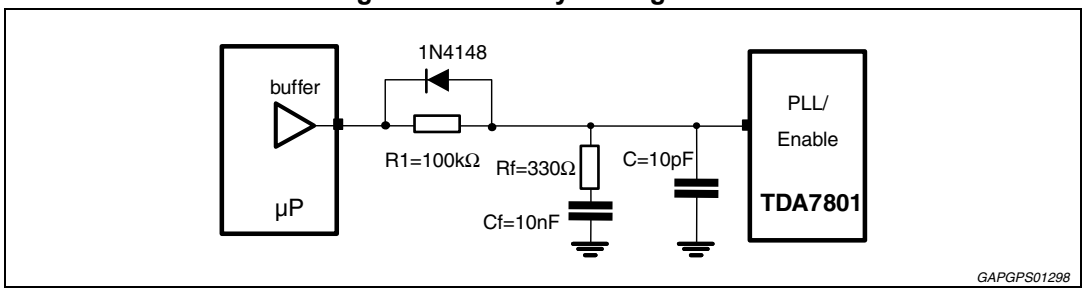
In amplifier-mode the PIN2 works as PLL filter pin. The TDA7801 will place this pin to have a precise voltage value.

During the transition from amplifier-mode to standby-mode, the device will try to force the Pin2 level sourcing a current I_{ILENB}.

5.2 Driving

In *Figure 26* an applicative schematic to drive the Pin 2 is reported. In the schematic, it is supposed that the TDA7801 is interfaced with a µP.

Figure 26. Standby driving circuit



The R_f and C_f components are respectively resistance and capacitance of the PLL filter. The resistance R1 and diode 1N4848 allows the Pin 2 to force to logic level low and the TDA7801 to force its voltage level in amplifier-mode. During the transition amplifier-mode/standby-mode the TDA7801 tries to forces the voltage on the PLL/Enable by sourcing a current flow. Since the PLL/ENABLE pin is forced at a voltage lower than V_{ILENB} in the above described conditions, the buffer input resistance should be chosen small enough to take this effect into account.

It's important to keep the PLL-Filter ground as close as possible to digital ground in the application board in order to minimize the PLL reference movement.

6 Functional description

6.1 Voltage supplies timing

TDA7801 internal voltage supplies rise time and fall time are determined by the two capacitors at pin 16 and 17, respectively digital supply pin (D3V3) and analog supply pin (A3V3). Capacitor on analog supply pin, (pin 17), and capacitor on digital supply, (pin 16), should respect the ratio 2:1. It is suggested to fix a minimum value of 22 µF on digital supply pin and 47 µF on analog supply pin, which correspond to a typical Turn-on time of 1.5 ms and a typical turn-off time of 8.5 ms.

6.2 Turn-on diagnostic description

Turn-on diagnostic is activated under I^2C bus request. Detectable output faults are:

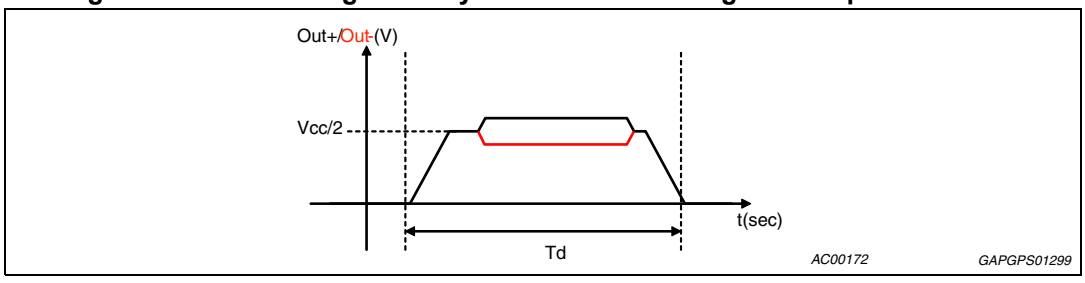
- Short to GND
- Short to V_s
- Short across the speaker
- Open load

In the TDA7801 a new diagnostic that exploits the presence of D/A converters has been implemented. To verify if some of the above connections are in place, a subsonic (inaudible) voltage pulse is digitally and internally generated and converted (*Figure 27*). The amplitude of this pulse is stopped when the current flowing through the speaker is the same as the prefixed one corresponding to a specified load. The exact knowledge of the voltage drop across the load in any phase of the diagnostic time gives the possibility to know the connected load.

During the observation time, the measured load is compared with tabled values in order to determine the result.

The turn-on diagnostic status is internally stored until a successive diagnostic pulse is requested.

Figure 27. Turn-on diagnostic cycle. Positive and negative output behaviour



A turn-on diagnostic cycle is activated writing '1' on the D7 of byte IB0 only when the amplifier is in Tristate-mode. Note that the turn-on diagnostic state machine is sensible to the rise edge of this bit. To run another cycle of turn-on diagnostic it is necessary to:

1. wait that the previous cycle ends;
2. clear the D7-IB0 bit.
3. write '1' on D7-IB0 bit.

It is possible to run the turn-on diagnostic several times by simply resetting the D7-IB0 meanwhile the amplifier is in amplifier mode and writing back '1' on D7-IB0 when the amplifier is in tristate mode.

Between two diagnostic sequences it is necessary to reset the data register by an I^2C reading instruction. Note that the reading instruction has been placed during the second diagnostic pulse.

The µP can program the TDA7801 in order to run a cycle of turn-on diagnostic and to move in amplifier-mode at the end of this cycle (*Figure 28*)); the I^2C bus instructions needed to program this sequence are:

11011000 -00100000-1XXXXXXX-1XXXXXXX

Note: The diagnostic enable bit (D7-IB0) has to be set before the amplifier mode bit (D7-IB1)

Figure 28. Turn-on diag. cycle with transition in amp. mode. Positive and negative output behaviour

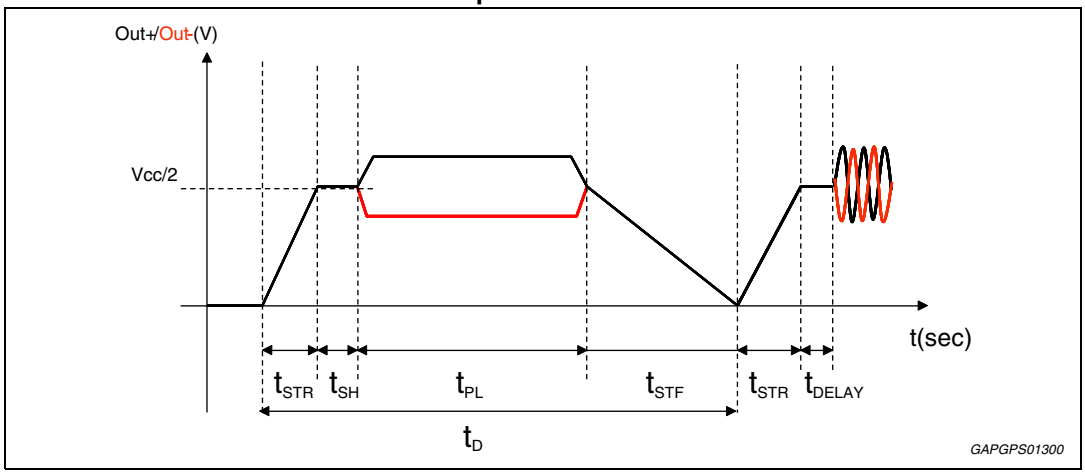


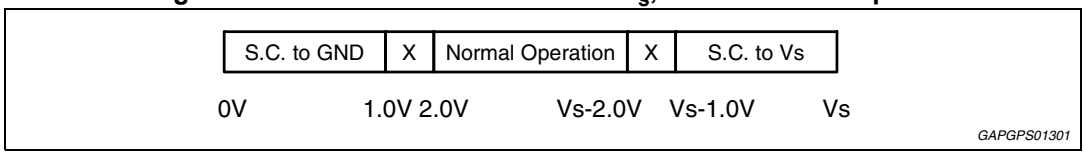
Table 7. Start-up diagnostic pulse typical timing

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max	
t_{STR}(1)	Start-up diagnostic rise	0.8	1.5	3	ms
t_{SH}(2)	Short to Vcc/Gnd check		5		ms
t_{PL}(2)	Plateau time		162		ms
t_{STF}(1)	Start-up diagnostic fall	6	8.5	14	ms
t_{DELAY}(2)	Delay time before play		5		ms
t_D	Diagnostic pulse		182	190	ms

1. These t_{STR} and t_{STF} values are relative to capacitors on A3V3 and D3V3 respectively equal to 47 µF and 22 µF. The t_{STR} and t_{STF} are proportional to capacitors value.
2. Values relative to fs = 44100Hz.

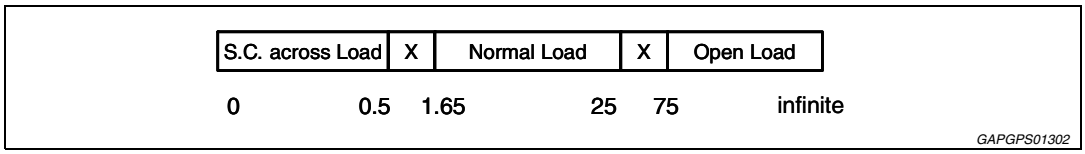
The information related to the outputs status is read and memorized at the end of the voltage pulse top. The diagnostic cycle last no more than Td. No audible noise is generated in the process. As for short to GND / Vs the fault-detection thresholds remain unchanged independently of the gain setting. They are as in *Figure 29*.

Figure 29. Short to GND and short to V_s, threshold description



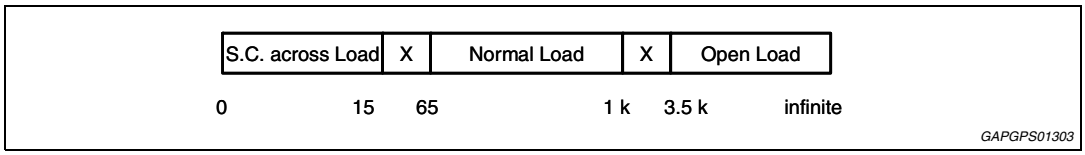
Concerning short across the speaker / open speaker, the threshold varies from speaker mode to booster mode diagnostic setting, since different loads are expected (either normal speaker's impedance or high impedance). The speaker or booster mode is selected with bit D6-IB0 (channel 1 and 3) and bit D5-IB0 (channel 2 and 4). The values in case of speaker mode gain are as in *Figure 30*.

Figure 30. Short across the speaker and open load threshold description, in amplifier mode.



If the booster mode is selected, the same thresholds will change as in *Figure 31*.

Figure 31. Short across the speaker and open load threshold description, in line driver mode.



When the amplifier is biased and the diagnostic is still enabled the permanent diagnostic takes place. The previous turn-on state is kept until a short appears at the outputs because only in this case a new diagnostic cycle can start.

6.3 Permanent diagnostic

Detectable conventional faults are:

- Short to GND
- Short to V_s
- Short across the speaker

The following additional features are provided:

- Output offset detection
- AC diagnostic

The TDA7801 diagnostic has 2 different cycles:

1. Restart cycle. It is a 1 ms pulse. During this period a check of the outputs is made.
2. Plateau cycle. It is a 100 ms pulse. During this period a check of the outputs is performed and the result of diagnostic analysis is communicated by means of I^2C bus.

The TDA7801 has 2 different operating behaviors when a fault occurs:

1. Restart mode, (D6-IB0='0'). The diagnostic is not enabled. Each audio channel operates independently of each other. If any of the a.m. faults occurs, only the