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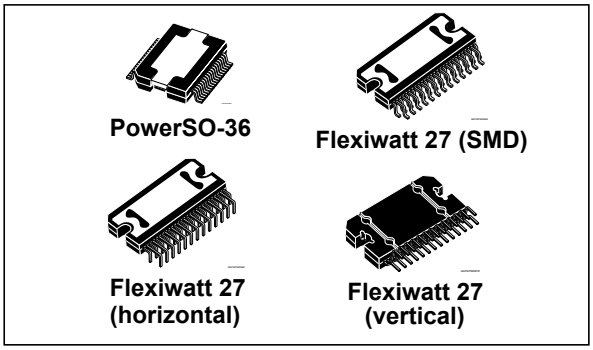
TDA7803A

High efficiency digital input automotive quad power amplifier with built-in diagnostics features, ’start stop’ compatible

Datasheet - production data



Features

- AEC-Q100 qualified
- 24-bit digital processing
- 115 dB dynamic range (A-weighted)
- SB-I (SB - improved) high efficiency operation the highest ’non - class D’ efficiency
- Parallel mode function availability
- High output power capability:
  - 4 x 27 W 4 Ω @ 14.4 V, 1 kHz, THD = 10%
  - 4 x 47 W 2 Ω @ 14.4 V, 1 kHz, THD = 10%
- Flexible mode control:
  - Full I^2C bus driving 1.8V/3.3V) with four addresses selectable (only for PowerSO36 package option)
  - Independent front/rear play/ mute
  - Selectable digital gains for very-low noise line-out function
  - Digital diagnostic with DC and AC load detections
- Start-stop compatibility (operation down to 6V)
- Sample rates: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Flexible serial data port (1.8 V / 3.3 V):
  - I^2S standard, TDM 4Ch, TDM 8Ch, TDM 16ch (8+8ch)
- Offset detector
- Independent front/rear clipping detector
- Programmable diagnostic pin
- CMOS compatible enable pin
- Thermal protection
- Pop free in mute to play transitions and viceversa

Description

The TDA7803A is a single chip quad bridge amplifier in advanced BCD technology integrating: a full D/A converter, digital input for direct connection to I^2S (or TDM) and powerful MOSFET output stages.

The integrated D/A converter allows the performance to reach an outstanding 115 dB S/N ratio with more than 110 dB of dynamic range.

Moreover the TDA7803A integrates an innovative high efficiency concept, optimized also for uncorrelated music signals. The device is designed to be compatible to battery modulation for class-G systems.

Thanks to this concept, the dissipated “output power” under average listening conditions can be reduced up to 50% when compared to the conventional class AB solutions.

The TDA7803A integrates also a programmable PLL that is able to lock at the input frequencies of 64*Fs for all the input configurations.

The device is equipped with a full diagnostics array that communicates the status of each speaker through the I^2C bus. The same I^2C bus allows to control several configurations of the device.

The TDA7803A is able to play music down to 6 V supply voltage - so it is compatible with the so called 'start stop' battery profile recently adopted by several car makers (thus reducing the fuel consumption and the impact over the environment).

Contents

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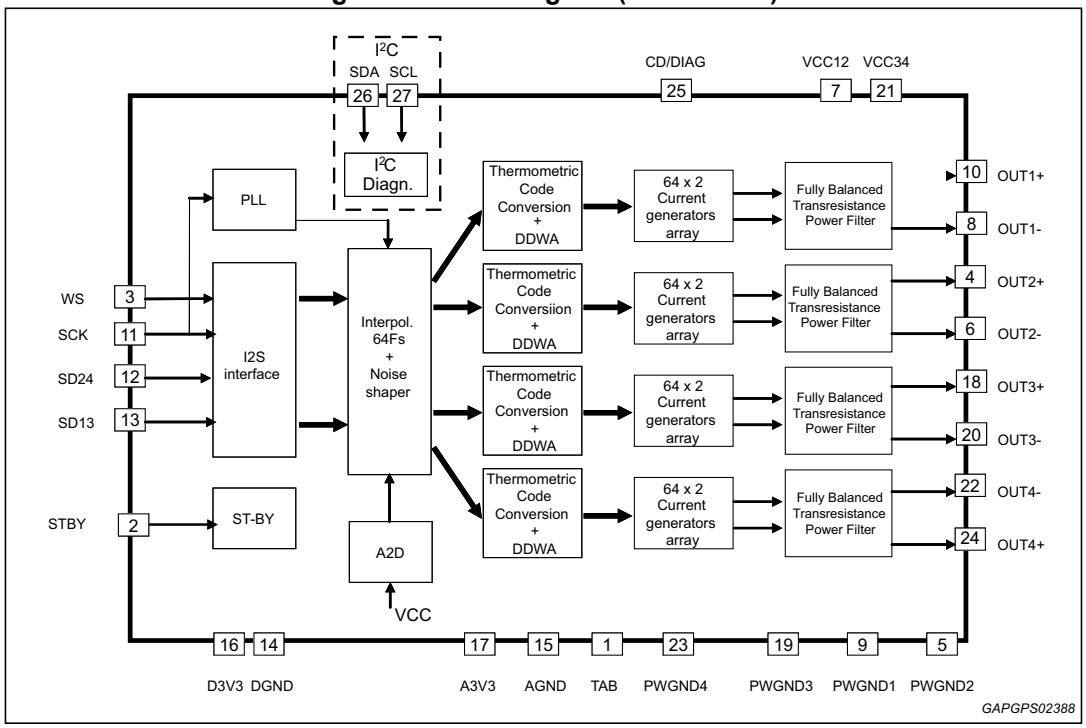
List of figures

1 Block diagram and pins description

1.1 Block diagram

Figure 1. Block diagram (Flexiwatt27)



1.2 Pins description

Figure 2. Pins connection diagrams

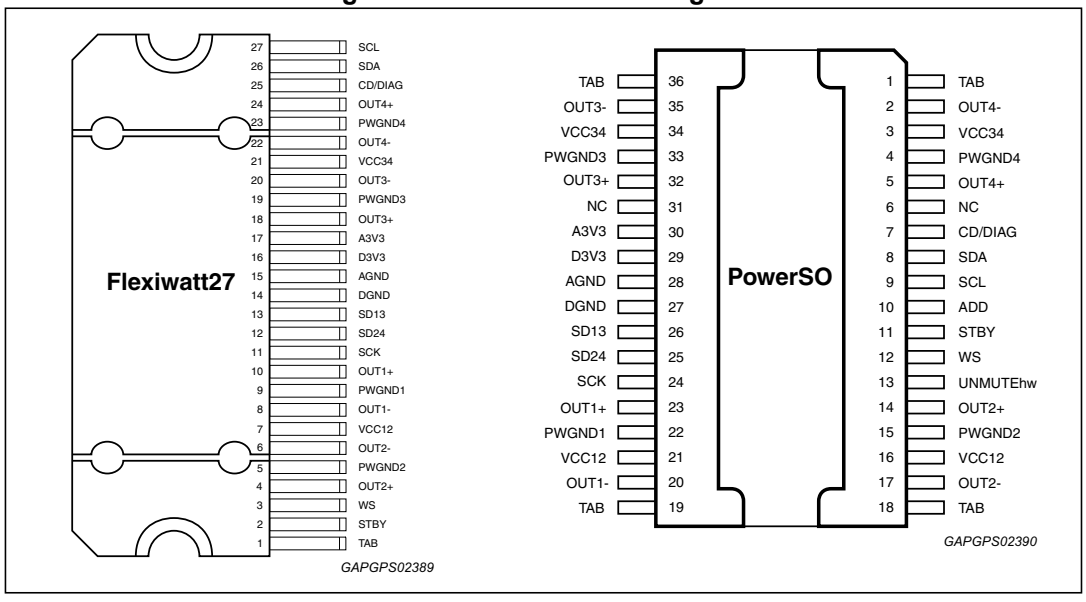


Table 1. Flexiwatt27 pins description

N°	Pin	Function	
1	TAB	TAB connection	Ground
2	STBY	STBY pin	Input
3	WS	Word select (I^2S bus)	Logic Input
4	OUT2+	Channel 2 (Left Rear) positive output	Power Output
5	PWGND2	Power ground channels 2	Power Ground
6	OUT2-	Channels 2 (Left Rear) negative output	Power Output
7	VCC12	Channel 1 and 2 positive supply	Battery
8	OUT1-	Channel 1 (Left Front) negative output	Power Output
9	PWGND1	Power ground channel 1	Power Ground
10	OUT1+	Channel 1 (Left Front) positive output	Power Output
11	SCK	Serial clock (I^2S bus)	Logic Input
12	SD24	Serial data channels 2 and 4 (I^2S bus)	Logic Input
13	SD13	Serial data channels 1 and 3 (I^2S bus)	Logic Input
14	DGND	Digital ground	Signal Ground
15	AGND	Analog ground	Signal Ground
16	D3V3	Digital 3.3V supply filter	Digital Regulator
17	A3V3	Analog 3.3V supply filter	Analog Regulator
18	OUT3+	Channels 3 (right front) positive output	Power Output
19	PWGND3	Power ground channel 3	Power Ground
20	OUT3-	Channels 3 (right front) negative output	Power Output
21	VCC34	Channels 3 and 4 positive supply	Battery
22	OUT4-	Channels 4 (right rear) negative output	Power Output
23	PWGND4	Power ground channel 4	Power Ground
24	OUT4+	Channels 4 (right rear) positive output	Power Output
25	CD/DIAG	Clip detector and diagnostic output	Open Drain Output
26	SDA	I^2C data	Signal Input
27	SCL	I^2C clock	Signal Input

Table 2. PowerSO36 pins description

N°	Pin	Function	
1	TAB	Device slug connection	Ground
2	OUT4-	Channels 4 (right rear) negative output	Power Output
3	VCC34	Channels 3 and 4 positive supply	Battery
4	PWGND4	Power ground channel 4	Power Ground
5	OUT4+	Channels 4 (right rear) positive output	Power Output
6	NC	Not connected	-
7	CD/DIAG	Clip detector and diagnostic output	Open Drain Output
8	SDA	I^2C data	Signal Input
9	SCL	I^2C clock	Signal Input
10	ADD	I^2C Address	Logic Input
11	STBY	STBY pin	Input
12	WS	Word select (I^2S bus)	Logic Input
13	UNMUTEhw	Unmute Hardware	Logic Input
14	OUT2+	Channel 2 (Left Rear) positive output	Power Output
15	PWGND2	Power ground channels 2	Power Ground
16	VCC12	Channel 1 and 2 positive supply	Battery
17	OUT2-	Channels 2 (Left Rear) negative output	Power Output
18	TAB	Device slug connection	Ground
19	TAB	Device slug connection	Ground
20	OUT1-	Channel 1 (Left Front) negative output	Power Output
21	VCC12	Channel 1 and 2 positive supply	Battery
22	PWGND1	Power ground channel 1	Power Ground
23	OUT1+	Channel 1 (Left Front) positive output	Power Output
24	SCK	Serial clock (I^2S bus)	Logic Input
25	SD24	Serial data channels 2 and 4 (I^2S bus)	Logic Input
26	SD13	Serial data channels 1 and 3 (I^2S bus)	Logic Input
27	DGND	Digital ground	Signal Ground
28	AGND	Analog ground	Signal Ground
29	D3V3	Digital 3.3V supply filter	Digital Regulator
30	A3V3	Analog 3.3V supply filter	Analog Regulator
31	NC	Not connected	-
32	OUT3+	Channels 3 (right front) positive output	Power Output
33	PWGND3	Power ground channel 3	Power Ground
34	VCC34	Channels 3 and 4 positive supply	Battery
35	OUT3-	Channels 3 (right front) negative output	Power Output
36	TAB	Device slug connection	Ground

2 Application diagrams

Figure 3. I²C bus mode application diagram (Flexiwatt))

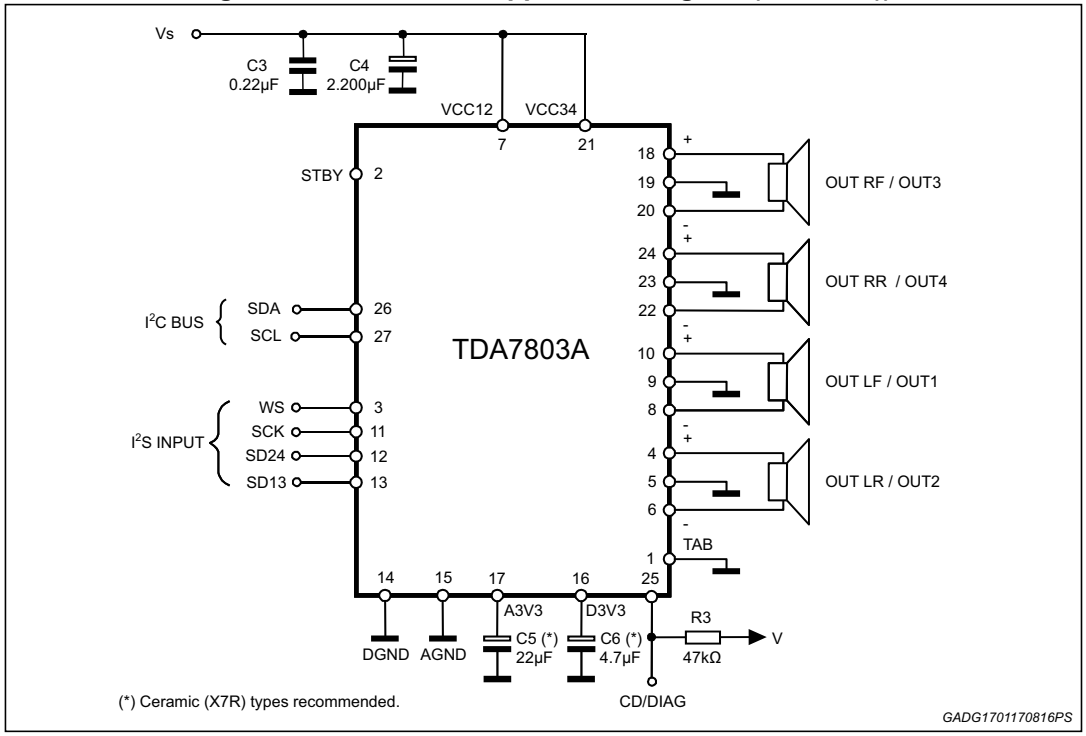
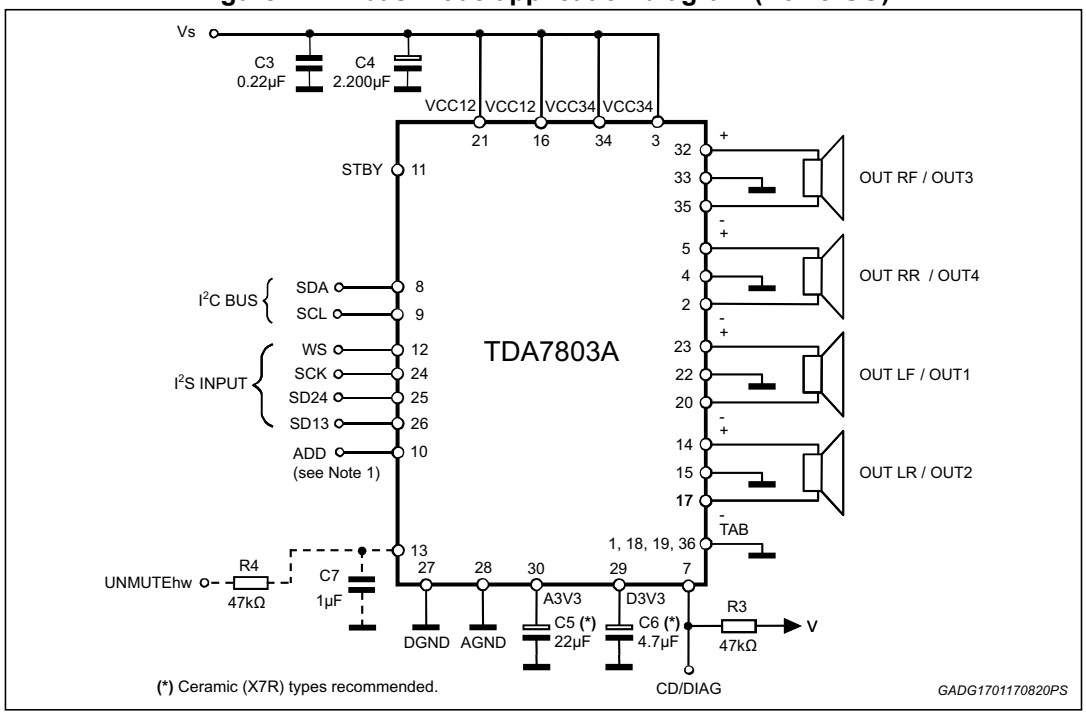


Figure 4. I²C bus mode application diagram (PowerSO)



1. Refer to *Section 9: I²C bus interface* for connection suggestions.

3 Electrical specification

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	DC supply voltage	-0.3 to 28	V
V_{peak}	Transient supply voltage for t = 100 ms	-0.3 to 50	V
V_{i2c}	I^2C bus pins voltage	-0.3 to 4.6	V
V_{i2s}	I^2S bus pins voltage	-0.3 to 4.6	V
V_{unmute}	Unmute hardware voltage (PSO36 only)	-0.3 to 4.6	V
V_{cd}	CD/Diag pin voltage	-0.3 to 20	V
V_{stby}	STBY pin voltage	-0.3 to 4.6	V
I_O	Output peak current (repetitive f > 10 Hz)	internally limited(1)	A
P_{tot}	Power dissipation T_{case} = 70 °C	85	W
T_{stg}, T_j	Storage and junction temperature	–55 to 150	°C
T_{amb}	Operative temperature range(2)	-40 to 105	°C
C_{max}	Maximum capacitor vs. ground connected to the output	10	nF
ESD_{HBM}	ESD protection HBM (3)	2000	V
ESD_{CDM}	ESD protection CDM (3)	500	V

1. Internally limited by overcurrent protection.
2. A suitable heatsink/dissipation system should be used to keep T_j inside the specified limits.
3. Conforming to Q100 ESD standard.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case (max.)	1	°C/W

3.3 Electrical characteristics

Referred to the test setup V_S = 14.4 V; R_L = 4 Ω; f = 1 kHz; tested at T_{amb} = 25 °C; functionality guaranteed for T_j = -40 °C to 150 °C; SB-I mode; unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General						
V_S	Supply voltage range	R_L = 4 Ω	6	-	18.5	V
		R_L = 2 Ω, std_bridge	6	-	16	V
		R_L = 2 Ω, SBI	6	-	16	V
I_{SB}	Standby current	-	-	1	4	µA
I_q	Total quiescent current in amplifier mode	Mute condition	-	170	210	mA
I_{qECO}	Total quiescent current in ECO mode	ECO mode	-	35	40	mA
A_M	Mute attenuation	-	80	-	-	dB
V_{OS}	Offset voltage	Mute and play	-25	-	+25	mV
V_{lowM}	V_{CC} low supply mute threshold (Min I^2C setting - default)	Attenuation <0.5 dB, digital mute disabled	-	-	5.6	V
		Attenuation ≥60 dB, digital mute disabled	5	-	-	V
$V_{POWONRESET}$	Supply voltage of power-on reset	-	-	3.5	-	V
V_{highM}	High supply mute threshold	Attenuation = -6 dB	19	-	21	V
Audio performances						
P_O	Output power	R_L = 4 Ω; max power (1)	40	43	-	W
		THD = 10 %	25	27	-	W
		THD = 1 %	20	22	-	W
		R_L = 2 Ω; THD 10%	44	47	-	W
		R_L = 2 Ω; THD 1%	34	37	-	W
		R_L = 2 Ω; max power (1)	69	72	-	W
THD_{SB}	Total harmonic distortion (Standard bridge)	P_O = 4 W, f=1 kHz, G_{V1}	-	0.015	0.04	%
		P_O = 4 W, f=10 kHz, G_{V1}	-	0.15	0.5	%
		R_L =100 Ω input=-10 dBFS, f = 1 kHz, $G_{V1,2,3,4}$	-	0.01	0.02	%
THD	Total harmonic distortion (SBI mode)	P_O = 2 W, f = 1 kHz, G_{V1}	-	0.015	0.04	%
		P_O = 6 W, f =1 kHz, G_{V1}	-	0.02	0.06	%

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_T(2)	Cross talk	f = 1 kHz	-	100	-	dB
		f = 10 kHz	-	80	-	dB
G_{V1}	Voltage gain 1	@ Amplitude = -18 dBFs	2.3	2.5	-	Vp
G_{V2}	Voltage gain 2		1.25	1.35	-	Vp
G_{V3}	Voltage gain 3		0.9	1	-	Vp
G_{V4}	Voltage gain 4		0.4	0.55	-	Vp
DR(2)	Dynamic range	A-wtd values, G_{V1} gain	-	115	-	dB
E_{out1}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V4}$	A-wtd values	- -	27 18	40 -	µV
E_{out2}	Output noise voltage $G_V = G_{V1}$ $G_V = G_{V4}$	ITU-R 468	- -	70 45	96 -	µV
SNR(2)	Signal to noise ratio	A-wtd values, G_{V1} gain	-	115	-	dB
ΔG_v	Channel Gain Mismatch	-	-0.5	-	0.5	dB
SSR	Supply slew rate	-	-	1	-	V/µs
PSRR	Power supply rejection ratio	f = 1 kHz; V_r = 1 Vpk;	60	70	-	dB
$\lvert\Delta V_{OITU}\rvert$	ITU Pop filter output voltage (standard bridge mode)	Eco mode to mute transition and vice versa	-	-	4	mV
		Mute to Play and Play to Mute transition(3)	-	0	-	mV
Clipping detector						
CD_{LK}	Clip det high leakage current	CD off, V = 3.3 V	-	0	1	µA
CD_{SAT}	Clip det sat. voltage	CD on; I_{CD} = 1 mA	-	50	-	mV
$CD1_{THD}$	Clip det THD threshold 1	-	-	2	3	%
$CD2_{THD}$	Clip det THD threshold 2	-	4	6	8	%
$CD3_{THD}$	Clip det THD threshold 3	-	9	12	14	%
Turn on diagnostics for parallel mode configuration						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
P_{vs}	Short to V_s det. (above this limit, the output is considered in short circuit to V_S)	-	V_s - 1	-	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).	-	2	-	V_s - 2	V
Lsc	Shorted load det.	-	-	-	0.7	Ω
Lop	Normal load det.	-	1.3	-	30	Ω
Lnop	Open load det.	-	70	-	-	Ω
Turn-on diagnostic for parallel mode configuration						
Lsc	Shorted load det.	-	-	-	0.35	Ω
Lop	Normal load det.	-	0.65	-	15	Ω
Lnop	Open load det.	-	35	-	-	Ω
Rss	Soft Short Diagnostic threshold (below this value, soft short resistance is recognized)	-	500	-	-	Ω
Turn-on diagnostic for line driver mode configuration						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	-	-	-	1	V
Pvs	Short to V_s det. (above this limit, the output is considered in short circuit to V_s)	-	V_s - 1	-	-	V
Pnop	Normal operation thresholds. (within these limits, the output is considered without faults).	-	2	-	V_s - 2	V
Lsc	Shorted load det.	-	-	-	20	Ω
Lop	Normal load det.	-	60	-	1400	Ω
Lnop	Open load det.	-	2600	-	-	Ω
Rss	Soft Short Diagnostic threshold (below this value, soft short resistance is recognized)	-	5.8(4)	-	-	kΩ
AC-diagnostic						
$I_{ACTRESH}$	AC diagnostic current threshold	IB4 – D4= ‘0’	250	375	500	mA
		IB4 – D4= ‘1’	125	187	250	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Permanent diagnostics						
Pgnd	Short to GND det. (below this limit, the output is considered in short circuit to GND)	Power amplifier in Mute or Play, one or more short circuits protection activated	-	-	1	V
Pvs	Short to V_s det. (above this limit, the Output is considered in short circuit to V_s)	-	V_s - 1	-	-	V
Pnop	Normal operation thresholds. (Within these limits, the output is considered without faults)	-	2	-	V_s - 2	V
L_{SC}	Shorted load det.	Parallel mode	-	-	0.35	Ω
		Speaker mode	-	-	0.7	
		Line driver mode	-	-	20	
L_{OP}	Normal load det.	Parallel mode	0.65	-	-	Ω
		Speaker mode	1.3	-	-	
		Line driver mode	60	-	-	
T_{ph}	Thermal protection junction temperature	Attenuation ≥60 dB	-	165	-	°C
T_{pl}		Attenuation <0.5 dB	-	155	-	°C
T_{w1}	Thermal warning junction temperature(5)	-	-	Tpl-5	-	°C
T_{w2}		-	-	Tpl-10	-	°C
T_{w3}		-	-	Tpl-20	-	°C
T_{w4}		-	-	Tpl-30	-	°C
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	Input low voltage	-	-	-	0.8	V
V_{IH}	Input high voltage	-	1.3	-	-	V
V_{olmax}	Maximum I2C data pin low voltage when current Isink is sinked	I_{sink} = 2 mA	-	-	0.27	V
		I_{sink} = 8 mA	-	-	0.7	V
I_{limax}	Maximum input leakage current	V = 3.6 V	-	-	1	µA
STBY pin						
V_{ILSTBY}	Input low voltage	-	-	-	1.2	V
V_{IHSTBY}	Input high voltage	-	2.4	-	-	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{ILSTBY}	Logic '0' output current	V_{IN} = 0.45 V	-	-	1	µA
I_{IHSTBY}	Logic '1' input current	V_{IN} = 2.3 V (IB0 D4=0)	-	-	1	µA
I^2S pins						
V_{IL-I2S}	Input low voltage	-	-	-	0.8	V
V_{IH-I2S}	Input high voltage	-	1.3	-	-	V
I_{IH}	Input high current	@ V_I = 3.3 V	-	-	1	µA
I_{IL}	Input low current	@ V_I = 0 V	-	-	1	µA
Unmute hardware (pin 13)						
V_{HW_UNMUTE}	Hardware unmute threshold (PSO36 only)	Attenuation ≥60 dB	-	-	1.2	V
		Attenuation <0.5 dB	2.6	-	-	V
I_{UNMUTE}	Input high current	@ V_I = 3.3 V	-	-	1	µA
	Input low current	@ V_I = 0 V	-	-	1	µA

1. Square-wave input / saturated output.
2. Evaluated at bench during product validation.
3. Guaranteed by design (intrinsically immune from any pop at mute to play and play to mute transitions)
4. The values are the ones that guarantee the correct working of the diagnostic. Since the value is strongly dependent on the loudspeaker, we decided to target the values for the limits of open load and short load diagnostic.
5. Thermal warning junction temperature values could be changed via I^2C bits IB5-d6,d7.

3.4 Electrical characteristics typical curves

Figure 5. Quiescent current vs. supply voltage

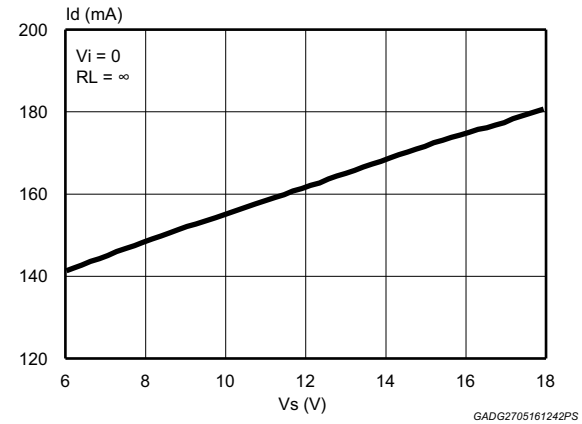


Figure 6. Output power vs. supply voltage (4 Ω)

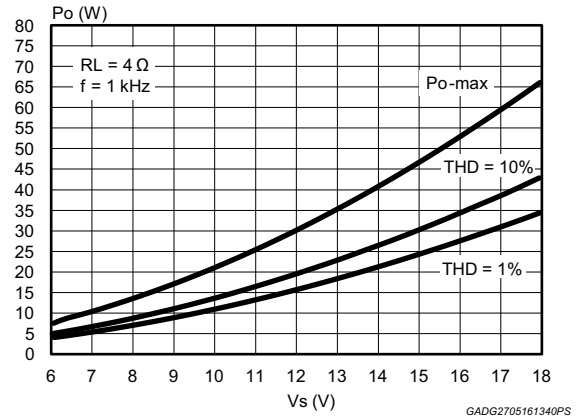


Figure 7. Output power vs. supply voltage (2 Ω, STD mode)

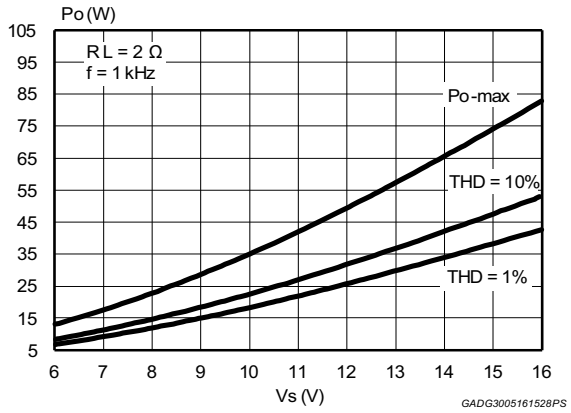


Figure 8. Distortion vs. output power (4 Ω, STD mode)

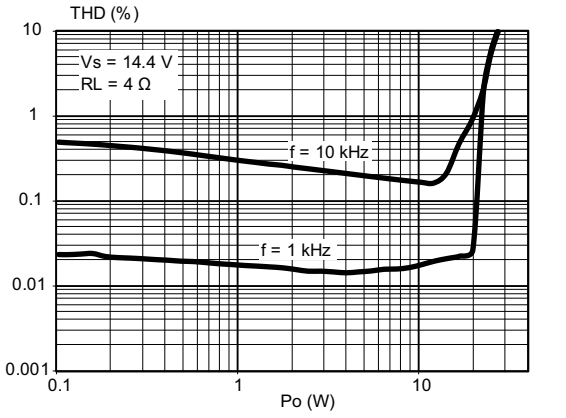


Figure 9. Distortion vs. output power (4 Ω, SBI mode)

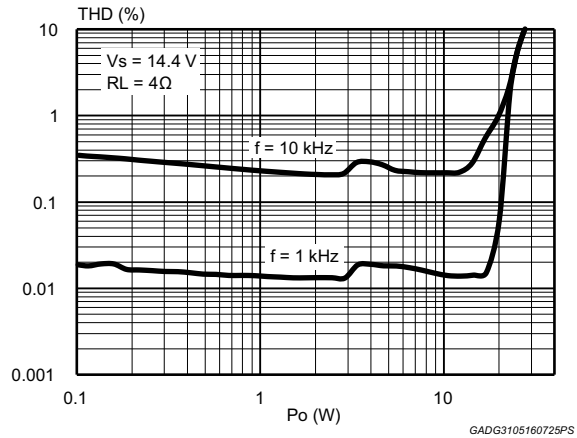


Figure 10. Distortion vs. output power (2 Ω, STD mode)

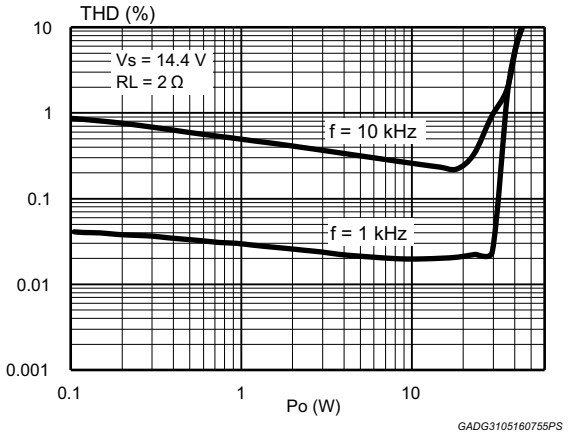


Figure 11. Distortion vs. output power (2 Ω, SBI mode)

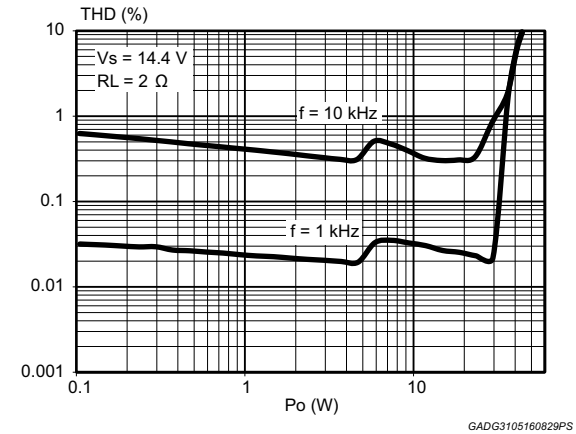


Figure 12. Distortion vs. frequency (4 Ω)

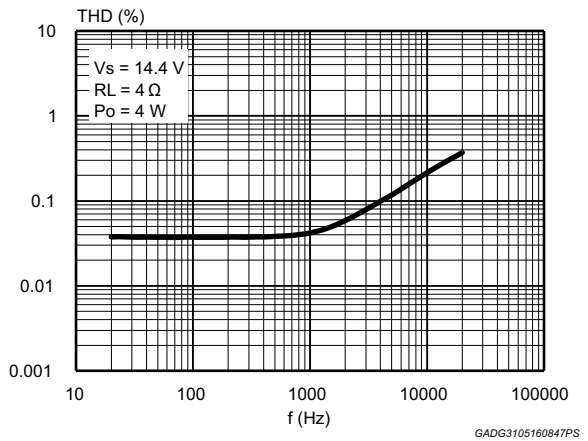


Figure 13. Distortion vs. frequency (2 Ω)

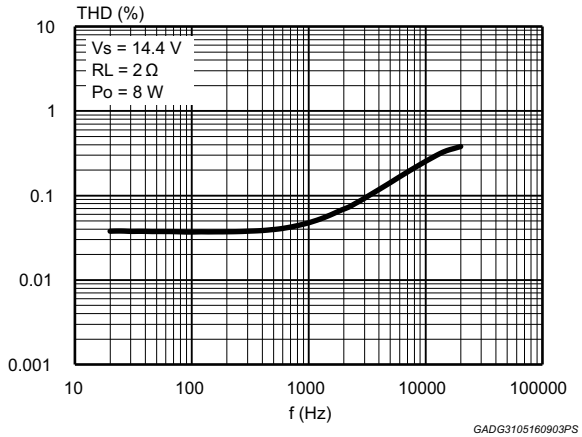


Figure 14. Distortion vs. output power (4 Ω, Vs = 6 V)

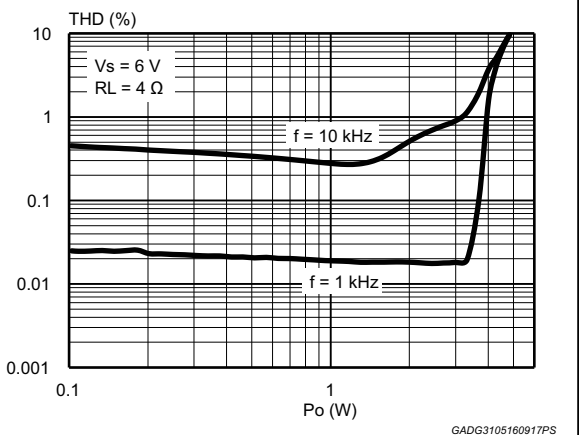


Figure 15. Distortion vs. output power (2 Ω, Vs = 6 V)

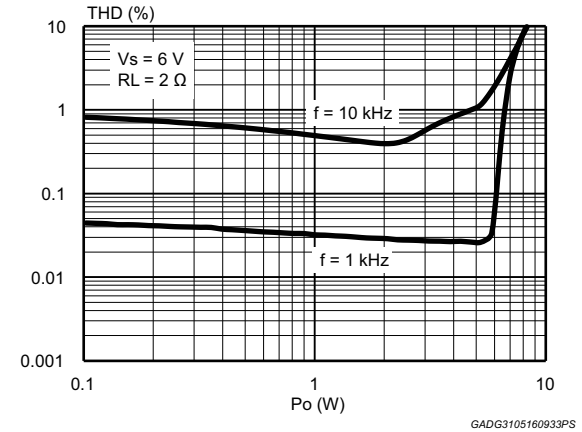


Figure 16. Vo vs. Vin (Gv1-2-3-4 settings)

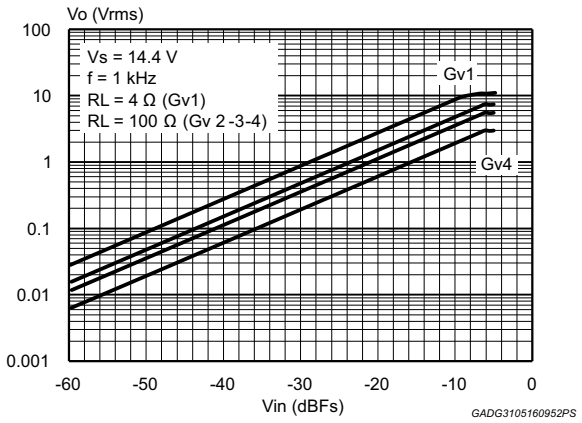


Figure 17. Vo vs. Vin (Gv1-2-3-4 settings + 6 dB dig. gain)

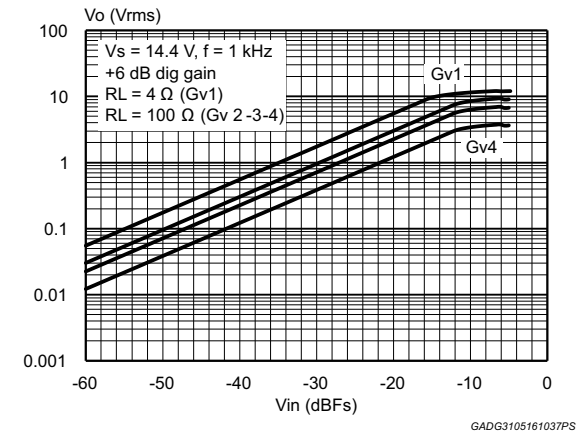


Figure 18. Distortion vs. output voltage (LD-Gv2)

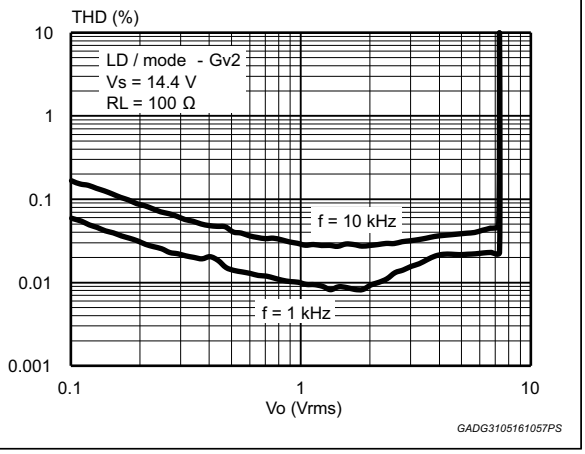


Figure 19. Distortion vs. output voltage (LD-Gv3)

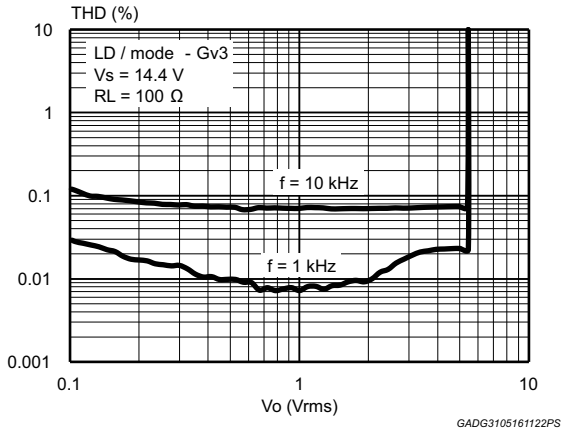


Figure 20. Distortion vs. output voltage (LD-Gv4)

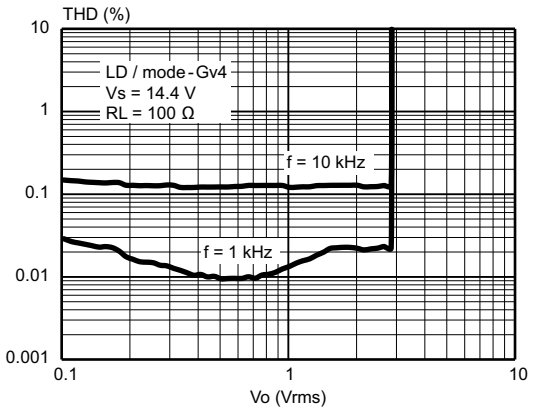


Figure 21. Output attenuation vs. Vs

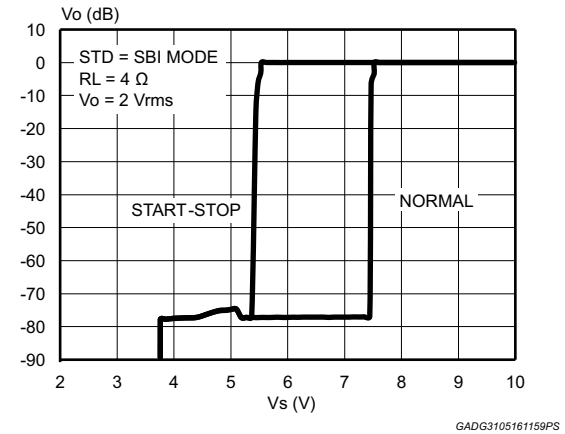


Figure 22. Crosstalk vs. frequency (STD mode)

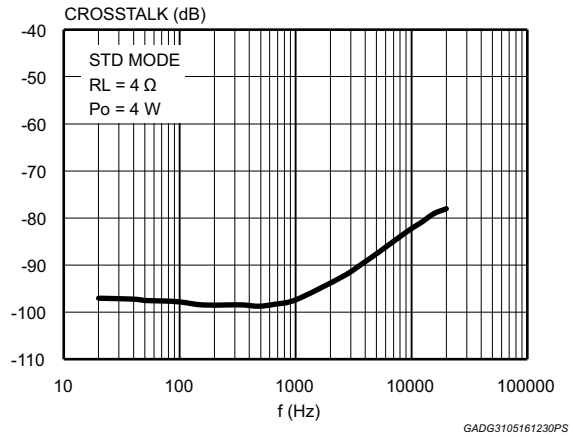


Figure 23. Crosstalk vs. frequency (SBI mode)

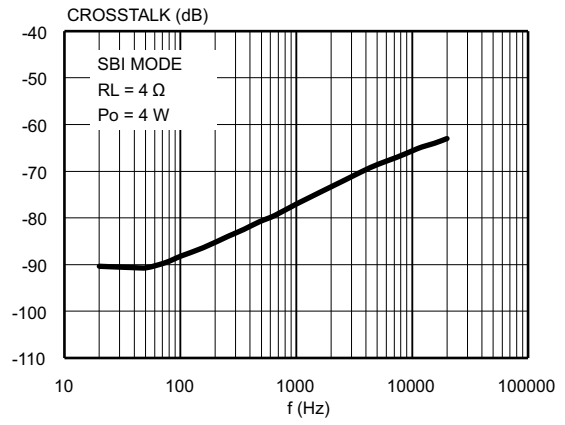


Figure 24. Supply voltage rejection vs. frequency

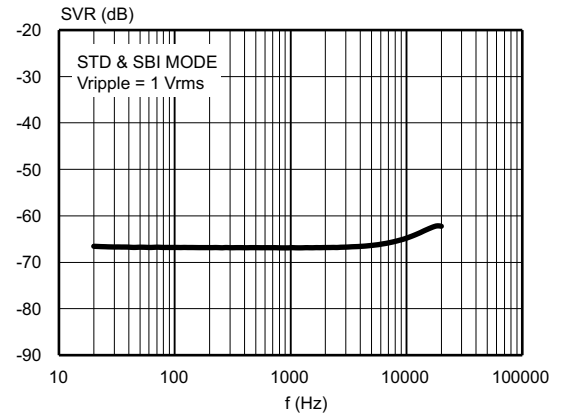


Figure 25. Total power dissipation & efficiency vs. Po (4 Ω, STD, Sine)

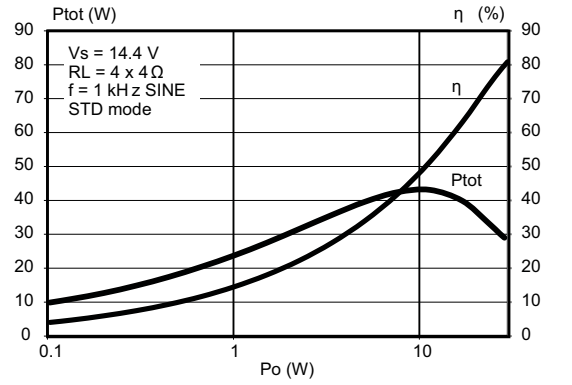


Figure 26. Total power dissipation & efficiency vs. Po (4 Ω, SBI, Sine)

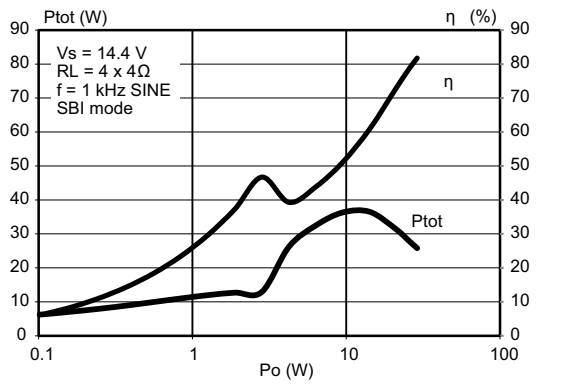


Figure 27. Total power dissipation & efficiency vs. Po (2 Ω, SBI, Sine)

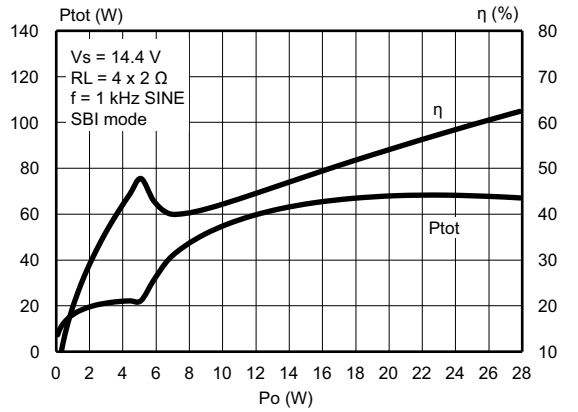


Figure 28. Power dissipation vs. average Po (audio program simulation, 4 Ω)

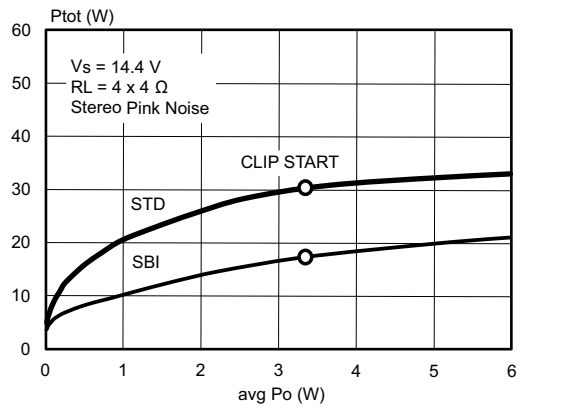


Figure 29. Power dissipation vs. average Po (audio program simulation, 2 Ω)

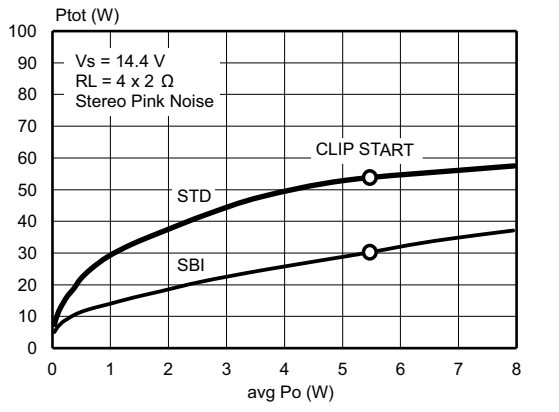
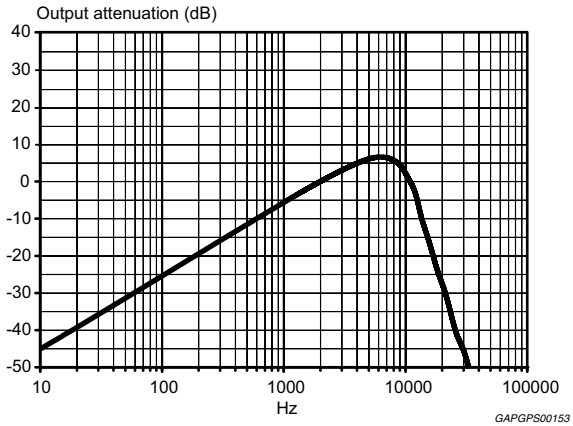


Figure 30. ITU R-ARM frequency response, weighting filter for transient pop



4 Operation states

TDA7803A functionality is regulated by means of a finite state machine.

Finite state machine diagram is reported in *Figure 31*.

Main states are:

- Standby
- ECO-mode
- Amplifier mode
- Turn-on diagnostic
- Permanent diagnostic

4.1 Standby state

When STBY pin is under VILSTBY voltage the amplifier is in stand-by state and the current consumption is very low.

4.2 ECO-mode state

When STBY pin is over VIHSTBY the amplifier is in a state of low current absorption, the ECO-mode. The short circuit protections are active and the amplifier is ready for receiving commands from micro-controller through I^2C interface.

Outputs and A3V3 supply are biased at 0 V.

4.3 Amplifier-mode state

When TDA7803A is in ECO-mode state, IB7-d0 is set to "1", (Amplifier-ON), and I^2S clock is present the amplifier moves to Amplifier-mode state.

The outputs are biased from 0 V to Vcc/2 and the current consumption reaches "Iq" level until the amplifier is set in MUTE or in PLAY with low level signal. User can move the amplifier from MUTE to PLAY and viceversa acting on IB2-d4, d3 bits.

A hardware unmute pin is available in PSO36 package only.

4.4 Turn-on and permanent diagnostic

TDA7803A provides a powerful and precise diagnostic both with speaker and line driver loads.

There are two main diagnostic states:

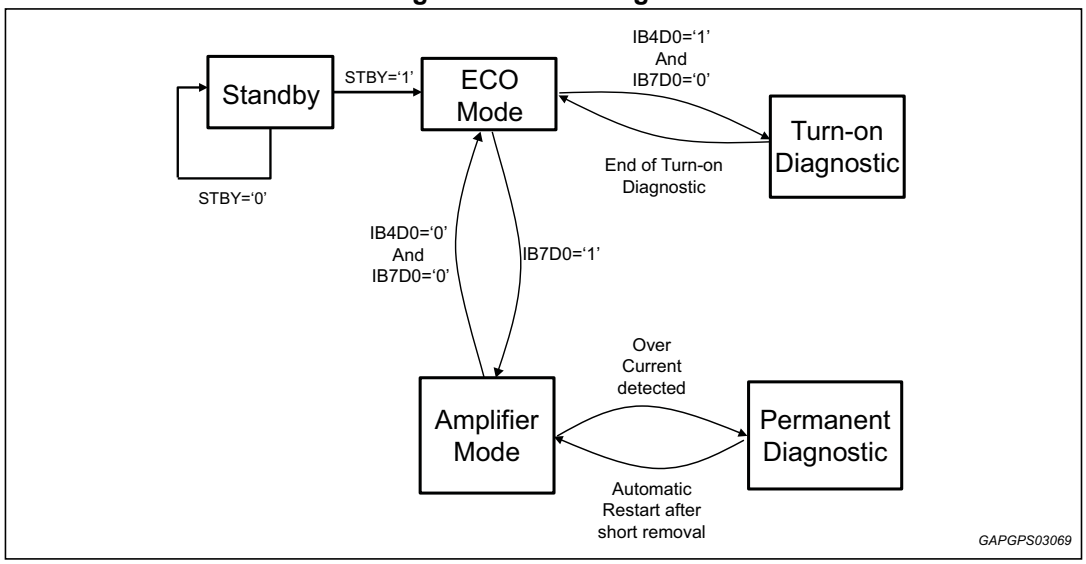
- Turn-on diagnostic
- Permanent diagnostic.

The Turn-on diagnostic could be run in ECO-mode state and is suggested for sensing the presence of faults before amplifier turn-on, in order to avoid unwanted or dangerous conditions due to wrong connections or absence of load.

The Permanent diagnostic is automatically run by TDA7803A when a fault occurs during PLAY and over current protections are triggered.

Turn-on and Permanent diagnostic functionality are described in *Section 6*.

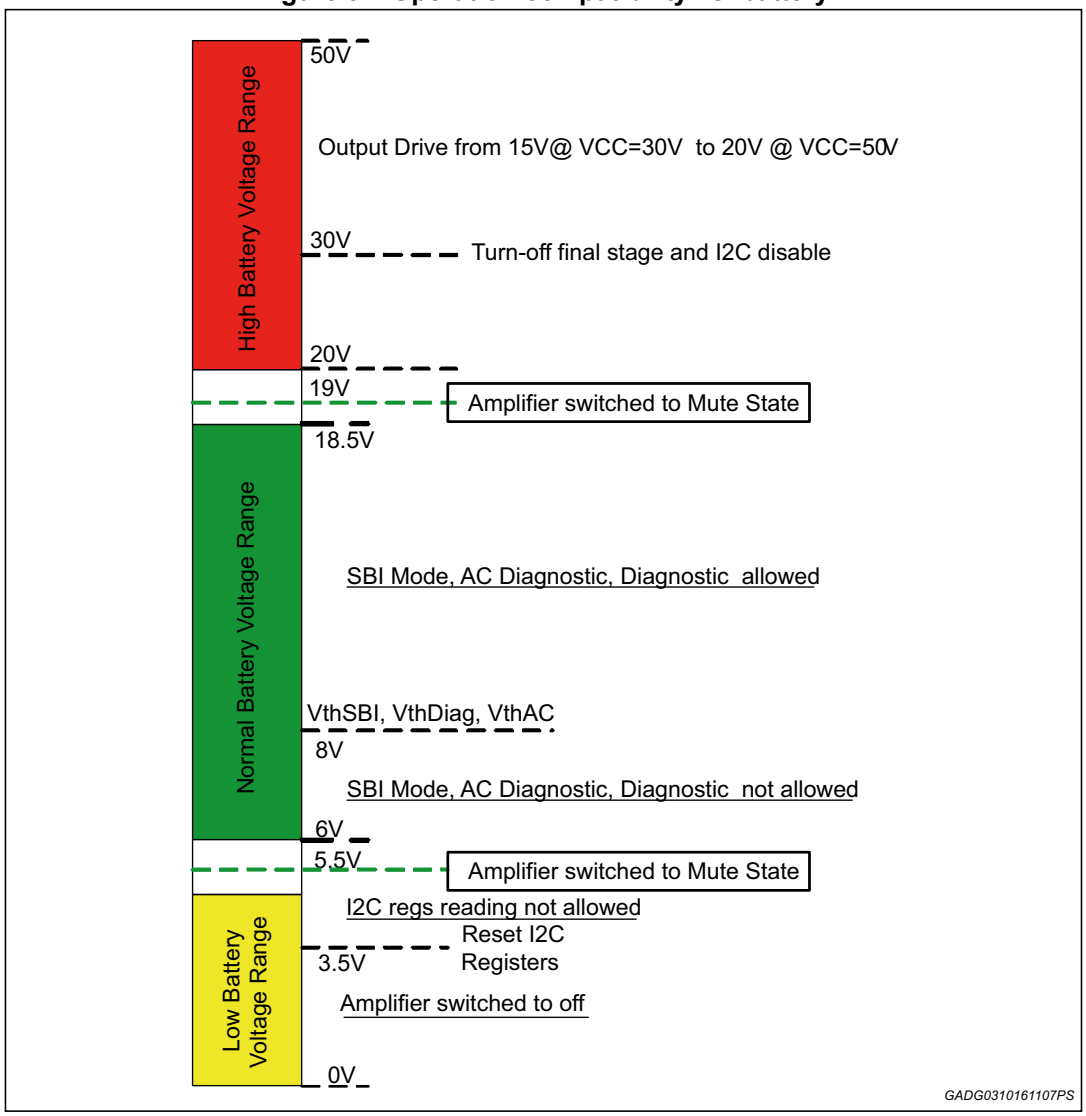
Figure 31. State diagram



5 Operation compatibility vs. battery

Here below the operation compatibility vs. the battery value is shown. For each battery voltage range, only a limited number of functions are available as it is shown below:

Figure 32. Operation compatibility vs. battery



6 Functional description

6.1 Voltage regulators timing

Pins D3V3 and A3V3 are respectively digital and analog internal regulators outputs. The D3V3 rises right after the STBY pin is at the logical value "1" and its rising time depends on the filter capacitor; the minimum value suggested for this filter is 4.7 µF.

The A3V3 rises after any command that moves the amplifier from ECO - mode; the rising time depends on the combined effect of the external capacitor on the pin and of an internal 2 ms ramp: if the capacitor value is 22 µF or lower, the internal ramp effect is dominant and the rising time will be about 2 ms. On the other hand, when the capacitor has a higher value, the rise time will be higher as well. The suggested value for this capacitor is 22 µF at least.

6.2 Turn-on diagnostic description

The turn-on diagnostic is triggered on the rising edge of bit IB4 D0 when IB7 D0 is "0". This happens when the amplifier is in ECO - mode. It is possible to run one or more turn-on diagnostic sequences according to the following procedure:

1. wait the previous cycle is over
2. read the data bytes DB1,DB2,DB3 and DB4

Please note that all these instructions must be sent while the amplifier is still in ECO - mode (IB7 D0 = "0"), otherwise they won't be executed.

Turn-on diagnostic does not start if V_{CC} is below 8 V or one of the muting condition is present, (low battery mute, high voltage mute, PLL-unlock mute, thermal mute, hardware pin mute).

Note: The diagnostic enable bit (IB4 D0) must be set before the amplifier mode bit (IB7 D0).

DB1, DB2, DB3 must be read before DB4 (after DB4 is read the DB1-2-3-4 are reset).

The detected faults are here described:

Soft Short to GND: it detects the presence of a resistor (see *Table 5* in “Turn-on diagnostic” section) connected between an output and ground, which could result in a wrong open load or short across load diagnostic result (causing an anomalous current consumption in some cases).

Soft Short to VS: it detects the presence of a resistor (see *Table 5* in “Turn-on diagnostic” section) connected between an output and battery, which could result in a wrong open load or short across load diagnostic result (causing an anomalous current consumption in some cases).

Short to GND: it detects the hard connection between an output and ground. The value of the short is able to pull the output between 1.5 V and ground.

Short to VS: it detects the hard connection between an output and battery. The value of the short is able to pull the output between (battery - 1.5 V) and battery.

Short across the speaker: it detects the hard connection across the speaker that is below a certain value. This value guarantees that the IC is able to drive any speaker configuration within the range specified in the datasheet.