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TDA8262HN

Fully integrated satellite tuner

Rev. 01 — 14 December 2004 Product data sheet

1. General description

The direct conversion QPSK demodulator is the front-end receiver dedicated to digital TV broadcasting, satisfying both DVB-S and DBS TV standards. The wide range oscillator (from 950 MHz to 2175 MHz) covers the American, European and Asian satellite bands, as well as the SMA-TV US standard.

The Zero-IF (ZIF) concept discards traditional IF filtering and intermediate conversion techniques.

Gain-controlled amplifiers in the RF guarantee optimum signal level. The variable gain is controlled by the signal returned from the Satellite Demodulator and Decoder (SDD) and applied to pin AGC.

The integrated LNA allows the IC to be directly connected to the LNB output. The LNA can be by-passed by an I^{2}C-bus selectable attenuation, providing a 20 dB extra attenuation in order to handle higher input signal levels of up to 0 dBm per channel.

An integrated loop-through realizes a copy of the input RF signal for another downconverter. This feature offers a BOM reduction and simplifies the application for dual channel demodulation like watch and record.

Connected at the RF input, an RMS level detector provides through I^{2}C-bus read mode the full band input signal level.

The LO quadrature outputs are derived from a high performance integrated LC oscillator. Its frequency is: $\frac{f_{LO}}{N} = \frac{f_{XTAL}}{R}$. Thanks to the low phase noise performance of the integrated LC oscillator which controls the LO frequency, the synthesizer offers a good performance for phase noise in the satellite band. The step size of the LO output frequency is equal to the comparison frequency.

Control data is entered via the I^{2}C-bus. The bus can be either 5.0 V or 3.3 V, allowing compatibility with most of existing microcontrollers.

An 8-byte frame is required to address the device and to program the main divider ratio, the reference divider ratio, the charge-pump current and the operating mode.

A flag is set when the loop is in-lock, readable during read operations, as well as the Power-on reset flag and RF input level.

The device has four selectable I^{2}C-bus addresses. Applying a specific voltage to pin AS selects an address. This feature gives the possibility to use up to four TDA8262HN ICs in the same system.

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2. Features

- Direct conversion QPSK and 8PSK demodulation (ZIF)
- 3.3 V DC supply voltage (no 30 V required)
- Power-down modes selectable by bus
- 950 MHz to 2175 MHz frequency range
- High range input level;
  - –70 dBm to –15 dBm at 75 Ω (normal mode)
  - Up to 0 dBm (20 dB attenuation configuration).
- Low noise RF input (integrated LNA)
- RF loop-through
- 0 dB to 55 dB continuous variable gain on RF input
- RF input level detector
- Switchable 0 dB to 9 dB additional gain on baseband output amplifier
- High AGC linearity (< 0.7 dB/step when used with an 8-bit DAC), AGC controlled voltage between 0.3 V and 3 V
- Programmable 5 MHz to 36 MHz 5th-order baseband filters for I and Q paths
- Fully integrated PLL frequency synthesizer
- Low phase noise fully integrated oscillator
- Operation from a 16 MHz crystal or external clock
- 5 frequency steps from 125 kHz to 2 MHz
- Crystal frequency output to drive the demodulator IC
- Compatible with 5 V and 3.3 V I^2C-bus
- Fully compatible and easy to interface with the PS digital satellite demodulators family
- 32-pin low thermal resistance package.

3. Applications

- Direct Broadcasting Satellite (DBS) QPSK demodulation
- Digital Video Broadcasting (DVB) QPSK demodulation
- BS digital 8PSK demodulation
- DVB-S2 8PSK demodulation.

4. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage			3.15	3.3	3.45	V
I_{CC}	supply current			-	175	-	mA
f_{osc}	oscillator frequency			950	-	2175	MHz
$\Delta\Phi$	absolute quadrature error	measured at 10 MHz		0	-	5	degree
$V_{o(I/Q)(rms)}$	recommended I and Q output voltage RMS value (QPSK signals)		[1]	-	200	-	mV
f_{LPF}	LPF cut-off frequency	5-bit controlled		-	5 to 36	-	MHz

Table 1: Quick reference data *...continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΦN_{osc}	oscillator phase noise in the satellite band	100 kHz offset; f_{comp} = 1 MHz	[2]	-	–100	–94	dBc/Hz
SNF_{SB}	synthesizer noise floor in the satellite band	1 kHz and 10 kHz offset; f_{comp} = 1 MHz	[2]	-	-	–78	dBc/Hz
AGC	amplifier gain control range			55	60	-	dB
T_{amb}	ambient temperature			–20	-	+85	°C

[1] The product is qualified with an output voltage of 550 mV (p-p) differential, however larger values can be used at baseband outputs that might have impact on the product performance.

[2] Phase noise in optimal conditions, see related application note.

5. Typical performances

- Noise figure at maximum gain: 8 dB
- High linearity:
  - IIP_2 = +2 dBm at –20 dBm input and 2.15 GHz
  - IIP_3 = +6 dBm at –20 dBm input and 2.15 GHz.
- Low synthesizer noise floor: –78 dBc/Hz at 1 kHz and 10 kHz offset with f_{comp} = 1 MHz
- AGC linearity: < 0.7 dB/step with a 8-bit DAC
- Maximum I/Q amplitude mismatch: 1 dB
- Maximum I/Q quadrature mismatch: 5°
- Symbol rates: from 1 MBd to 45 MBd.

6. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8262HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1

7. Block diagram

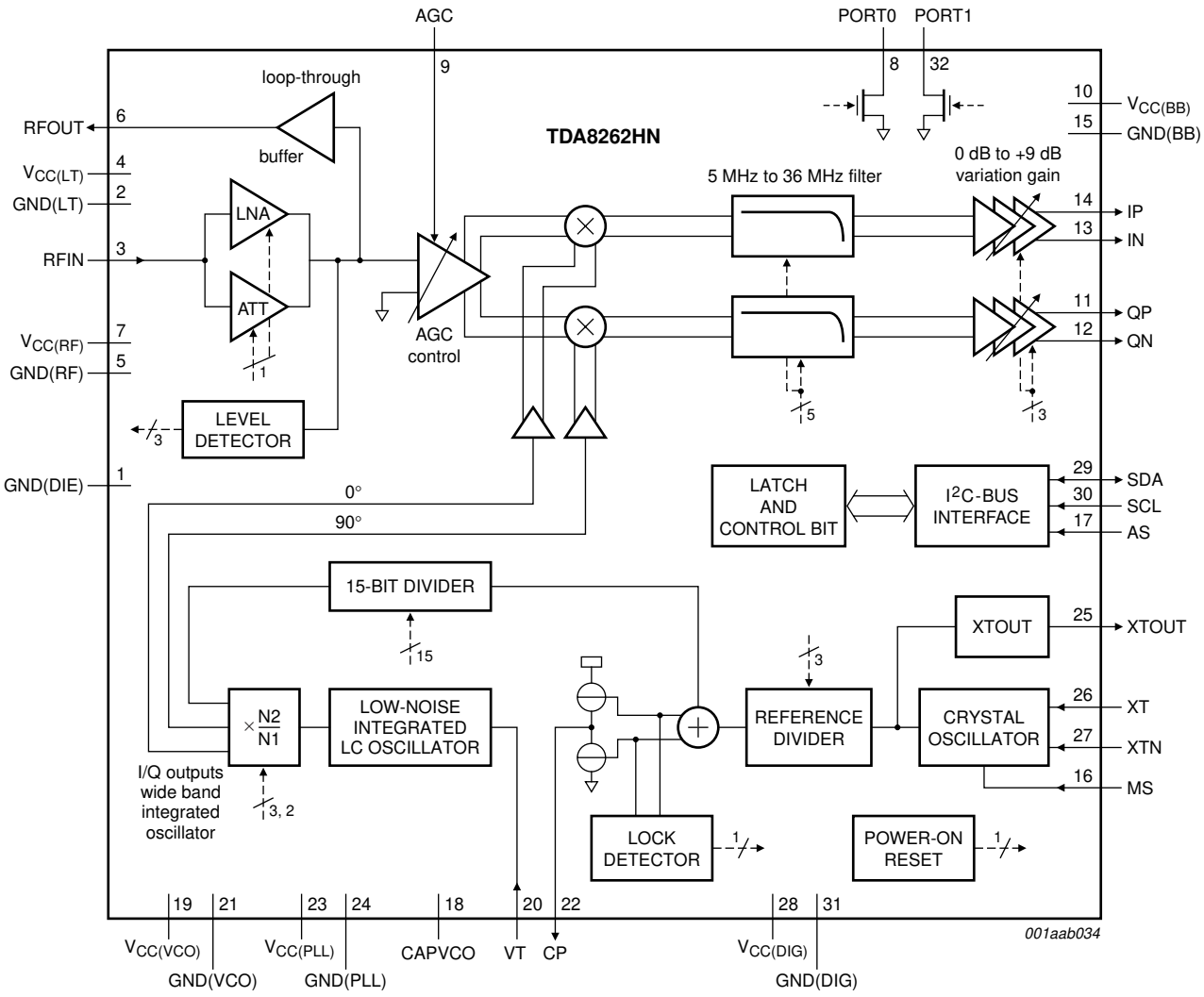


Fig 1. Block diagram

8. Pinning information

8.1 Pinning

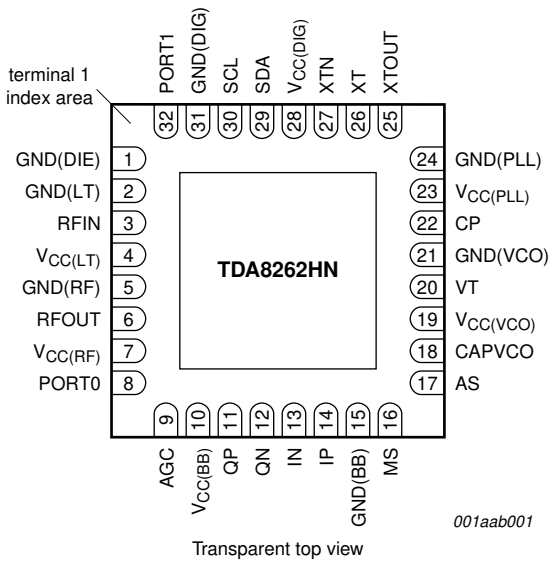


Fig 2. Pin configuration

8.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
GND(DIE)	1	isolation ground
GND(LT)	2	LNA and loop-through ground
RFIN	3	RF input
$V_{CC(LT)}$	4	LNA and loop-through supply voltage
GND(RF)	5	RF ground
RFOUT	6	RF output
$V_{CC(RF)}$	7	RF supply voltage
PORT0	8	pull-down port 0
AGC	9	automatic gain control input
$V_{CC(BB)}$	10	baseband supply voltage
QP	11	Q positive output
QN	12	Q negative output
IN	13	I negative output
IP	14	I positive output
GND(BB)	15	baseband ground
MS	16	master/slave crystal oscillator mode input
AS	17	address select input
CAPVCO	18	internal LC VCO regulation capacitor

Table 3: Pin description *...continued*

Symbol	Pin	Description
$V_{CC(VCO)}$	19	VCO supply voltage
VT	20	VCO tuning voltage input
GND(VCO)	21	VCO ground
CP	22	charge pump output
$V_{CC(PLL)}$	23	PLL supply voltage
GND(PLL)	24	PLL ground
XTOUT	25	16 MHz frequency for external ICs output
XT	26	16 MHz crystal oscillator input
XTN	27	16 MHz crystal oscillator input
$V_{CC(DIG)}$	28	digital supply voltage
SDA	29	I^2C-bus data input/output
SCL	30	I^2C-bus clock input
GND(DIG)	31	digital ground
PORT1	32	pull-down port 1

9. Tuner configuration

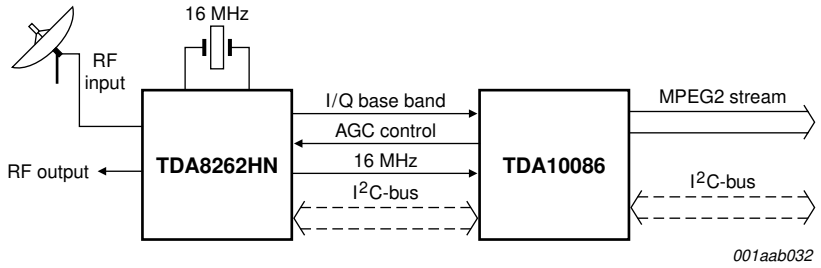


Fig 3. Tuner configuration for one channel

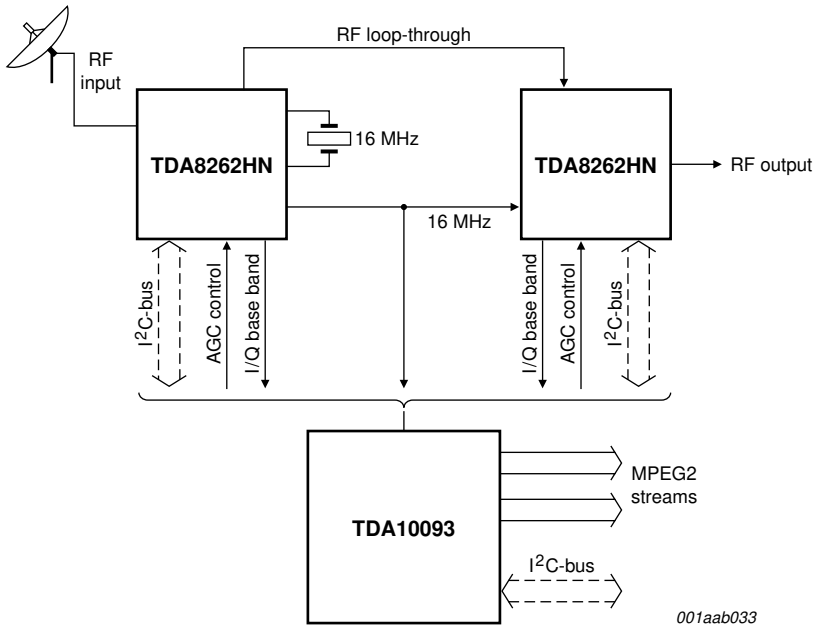


Fig 4. Tuner configuration for two channels (watch and record)

10. Functional description

The TDA8262HN contains the core of the RF analog part of a digital satellite receiver. The signal coming from the LNB is coupled to the RF inputs. The internal circuitry performs the Zero-IF quadrature frequency conversion and two in-phase (IP/IN) and two quadrature (QP/QN) output signals can directly be used to feed a Satellite Demodulator and Decoder circuit (SDD). Low pass filter cut-off frequency can be adjusted from 5 MHz to 36 MHz in 32 steps. This allows a large flexibility in the SDD input. 10 gain values are present at output amplifier to compensate cut-off frequency adjustment and single output application.

The IC gain controlled amplifier before the mixer is controlled by the SDD through pin AGC.

An input level detector gives the wide band RF level. This information is available through I^{2}C-bus in read mode.

The internal loop controls a fully integrated VCO, to cover the range from 950 MHz to 2175 MHz. This VCO provides both in phase and quadrature signals to drive the two mixers.

The output of the 15-bit programmable divider passes through the phase comparator where it is compared in both phase and frequency to the comparison frequency (f_{comp}). This f_{comp} is derived from the signal present at the XT/XTN pins (f_{XTAL}), divided down in the reference divider. The buffered signal on pin XTOUT is able to drive the crystal frequency input of the SDD, which saves a crystal in the application.

The output of the phase comparator drives the charge pump and loop amplifier section. Pin CP is the output of the charge pump, and pin VT drives the tuning voltage to the varicap diode of the voltage controlled oscillator. The loop filter has to be connected between pins CP and VT.

For test and alignment purposes, it is possible to release the tuning voltage output and to apply an external voltage on the VT pin, as well as to select the charge pump sink, source or off.

Three independent area of power-down are available by programming I²C-bus:

- Loop-through part
- RF and synthesizer part
- Crystal oscillator and XTOUT part.

10.1 Gain distribution

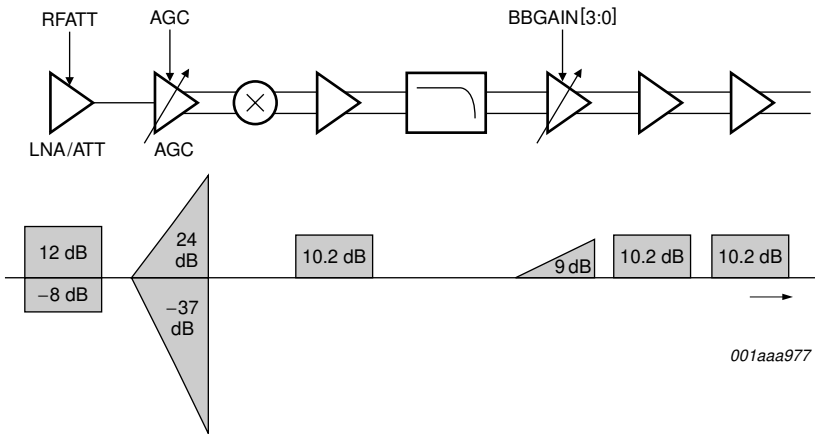


Fig 5. Gain distribution; typical values

11. Programming

The programming of the TDA8262HN is done through the I²C-bus. The READ/WRITE selection is done through the R/W bit (address LSB). The TDA8262 fulfils the fast mode I²C-bus specification, according to the *Philips I²C-bus specification, see document 9398 393 40011.*

11.1 I²C-bus inputs

The I²C-bus lines SCL and SDA can be connected to an I²C-bus system tied to either 3.3 V or 5.0 V, which allows direct connection to most of existing microcontrollers.

Data transfer format should be MSB first, and 8-bit word + acknowledge bit.

Pins used for the I²C-bus:

- Pin SCL is the clock input
- Pin SDA is the data input/output

- Pin AS is for address selection.

11.2 Address selection

Table 4: Address selection (pin AS)

Voltage on pin AS	Write address	Read address
0 V to 0.1 × V_{CC}	C0	C1
0.2 × V_{CC} to 0.3 × V_{CC} or open pin	C2	C3
0.4 × V_{CC} to 0.6 × V_{CC}	C4	C5
0.9 × V_{CC} to V_{CC}	C6	C7

11.3 Master-slave selection

Table 5: Master-slave selection (pin MS)

Voltage on pin MS	Crystal oscillator mode
0 V to 0.1 × V_{CC}	master
0.9 × V_{CC} to V_{CC}	slave

11.4 Data transfer in write mode

The data transfer in write mode use the following pattern:

Table 6: I^2C-bus write mode data transfer pattern

START	address	ack	subaddress	ack	data 1	ack	data 2	ack	data n	ack	STOP

Subaddress is automatically incremented starting from the initial value.

11.5 I^2C-bus table in write mode

Table 7: I^2C-bus write mode map

Subaddress (hex)	MSB							LSB
	7	6	5	4	3	2	1	0
0X	PDPLL	PDZIF	PDLOOPT	PDXTOUT	PDRSSI	PDLNA	PDXTAL	TEST1
1X	R2	R1	R0	D4	D3	D2	D1	D0
2X	N14	N13	N12	N11	N10	N9	N8	N7
3X	N6	N5	N4	N3	N2	N1	N0	CALMANUAL
4X	FC4	FC3	FC2	FC1	FC0	-	-	-
5X	BBGAIN3	BBGAIN2	BBGAIN1	BBGAIN0	-	-	-	RFATT
6X	CPCURSEL	CPTST	FUP	FDN	CP2TST	FPFD2	CPHIGH	-
7X	AMPVCO2	AMPVCO1	AMPVCO0	-	-	-	PORT1	PORT0
8X	CALTIME	-	-	SELVTH1	SELVTH0	SELVTL1	SELVTL0	-
9X	BBIAS3	BBIAS2	BBIAS1	BBIAS0	-	-	-	-

11.6 I²C-bus table in write mode (default at POR)

Table 8: I²C-bus write mode map (default at POR) [1]

Subaddress (hex)	MSB							LSB
	7	6	5	4	3	2	1	0
0X	0	0	0	0	1	0	0	1
1X	0	0	1	0	0	0	0	0
2X	0	0	0	0	0	0	0	1
3X	0	0	0	0	0	0	0	1
4X	0	0	0	0	0	-	-	-
5X	0	0	0	0	-	-	-	0
6X	0	0	X	X	0	X	0	-
7X	1	0	0	-	-	-	0	0
8X	0	-	-	0	0	0	0	-
9X	0	0	0	0	-	-	-	-

[1] X means don't care.

11.7 Bit description I²C-bus write mode

Table 9: Power-down section

Bit	Description	State
PDPLL	power-down of all the synthesizer part	0 = function on; 1 = function off
PDZIF	power-down of all signal decoding part except LNA, RSSI and loop-through	0 = function on; 1 = function off
PDLOOPT	power-down of the loop-through	0 = function on; 1 = function off
PDXTOUT	power-down of the XTOUT output	0 = function on; 1 = function off
PDRSSI	power-down of the input level detector (RSSI)	0 = function on; 1 = function off
PDLNA	power-down of the low noise amplifier	0 = function on; 1 = function off
PDXTAL	power-down of the crystal oscillator	0 = function on; 1 = function off
TEST1	used for test purposes only	must be logic 1

Table 10: Reference divider range; bits R[2:0]

These bits select the ratio between the comparison frequency and the crystal frequency.

R2	R1	R0	Decimal	Comparison frequency
0	0	0	0	2 MHz
0	0	1	1	1 MHz
0	1	0	2	500 kHz
0	1	1	3	250 kHz
1	0	0	4	125 kHz
1	0	1	5	125 kHz
1	1	0	6	125 kHz
1	1	1	7	125 kHz

Table 11: VCO preprogramming range; bits D[4:0]

These bits are also called Dword: It determines the ratio between LO frequency and VCO frequency. The bits are used for the calibration protocol of the internal VCO.

D4	D3	D2	D1	D0	Decimal	Ratio f_{LO} to f_{VCO}
0	0	0	0	0	0	0.27
0	0	0	0	1	1	0.29
0	0	0	1	0	2	0.31
0	0	0	1	1	3	0.33
0	0	1	0	0	4	0.36
0	0	1	0	1	5	0.36
0	0	1	1	0	6	0.38
0	0	1	1	1	7	0.40
0	1	0	0	0	8	0.42
0	1	0	0	1	9	0.43
0	1	0	1	0	10	0.44
0	1	0	1	1	11	0.45
0	1	1	0	0	12	0.46
0	1	1	0	1	13	0.47
0	1	1	1	0	14	0.50
0	1	1	1	1	15	0.54
1	0	0	0	0	16	0.55
1	0	0	0	1	17	0.56
1	0	0	1	0	18	0.58
1	0	0	1	1	19	0.60
1	0	1	0	0	20	0.63
1	0	1	0	1	21	0.64
1	0	1	1	0	22	0.67
1	0	1	1	1	23	0.70
1	1	0	0	0	24	0.75
1	1	0	0	1	25	0.78
1	1	0	1	0	26	0.88
1	1	0	1	1	27	0.88
1	1	1	0	0	28	0.88
1	1	1	0	1	29	0.88
1	1	1	1	0	30	0.88
1	1	1	1	1	31	0.88

Table 12: Main divider range; bits N[14:0]

These bits control the ratio between the LO frequency and the comparison frequency.

N[14:0]	Ratio
Binary value	The ratio N is equal to $N14 \times 2^{14} + N13 \times 2^{13} + ...N1 \times 2^{1} + N0$

Table 13: Selects manual or automatic LC oscillator calibration; bit CALMANUAL

This bit controls the LC VCO frequency programming mode.

CALMANUAL	Action
0	automatic process control; the LC VCO searches the better ratio of the Dword to have the optimum tuning frequency
1	manual process control; the LC VCO is tuned by selecting the programmed Dword

Table 14: RX baseband cut-off frequency control; bits FC[4:0]:

The register selects the cut-off frequency of the RX baseband filter. The cut-off frequency can be set from 5 MHz to 36 MHz in 32 steps of 1 MHz

FC4	FC3	FC2	FC1	FC0	Decimal	Baseband cut-off frequency (MHz) [1]
0	0	0	0	0	0	5
0	0	0	0	1	1	6
0	0	0	1	0	2	7
0	0	0	1	1	3	8
0	0	1	0	0	4	9
0	0	1	0	1	5	10
0	0	1	1	0	6	11
0	0	1	1	1	7	12
0	1	0	0	0	8	13
0	1	0	0	1	9	14
0	1	0	1	0	10	15
0	1	0	1	1	11	16
0	1	1	0	0	12	17
0	1	1	0	1	13	18
0	1	1	1	0	14	19
0	1	1	1	1	15	20
1	0	0	0	0	16	21
1	0	0	0	1	17	22
1	0	0	1	0	18	23
1	0	0	1	1	19	24
1	0	1	0	0	20	25
1	0	1	0	1	21	26
1	0	1	1	0	22	27
1	0	1	1	1	23	28
1	1	0	0	0	24	29
1	1	0	0	1	25	30
1	1	0	1	0	26	31
1	1	0	1	1	27	32
1	1	1	0	0	28	33

Table 14: RX baseband cut-off frequency control; bits FC[4:0]: *…continued*

The register selects the cut-off frequency of the RX baseband filter. The cut-off frequency can be set from 5 MHz to 36 MHz in 32 steps of 1 MHz

FC4	FC3	FC2	FC1	FC0	Decimal	Baseband cut-off frequency (MHz) [1]
1	1	1	0	1	29	34
1	1	1	1	0	30	35
1	1	1	1	1	31	36

[1] Typical values at nominal process and room temperature.

Table 15: RX baseband gain control; bits BBGAIN[3:0]

These bits control the additional gain of the baseband between 0 dB and 9dB

BBGAIN3	BBGAIN2	BBGAIN1	BBGAIN0	Decimal	Additional gain in dB [1]
0	0	0	0	0	0
0	0	0	1	1	0
0	0	1	0	2	0
0	0	1	1	3	0
0	1	0	0	4	0
0	1	0	1	5	1.6
0	1	1	0	6	3
0	1	1	1	7	4.6
1	0	0	0	8	6.3
1	0	0	1	9	7.3
1	0	1	0	10	8.2
1	0	1	1	11	8.5
1	1	0	0	12	8.8
1	1	0	1	13	8.8
1	1	1	0	14	9
1	1	1	1	15	9

[1] Typical values at nominal process and room temperature.

Table 16: 20 dB RF attenuation control; bit RFATT

This bit controls the RF attenuation inside the LNA amplifier.

RFATT	Action
0	normal gain of RF path
1	20 dB attenuation. When active, the LNA works in attenuation (–8 dB gain). The loop-through signal is also attenuated by 20 dB.

Table 17: Select main loop charge-pump current; bit CPCURSEL

CPCURSEL	Action
0	low charge-pump current
1	high charge-pump current

Table 18: Main loop charge pump test; bits CPTST, FUP and FDN

These bits force the inputs of the main loop charge pump. Thus the current and leakage measurement could be done. This test could be used also to force the LC VCO at its maximum or minimum tuning voltage.

CPTST	FUP	FDN	Actions
0	X	X	test disable
1	0	0	sink and source off; leakage measurement
1	0	1	sink off and source on; source measurement
1	1	0	sink on and source off; sink measurement
1	1	1	sink on and source on

Table 19: Second loop charge pump test; bits CP2TST and FPFD2

These bits force the inputs of the second loop charge pump. This test could be used to force the LO VCO at its maximum or minimum tuning voltage.

CP2TST	FPFD2	Actions
0	X	test disable
1	0	sink on and source off; LO VCO maximum frequency measurement
1	1	sink off and source on; LO VCO minimum frequency measurement

Table 20: Select main loop charge-pump current; bit CPHIGH

CPHIGH	Action
0	first charge pump active (low currents)
1	second charge pump active (high currents)

Table 21: Amplitude of the internal VCO; bits AMPVCO[2:0]

These bits control the amplitude of the internal LC VCO.

AMPVCO[2:0]	Value
Binary value	The allowed value is AMPVCO[2:0] = 100 (decimal 4). The product is specified only with this value, other settings may lead to different performance.

Table 22: Control port output; bits PORT[1:0]

Bit PORT1 controls the use of PORT1 and bit PORT0 controls the use of PORT0. Outputs PORTn are realized with open-drain NMOS transistors.

PORTn	Action
0	PORTn at high-impedance
1	PORTn in sink mode; minimum 9 mA drive capability

Table 23: Calibration wait time control; bit CALTIME

This bit controls the duration of the wait time of the calibration. This time is used to wait PLL locking after programming a Dword. The reference clock of the time is the comparison frequency of the PLL

CALTIME	f_c divider ratio	Wait time for f_{comp} = 1 MHz (ms)
0	28673	28.673
1	32769	32.769

Table 24: Maximum voltage tuning threshold for calibration control; bits SELVTH[1:0]

These bits control the voltage threshold for the ACUP comparator. The ACUP and ACDN comparators sense the LC VCO tuning voltage at pin VT.

SELVTH1	SELVTH0	Decimal	Threshold VTH (V) [1] [2]
0	0	0	1.8
0	1	1	1.9
1	0	2	2.0
1	1	3	2.1

[1] Typical values at nominal process and room temperature.

[2] The recommended value is SELVTH[1:0] = 11 (decimal 3).

Table 25: Minimum voltage tuning threshold for calibration control; bits SELVTL[1:0]

These bits control the voltage threshold for the ACDN comparator. The ACUP and ACDN comparators sense the LC VCO tuning voltage at pin VT.

SELVTL1	SELVTL0	Decimal	Threshold VTL (V) [1] [2]
0	0	0	0.6
0	1	1	0.5
1	0	2	0.4
1	1	3	0.3

[1] Typical values at nominal process and room temperature.

[2] The recommended value is SELVTL[1:0] = 01 (decimal 1).

Table 26: Baseband bias current control; bits BBIAS[3:0]

This register modifies the baseband bias current through different parts: Output buffer or other amplifier.

BBIAS[3:0]	Value
Binary value	The allowed value is BBIAS[3:0] = 1101 (decimal 13). The product is specified only with this value, other settings may lead to different performance.

11.8 Data transfer in read mode

The data transfer in read mode use the following pattern.

Table 27: I^2C-bus read mode data transfer pattern

START	address	ack	data 1	ack	data 2	ack	STOP

11.9 I^2C-bus table in read mode

Table 28: I^2C-bus read mode map [1]

Byte	MSB							LSB
	7	6	5	4	3	2	1	0
0	POR	LOCK	ACUP	ACDN	ERRORCAL	X	X	X
1	1	INLEVEL1	INLEVEL0	DW4	DW3	DW2	DW1	DW0

[1] X can be 1 or 0 and needs to be masked in the microcontrollers' software; MSB is transmitted first.

11.10 Bit description I²C-bus read mode

Table 29: Power-on reset; bit POR

POR	Action
0	Normal operation
1	This bit is set to logic 1 at the $V_{CC(DIG)}$ power supply ramp-up. It is reset to logic 0 after the first read of the IC. When $V_{CC(DIG)}$ falls below 2 V typical, this bit is set to logic 1. This is to prevent loss in internal I²C-bus registers programming.

Table 30: Synthesizer lock indicator; bit LOCK

LOCK	Action
0	synthesizer is not locked
1	synthesizer is locked

Table 31: Auto calibration up threshold control; bit ACUP

ACUP	Action
0	LC VCO tuning voltage is lower than VTH (see Table 24)
1	LC VCO tuning voltage is higher than VTH (see Table 24)

Table 32: Auto calibration down threshold control; bit ACDN

ACDN	Action
0	LC VCO tuning voltage is higher than VTL (see Table 25)
1	LC VCO tuning voltage is lower than VTL (see Table 25)

Table 33: Calibration defect detection; bit ERRORCAL

ERRORCAL	Action
0	no defect detected
1	calibration unit control tries to go lower than the minimum or higher than the maximum Dword ratio

Table 34: RF input level indicator; bits INLEVEL[1:0]

This register gives the RF input level in dBm

INLEVEL1	INLEVEL0	Decimal	RF power (dBm) [1]
0	0	0	< −30
0	1	1	−30 to −20
1	0	2	−20 to −15
1	1	3	> −15

[1] Typical values at nominal process and room temperature. Values are valid only when LNA path is selected (bit RFATT = 0).

Table 35: Internal Dword register; bits DW[4:0]

This register gives the internal Dword value. This value could be the programmed D[4:0] value in manual mode or the calculated value after LC VCO calibration in automatic mode.

DW[4:0]	Description
Binary value	The f_{LO} to f_{VCO} ratio is the same as shown in Table 11

12. Internal circuitry

Table 36: Internal circuitry

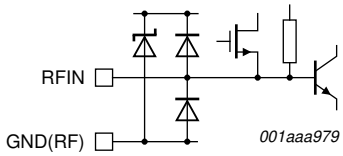
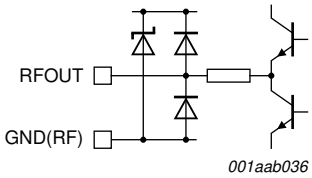
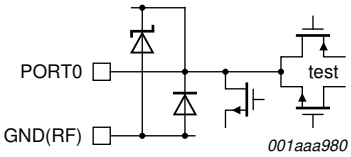
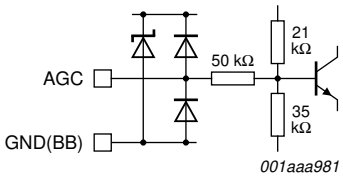
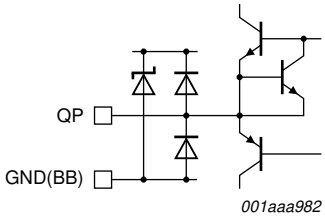
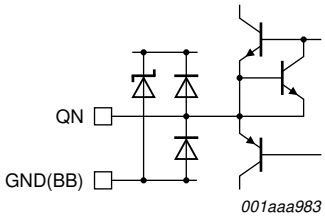
Symbol	Pin	Equivalent circuit
RFIN	3	
RFOUT	6	
PORT0	8	
AGC	9	
QP	11	
QN	12	

Table 36: Internal circuitry *…continued*

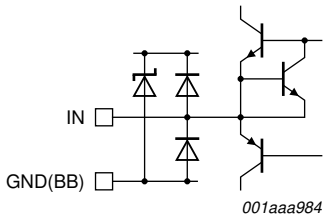
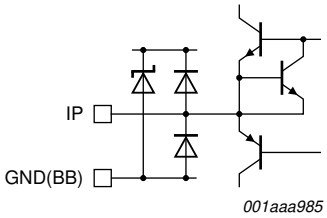
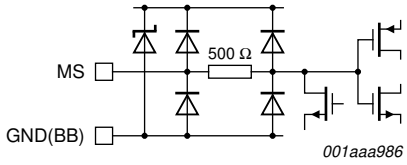
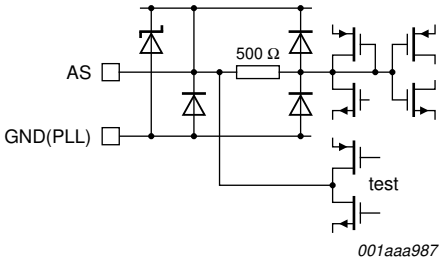
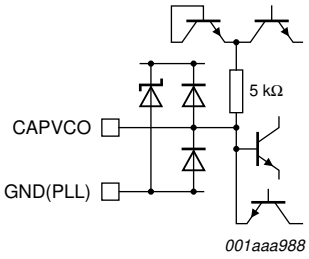
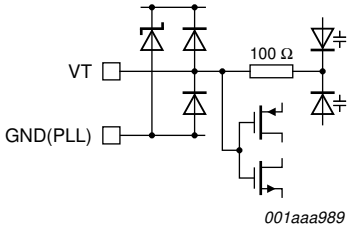
Symbol	Pin	Equivalent circuit
IN	13	
IP	14	
MS	16	
AS	17	
CAPVCO	18	
VT	20	

Table 36: Internal circuitry *…continued*

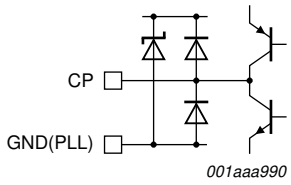
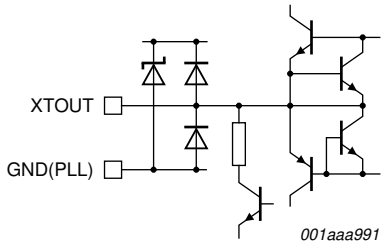
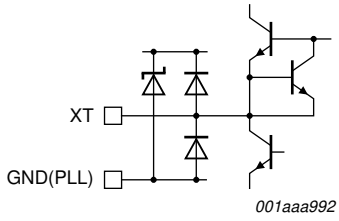
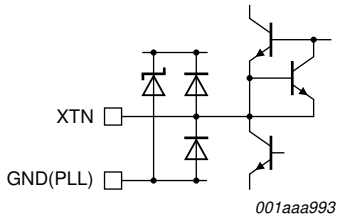
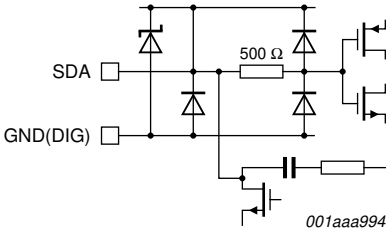
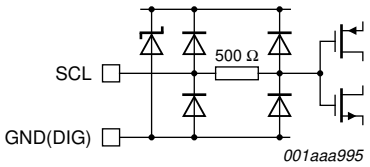
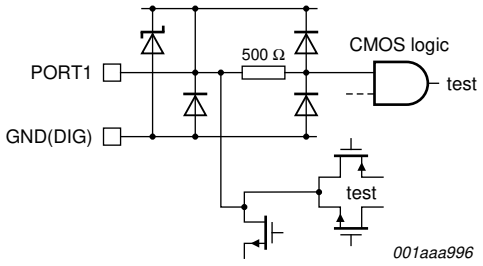
Symbol	Pin	Equivalent circuit
CP	22	
XTOUT	25	
XT	26	
XTN	27	
SDA	29	
SCL	30	

Table 36: Internal circuitry *...continued*

Symbol	Pin	Equivalent circuit
PORT1	32	

13. Limiting values

Table 37: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). [1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+3.6	V
V_I	input voltage	pins SDA, SCL, PORT1 and PORT0		–0.3	+5.5	V
		pin RFIN		–0.3	V_{CC} – 0.3	V
		all other pins				
		V_{CC} < 3.3 V		–0.3	V_{CC} + 0.3	V
		V_{CC} ≥ 3.3 V		–0.3	+3.6	V
T_{amb}	ambient temperature			–20	+85	°C
T_{stg}	storage temperature			–40	+125	°C
T_j	junction temperature			-	125	°C
t_{sc}	short circuit time		[2]	-	10	s
V_{esd}	electrostatic discharge voltage	human body model				
		pin PORT0 (pin 8)		-	±1000	V
		all other pins	[3]	-	±2000	V
		machine model	[4]	-	±200	V

[1] Maximum ratings cannot be exceeded, not even momentarily without causing irreversible damages to the IC. Maximum ratings cannot be accumulated.

[2] Each pin to V_{CC} or GND; except RFIN pin which should never exceed V_{CC} – 0.3 V.

[3] Test in accordance with *JEDEC specification EIA/JESD22-114B*.

[4] Test in accordance with *JEDEC specification EIA/JESD22-A115-A*.

14. Thermal characteristics

Table 38: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance junction to ambient	JEDEC 4 layer test board with 9 thermal vias (exposed die pad soldered on board)	43	K/W

15. Characteristics

Table 39: Characteristics

T_{amb} = 25 °C; V_{CC} = 3.3 V; output level on differential I/Q output is 550 mV (p-p); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage			3.15	3.3	3.45	V
I_{CC}	supply current	all power-down bits are 0		-	175	-	mA
		all power-down bits are 1		-	6	-	mA
		only bits PDXTOUT and PDXTAL are 0		-	30	-	mA
		only bits PDLNA and PDLOOPT are 0		-	45	-	mA
V_{POR}	voltage limit when POR is active			1.5	-	2.5	V
RF and Baseband							
$LO_{L(RFIN)}$	LO leakage through RF inputs	between 950 MHz and 2175 MHz		-	–85	-	dBm
Z_i	input impedance			-	75	-	Ω
$Z_{o(l-t)i}$	loop-through output impedance			-	75	-	Ω
$Z_{L(I/Q)(max)}$	maximum load on each IP, IN, QP and QN output	single mode		-	10	-	pF
				-	1	-	kΩ
G_{LT}	LNA to loop-through gain	LNA configuration		–2	-	2	dB
		attenuated configuration		-	–18	-	dB
$LO_{L(RFOUT)}$	LO leakage on pin RFOUT	between 950 MHz and 2175 MHz		-	–85	-	dBm
$RF_{isolation}$	isolation between loop-through and RF input			-	30	-	dB
$V_{O(I/Q)}$	DC voltage on I/Q output			-	1.65	-	V
$\Delta G_{v(BB)(min)}$	minimum baseband additional gain	BBGAIN [3:0] = 0h		-	0	-	dB
$\Delta G_{v(BB)(max)}$	maximum baseband additional gain	BBGAIN [3:0] = Fh		-	9	-	dB
$V_{o(I/Q)(p-p)}$	typical AC output voltage on differential I/Q output; peak-to-peak value	differential voltage		-	550	-	mV
$V_{o(I/Q)(rms)}$	recommended I and Q output voltage RMS value (QPSK signals)		[1]	-	200	-	mV
IIP_2	second-order interception point at RF input	f_i = 2150 MHz; P_{RFIN} = –20 dBm	[2]	-	2	-	dBm
IIP_3	third-order interception point at RF input	P_{RFIN} = –20 dBm	[3]				
		f_i = 2150 MHz		-	6	-	dBm
		f_i = 950 MHz		-	0	-	dBm
F	noise figure	maximum gain; V_{AGC} = 3 V		-	7.7	8.5	dB
$G_{v(I-Q)(M)}$	voltage gain mismatch between I and Q	measured at 10 MHz; f_{LPF} = 36 MHz		-	-	1	dB
$G_{v(I/Q)(R)}$	voltage gain ripple for I or Q	f_{LPF} = 36 MHz; 22.5 MHz band		-	-	2	dB
$\Delta\Phi$	absolute quadrature error	measured at 10 MHz; f_{LPF} = 36 MHz		0	-	5	degree
$t_{d(g)(I-Q)}$	group delay mismatch in between I and Q	f_{LPF} = 36 MHz; 22.5 MHz band		-	0	-	ns

Table 39: Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; output level on differential I/Q output is 550 mV (p-p); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{d(g)(I/Q)(R)}$	group delay ripple for I or Q	f_{LPF} = 36 MHz; 22.5 MHz band		-	5	-	ns
$\alpha_{60(I/Q)}$	rejection at 60 MHz for I and Q	f_{LPF} = 36 MHz		-	30	-	dB
$f_{LPF(min)}$	minimum filter cut-off frequency	FC [4:0] = 00h		-	5	-	MHz
$f_{LPF(max)}$	maximum filter cut-off frequency	FC [4:0] = 1Fh		-	36	-	MHz
Voltage gain from RF input to IP, IN, QP and QN outputs; differential output; f_{LPF} = 36 MHz; BBGAIN[3:0] = 0h.							
$G_{v(LNA)(min)}$	minimum voltage gain for LNA configuration	V_{AGC} = 0.3 V		-	6	-	dB
$G_{v(LNA)(max)}$	maximum voltage gain for LNA configuration	V_{AGC} = 3 V		-	67	-	dB
$G_{v(a)(min)}$	minimum voltage gain for attenuated configuration	V_{AGC} = 0.3 V		-	–14	-	dB
$G_{v(a)(max)}$	maximum voltage gain for attenuated configuration	V_{AGC} = 3 V		-	47	-	dB
AGC	amplifier gain control range			55	60	-	dB
VCO and synthesizer							
VCO							
f_{osc}	oscillator frequency range			950	-	2175	MHz
ΦN_{osc}	oscillator phase noise in the satellite band	100 kHz offset, out of the PLL bandwidth	[4]	-	–100	–94	dBc/Hz
SNF_{SB}	synthesizer noise floor in the satellite band	1 kHz and 10 kHz offset; f_{comp} = 1 MHz	[4]	-	-	–78	dBc/Hz
MDR	main divider ratio			128	-	32767	
Crystal oscillator and XTOUT							
Z_{osc}	crystal oscillator negative impedance	absolute value		500	-	-	Ω
f_{XTAL}	crystal frequency			16	16	16	MHz
Z_{XTAL}	recommended crystal series resistance			-	-	150	Ω
$V_{o(p-p)}$	output voltage (peak-to-peak value)	crystal oscillator output		550	750	-	mV
MS input							
I_h	high level input current	$V_{MS} = V_{CC}$		–50	-	+50	µA
I_l	low level input current	V_{MS} = 0 V		–50	-	+50	µA
Charge pump and tuning voltage							
I_L	charge pump leakage current			–10	0	+10	nA
$I_{l(min)}$	charge pump low; min current	CPHIGH = 0 and CPCURSEL = 0		0.67	0.9	1.13	mA
$I_{l(max)}$	charge pump low; max current	CPHIGH = 0 and CPCURSEL = 1		0.97	1.3	1.63	mA
$I_{h(min)}$	charge pump high, min current	CPHIGH = 1 and CPCURSEL = 0		1.27	1.7	2.13	mA
$I_{h(max)}$	charge pump high, max current	CPHIGH = 1 and CPCURSEL = 1		1.87	2.5	3.13	mA
I^2C-bus and PORTn							
SDA/SCL input							
V_{IL}	LOW-level input voltage	5 V and 3.3 V bus		-	-	0.99	V
V_{IH}	HIGH-level input voltage	5 V and 3.3 V bus		2.3	-	-	V

Table 39: Characteristics *...continued*

T_{amb} = 25 °C; V_{CC} = 3.3 V; output level on differential I/Q output is 550 mV (p-p); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{HI}	HIGH-level leakage current	V_{IH} = 3.3 V; V_{CC} = 0 V or 3.3 V	-	-	10	µA
I_{LI}	LOW-level leakage current	V_{IL} = 0 V; V_{CC} = 3.3 V	−10	-	-	µA
f_{SCL}	input clock frequency		-	-	400	kHz
SDA output						
V_O	output voltage during acknowledge	I_{sink} = 3 mA	-	-	0.4	V
AS input						
I_{ASh}	high level input current	$V_{AS} = V_{CC}$	−100	-	+100	µA
I_{ASl}	low level input current	V_{AS} = 0 V	−100	-	+100	µA
PORTn						
V_O	PORTn maximum output voltage	I_{sink} = 9 mA	-	-	0.4	V

[1] The product is qualified with an output voltage of 550 mV (p-p) differential, however larger values can be used at baseband outputs that might have impact on the product performance.

[2] $IIP_2 = -20 + (P1 - P2)$ [dBm].

Wanted signal: RF1 is 2140 MHz, P_{RFIN} = −20 dBm, and the AGC adjusted to get 550 mV (p-p) on the differential output. The output level is P1.

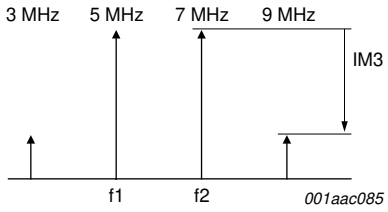
Unwanted signal: RF1 is 1040 MHz and P_{RFIN} = −20 dBm and RF2 is 1100 MHz and P_{RFIN} = −20 dBm. The output level of (RF1 + RF2) on the output pins is P2.

[3] $IIP_3 = -23 + \frac{IM3}{2}$ [dBm], see Figure 6

Wanted signal: RF1 is LO + 5 MHz, P_{RFIN} = −20 dBm, and the AGC adjusted to get 550 mV (p-p) on the differential output.

Unwanted signal: RF1 is LO + 5 MHz and P_{RFIN} = −23 dBm and RF2 is LO + 7 MHz and Pin = −23 dBm

[4] Phase noise in optimal conditions, see related application note.



IM3 is the difference between the wanted signal and the unwanted signal (2f1 − f2) and (2f2 − f1) on output pins

Fig 6. Base band spectrum

16. Application information

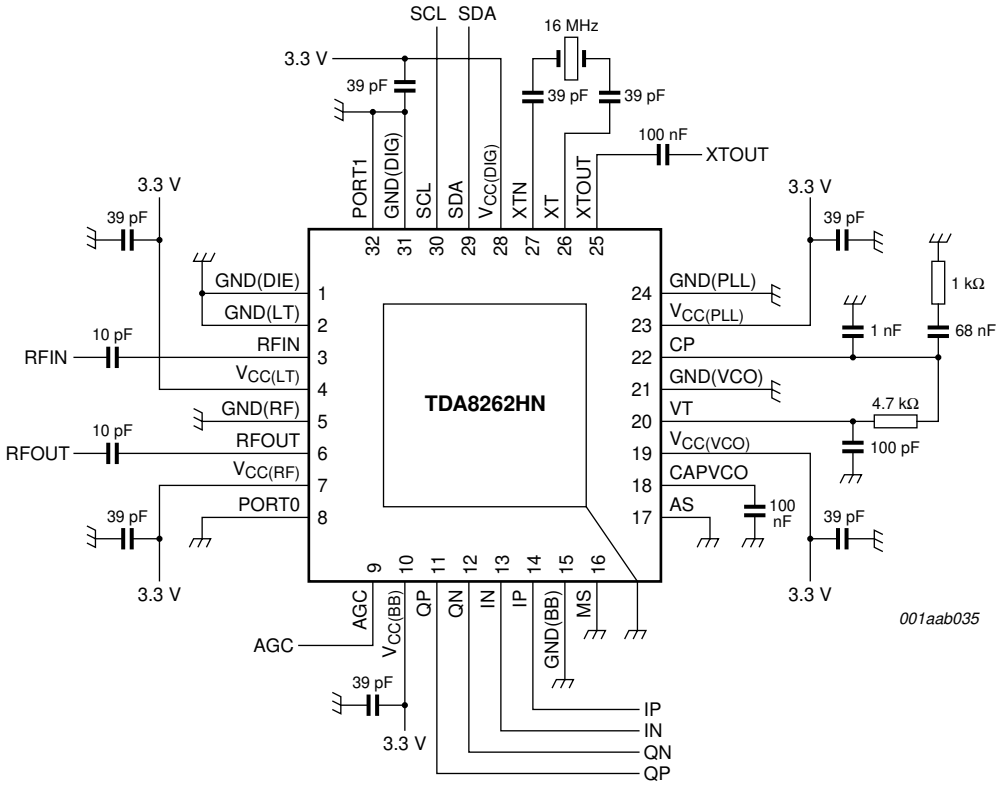
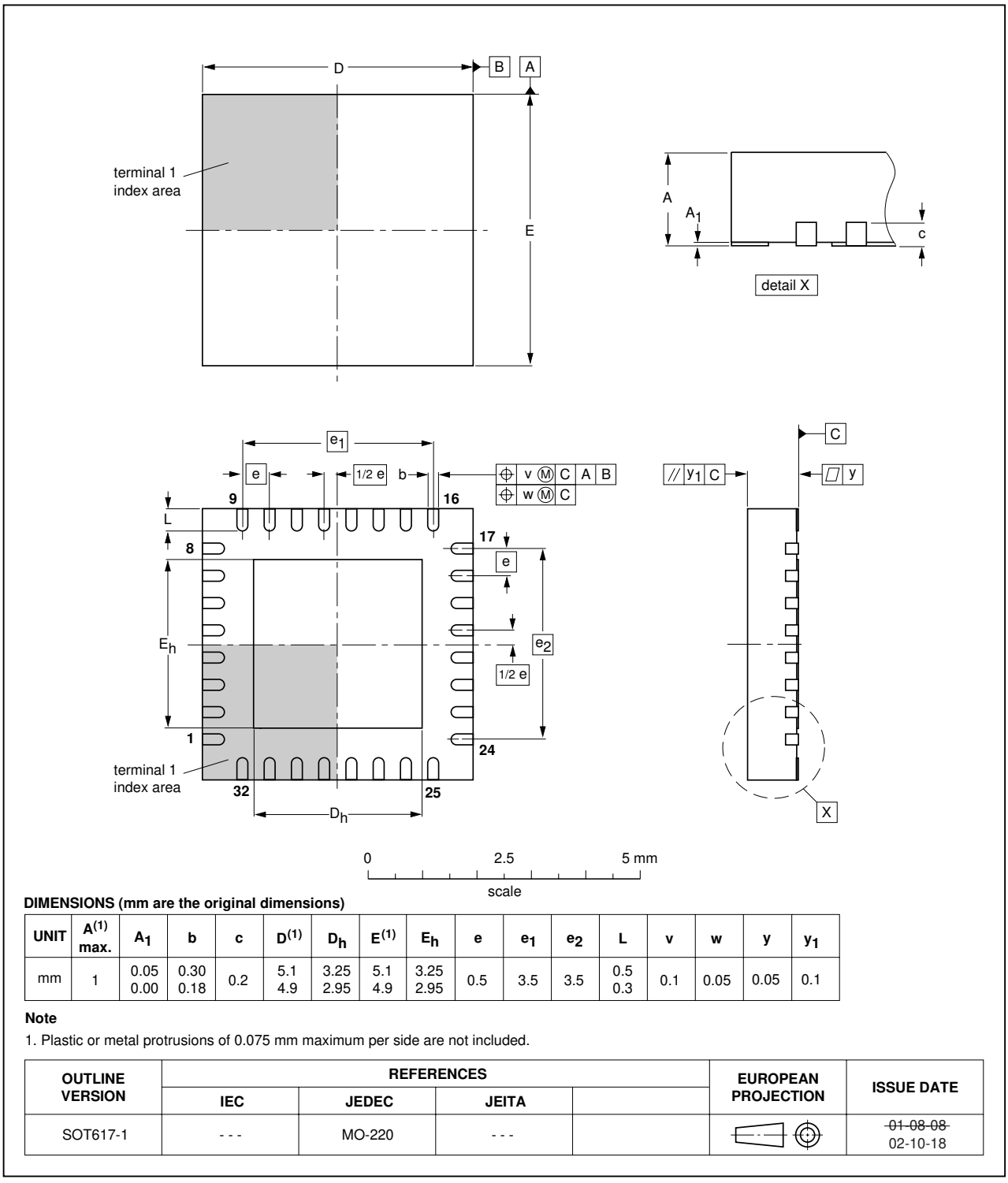


Fig 7. Typical application circuit

17. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 8. Package outline SOT617-1 (HVQFN32)