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TDA8295

Digital global standard low IF demodulator for analog TV and FM radio

Rev. 01 — 4 February 2008 Product data sheet

1. General description

The TDA8295 is an alignment-free digital multistandard vision and sound low IF signal PLL demodulator for positive and negative video modulation including AM and FM mono sound processing. It can be used in all countries worldwide for M/N, B/G/H, I, D/K, L and L-accent standard. CVBS and SSIF/mono audio is provided via two DACs. FM radio preprocessing is included for simple interfacing with demodulator/stereo decoder backends.

The IC is especially suited for the application with the NXP Silicon Tuner TDA8275A or TDA1827x.

All the processing is done in the digital domain.

The chip has an 'easy programming' mode to make the I²C-bus protocol very simple. In principle, only one bit sets the proper standard with recommended content. However, if this is not suitable, free programming is always possible.

2. Features

- Digital IF demodulation for all analog TV standards worldwide (M/N, B/G/H, D/K, I, L and L-accent standard)
- Multistandard true synchronous demodulation with active carrier regeneration
- Alignment-free
- 16 MHz typical reference frequency input (from low IF tuner) or operating as crystal oscillator
- Internal PLL synthesizer which allows the use of a low-cost crystal (typically 16 MHz)
- Especially suited for the NXP Silicon Tuner TDA8275A or TDA1827x
- No SAW filter needed
- Low application effort and external component count in combination with the TDA8275A or TDA1827x
- Pin compatible with predecessor TDA8290
- Simple upgrade of TDA8290 possible
- 12-bit IF ADC on chip running with 54 MHz or 27 MHz
- Two 10-bit DACs on chip for CVBS and SSIF or audio
- Easy programming for I²C-bus
- High flexibility due to various I²C-bus programming registers
- I²C-bus interface and I²C-bus feed-through for tuner programming
- Four I²C-bus addresses selectable via two external pins

- Gated IF AGC acting on black level by using H/V PLL or peak IF AGC (I^2C-bus selectable)
- Internal digital logarithmic IF AGC amplifier with up to 48 dB gain and 68 dB control range
- Peak search tuner IF AGC for optimal adaptive drive of the IF ADC
- Switchable IF PLL and IF AGC loop bandwidths
- Precise AFC and lock detector
- Accurate group delay equalization for all standards
- Very robust IF demodulator coping with adverse field conditions
- Wide PLL pull-in range up to ±1660 kHz (I^2C-bus selectable)
- CVBS and SSIF or audio output with simple postfilter (capacitor only)
- CVBS gain levelling stage to provide nearly constant signal amplitude during overmodulation
- Video equalizer with eight settings
- Nyquist filter in video baseband
- Excellent video S/N (typically 62 dB weighted)
- High selectivity video low-pass filter for all standards
- Low video into sound crosstalk
- Sound performance comparable to QSS single reference concepts
- AM/FM mono sound demodulator
- Switchable de-emphasis
- Excellent FM sound
- Good AM sound
- High FM Deviation mode for China
- Preprocessing of FM radio (mono and stereo) with highly selective digital band-pass filter
- No ceramic filter or external components needed for FM radio
- FM radio available in mono
- Automatic or forced mute for mono sound
- Automatic or forced blank for video
- Mostly digital FIR filter implementation (NSC notches and video low-pass filters)
- Three GPIO pins
- Low total power dissipation (typically 324 mW)
- Standby mode (typically 7 mW)
- 40-pin HVQFN package
- CMOS technology (0.12 µm 1.2 V and 3.3 V)

3. Applications

- PC TV applications
- DVD recorders

4. Quick reference data

Table 1. Quick reference data

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
$V_{DD(1V2)}$	supply voltage (1.2 V)	digital and analog		1.08	1.2	1.32	V
$V_{DD(3V3)}$	supply voltage (3.3 V)	digital and analog		2.97	3.3	3.63	V
$I_{DD(tot)(1V2)}$	total supply current (1.2 V)			-	28	33	mA
$I_{DD(tot)(3V3)}$	total supply current (3.3 V)		[1]	-	125	136	mA
P_{tot}	total power dissipation	default settings; 75 Ω drive; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 1 kΩ	[1]	-	434	490	mW
		Power-save mode; f_s = 54 MHz at ADC; including DAC loads; R_{RSET} = 2 kΩ; see Section 13.6	[2]	-	324	369	mW
		Standby mode		-	7	10	mW
IF input							
$V_{i(p-p)}$	peak-to-peak input voltage	for full-scale ADC input (0 dBFS)		1.8	2.0	2.2	V
V_i	input voltage	operational input related to ADC full scale; all standards; sum of all signals		–3	–3	–3	dBFS
f_i	input frequency	PC / SC1					
		M/N standard		-	5.75 / 1.25	-	MHz
		B standard		-	6.75 / 1.25	-	MHz
		G/H standard		-	7.75 / 2.25	-	MHz
		I standard		-	7.75 / 1.75	-	MHz
		DK and L standard		-	7.75 / 1.25	-	MHz
		L-accent standard		-	1.25 / 7.75	-	MHz
		FM radio		-	1.25	-	MHz
Carrier recovery FPLL							
$B_{-3dB(cl)}$	closed-loop –3 dB bandwidth	wide		60	60	60	kHz
Δf_{pullin}	pull-in frequency range		[3]	±830	±830	±830	kHz
$m_{over(PC)}$	picture carrier overmodulation index	black for L/L-accent standard; flat field white else		115	117	-	%
IF demodulation (video equalizer in Flat mode)							
$\alpha_{sup(stpb)}$	stop-band suppression	video low-pass filter (M/N, B/G/H, I, D/K, L/L-accent standard)		-	–60	-	dB
$t_{ripple(GDE)}$	group delay equalizer ripple time	peak value for B/G/H half, D/K half, I flat, M (FCC) full, L/L-accent full standard		-	20	40	ns

Table 1. Quick reference data *...continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CVBS output						
$V_{o(p-p)}$	peak-to-peak output voltage	negative PC modulation (all standards except L/L-accent); 75 Ω DC load; sync-white modulation				
		90 % (nominal)	0.8	1.0	1.2	V
		positive PC modulation (L/L-accent standard); 75 Ω DC load; sync-white modulation				
		97 % (nominal)	0.8	1.0	1.2	V
$B_{video(-3dB)}$	−3 dB video bandwidth	overall video response; CVBS equalizer flat				
		all standards except M/N	4.8	4.85	-	MHz
		M/N standard	3.9	4.05	-	MHz
$\alpha_{resp(f)}$	frequency response	video equalizer; 8 equally spaced settings; value at 3.9 MHz	−5	-	+4.5	dB
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	-	1.5	3	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*	-	1.5	3	deg
$(S/N)_w$	weighted signal-to-noise ratio	all standards; unified weighting filter (*"ITU-T J.61"*); PC at −6 dBFS	58	62	-	dB
SSIF/mono sound output						
$V_{o(SSIF)(RMS)}$	RMS SSIF output voltage	1 kΩ DC or AC load; no modulation; PC / SC1 = 13 dB; scaled linearly for all other ratios				
		all standards except B/G/H	30	35	40	mV
		B/G/H standard	27	32	37	mV
		FM radio (single carrier)	460	530	610	mV
$V_{o(AF)(RMS)}$	RMS AF output voltage	1 kΩ DC or AC load				
		M standard; 54 % modulation degree (±13.5 kHz FM deviation before pre-emphasis)	125	143	165	mV
		B, G/H, I, D, K standard; 54 % modulation degree (±27 kHz FM deviation before pre-emphasis)	125	143	165	mV
$\alpha_{hr(AF)}$	AF headroom	before clipping; 1 kΩ DC or AC load				
		M standard; related to ±25 kHz peak deviation before pre-emphasis	7	7	7	dB
		B, G/H, I, D, K standard; related to ±50 kHz peak deviation before pre-emphasis	7	7	7	dB
THD	total harmonic distortion	FM; for 50 kHz deviation before pre-emphasis (25 kHz for M standard)	-	0.1	0.2	%
		AM; m = 80 %	-	0.6	1	%

Table 1. Quick reference data *...continued*

Power supplies 3.3 V, 1.2 V; T_{amb} = 25 °C; PC / SC1 for L and M = 10 dB, all others 13 dB; residual picture carrier for L = 3 %, all others 10 %; FM/AM modulation = 54 %, 1 kHz modulation frequency; measured in application PCB (see Figure 12) with 16 MHz crystal frequency, loaded with 75 Ω (CVBS) and 1 kΩ (SSIF/audio). Values are meant for 'easy programming' settings (recommended) except internal mono audio and IF demodulation. The low IF spectrum is delivered by a professional downconverter.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$B_{AF(-3dB)}$	–3 dB AF bandwidth	AM	20	27	-	kHz
		FM	40	50	-	kHz
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	via internal mono sound demodulator; *"ITU-R BS.468-4"*; FM mode related to 27 kHz deviation before pre-emphasis; 10 % residual PC; SC1				
		color bar picture	54	58	-	dB
		via internal mono sound demodulator; *"ITU-R BS.468-4"*; AM; m = 54 %; 3 % residual PC; SC1				
		color bar picture	43	46	-	dB

[1] 50 % ADC current; 100 % video DAC current; 50 % sound DAC current.

[2] 50 % ADC current; 50 % video DAC current; 25 % sound DAC current.

[3] The pull-in range can be doubled to ±1660 kHz by I²C-bus register like described in Table 16. Then the AFC read-out has 256 steps.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8295HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

6. Functional diagram

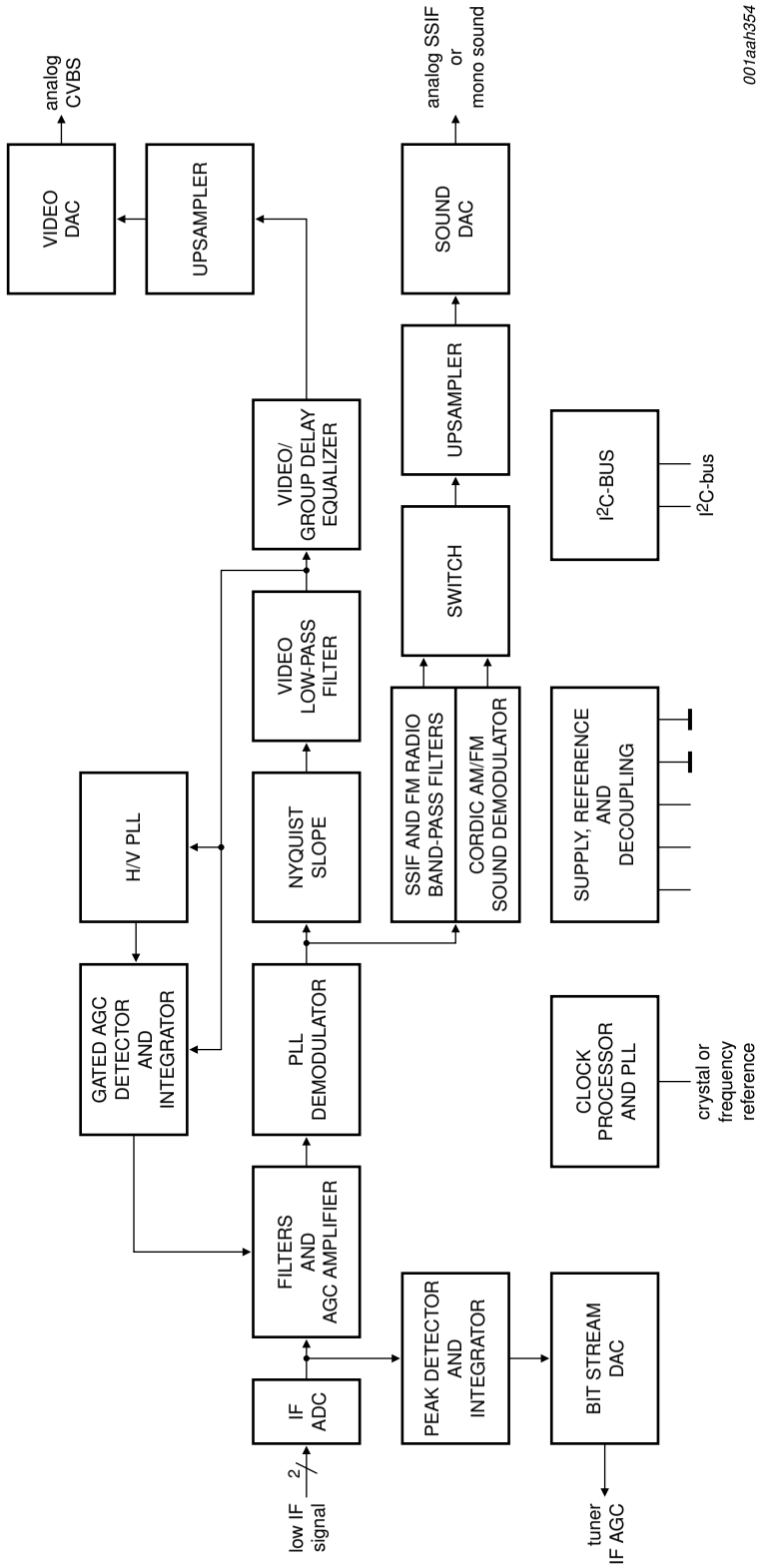

Fig 1. Functional diagram of TDA8295

7. Pinning information

7.1 Pinning

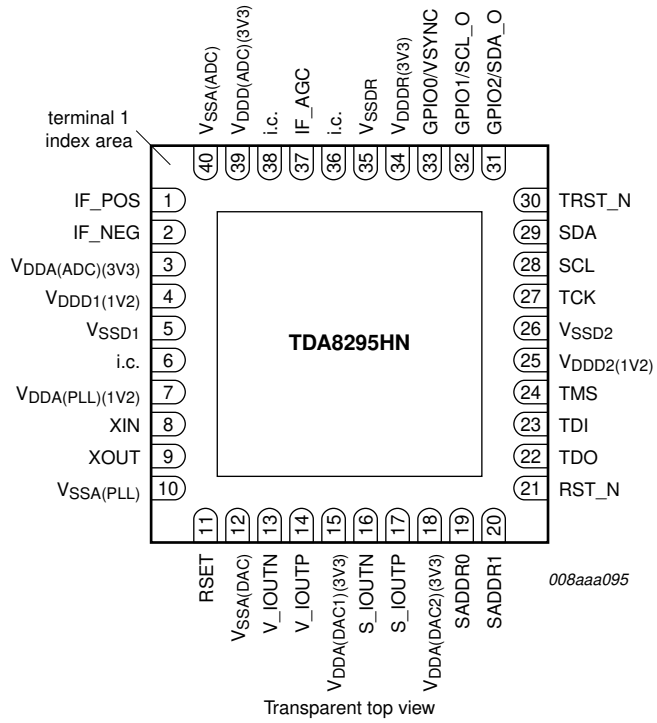

Fig 2. Pin configuration for HVQFN40

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol
1	IF_POS	2	IF_NEG
3	$V_{DDA(ADC)(3V3)}$	4	$V_{DDD1(1V2)}$
5	V_{SSD1}	6	i.c.
7	$V_{DDA(PLL)(1V2)}$	8	XIN
9	XOUT	10	$V_{SSA(PLL)}$
11	RSET	12	$V_{SSA(DAC)}$
13	V_IOUTN	14	V_IOUTP
15	$V_{DDA(DAC1)(3V3)}$	16	S_IOUTN
17	S_IOUTP	18	$V_{DDA(DAC2)(3V3)}$
19	SADDR0	20	SADDR1
21	RST_N	22	TDO
23	TDI	24	TMS
25	$V_{DDD2(1V2)}$	26	V_{SSD2}
27	TCK	28	SCL
29	SDA	30	TRST_N

Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol
31	GPIO2/SDA_O	32	GPIO1/SCL_O
33	GPIO0/VSYNC	34	$V_{DDDR(3V3)}$
35	V_{SSDR}	36	i.c.
37	IF_AGC	38	i.c.
39	$V_{DDD(ADC)(3V3)}$	40	$V_{SSA(ADC)}$

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1][2]	Description
Reset			
RST_N	21	I	The RST_N input is asynchronous and active LOW, and clears the TDA8295. When RST_N goes LOW, the circuit immediately enters its Reset mode and normal operation will resume four XIN signal falling edges later after RST_N returns HIGH. Internal register contents are all initialized to their default values. The minimum width of RST_N at LOW level is four XIN clock periods.
Reference			
XIN	8	I	Crystal oscillator input pin. In Slave mode (typically), the XIN input simply receives a 16 MHz clock signal from an external device (typically from the TDA8275A or TDA1827x). In Oscillator mode, a fundamental 16 MHz (typically) crystal is connected between pin XIN and pin XOUT.
XOUT	9	O	Crystal oscillator output pin. In Slave mode, the XOUT output is not connected. In Oscillator mode a fundamental 16 MHz (typically) crystal is connected between pin XIN and pin XOUT.
I²C-bus			
SDA	29	I/O, OD	I²C-bus bidirectional serial data. SDA is an open-drain output and therefore requires an external pull-up resistor (typically 4.7 kΩ).
SCL	28	I	I²C-bus clock input. SCL is nominally a square wave with a maximum frequency of 400 kHz. It is generated by the system I²C-bus master.
SADDR0	19	I	These two bits allow to select four possible I²C-bus addresses, and therefore permits to use several TDA8295 in the same application and/or to avoid conflict with other ICs. The complete I²C-bus address is: 1, 0, 0, SADDR1, 0, 1, SADDR0 (see also Section 9.1).
SADDR1	20	I	
I²C-bus feed-through switch or GPIO			
GPIO2/SDA_O	31	I/O, OD	SDA_O is equivalent to SDA but can be 3-stated by I²C-bus programming. It is the output of a switch controlled by I2CSW_EN parameter. SDA_O is an open-drain output and therefore requires an external pull-up resistor (see Section 9.3.20).
GPIO1/SCL_O	32	I/O, OD	SCL_O is equivalent to SCL input but can be 3-stated by I²C-bus programming. SCL_O is an open-drain output and therefore requires an external pull-up resistor (see Section 9.3.20). For proper functioning of the I²C-bus feed-through, a capacitor C = 33 pF to GND must be added (see Section 13.6).
V-sync or GPIO			
GPIO0/VSYNC	33	I/O, OD	vertical synchronization pulse needed for the NXP Silicon Tuner (see Section 9.3.20)
Tuner IF AGC			
IF_AGC	37	I/O, OD, T	tuner IF AGC output

Table 4. Pin description *...continued*

Symbol	Pin	Type[1][2]	Description
Boundary scan			
TMS	24	I	Test mode select provides the logic levels needed to change the TAP controller from state to state during the boundary scan test.
TRST_N	30	I	Test reset is used to reset the TAP controller (active LOW). Grounding is mandatory in Functional mode.
TCK	27	I	Test clock is used to drive the TAP controller.
TDI	23	I	Test data input is the serial data input for the test data instruction.
TDO	22	O	Test data output is the serial test data output pin. The data is provided on the falling edge of TCK.
ADC			
IF_POS	1	AI	IF positive analog input for internal ADC
IF_NEG	2	AI	IF negative analog input for internal ADC
DAC			
V_IOUTP	14	AO	positive analog current output of the video output
V_IOUTN	13	AO	negative analog current output of the video output
S_IOUTP	17	AO	positive analog current output of the SSIF/mono sound output
S_IOUTN	16	AO	negative analog current output of the SSIF/mono sound output
RSET	11	I	External bias setting of the DACs. An external resistor (1 kΩ typical) has to be connected between RSET and the analog ground of the board. This resistor generates the current into the DACs and also defines the full scale output current. The total parasitic capacitance seen externally from the RSET pin has to be lower than 20 pF.
Supplies and grounds			
$V_{DDA(DAC1)(3V3)}$	15	PS	DAC1 (video DAC) and DAC reference module analog supply voltage (3.3 V typical)
$V_{DDA(DAC2)(3V3)}$	18	PS	DAC2 (sound DAC) analog supply voltage (3.3 V typical)
$V_{SSA(DAC)}$	12	GND	DAC reference module analog ground supply voltage (0 V typical)
$V_{DDA(ADC)(3V3)}$	3	PS	IF ADC analog supply voltage (3.3 V typical)
$V_{DDD(ADC)(3V3)}$	39	PS	IF ADC digital supply voltage (3.3 V typical)
$V_{SSA(ADC)}$	40	GND	ADC analog ground supply voltage (0 V typical)
$V_{DDD1(1V2)}$	4	PS	ADC, PLL and DACs digital supply voltage (1.2 V typical)
V_{SSD1}	5	GND	ADC, PLL and DACs digital ground supply voltage (0 V typical)
$V_{DDA(PLL)(1V2)}$	7	PS	crystal oscillator and clock PLL analog supply voltage (1.2 V typical)
$V_{SSA(PLL)}$	10	GND	crystal oscillator and clock PLL analog ground supply voltage (0 V typical)
$V_{DDD2(1V2)}$	25	PS	core digital supply voltage (1.2 V typical)
V_{SSD2}	26	GND	core digital ground supply voltage (0 V typical)
$V_{DDDR(3V3)}$	34	PS	ring digital supply voltage (3.3 V typical)
V_{SSDR}	35	GND	ring digital ground supply voltage (0 V typical)
Other pins			
i.c.	36	I	internally connected; connect to ground
i.c.	38	I	internally connected; connect to ground
i.c.	6	I	internally connected; connect to ground

[1] All digital inputs are 5 V tolerant (except pin XIN).

[2] The pin types are defined in Table 5.

Table 5. Pin type description

Type	Description
AI	analog input
AO	analog output
GND	ground
I	digital input
I/O	digital input and output
O	digital output
OD	open-drain output
PS	power supply
T	3-state

8. Functional description

8.1 IF ADC

The low IF spectrum (1 MHz to 10 MHz) from the Silicon Tuner TDA8725A or TDA1827x is fed symmetrically to the 12-bit IF ADC of the TDA8295, where it is sampled with 54 MHz or 27 MHz. All the anti-aliasing filtering is already done in the Silicon Tuner.

8.2 Filters

The internal filters permit to reduce the sampling rate to 13.5 MHz, and to form a complex signal to ease the effort of further signal processing. Before this, the DC offset (coming from the ADC) is removed.

In addition, standard dependent notch filters for the adjacent sound carriers protect the picture carrier PLL from malfunctioning and avoid disturbances (i.e. moire) becoming visible in the video output.

8.3 PLL demodulator

The second-order PLL is the core block of the whole IC. It is very robust against adverse field conditions, like excessive overmodulation, no residual carrier presence or unwanted phase or frequency modulation of the picture carrier. The PLL output is the synchronously demodulated channel.

The AFC data is available via the I^2C-bus.

8.4 Nyquist filter, video low-pass filter, video and group delay equalizer, video leveling

The afore-mentioned down-mixed complex signal at the mixer CORDIC output, already consisting of the demodulated content of the picture carrier together with the sound carriers (the so-called intercarriers), is running through a Nyquist filter to get a flat video response and is made real.

Afterwards, a video low-pass filter suppresses the sound carriers and other disturbers.

Next comes the equalizer circuit to remove the transmitter group delay predistortion.

A video leveling stage follows, which brings the output within the SCART specification (3dB overall), despite heavy overmodulation. The response time is made very slow.

Finally, a video equalizer allows to compensate the perhaps non-flat frequency response from the tuner or to change the overall video response according to customer wish (i.e. peaking or early roll-off).

8.5 Upsampler and video DAC

The filtered and compensated CVBS signal is connected to the oversampled 10-bit video DAC (f_s = 108 MHz) via an interpolation stage. The strong oversampling replaces a former complicated LCR postfiltering by a simple first-order RC low-pass filter to remove the DAC image frequencies sufficiently. This holds also for the sound DAC, described in Section 8.6.

8.6 SSIF/mono sound processing

The complex signal is routed via a band-pass and interpolation filter to the 10-bit sound DAC for the recovery of the second sound carriers (SSIF). A very sharp band-pass filter at 5.5 MHz is added in the FM Radio mode to remove neighbor channels. This also eases the dynamic burden on the following ADC in the demodulator/decoder chip. The afore-mentioned high-selectivity band-pass, which replaces the former ceramic filter, is located behind a frequency shifter. In there, the incoming wanted FM radio channel from the Silicon Tuner is changed from 1.25 MHz to 5.5 MHz.

Moreover, the complex signal is demodulated in a linear CORDIC detector and low-pass filtered to attenuate the video spectrum and the second sound carrier, respectively other disturbers above the intercarrier. The output of the linear CORDIC (phase information) is differentiated for getting the demodulated FM audio. The AM demodulation is executed in a synchronous fashion by using a narrow-band PLL demodulator.

A de-emphasis filter is implemented for FM standards, before the audio is interpolated to 108 MHz as in the CVBS case.

The mono audio is made available in the sound DAC via an I^2C-bus controlled selector in case the intercarrier path is not used for driving an external stereo demodulator.

However, if the mono audio output has to meet the SCART specification, an external cheap operational amplifier with 12 dB gain becomes necessary, because the low supply voltage for the TDA8295 doesn't allow such high levels like 2 V (RMS) maximum.

8.7 Tuner IF AGC

This AGC controls the tuner IF AGC amplifier in the TDA8275A or TDA1827x in such a way, that the IF ADC is always running with a permanent headroom of 3 dB for the sum of all signals present at the ADC input. This ensures an always optimal exploitation of the dynamic range in the IF ADC.

The detection is done in peak Search mode during a field period. The attack time is made much faster than the decay time in order to avoid transient clipping effects in the IF ADC. This can happen during channel change or airplane flutter conditions.

The above wideband, slowly acting AGC loop (uncorrelated) is of first-order integral action. It is closed via the continuous tuner IF AGC amplifier in the Silicon Tuner via a bit stream DAC (PWM signal at 13.5 MHz, 27 MHz or 54 MHz) and an external and uncritical first-order RC low-pass.

8.8 Digital IF AGC

Common to both IF AGC concepts is the peak search algorithm as long as the H/V PLL is not locked. This is of advantage for the acquisition by avoiding hang-ups due to excessive overloading, so being able to leave the saturated condition by reducing the gain.

Two Detection modes are made available in the IC via I^{2}C-bus.

- Black level gated AGC:

  The first mode uses an IF AGC detector which is gated with a very robust and well-proven H/V sync PLL block on board. Gating occurs on the black level (most of the time on the back porch) of the video signal and the control is delivered after an error integration and exponential weighting to the internal IF AGC amplifier. This IF AGC amplifier, in fact a multiplier, has a control range of −20 dB to +48 dB.

- Peak AGC:

  A fast attack and slow decay action cares for a good and nearly clip-free transient behavior. This proved to be more robust for non-standard signals, like sync clipping along the transmitter/receiver chain.

  With respect to the IF AGC speed generally, only the gated black level or peak sync IF AGC can be made fast. However the peak search one, used for positive modulation standards (L and L-accent standard), is rather slow because the VITS is present only once in a field.

  The correlated or narrow-band AGC loop, closed via the continuous IF AGC amplifier in the TDA8295, is of first-order integral action and settles at a constant IF input level with a permanent headroom of 12 dB (picture carrier). This headroom is needed for the own sound carriers and the leaking neighbor (N − 1) spectrum.

8.9 Clock generation

Finally, either an external reference frequency (i.e. from the Silicon Tuner) or an own on-chip crystal oscillator in the TDA8295 feeds the internal PLL synthesizer to generate the necessary clock signals.

9. I^{2}C-bus control

9.1 Protocol of the I^{2}C-bus serial interface

The TDA8295 internal registers are accessible by means of the I^{2}C-bus serial interface. The SDA bidirectional pin is used as the data input/output pin and SCL as the clock input pin. The highest SCL speed is 400 kHz.

9.1.1 Write mode

S	BYTE 1	A	BYTE 2	A	BYTE 3	A		BYTE n	A	P
start	address 0	ack	start index	ack	data 1	ack	....	data n	ack	stop

001aad381

Fig 3. I²C-bus Write mode

Table 6. Address format

7	6	5	4	3	2	1	0
1	0	0	SADDR1	0	1	SADDR0	R/W

Table 7. I²C-bus transfer description

Field	Bit	Description
S	-	START condition
Byte 1	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 0 for write action
A	-	acknowledge
Byte 2	7 to 0	start index
A	-	acknowledge
Byte 3	7 to 0	data 1
A	-	acknowledge
:		
Byte n	7 to 0	data n
A	-	acknowledge
P	-	STOP condition

S	BYTE 1	A	BYTE 2	A	BYTE 3	A	P
start	1000 0100	ack	0000 0001	ack	0000 0010	ack	stop

001aah355

a. Address 84h, write 02h in register 01h

S	BYTE 1	A	BYTE 2	A	BYTE 3	A	BYTE 4	A	P
start	1000 0100	ack	0000 0010	ack	0000 0101	ack	0000 0100	ack	stop

001aah356

b. Address 84h, write 05h in register 02h and 04h in register 03h

Fig 4. Examples I²C-bus Write mode

9.1.2 Read mode

S	BYTE 1	A	BYTE 2	A	S	BYTE 3	A	BYTE 4	A		BYTE n	A	P
start	address 0	ack	start index	ack	start	address 1	ack	value 1	ack	....	value n	ack	stop

001aad423

Fig 5. I²C-bus Read mode

Table 8. I²C-bus transfer description

Field	Bit	Description
S	-	START condition
Byte 1	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 0 for write action
A	-	acknowledge
Byte 2	7 to 0	start index
A	-	acknowledge
S	-	START condition (without stop before)
Byte 3	7 to 5	device address
	4	SADDR1
	3 and 2	device address
	1	SADDR0
	0	R/W = 1 for read action
A	-	acknowledge
Byte 4	7 to 0	value 1
A	-	acknowledge
:		
Byte n	7 to 0	value n
A	-	acknowledge
P	-	STOP condition

S	BYTE 1	A	BYTE 2	A	S	BYTE 3	A	BYTE 4	A	BYTE 5	A	P
start	1000 0100	ack	0000 0010	ack	start	1000 0101	ack	0000 0101	ack	0000 0100	ack	stop

001aah357

Address 84h, read register 02h with value 05h and read register 03h with value 04h

Fig 6. Example I²C-bus Read mode

9.2 Register overview

The TDA8295 internal registers are accessible by means of the I^2C-bus serial interface as described in Section 9.1. In Table 9 and Table 10 an overview of all the registers is given, the register description can be found in Section 9.3.

Table 9. I²C-bus registers

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
00h	STANDARD	STANDARD[7:0]							
01h	EASY_PROG	-	-	-	-	-	-	-	ACTIVE
02h	DIV_FUNC	AGC_SEL	AGC_TRI	-	-	0	POL_DET	VID_MOD	IF_SWAP
03h	ADC_HEADR	-	-	-	-	ADC_HEADR[3:0]			
04h	PC_PLL_FUNC	PC_PLL_BW[4:0]					PLL_ON	PULL_IN	CAR_DET
05h	PC_PLL_THRES	-	-	-	-	PH_ERR_THRES[3:0]			
06h	PC_PLL_WGT	PHASE_PER	PHASE_GAIN[6:0]						
07h	PC_FLL_FUNC	FLL_ON	LIM_ON	FLL_LIM[5:0]					
08h	CARDET_LEVEL	-	-	-	CAR_DET_LVL[4:0]				
09h	DTO_PC_LOW	DTO_PC[7:0]							
0Ah	DTO_PC_MID	DTO_PC[15:8]							
0Bh	DTO_PC_HIGH	DTO_PC[23:16]							
0Ch	DTO_SC_LOW	DTO_SC[7:0]							
0Dh	DTO_SC_MID	DTO_SC[15:8]							
0Eh	DTO_SC_HIGH	DTO_SC[23:16]							
0Fh	FILTERS_1	VID_FILT[2:0]			NOTCH_FILT[4:0]				
10h	FILTERS_2	-	-	-	DC_NOTCH	SBP[3:0]			
11h	GRP_DELAY	-	-	-	GRP_DEL[4:0]				
12h	D_IF_AGC_SET_1	D_IF_AGC_CORR	D_IF_AGC_MODE	D_IF_AGC_AVG[4:0]					RST_INT
13h	D_IF_AGC_SET_2	D_AGC_ERR_LIM	D_IF_AGC_BW[6:0]						
14h	D_IF_AGC_FORCE	D_FORCE	D_FORCE_VAL[6:0]						
15h	T_IF_AGC_SET	POL_TIF	T_IF_AGC_SPEED[6:0]						
16h	T_IF_AGC_LIM	UP_LIM[3:0]				LOW_LIM[3:0]			
17h	T_IF_AGC_FORCE	T_FORCE	T_FORCE_VAL[6:0]						
18h	T_IF_AGC_FS	-	-	-	-	-	T_IF_AGC_FS[2:0]		
19h to 1Bh	reserved	reserved							
1Ch	V_SYNC_DEL	VS_WIDTH[1:0]		VS_POL	VS_DEL[4:0]				
1Dh	CVBS_SET	-	-	-	-	-	FOR_BLK	AUTO_BLK	VID_LVL

Table 9. I²C-bus registers *…continued*

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
1Eh	CVBS_LEVEL	CVBS_LVL[7:0]							
1Fh	CVBS_EQ	CVBS_EQ[7:0]							
20h	SOUNDSET_1	-	AM_FM_SND[1:0]		DEEMPH[4:0]				
21h	SOUNDSET_2	-	-	-	HD_DK	FOR_MUTE	AUTO_MUTE	SSIF_SND[1:0]	
22h	SOUND_LEVEL	-	-	-	SND_LVL[4:0]				
23h	SSIF_LEVEL	-	-	-	SSIF_LVL[4:0]				
24h	ADC_SAT	ADC_SAT[7:0]							
25h	AFC	AFC[7:0]							
26h	HVPLL_STAT	-	-	NOISE_DET	MAC_DET	FIDT	V_LOCK	F_H_LOCK	N_H_LOCK
27h	D_IF_AGC_STAT	D_IF_AGC_STAT[7:0]							
28h	T_IF_AGC_STAT	T_IF_AGC_STAT[7:0]							
29h	reserved	reserved							
2Ah	ANALOG_DEBUG	-	-	-	-	-	-	ADC_TEST	DAC_TEST
2Bh to 2Eh	not used	-	-	-	-	-	-	-	-
2Fh	IDENTITY	IDENTITY[7:0]							
30h	CLB_STDBY	-	-	-	-	-	-	STDBY	CLB
31h	reserved	-	-	-	-	reserved			
32h	ANALOG_STAT	-	LOAD_DACV	LOAD_DACS	PLL_LOCK	reserved			
33h	ADC_CTL	GAINSET	CS[2:0]			DCIN	TWOS	SLEEP	PD_ADC
34h	ADC_CTL_2	-	-	-	-	-	-	AD_PLL_BYP	AD_SR54M
35h	VIDEODAC_CTL	0	B_DA_V[5:0]						PD_DA_V
36h	AUDIODAC_CTL	0	B_DA_S[5:0]						PD_DA_S
37h	DAC_REF_CLK_CTL	-	DA_CLK_INV	DA_PLL_BYP	B_REF[3:0]				PD_DA_REF
38h	PLL_REG00	0	0	PLL_AUTO	0	0	0	0	0
39h to 3Bh	not used	-	-	-	-	-	-	-	-
3Ch	PLL_REG04	-	-	-	-	-	0	0	0
3Dh	not used	-	-	-	-	-	-	-	-
3Eh	PLL_REG06	0	CLK_EN	BYP_PLL	DIRECTO	DIRECTI	0	0	PD_PLL

Table 9. I²C-bus registers *…continued*

Index	Name	7 (MSB)	6	5	4	3	2	1	0 (LSB)
3Fh	PLL_REG07	-	0	0	0	0	0	0	0
40h	PLL_REG08	MSEL[7:0]							
41h	PLL_REG09	NSEL[6:0]							0
42h	PLL_REG10	0	0	0	PSEL[4:0]				
43h	XTALOSC_CTL	-	-	-	-	-	HF	0	0
44h	GPIOREG_0	GP1_CF[3:0]				GP0_CF[3:0]			
45h	GPIOREG_1	I2CSW_EN	I2CSW_ON	-	-	GP2_CF[3:0]			
46h	GPIOREG_2	CLK_INV_GP2	CLK_INV_GP1	CLK_INV_GP0	-	-	GP2_VAL	GP1_VAL	GP0_VAL

Table 10. I²C-bus register reference

Index	Name	I²C-bus access	Default value	Reference
00h	STANDARD	R/W	01h	Table 11
01h	EASY_PROG	R/W	00h	Table 12
02h	DIV_FUNC	R/W	04h	Table 14
03h	ADC_HEADR	R/W	01h	Table 15
04h	PC_PLL_FUNC	R/W	27h	Table 16
05h	PC_PLL_THRES	R/W	04h	Table 17
06h	PC_PLL_WGT	R/W	10h	Table 18
07h	PC_FLL_FUNC	R/W	84h	Table 19
08h	CARDET_LEVEL	R/W	08h	Table 20
09h	DTO_PC_LOW	R/W	85h	Table 21
0Ah	DTO_PC_MID	R/W	F6h	Table 21
0Bh	DTO_PC_HIGH	R/W	92h	Table 21
0Ch	DTO_SC_LOW	R/W	55h	Table 22
0Dh	DTO_SC_MID	R/W	55h	Table 22
0Eh	DTO_SC_HIGH	R/W	55h	Table 22
0Fh	FILTERS_1	R/W	21h	Table 23
10h	FILTERS_2	R/W	11h	Table 24
11h	GRP_DELAY	R/W	01h	Table 25
12h	D_IF_AGC_SET_1	R/W	A0h	Table 26
13h	D_IF_AGC_SET_2	R/W	90h	Table 27
14h	D_IF_AGC_FORCE	R/W	67h	Table 28
15h	T_IF_AGC_SET	R/W	88h	Table 29
16h	T_IF_AGC_LIM	R/W	F0h	Table 30
17h	T_IF_AGC_FORCE	R/W	3Fh	Table 31
18h	T_IF_AGC_FS	R/W	02h	Table 32
19h	reserved	R/W	88h	-
1Ah	reserved	R/W	80h	-
1Bh	reserved	R/W	00h	-
1Ch	V_SYNC_DEL	R/W	6Fh	Table 33
1Dh	CVBS_SET	R/W	01h	Table 34
1Eh	CVBS_LEVEL	R/W	73h	Table 35
1Fh	CVBS_EQ	R/W	08h	Table 36
20h	SOUNDSET_1	R/W	21h	Table 37
21h	SOUNDSET_2	R/W	02h	Table 38
22h	SOUND_LEVEL	R/W	08h	Table 39
23h	SSIF_LEVEL	R/W	04h	Table 40
24h	ADC_SAT	R	-	Table 41
25h	AFC	R	-	Table 42
26h	HVPLL_STAT	R	-	Table 44
27h	D_IF_AGC_STAT	R	-	Table 45
28h	T_IF_AGC_STAT	R	-	Table 46

Table 10. I²C-bus register reference …continued

Index	Name	I²C-bus access	Default value	Reference
29h	reserved	R	-	-
2Ah	ANALOG_DEBUG	R/W	00h	Table 47
2Bh to 2Eh	not used	-	-	-
2Fh	IDENTITY	R	-	Table 48
30h	CLB_STDBY	R/W	01h	Table 49
31h	reserved	R/W	00h	-
32h	ANALOG_STAT	R	-	Table 50
33h	ADC_CTL	R/W	24h	Table 51
34h	ADC_CTL_2	R/W	01h	Table 52
35h	VIDEODAC_CTL	R/W	7Eh	Table 53
36h	AUDIODAC_CTL	R/W	00h	Table 54
37h	DAC_REF_CLK_CTL	R/W	00h	Table 55
38h	PLL_REG00	R/W	20h	Table 56
39h to 3Bh	not used	-	-	-
3Ch	PLL_REG04	R/W	00h	Table 57
3Dh	not used	R/W	-	-
3Eh	PLL_REG06	R/W	61h	Table 58
3Fh	PLL_REG07	R/W	00h	Table 60
40h	PLL_REG08	R/W	1Ah	Table 60
41h	PLL_REG09	R/W	02h	Table 60
42h	PLL_REG10	R/W	01h	Table 60
43h	XTALOSC_CTL	R/W	00h	Table 61
44h	GPIOREG_0	R/W	11h	Table 62
45h	GPIOREG_1	R/W	01h	Table 63
46h	GPIOREG_2	R/W	07h	Table 65

9.3 Register description

If registers (or bit groups contained in registers) are programmed with invalid values, i.e. values different from those described in the tables below, the default behavior is chosen for the related block.

9.3.1 Standard setting with easy programming

With the implemented ‘easy programming’, only one bit sets the TV or FM radio standard with recommended register content. If not suitable however, any of these registers can be written with other settings. With the rising edge of the bit ACTIVE, the registers 02h to 23h are programmed internally with the standard dependent settings according to Table 13. The content of registers with address 24h and higher is untouched.

Table 11. STANDARD register (address 00h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 0	STANDARD[7:0]	R/W		TV or FM radio standard selection (easy programming)
			0000 0001*	M/N standard
			0000 0010	B standard
			0000 0100	G/H standard
			0000 1000	I standard
			0001 0000	D/K standard
			0010 0000	L standard
			0100 0000	L-accent standard
			1000 0000	FM radio

Table 12. EASY_PROG register (address 01h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 1	-	R/W	-	not used
0	ACTIVE	R/W		With the rising edge of this bit, the registers 02h to 23h are programmed with the standard dependent settings (see Table 13).
			0*	no action
			1	no action
			0 to 1	activate easy programming

Example: To set the device to B standard e.g., please do the following steps.

1. Write 02h to register STANDARD, address 00h (set B standard)
2. Write 00h to register EASY_PROG, address 01h (make sure that ACTIVE = 0)
3. Write 01h to register EASY_PROG, address 01h (due to 0 to 1 transition of ACTIVE the device is set to B standard, i.e. registers 02h to 23h are programmed automatically according to Table 13)
4. Write 01h to register EASY_PROG, address 01h (reset ACTIVE to logic 0)

Table 13. Easy programming values

Register		Standard							
Index	Name	M/N[1]	B	G/H	I	D/K	L	L-accent	FM radio
02h	DIV_FUNC	04h	04h	04h	04h	04h	06h	07h	00h
03h	ADC_HEADR	01h	01h	01h	01h	01h	01h	01h	01h
04h	PC_PLL_FUNC	27h	27h	27h	27h	27h	27h	27h	22h
05h	PC_PLL_THRES	04h	04h	04h	04h	04h	04h	04h	04h
06h	PC_PLL_WGT	10h	10h	10h	10h	10h	10h	10h	10h
07h	PC_FLL_FUNC	84h	84h	84h	84h	84h	84h	84h	04h
08h	CARDET_LEVEL	08h	08h	08h	08h	08h	08h	08h	08h
09h	DTO_PC_LOW	85h	00h	7Bh	7Bh	7Bh	7Bh	26h	00h
0Ah	DTO_PC_MID	F6h	00h	09h	09h	09h	09h	B4h	00h
0Bh	DTO_PC_HIGH	92h	80h	6Dh	6Dh	6Dh	6Dh	17h	80h
0Ch	DTO_SC_LOW	55h	DAh	DAh	1Dh	5Fh	5Fh	5Fh	DAh
0Dh	DTO_SC_MID	55h	4Bh	4Bh	C7h	42h	42h	42h	4Bh
0Eh	DTO_SC_HIGH	55h	68h	68h	71h	7Bh	7Bh	7Bh	68h
0Fh	FILTERS_1	21h	42h	44h	44h	44h	44h	44h	90h
10h	FILTERS_2	11h	12h	12h	12h	12h	12h	12h	14h
11h	GRP_DELAY	01h	02h	02h	10h	04h	08h	08h	10h
12h	D_IF_AGC_SET_1	A0h	A0h	A0h	A0h	A0h	A0h	A0h	A0h
13h	D_IF_AGC_SET_2	90h	90h	90h	90h	90h	90h	90h	08h
14h	D_IF_AGC_FORCE	67h	67h	67h	67h	67h	67h	67h	E7h
15h	T_IF_AGC_SET	88h	88h	88h	88h	88h	88h	88h	88h
16h	T_IF_AGC_LIM	F0h	F0h	F0h	F0h	F0h	F0h	F0h	F0h
17h	T_IF_AGC_FORCE	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh	3Fh
18h	T_IF_AGC_FS	02h	02h	02h	02h	02h	02h	02h	02h
19h	reserved	88h	88h	88h	88h	88h	88h	88h	88h
1Ah	reserved	80h	80h	80h	80h	80h	80h	80h	80h
1Bh	reserved	00h	00h	00h	00h	00h	00h	00h	00h
1Ch	V_SYNC_DEL	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh	6Fh
1Dh	CVBS_SET	01h	01h	01h	01h	01h	01h	01h	04h
1Eh	CVBS_LEVEL	73h	73h	73h	73h	73h	6Ch	6Ch	73h
1Fh	CVBS_EQ	08h	08h	08h	08h	08h	08h	08h	10h
20h	SOUNDSET_1	21h	22h	22h	22h	22h	44h	44h	22h
21h	SOUNDSET_2	02h	02h	02h	02h	02h	02h	02h	02h
22h	SOUND_LEVEL	08h	04h	04h	04h	04h	04h	04h	02h
23h	SSIF_LEVEL	04h	04h	04h	04h	04h	04h	04h	04h

[1] M/N standard settings are equal to the power-on reset (default) values.

9.3.2 Diverse functions (includes tuner IF AGC Pin mode)

Table 14. DIV_FUNC register (address 02h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	AGC_SEL	R/W		It determines the tuner IF AGC output Pin mode. The open-drain output can be used in special applications in need of a higher control voltage.
			0*	Normal mode
			1	Open-drain mode
6	AGC_TRI	R/W		When AGC_TRI is set to logic 1 the tuner IF AGC output pin is in 3-state mode. This mode is useful for paralleling a channel decoder for instance.
			0*	Normal mode
			1	3-state mode
5 and 4	-	R/W	-	not used
3	-	R/W	0	reserved, must be set to logic 0
2	POL_DET	R/W		The polarity detector ensures the proper polarity of the video signal. So, the sync impulses of the video output are near ground level.
			0	polarity detector off
			1*	polarity detector on
1	VID_MOD	R/W		Selects video modulation. The only standards with positive video modulation are L and L-accent.
			0*	negative video modulation
			1	positive video modulation
0	IF_SWAP	R/W		When HIGH, the demodulator expects a swapped IF spectrum. This is the case in L-accent standard. This option is also built in for flexibility reasons.
			0*	normal IF spectrum expected
			1	swapped IF spectrum expected

9.3.3 ADC headroom

Table 15. ADC_HEADR register (address 03h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	-	not used
3 to 0	ADC_HEADR[3:0]	R/W		ADC_HEADR adjusts the needed headroom for the wanted channel's own sound carriers and the N – 1 adjacent sound carriers (PC in L-accent standard). The ADC headroom is related to the sum of all signals. This function is built in for debugging purposes.
			0001*	ADC headroom 3 dB
			0010	ADC headroom 6 dB
			0100	ADC headroom 9 dB
			1000	ADC headroom 12 dB

9.3.4 Picture carrier PLL functions

Table 16. PC_PLL_FUNC register (address 04h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 3	PC_PLL_BW[4:0]	R/W		picture carrier PLL loop bandwidth selection
			0 0001	loop bandwidth 15 kHz
			0 0010	loop bandwidth 30 kHz
			0 0100*	loop bandwidth 60 kHz
			0 1000	loop bandwidth 130 kHz
			1 0000	loop bandwidth 280 kHz (for very bad transmitter quality)
2	PLL_ON	R/W		the picture carrier PLL can be disengaged (e.g. in FM radio standard)
			0	PLL off (FM radio)
			1*	PLL on
1	PULL_IN	R/W		PULL_IN selects the pull-in range of the picture carrier PLL/FPLL
			0	pull-in range ±1.66 MHz
			1*	pull-in range ±830 kHz
0	CAR_DET	R/W		The carrier detector freezes the PLL in case of a picture carrier overmodulation (especially when the picture carrier is very low or disappears). In addition, the picture carrier DTO value is forced to an optimal one to avoid picture carrier phase drift. To adjust the threshold see CAR_DET_LVL.
			0*	carrier detector off
			1	carrier detector on

Table 17. PC_PLL_THRES register (address 05h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7 to 4	-	R/W	-	not used
3 to 0	PH_ERR_THRES[3:0]	R/W		When the settable threshold for the linear phase detector as part of the picture carrier PLL is passed, the phase detector slope is weighted according to the settings in PHASE_GAIN. This feature is of advantage during adverse field conditions. In case multipath happens like ghosts, the PC PLL should not follow the sudden phase jumps. So, the PC PLL is made slow (lower loop bandwidth) with PC_PLL_THRES after surpassing the threshold. This threshold is related to a fraction of FS. There, FS is 90° if PHASE_PER is logic 0 (default) or 180° when logic 1. If the ICPM or ICFM is large because of bad transmitters with oscillator pulling or modulator imbalance, the PC PLL should follow as true as possible. This can be done by increasing the loop bandwidth with overweighting (see PHASE_GAIN, Table 18).
			0001	$^1/_{32}$ FS
			0010	$^1/_{16}$ FS
			0100*	$^1/_8$ FS
			1000	$^1/_4$ FS

Table 18. PC_PLL_WGT register (address 06h) bit description

*Legend: * = default value.*

Bit	Symbol	Access	Value	Description
7	PHASE_PER	R/W		By default, the linear phase detector transfer function is repetitive in π. This allows a good picture carrier overmodulation performance, because the PC PLL doesn't need to reacquire the 180° phase modulation, caused by the excessive AM index above m = 100 % (negative residual picture carrier).
			0*	π (needed for overmodulation)
			1	2π
6 to 0	PHASE_GAIN[6:0]	R/W		phase error weighting (adaptive loop speed), see also PH_ERR_THRES in Table 17 for explanation
			000 0001	× $^1/_{16}$
			000 0010	× $^1/_8$
			000 0100	× $^1/_4$
			000 1000	× $^1/_2$
			001 0000*	flat (no weighting)
			010 0000	× 2
			100 0000	× 4