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TDA8559T

Low-voltage stereo headphone amplifier

Rev. 03 — 15 May 2006 Product data sheets

1. General description

The TDA8559T is a stereo amplifier that operates over a wide supply voltage range from 1.9 V to 30 V and consumes a very low quiescent current. This makes it suitable for battery fed applications (2 × 1.5 V cells). Because of an internal voltage buffer, this device can be used with or without a capacitor connected in series with the load. It can be applied as a headphone amplifier, but also as a mono amplifier with a small speaker (25 Ω), or as a line driver in mains applications.

2. Features

- Operating voltage from 1.9 V to 30 V
- Very low quiescent current
- Low distortion
- Few external components
- Differential inputs
- Usable as a mono amplifier in Bridge-Tied Load (BTL) or stereo Single-Ended (SE)
- Single-ended mode without loudspeaker capacitor
- Mute and Standby mode
- Short-circuit proof to ground, to supply voltage (< 10 V) and across load
- No switch on or switch off clicks
- ESD protected on all pins

3. Applications

- Portable telephones
- MP3 players
- Portable audio
- Mains fed equipment

PHILIPS

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_P	operating supply voltage			1.9	3	30	V
$I_{q(tot)}$	total quiescent current	open load		-	2.75	4	mA
I_{stb}	standby supply current	open load		-	-	10	µA
Stereo application							
P_o	output power	THD = 10 %		30	35	-	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	[1]	-	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz	[1]	-	0.1	-	%
G_v	voltage gain			25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB		-	750	-	kHz
BTL application							
P_o	output power	THD = 10 %		125	140	-	mW
THD	total harmonic distortion	P_o = 70 mW; f_i = 1 kHz		-	0.05	0.1	%
		P_o = 70 mW; f_i = 10 kHz		-	0.1	-	%
G_v	voltage gain			31	32	33	dB

[1] Measured with low-pass filter 30 kHz.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8559T	SO16	plastic small outline package; 16 leads; body width 3.9 mm; body thickness 1.47 mm	SOT109-1

6. Block diagram

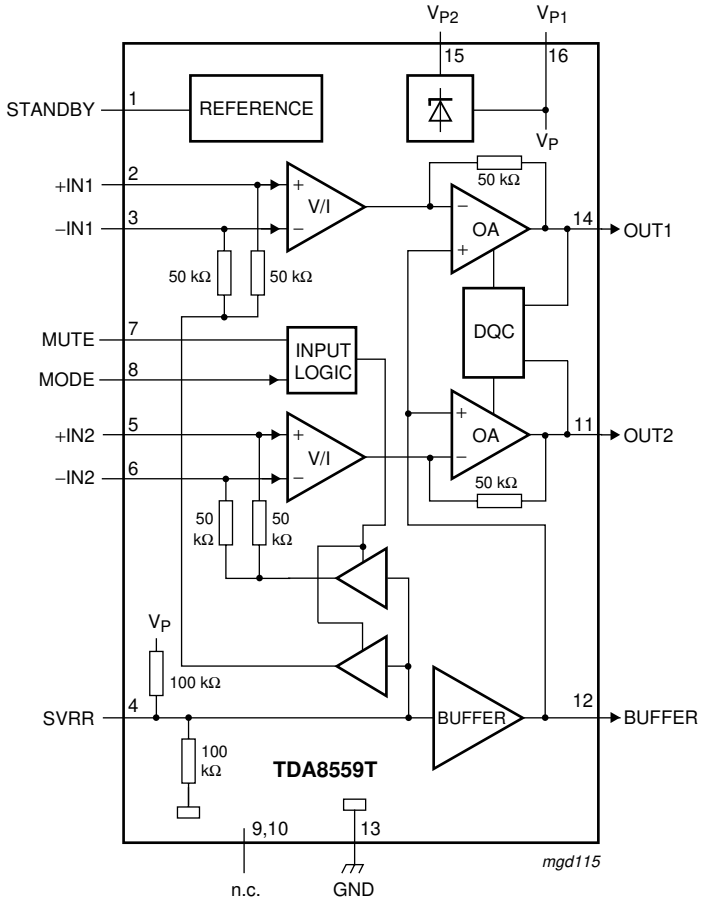
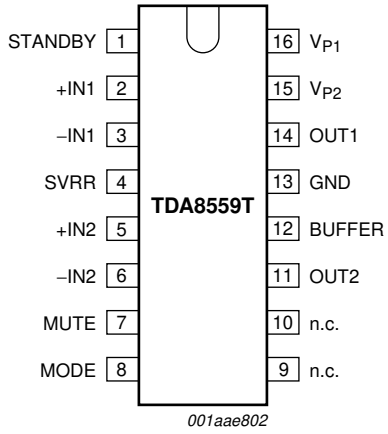


Fig 1. Block diagram

7. Pinning information

7.1 Pinning



Top view

Fig 2. Pin configuration

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
STANDBY	1	standby select
+IN1	2	non-inverting input 1
–IN1	3	inverting input 1
SVRR	4	supply voltage ripple rejection
+IN2	5	non-inverting input 2
–IN2	6	inverting input 2
MUTE	7	mute select
MODE	8	input mode select
n.c.	9	not connected
n.c.	10	not connected
OUT2	11	output 2
BUFFER	12	buffer output ($0.5V_P$)
GND	13	ground
OUT1	14	output 1
V_{P2}	15	high supply voltage
V_{P1}	16	low supply voltage

8. Functional description

The TDA8559T contains two amplifiers with differential inputs, a $0.5V_P$ output buffer and a high supply voltage stabilizer. Each amplifier consists of a voltage-to-current converter (V/I), an output amplifier and a common dynamic quiescent current controller. The gain of each amplifier is internally fixed at 26 dB (= 20 ×). The $0.5V_P$ output can be used as a replacement for the single-ended capacitors. The two amplifiers can also be used as a mono amplifier in a BTL configuration thereby resulting in more output power.

With three mode select pins, the device can be switched into the following modes:

1. Standby mode (I_P < 10 μA)
2. Mute mode
3. Operation mode, with two input selections (the input source is directly connected or connected via coupling capacitors at the input).

The ripple rejection in the stereo application with a single-ended capacitor can be improved by connecting a capacitor between the $0.5V_P$ capacitor pin and ground.

The device is fully protected against short-circuiting of the output pins to ground, to the low supply voltage pin and across the load.

8.1 V/I converters

The V/I converters have a transconductance of 400 μS. The inputs are completely symmetrical and the two amplifiers can be used in opposite phase. The Mute mode causes the V/I converters to block the input signal. The input mode pin selects two applications in which the V/I converters can be used.

The first application (input mode pin floating) is used with a supply voltage below 6 V. The input DC level is at ground level (the unused input pin connected to ground) and no input coupling capacitors are necessary. The maximum converter output current is sufficient to obtain an output swing of 3 V (peak).

In the second application with a supply voltage greater than 6 V (input mode pin HIGH), the input mode pin is connected to V_P. In this configuration (input DC level is $0.5V_P$ + 0.6 V) the input source must be coupled with a capacitor and the two unused input pins must be connected via a capacitor to ground, to improve noise performance. This application has a higher quiescent current, because the maximum output current of the V/I converter is higher to obtain an output voltage swing of 9 V (peak).

8.2 Output amplifiers

The output amplifiers have a transresistance of 50 kΩ, a bandwidth of approximately 750 kHz and a maximum output current of 100 mA. The mid-tap output voltage equals the voltage applied at the non-inverting pin of the output amplifier. This pin is connected to the output of the $0.5V_P$ buffer. This reduces the distortion when the load is connected between an output amplifier and the buffer (because feedback is applied over the load).

8.3 Buffer

The buffer delivers $0.5V_P$ to the output with a maximum output (sink and source) current of 200 mA (peak).

8.4 Dynamic quiescent controller

The Dynamic Quiescent Current controller (DQC) gives the advantage of low quiescent current and low distortion. When there are high frequencies in the output signal, the DQC will increase the quiescent current of the two output amplifiers and the buffer. This will reduce the crossover distortion that normally occurs at high frequencies and low quiescent current. The DQC gives output currents that are linear with the amplitude and the frequency of the output signals. These currents control the quiescent current.

8.5 Stabilizer

The TDA8559T has a voltage supply range from 1.9 V to 30 V. This range is divided over two supply voltage pins. Pin 16 is 1.9 V to 18 V (breakdown voltage of the process); this pin is preferred for supply voltages less than 18 V. Pin 15 is used for applications where V_P is approximately 6 V to 30 V. The stabilizer output is internally connected to the supply voltage pin 16. In the range from 6 V to 18 V, the voltage drop to pin 16 is 1 V. In the range from 18 V to 30 V the stabilizer output voltage (to pin 16) is approximately 17 V.

8.6 Input logic

The MUTE pin (pin 7) selects the Mute mode of the V/I converters. LOW (TTL/CMOS) level is mute. A voltage between 0.5 V (low level) and 1.5 V (high level) causes a soft mute to operate (no plops). When pin 7 is floating or greater than 1.5 V it is in the operating condition.

The input mode pin must be connected to V_P when the supply voltage is greater than 6 V. The input mode logic raises the tail current of the V/I converters and enables the two buffers to bias the inputs of the V/I converters.

8.7 Reference

This circuit supplies all currents needed in this device. With the Standby mode pin 1 (TTL/CMOS), it is possible to switch to the Standby mode and reduce the total quiescent current to below 10 μA.

9. Internal circuitry

Table 4. Internal circuits

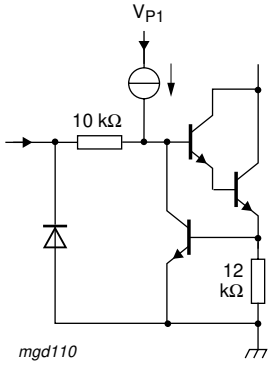
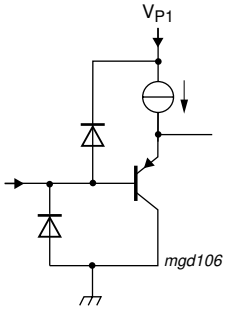
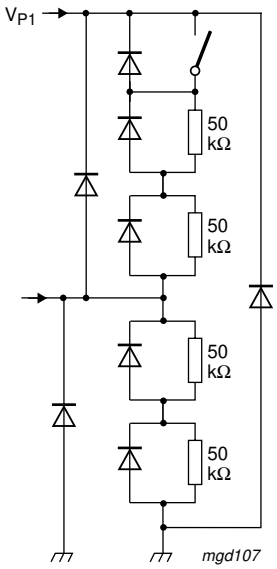
Symbol	Pin	Equivalent circuit
STANDBY	1	
+IN1, −IN1, +IN2 and −IN2	2, 3, 5 and 6	
SVRR	4	

Table 4. Internal circuits *…continued*

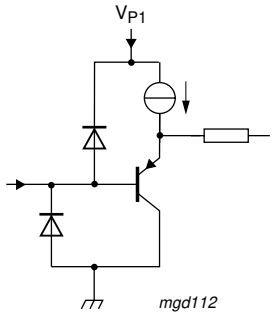
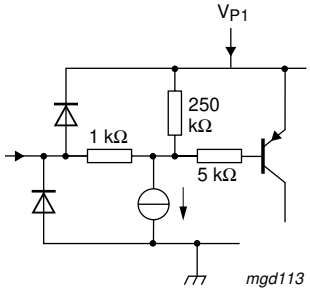
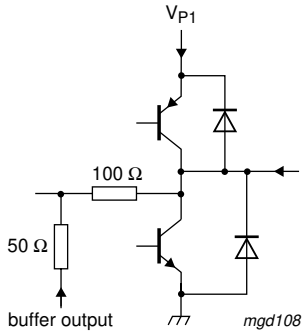
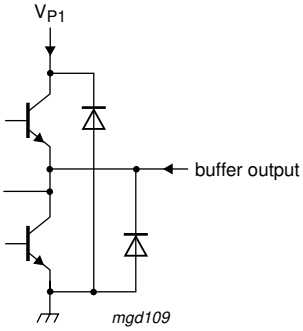
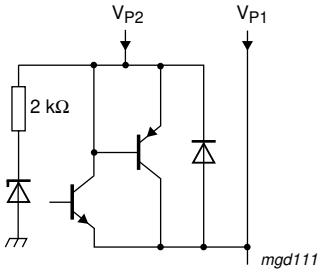
Symbol	Pin	Equivalent circuit
MUTE	7	
MODE	8	

Table 4. Internal circuits *…continued*

Symbol	Pin	Equivalent circuit
OUT2 and OUT1	11 and 14	
BUFFER	12	
V_{P2} and V_{P1}	15 and 16	

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{P2(max)}$	maximum supply voltage (pin 15)		-	30	V
$V_{P1(max)}$	maximum supply voltage (pin 16)		-	18	V
$V_{i(max)}$	maximum input voltage		-	18	V
I_{ORM}	peak output current	repetitive	-	150	mA
P_{tot}	total power dissipation		-	1.19	W
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_{vj}	virtual junction temperature		-	150	°C
t_{sc}	short-circuiting time	V_P < 10 V	-	1	h

11. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	105	K/W

12. Characteristics

Table 7. Characteristics

V_P = 3 V; T_{amb} = 25 °C; f_i = 1 kHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DC characteristics							
V_P	operating supply voltage		[1]	1.9	3	30	V
$I_{q(tot)}$	total quiescent current	open load		-	2.75	4	mA
I_{stb}	standby supply current	open load		-	-	10	µA
V_1	Standby mode voltage	standby		0	-	0.5	V
		operating		1.5	-	18	V
V_7	Mute mode voltage	mute		0	-	0.5	V
		operating		1.5	-	18	V
I_{bias}	input bias current			-	100	300	nA
Single-ended stereo application (R_L = 32 Ω)							
P_o	output power	THD = 10 %		30	35	-	mW
THD	total harmonic distortion	P_o = 20 mW; f_i = 1 kHz	[2]	-	0.075	0.15	%
		P_o = 20 mW; f_i = 10 kHz	[2]	-	0.1	-	%
G_v	voltage gain			25	26	27	dB
f_{ss}	small signal roll-off frequency	–1 dB		-	750	-	kHz
α_{cs}	channel separation	R_s = 5 kΩ		40	-	-	dB
$\lvert\Delta G_v\rvert$	channel unbalance			-	-	1	dB

Table 7. Characteristics *...continued*

V_P = 3 V; T_{amb} = 25 °C; f_i = 1 kHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{no}	noise output voltage		[3]	-	70	85	μV
$V_{no(mute)}$	noise output voltage in mute		[3]	-	20	30	μV
$V_{o(mute)}$	output voltage in mute		[4]	-	-	30	μV
V_{mt}	mid-tap voltage			1.4	1.5	1.6	V
Z_i	input impedance			75	100	125	kΩ
V_{os}	DC output offset voltage		[5]	-	-	100	mV
SVRR	supply voltage ripple rejection		[6]	45	55	-	dB
BTL application (R_L = 25 Ω)							
P_o	output power	THD = 10 %		125	140	-	mW
THD	total harmonic distortion	P_o = 70 mW; f_i = 1 kHz		-	0.05	0.1	%
		P_o = 70 mW; f_i = 10 kHz		-	0.1	-	%
G_v	voltage gain			31	32	33	dB
f_{ss}	small signal roll-off frequency	−1 dB		-	750	-	kHz
V_{no}	noise output voltage		[3]	-	100	120	μV
$V_{no(mute)}$	noise output voltage in mute		[3]	-	25	40	μV
$V_{o(mute)}$	output voltage in mute		[4]	-	-	40	μV
Z_i	input impedance			39	50	61	kΩ
V_{os}	DC output offset voltage		[7]	-	-	150	mV
SVRR	supply voltage ripple rejection		[6]	39	49	-	dB
Line driver application (R_L = 1 kΩ)							
V_o	line output voltage			0.1	-	2.9	V

[1] The supply voltage range at pin V_{P1} is from 1.9 V to 18 V. Pin V_{P2} is used for the voltage range from 6 V to 30 V.

[2] Measured with low-pass filter 30 kHz.

[3] Noise output voltage measured with a bandwidth of 20 Hz to 20 kHz, unweighted. R_s = 5 kΩ.

[4] RMS output voltage in mute is measured with V_i = 200 mV (RMS); f = 1 kHz.

[5] DC output offset voltage is measured between the signal output and the $0.5V_P$ output.

[6] The ripple rejection is measured with a ripple voltage of 200 mV (RMS) applied to the positive supply rail (R_s = 0 kΩ).

[7] DC output offset voltage is measured between the two signal outputs.

13. Application information

13.1 General

For applications with a maximum supply voltage of 6 V (input mode low) the input pins need a DC path to ground (see Figure 3 and Figure 4). For applications with supply voltages in the range from 6 V to 18 V (input mode HIGH) the input DC level is $0.5V_P$ + 0.6 V. In this situation the input configurations illustrated in Figure 5 and Figure 6 have to be used.

The capacitor Cb is recommended for stability improvement. The value may vary between 10 nF and 100 nF. This capacitor should be placed close to the IC between pin 12 and pin 13.

13.2 Heatsink design

The standard application is stereo headphone single-ended with a 32 Ω load impedance to buffer (see Figure 9). The headphone amplifier can deliver a peak output current of 150 mA into the load.

For the SO16 envelope $R_{th(j-a)}$ = 105 K/W; the maximum sinewave power dissipation for T_{amb} = 25 °C is: $1.2\ \text{W} = \frac{150 - 25}{105}$

For T_{amb} = 60 °C the maximum total power dissipation is: $0.85\ \text{W} = \frac{150 - 60}{105}$

13.3 Test conditions

T_{amb} = 25 °C; unless otherwise specified: V_P = 3 V, f = 1 kHz, R_L = 32 Ω, Gain = 26 dB, low input mode, band-pass filter: 22 Hz to 30 kHz. The total harmonic distortion as a function of frequency was measured with low-pass filter of 80 kHz. The quiescent current has been measured without any load impedance.

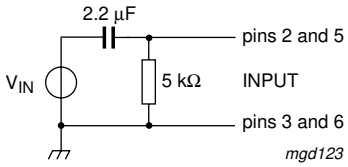
In applications with coupling capacitors towards the load, an electrolytic capacitor has to be connected to pin 4 (SVRR).

1. The graphs for the single-ended application have been measured with the application illustrated in Figure 9; input configuration for input mode low (Figure 4) and input configuration for input mode high (Figure 6).
2. The graphs for the BTL application ‘input mode low’ have been measured with the application circuit illustrated in Figure 11 and the input configuration illustrated in Figure 4.
3. The graphs for the line-driver application have been measured with the application circuit illustrated in Figure 13 and the input configuration illustrated in Figure 6; input mode high.

13.4 Input configurations

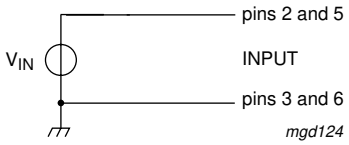
The IC can be applied in two ways, ‘input mode low’ and ‘input mode high’. This can be selected by the input mode at pin 8:

1. Input mode low: pin 8 floating: The DC level of the input pins has to be between 0 V and (V_P – 1.8 V). A DC path to ground is needed. The maximum output voltage is approximately 2.1 V (RMS). Input configurations illustrated in Figure 3 and Figure 4 should be used.
2. Input mode high: pin 8 is connected to V_P: This mode is intended for supply voltages > 6 V. It can deliver a maximum output voltage of approximately 6 V (RMS) at THD = 0.5 %. The DC voltage level of the input pins is ($0.5V_P$ + 0.6 V). Coupling capacitors are necessary. Input configurations illustrated in Figure 5 and Figure 6 should be used.



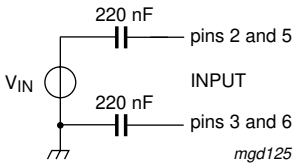
V_P < 6 V.

Fig 3. Input configuration; with input capacitor



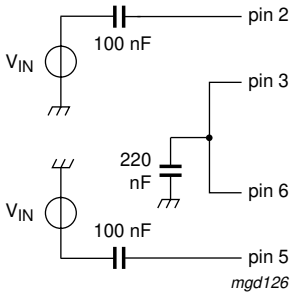
V_P < 6 V.

Fig 4. Input configuration; without input capacitor



V_P < 6 V.

Fig 5. Input configuration



At V_P < 6 V, combined negative inputs.

Fig 6. Input configuration

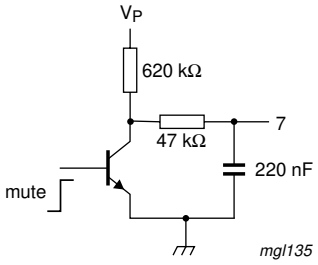


Fig 7. Soft mute

13.5 Standby/mute

1. The Standby mode (V_1 < 0.5 V) is intended for power saving purpose. Then the total quiescent current is < 10 μA.
2. To avoid 'pop-noise' during switch-on or switch-off the IC can be muted (V_7 < 0.5 V). This can be achieved by a 'soft-mute' circuit or by direct control from a microcontroller.

13.6 Application 1: SE with loudspeaker capacitor

The value of capacitor Cr influences the behavior of the Supply Voltage Ripple Rejection (SVRR) at low frequencies; increasing the value of Cr increases the performance of the SVRR; see Figure 8.

13.7 Application 2: SE to buffer (without loudspeaker capacitor)

This is the basic headphone application. The advantage of this application with respect to application 1, is that it needs only one external component (Cb) in the event of stability problems; see Figure 9.

13.8 Application 3: Improved SE to buffer (without loudspeaker capacitor)

This application is an improved configuration of application 2. The distinction between the two is connecting the loads in opposite phase. This lowers the average current through the SE buffer. It should be noted that a headphone cannot be used because the load requires floating terminals; see Figure 10.

13.9 Application 4: Bridge tied load mono amplifier

This configuration delivers four times the output power of the SE application with the same supply and load conditions. The capacitor Cr is not required; see Figure 11.

13.10 Application 5: Line driver application

The TDA8559T delivers a virtual rail-to-rail output voltage and is also usable in a low voltage environment, as a line driver. In this application the input needs a DC path to ground, input configurations illustrated in Figure 3 and Figure 4 should be used. The value of capacitor Cr influences the behavior of the SVRR at low frequencies; increasing the value of Cr increases the performance of the SVRR; see Figure 12.

13.11 Application 6: Line driver application

The TDA8559T delivers a virtual rail-to-rail output voltage. Because the input mode has to be high, the input configurations illustrated in Figure 5 and Figure 6 should be used. This application can also be used for headphone application, however, due to the limited output current and the limited output power at the headphone, series resistors have to be used between the output pins and the load; see Figure 13.

The value of capacitor Cr influences the behavior of the SVRR at low frequencies; increasing the value of Cr increases the performance of the SVRR.

13.12 Application 7: Line driver application

With the supply voltage connected to pin 15 it is possible to use the head amplifier above the maximum of 18 V to pin 16. The internal supply voltage will be reduced to a maximum of approximately 17 V.

This will be convenient in applications where the supply voltage is higher than 18 V, however an output voltage swing that reaches the higher supply voltage is not required. the input configurations illustrated in Figure 5 and Figure 6 should be used. This application can also be used for headphone applications. However, due to the limited output current, series resistors have to be used between the output pins and the load; see Figure 14.

13.13 Application diagrams

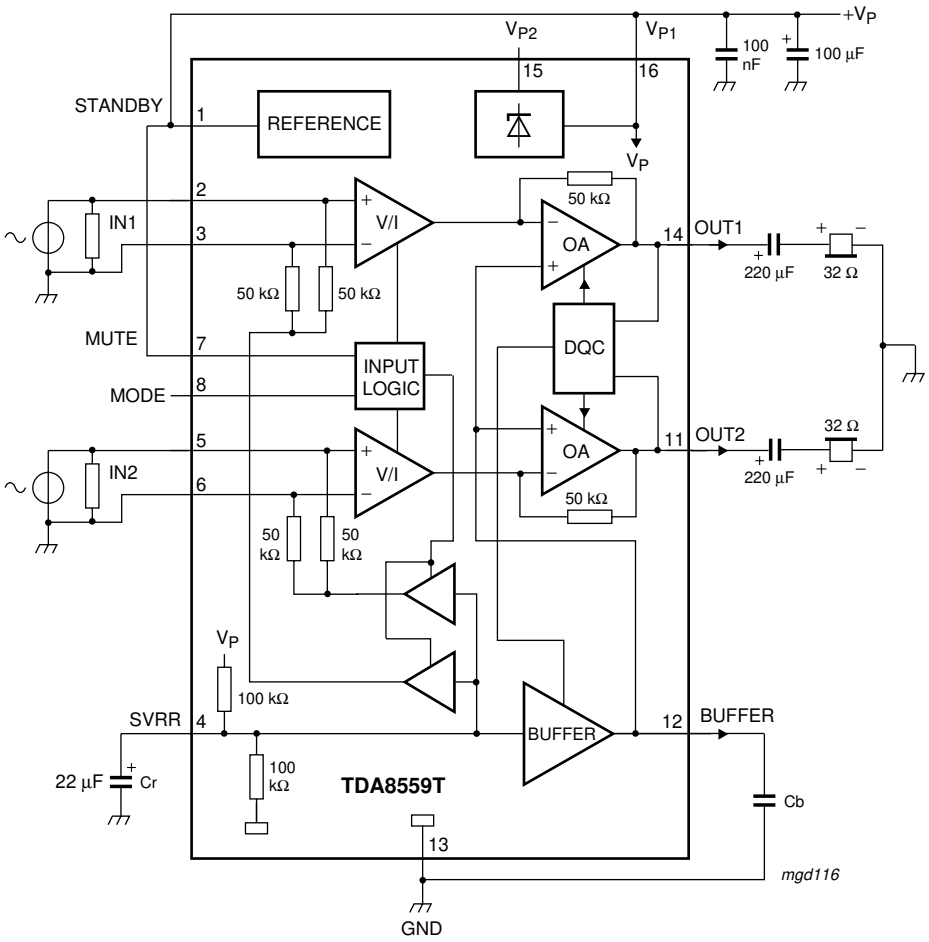


Fig 8. Application 1; single-ended with loudspeaker capacitor

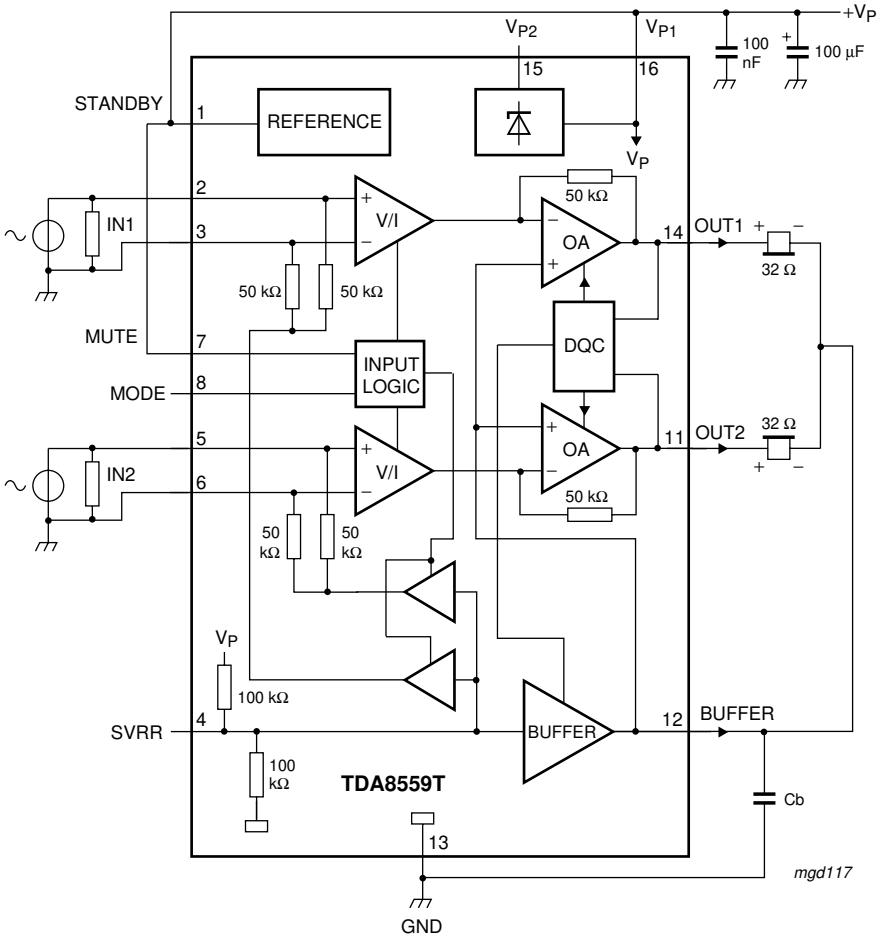


Fig 9. Application 2; single-ended to buffer (without loudspeaker capacitor)

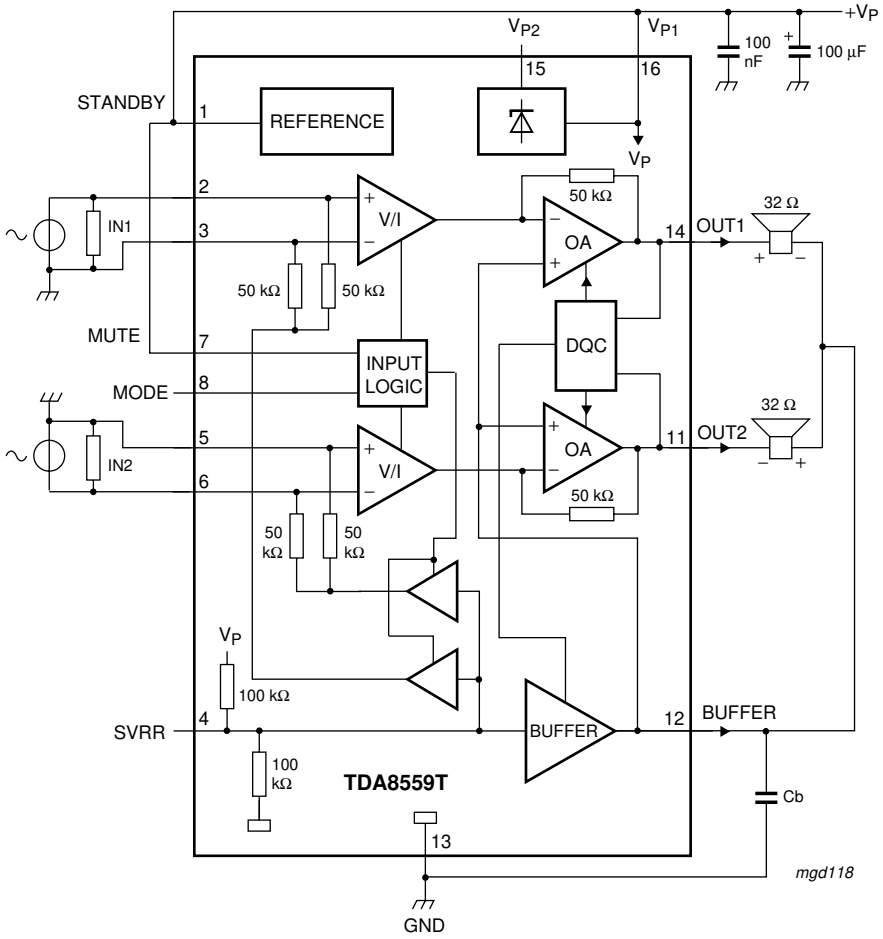


Fig 10. Application 3; improved single-ended to buffer (without loudspeaker capacitor)

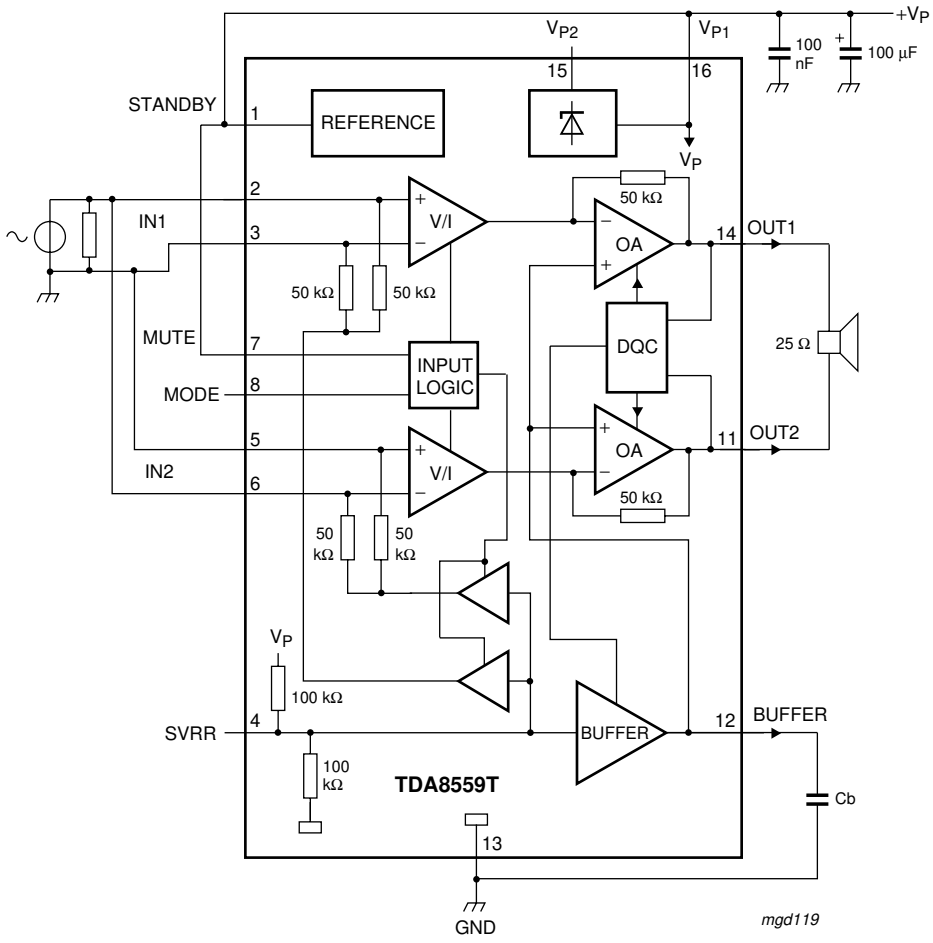
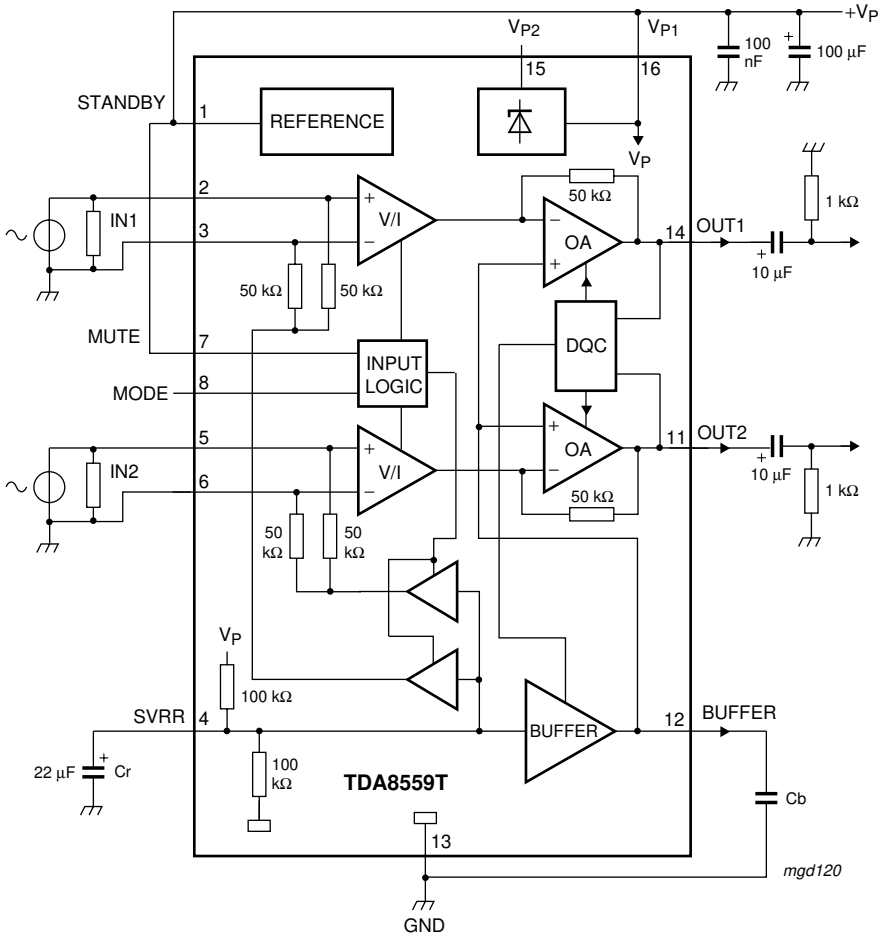
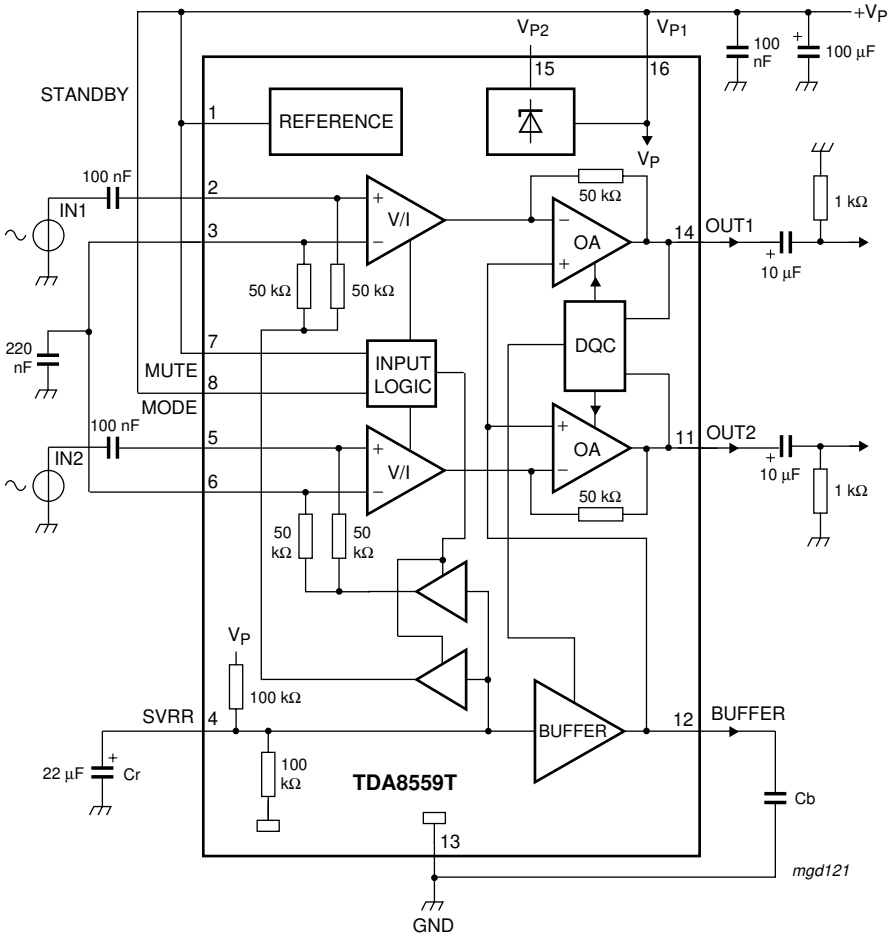


Fig 11. Application 4; BTL mono amplifier



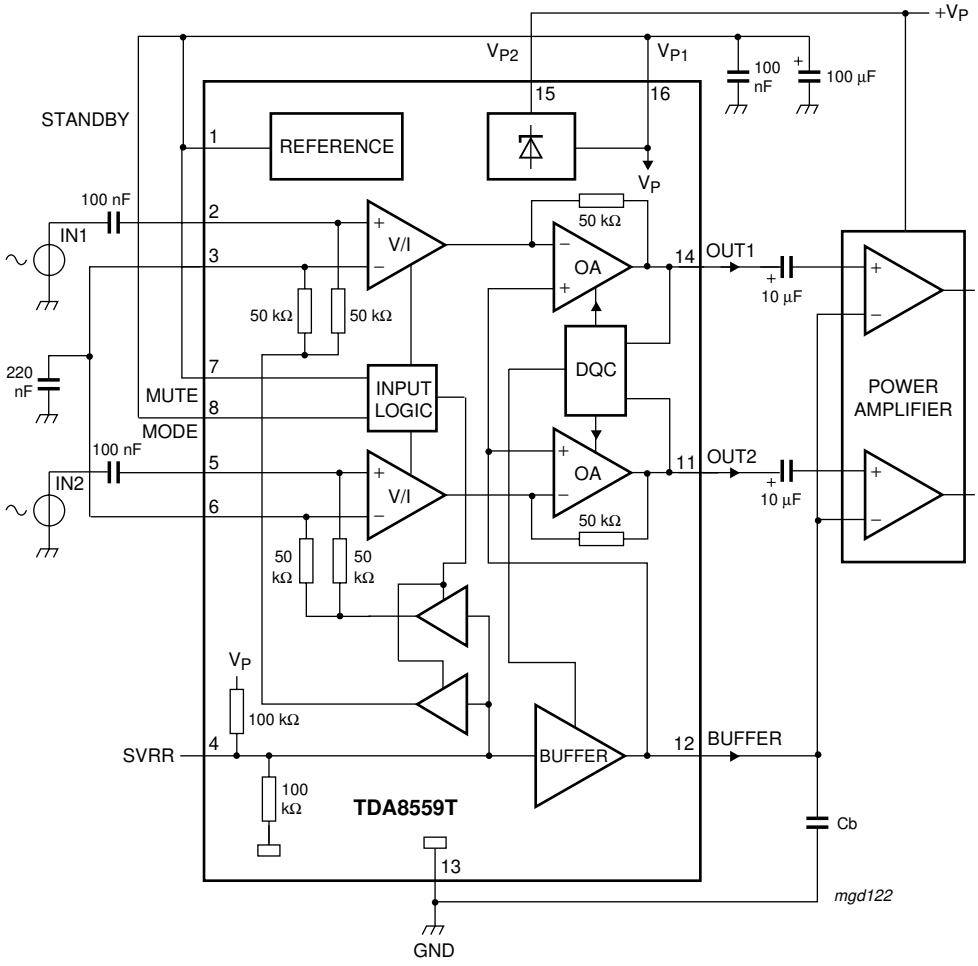
V_P = 1.9 V to 6 V.

Fig 12. Application 5; line driver application



V_P = 6 V to 18 V.

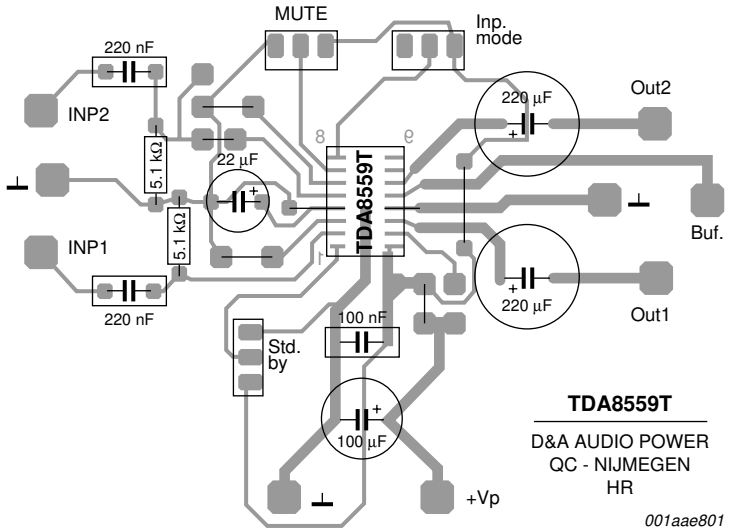
Fig 13. Application 6; line driver application



V_P = 6 V to 30 V.

Fig 14. Application 7; line driver application

13.14 Printed-circuit board layout

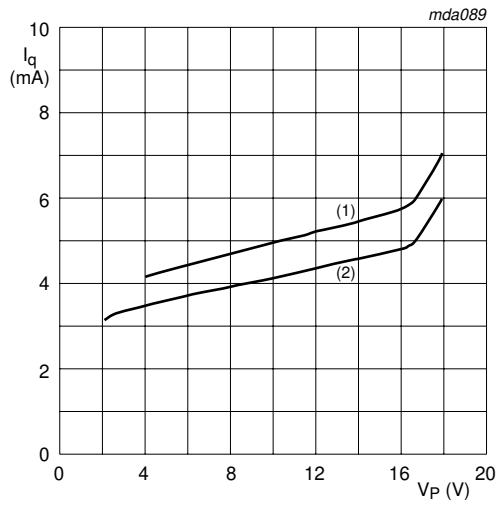


Top view component side.

Fig 15. Printed-circuit board layout

The Printed-Circuit Board (PCB) layout supports all applications as illustrated in Figure 8 to Figure 14. The PCB layout has been assembled for input configuration as shown in Figure 3, and output and supply configuration as shown in Figure 8 for a maximum supply voltage of 6 V.

13.15 Response curves for low input mode



(1) High mode.

(2) Low mode.

Fig 16. I_q as a function of V_P (stereo headphone)

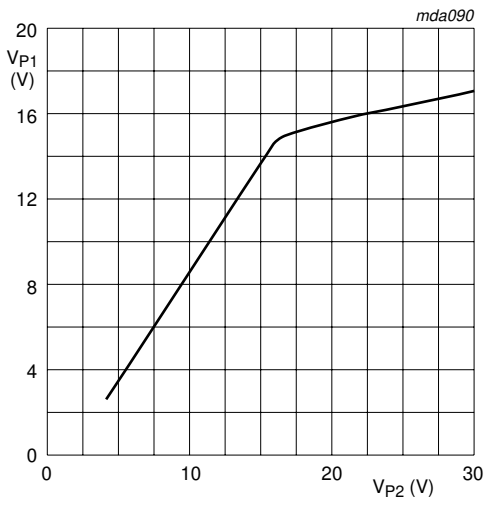
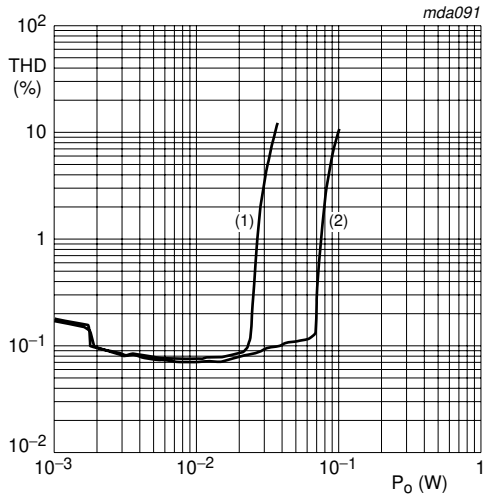


Fig 17. V_{P1} as a function of V_{P2} (stereo headphone)

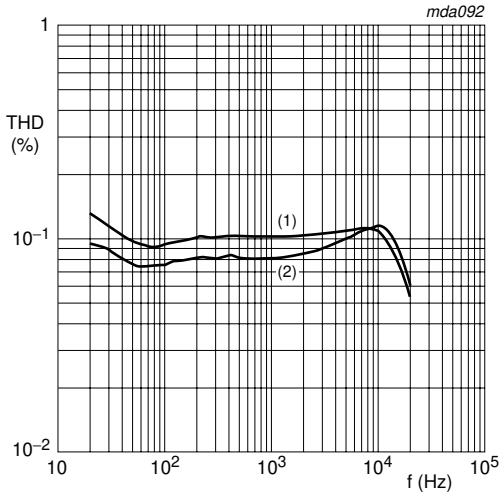


f = 1 kHz.

(1) V_P = 3 V, R_L = 32 Ω.

(2) V_P = 5 V, R_L = 32 Ω.

Fig 18. THD as a function of P_o (stereo headphone)

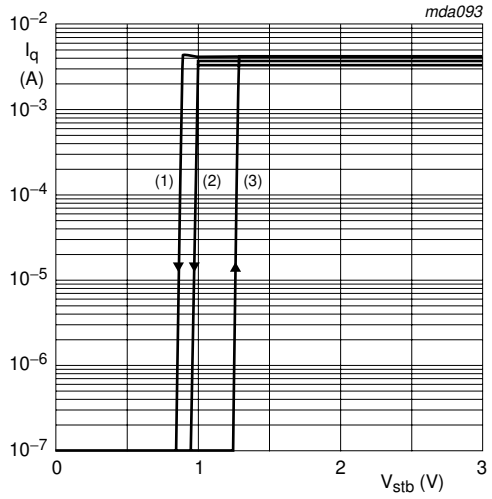


R_L = 32 Ω.

(1) V_P = 5 V, THD = 50 mW.

(2) V_P = 3 V, THD = 20 mW.

Fig 19. THD as a function of frequency (stereo headphone)

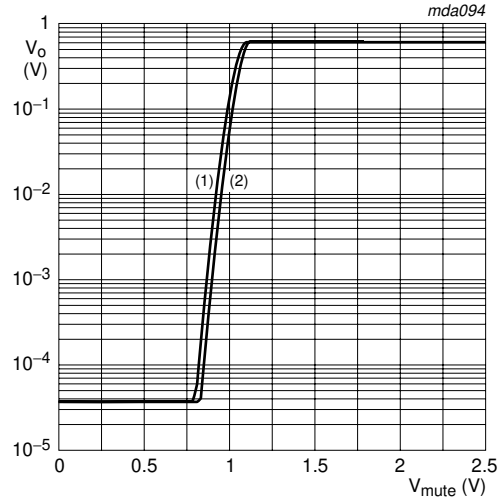


(1) V_P = 12 V.

(2) V_P = 3 V and 6 V.

(3) V_P = 3 V, 6 V and 12 V.

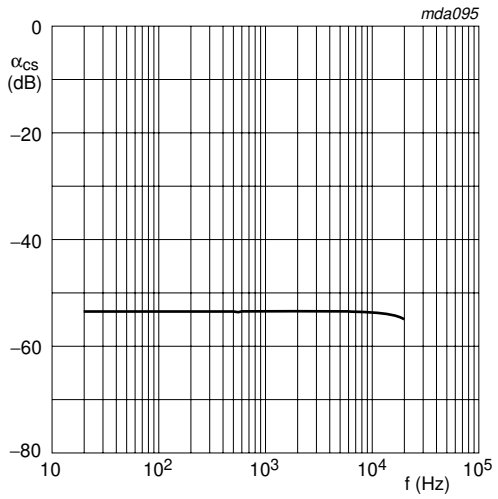
Fig 20. I_q as a function of V_{stb} (stereo headphone)



(1) V_P = 3 V.

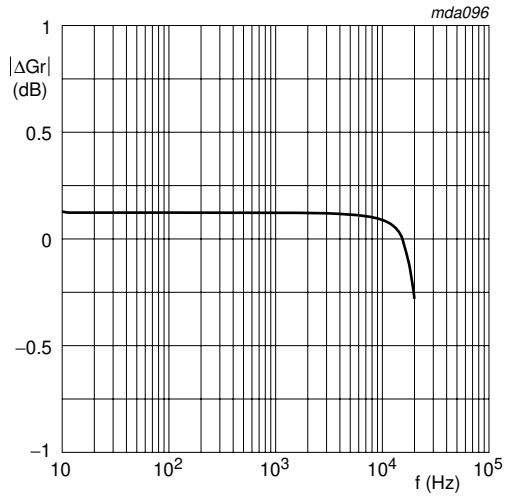
(2) V_P = 12 V.

Fig 21. V_o as a function of V_{mute} (stereo headphone)



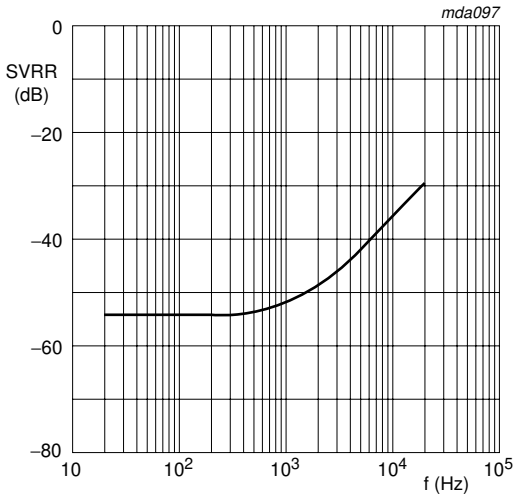
V_P = 3 V, V_i = 20 mV.

Fig 22. Channel separation as a function of frequency (stereo headphone)



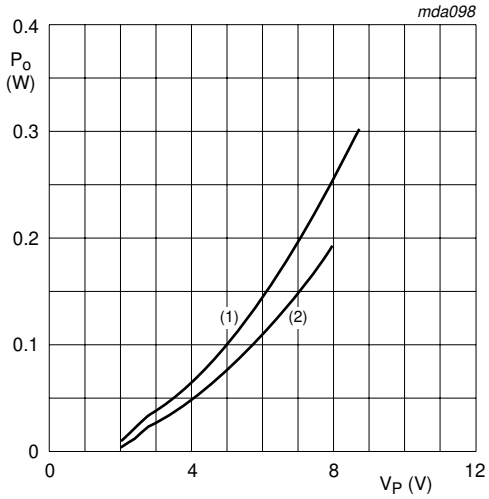
V_P = 3 V, V_i = 20 mV.

Fig 23. Channel unbalance as a function of frequency (stereo headphone)



V_P = 3 V, R_s = 0 Ω, V_r = 0.2 V (RMS).

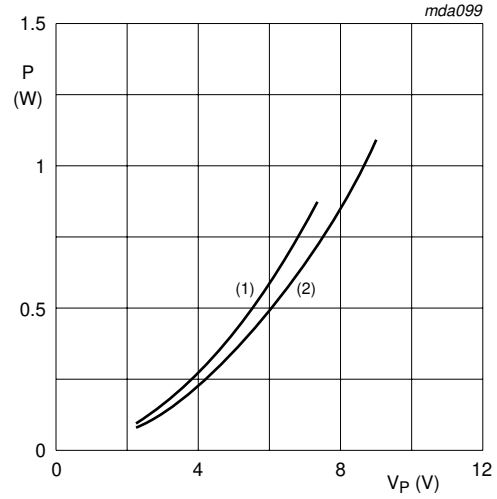
Fig 24. SVRR as a function of frequency (stereo headphone)



(1) R_L = 32 Ω, THD = 10 %.

(2) R_L = 32 Ω, THD = 0.5 %.

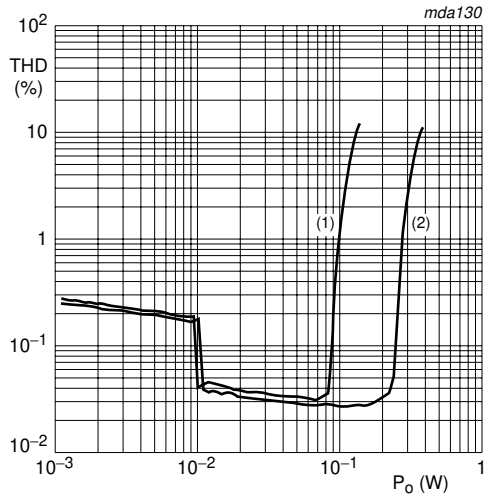
Fig 25. P_o as a function of V_P (stereo headphone)



(1) R_L = 25 Ω.

(2) R_L = 32 Ω.

Fig 26. Total worst case power dissipation as a function of supply voltage (SE) (stereo headphone)

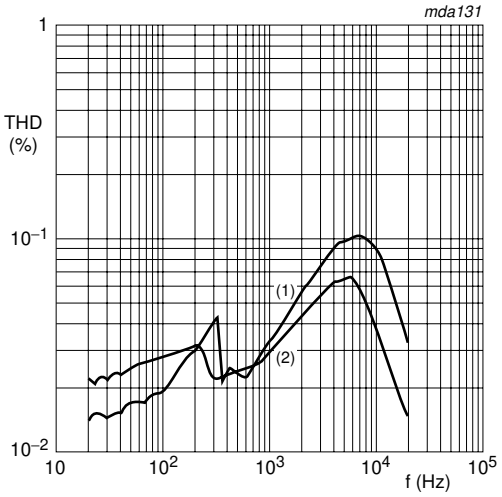


f = 1 kHz.

(1) V_P = 3 V, R_L = 25 Ω.

(2) V_P = 5 V, R_L = 25 Ω.

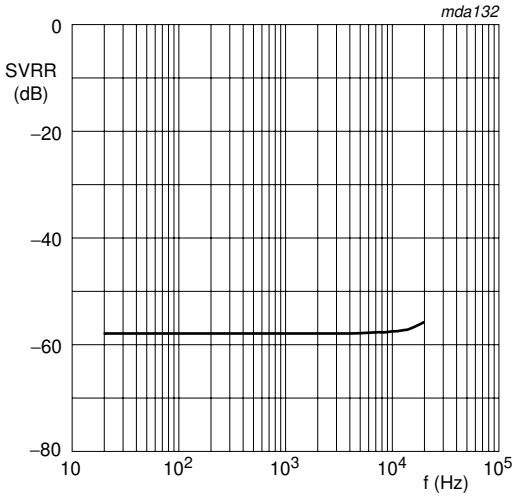
Fig 27. THD as a function of P_o (BTL mono)



(1) V_P = 3 V, R_L = 25 Ω, THD = 70 mW.

(2) V_P = 5 V, R_L = 25 Ω, THD = 150 mW.

Fig 28. THD as a function of frequency (BTL mono)



V_P = 3 V, R_s = 0 Ω, V_r = 0.2 V (RMS).

Fig 29. SVRR as a function of frequency (BTL mono)