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1. General description

The TDA8594 is a complementary quad Bridge Tied Load (BTL) audio power amplifier made in BCDMOS technology. It contains four independent amplifiers in BTL configuration. Through the I2C-bus, diagnosis of temperature warning and clipping level is fully programmable and the information available via two diagnostic pins is selectable. The status of each amplifier (output offset, load or no load, short-circuit or speaker incorrectly connected) can be read separately.

2. Features and benefits

2.1 General

- Operates in legacy mode (non I2C-bus) and I2C-bus mode (3.3 V and 5 V compliant)
- Three hardware-programmable I2C-bus addresses
- Drives 4 Ω or 2 Ω loads
- Speaker fault detection
- Independent short-circuit protection per channel
- Loss of ground and open V_P safe (with 200 mΩ series impedance and a supply decoupling capacitor of 2200 μF maximum)
- All outputs short-circuit proof to ground, supply voltage and across the load
- All pins short-circuit proof to ground
- Temperature-controlled gain reduction to prevent audio holes at high junction temperatures
- Low battery voltage detection
- Offset detection
- This part has been qualified in accordance with AEC-Q100

2.2 I2C-bus mode

- DC load detection: open-circuit, short-circuit and load present
- AC load (tweeter) detection
- During start-up, can detect which load is connected so the appropriate gain can be selected without audio pop
- Independently selectable soft mute of front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4)
- Programmable gain (26 dB and 16 dB) of front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4)

I²C-bus controlled 4 × 50 W power amplifier

- ■ Fully programmable diagnostic levels can be set:
  - ◆ Programmable clip detection: 2 %, 5 % or 10 %
  - ◆ Programmable thermal pre-warning
- ■ Selectable information on the DIAG and STB pins:
  - ◆ The STB pin can be programmed/multiplexed with second clip detection
  - ◆ Clip information of each channel can be directed separately to the DIAG pin or the STB pin
  - ◆ Independent enabling of thermal, clip or load fault detection (short across or to V_P or to ground) on DIAG pin

3. Quick reference data

Table 1.   Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	supply voltage	$R_L = 4 \ \Omega$	8	14.4	18	V
I_q	quiescent current	no load	-	270	400	mA
P_o	output power	$V_P = 14.4$ V				
		$R_L = 4 \ \Omega$; THD = 0.5 %	19	22	-	W
		$R_L = 4 \ \Omega$; THD = 10 %	26	28	-	W
		$R_L = 4 \ \Omega$; maximum power; $V_i = 2$ V (RMS) square wave	42	44	-	W
		$R_L = 2 \ \Omega$; maximum power; $V_i = 2$ V (RMS) square wave	70	75	-	W
THD	total harmonic distortion	$R_L = 4 \ \Omega$; f = 1 kHz; $P_o = 1$ W to 12 W	-	0.01	0.1	%
$V_{n(o)}$	output noise voltage	filter 20 Hz to 22 kHz; $R_S = 1$ kΩ				
		normal mode	-	45	65	μV
		line driver mode	-	22	29	μV

4. Ordering information

Table 2.   Ordering information

Type number	Package			
	Name	Description		Version
TDA8594J	DBS27P	plastic DIL-bent-SIL (special bent) power package; 27 leads (lead length 6.8 mm)		SOT827-1
TDA8594SD	RDBS27P	plastic rectangular-DIL-bent-SIL (reverse bent) power package; 27 leads (row spacing 2.54 mm)		SOT878-1

5. Block diagram
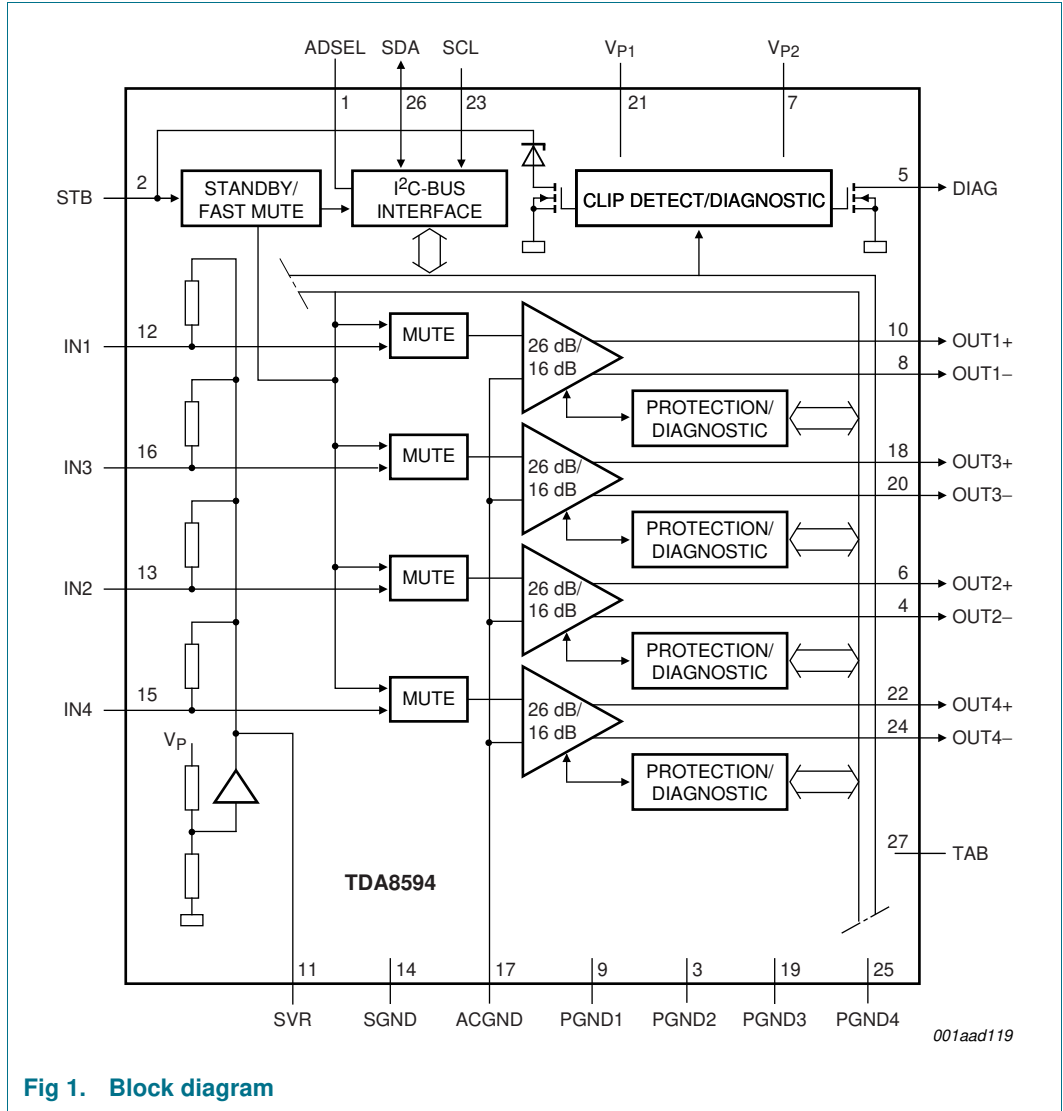
Fig 1. Block diagram

6. Pinning information

6.1 Pinning

ADSEL 1
STB 2
PGND2 3
OUT2− 4
DIAG 5
OUT2+ 6
V_{P2} 7
OUT1− 8
PGND1 9
OUT1+ 10
SVR 11
IN1 12
IN2 13
SGND 14
IN4 15
IN3 16
ACGND 17
OUT3+ 18
PGND3 19
OUT3− 20
V_{P1} 21
OUT4+ 22
SCL 23
OUT4− 24
PGND4 25
SDA 26
TAB 27

TDA8594

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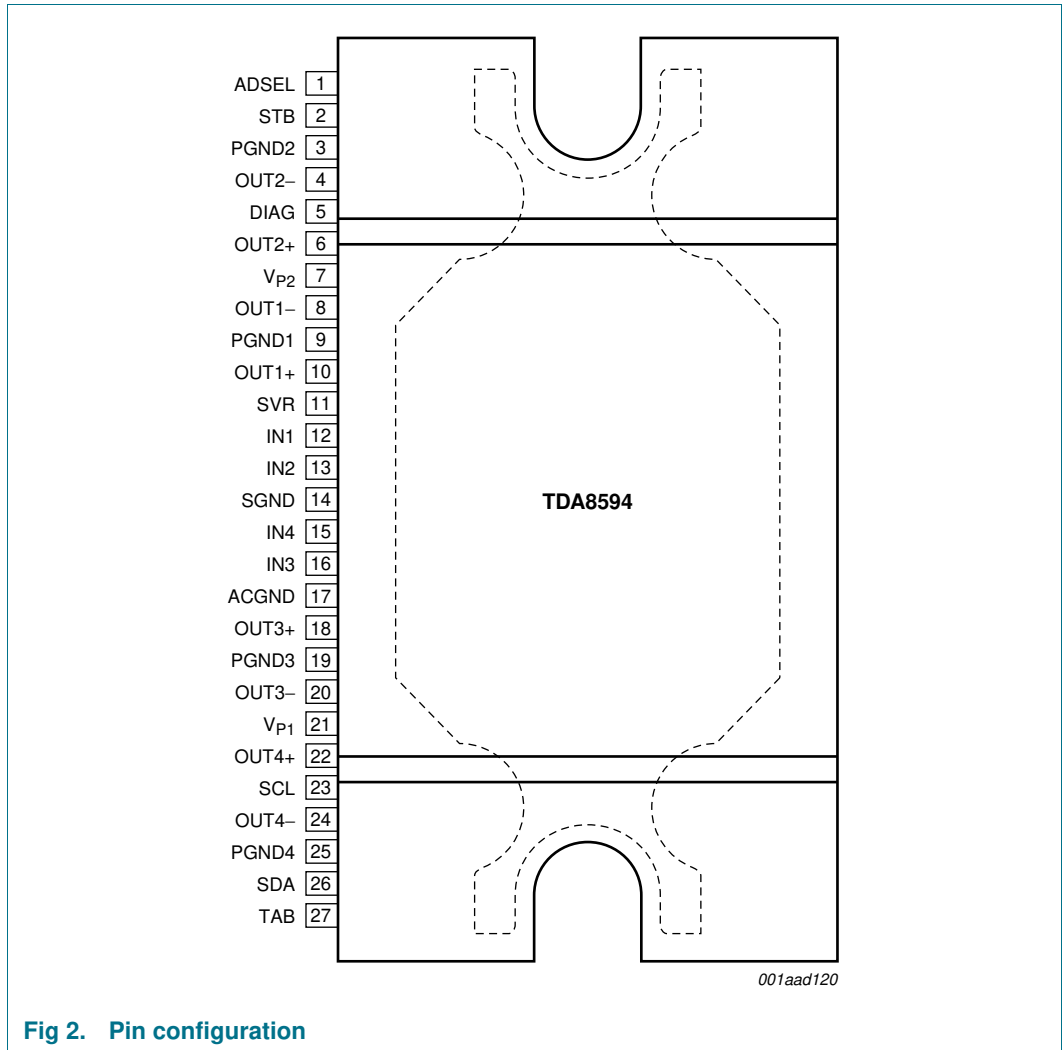
Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
ADSEL	1	I²C-bus address select input
STB	2	standby (I²C-bus mode) or mode pin (legacy mode); programmable second clip indicator
PGND2	3	power ground channel 2
OUT2−	4	negative channel 2 output
DIAG	5	diagnostic/clip detection output
OUT2+	6	positive channel 2 output
V_{P2}	7	supply voltage 2

Table 3.   **Pin description** …*continued*

Symbol	Pin	Description
OUT1−	8	negative channel 1 output
PGND1	9	power ground channel 1
OUT1+	10	positive channel 1 output
SVR	11	half supply filter capacitor
IN1	12	channel 1 input
IN2	13	channel 2 input
SGND	14	signal ground
IN4	15	channel 4 input
IN3	16	channel 3 input
ACGND	17	AC ground input
OUT3+	18	positive channel 3 output
PGND3	19	power ground channel 3
OUT3−	20	negative channel 3 output
V_{P1}	21	supply voltage 1
OUT4+	22	positive channel 4 output
SCL	23	I²C-bus clock input
OUT4−	24	negative channel 4 output
PGND4	25	power ground channel 4
SDA	26	I²C-bus data input/output
TAB	27	heatsink connection, must be connected to ground

To keep the output pins on the front side, special reverse bending is applied.

7. Functional description

The TDA8594 is a complementary quad BTL audio power amplifier made in BCDMOS technology. It contains four independent amplifiers in BTL configuration (see Figure 1). Through the I²C-bus, the diagnostic functions of temperature level and clip level are fully programmable and the information to be shown on the two diagnostic pins can be selected. The status of each amplifier (output offset, load or no load, short-circuit or speaker incorrectly connected) can be read separately. The TDA8594 is protected against overvoltage, short-circuit, over-temperature, open ground and open V_P connections.

Three different I²C-bus addresses are selected with an external resistor connected to the ADSEL pin. If the ADSEL pin is short-circuit to ground, the TDA8594 operates in legacy mode. In this mode, no I²C-bus is needed and the function of the STB pin will change from two-level (Standby mode and On mode) to a three-level pin (Standby mode, On mode and mute).

7.1 Input stage

The input stage is a high-impedance pseudo-differential input stage. The negative inputs of the four channels are combined on the ACGND pin. For the best performance on supply voltage ripple rejection and pop noise, the capacitor connected to the ACGND pin must be four times the value of the input capacitor (or as close to the value as possible).

7.2 Output stage

The output stage of each amplifier channel consists of two PMOS power transistors and two NMOS transistors in a BTL configuration. The process used is the BCDMOS process with an isolated substrate, Silicon On Insulator (SOI) process, which has almost no parasitic components and therefore prevents latch-up.

7.3 Distortion (clip) detection

If the output of the amplifier starts clipping to the supply voltage or to ground, the output will become distorted. If the distortion per channel exceeds a selectable threshold (2 %, 5 % or 10 %), one of the two diagnostic pins (DIAG pin or STB pin) will be activated. To be able to detect if, for instance, the front channels (channel 1 and channel 3) or rear channels (channel 2 and channel 4) are clipping, the clip information can be directed per channel to the DIAG pin or the STB pin. It is possible to have only the clip information on the diagnostic pins by disabling the temperature and load information on the DIAG pin. In this mode the temperature and load protection are still functional but can only be read via the I²C-bus.

7.4 Output protection and short-circuit operation

When a short-circuit to ground, V_P or across the load occurs on one or more outputs of an amplifier, only the amplifier with the short-circuit is switched off. The channel that has a short-circuit and the type of short-circuit can be read-back via the I²C-bus. If the DIAG pin is enabled for load fault information (IB2[D4] = 0) the DIAG pin will be pulled LOW. After 16 ms the amplifier will be switched on again and, if the short-circuit conditions still occur, the amplifier will be switched off.

The 16 ms cycle will reduce the dissipation. To prevent audible distortion, the amplifier channel with the short-circuit can be disabled via the I²C-bus.

7.5 SOAR protection

The output transistors are protected by Safe Operating ARea (SOAR) protection. The TDA8594 has a two-stage SOAR protection:

- If the differential output voltage across the load is less than 1 V, and the current through the load is more than 4 A, the amplifier channel will be switched off for 16 ms. To prevent incorrect switch-off with an inductive load or very high input signals, the condition ($V_o < 1$ V and $I_L > 4$ A) must exist for more than 300 μs.
- If the differential output voltage across the load is more than 1 V, and the current through the load is more than 8 A, the amplifier channel will be switched off for 16 ms.

7.6 Speaker protection

To prevent damage of the speaker when one side of the speaker is connected to ground, a missing current protection is implemented. When in one channel the current in the high side power is not equal to the current in the low side power, a fault condition is assumed and the channel will be switched off. The speaker protection will be activated under the following conditions:

- $V_o < 1.75$ V and $I_{missing(det)} > 1$ A for 80 μs
- $V_o > 1.75$ V and $I_{missing(det)} > 3$ A for 80 μs

7.7 Standby and mute operation

The function of the STB pin is different in legacy mode and I²C-bus mode.

7.7.1 Legacy mode (pin ADSEL connected to ground)

The function of the STB pin will change from standby/operating to standby/mute/operating and the amplifier will start directly when the STB is put into mute or operating mode. Mute operating is controlled via an internal timer (20 ms) to minimize mute-on pops. When the STB pin is switched directly from operating to standby, first the fast mute will be activated (switching to mute within 100 μs) and then the amplifier will shut-down.

7.7.2 I²C-bus mode

When the STB pin is LOW, the total quiescent current is low, and the I²C-bus lines will not be loaded.

When the STB pin is switched HIGH, the TDA8594 is put in operating condition and will perform a Power-On Reset (POR), which results in a LOW level DIAG pin. The TDA8594 will start up when instruction bit IB1[D0] is set. Bit D0 will also reset the 'power-on reset occurred' bit (DB2[D7]) and releases the DIAG pin.

The soft mute and fast mute can be activated via the I²C-bus. The soft mute can be activated independently for the front channels (channel 1 and channel 3) and rear channels (channel 2 and channel 4), and mutes the audio in 20 ms. The fast mute activates the mute for all channels at the same time and mutes the audio in 0.1 ms. Releasing the mute after a fast mute will be by a soft un-mute of approximately 20 ms.

When the STB pin is switched to Standby mode and the amplifier has started, first the fast mute will be activated and then the amplifier will shut-down. For instance, during an engine start, it is possible to fully mute the amplifiers within 100 μs by switching the STB pin to zero.

7.8 Start-up and shut-down sequence

To prevent the amplifier producing switch-on or switch-off pop noise, the capacitor on the SVR pin is used for smooth start-up and shut-down. Increasing the value of the SVR capacitor will mean a longer start-up and shut-down time. The amplifier output voltage is charged to half the supply voltage minus 1.4 V in mute condition, independent of the I²C-bus mute settings in I²C-bus mode or STB voltage in legacy mode. The last 1.4 V, where the output will reach half the supply voltage, is used to release the mute if the I²C-bus bits were set to mute off (IB2[D2:D0] = 000; V_{STB} > 6.5 V in legacy mode), or will stay in mute when the bits were set to mute (2.6 V < V_{STB} < 4.5 V in legacy mode).

When the amplifier is switched off by pulling the STB pin LOW, the amplifier is first muted (fast mute) and then the capacitor on the SVR pin is discharged. With an SVR capacitor of 22 μF, the standby current has reached 1 second after the STB pin is switched to zero (see Figure 3, Figure 4, Figure 5 and Figure 6).

The start-up and shut-down pop can be further decreased by activating the low pop mode. When the low pop mode is enabled (IB2[D3] = 0), the output voltage rise from ground level during start-up will be slower (see Figure 5). This will decrease the pop even more but will increase the start-up time.

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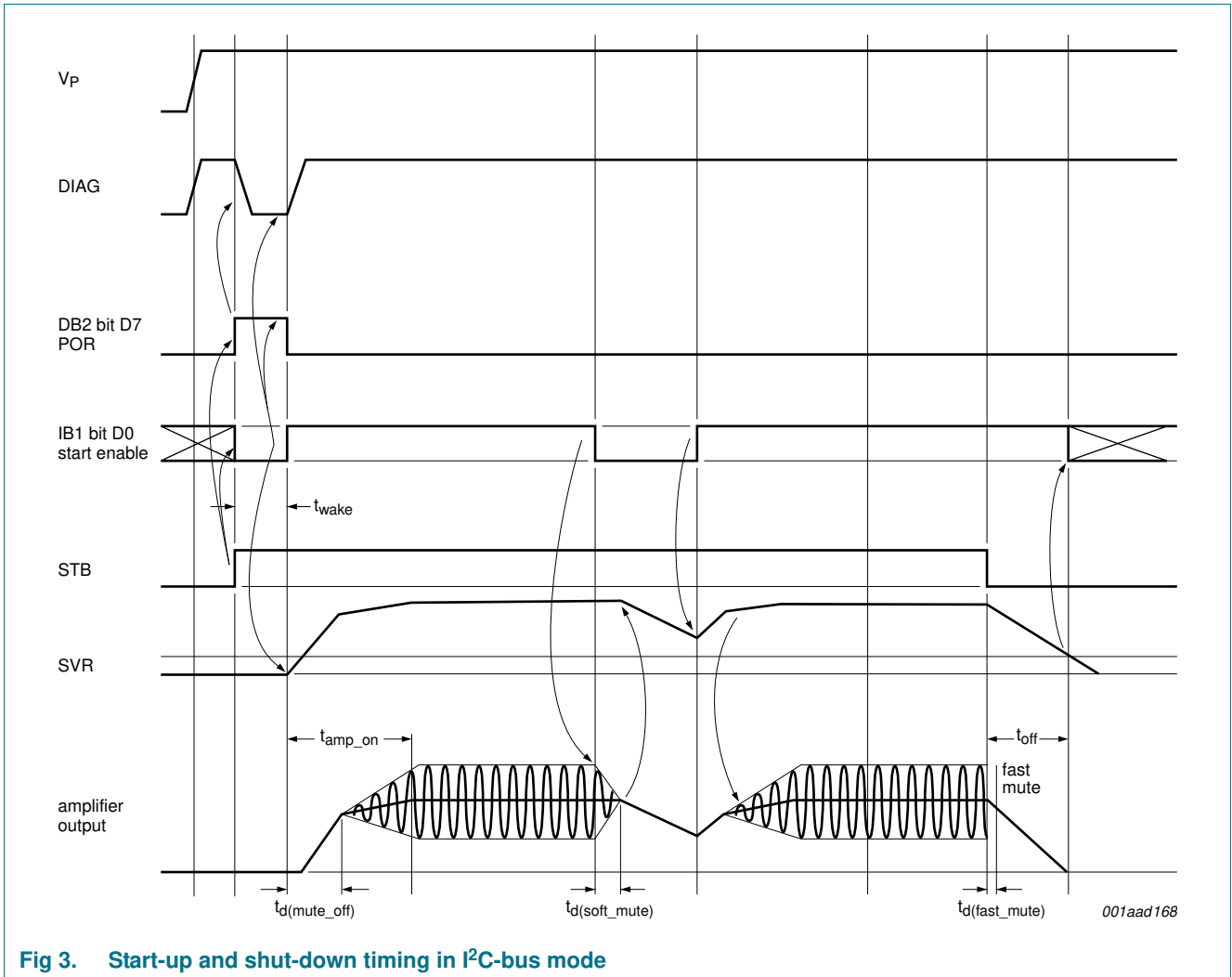
Fig 3.   Start-up and shut-down timing in I²C-bus mode

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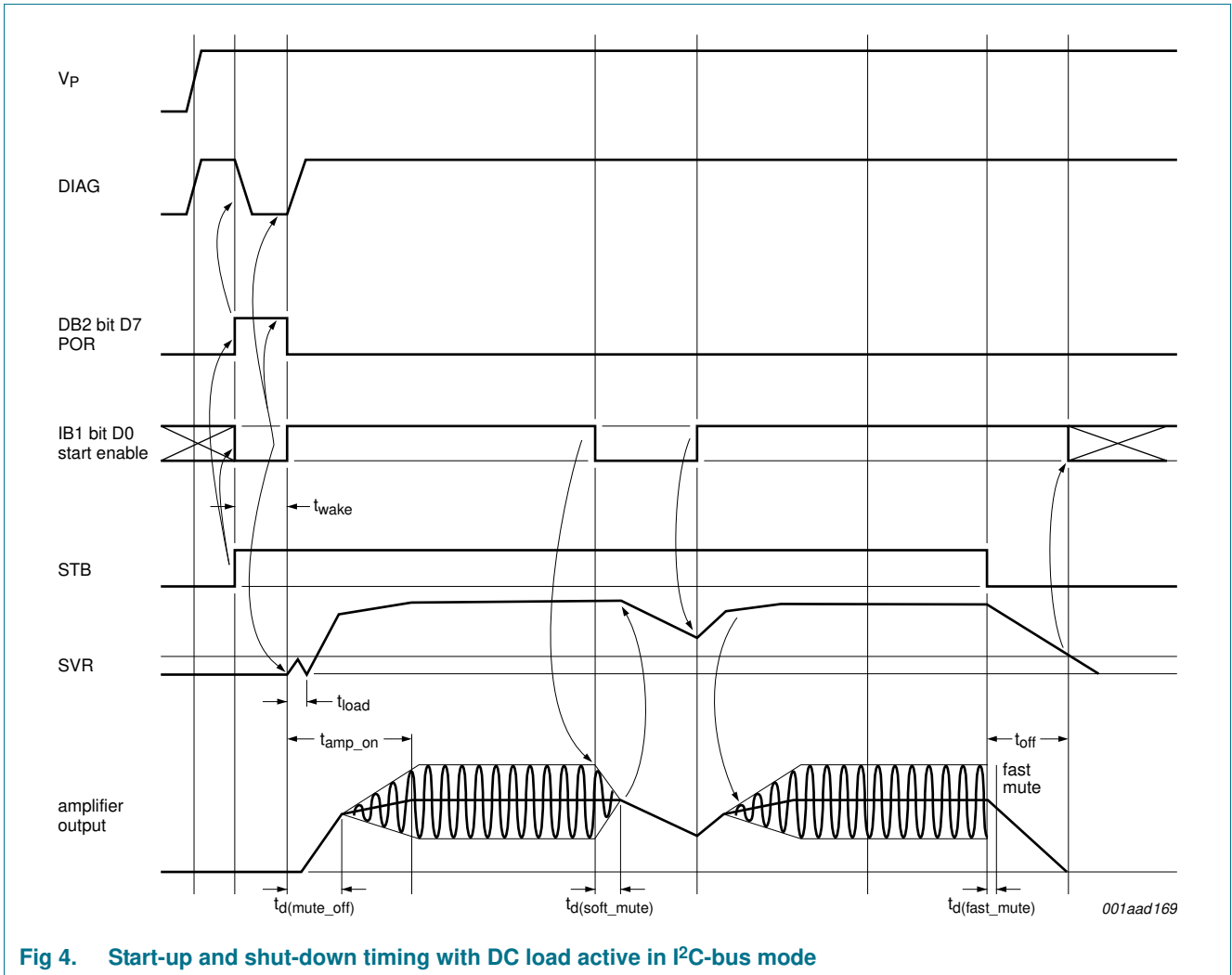
Fig 4. **Start-up and shut-down timing with DC load active in I²C-bus mode**

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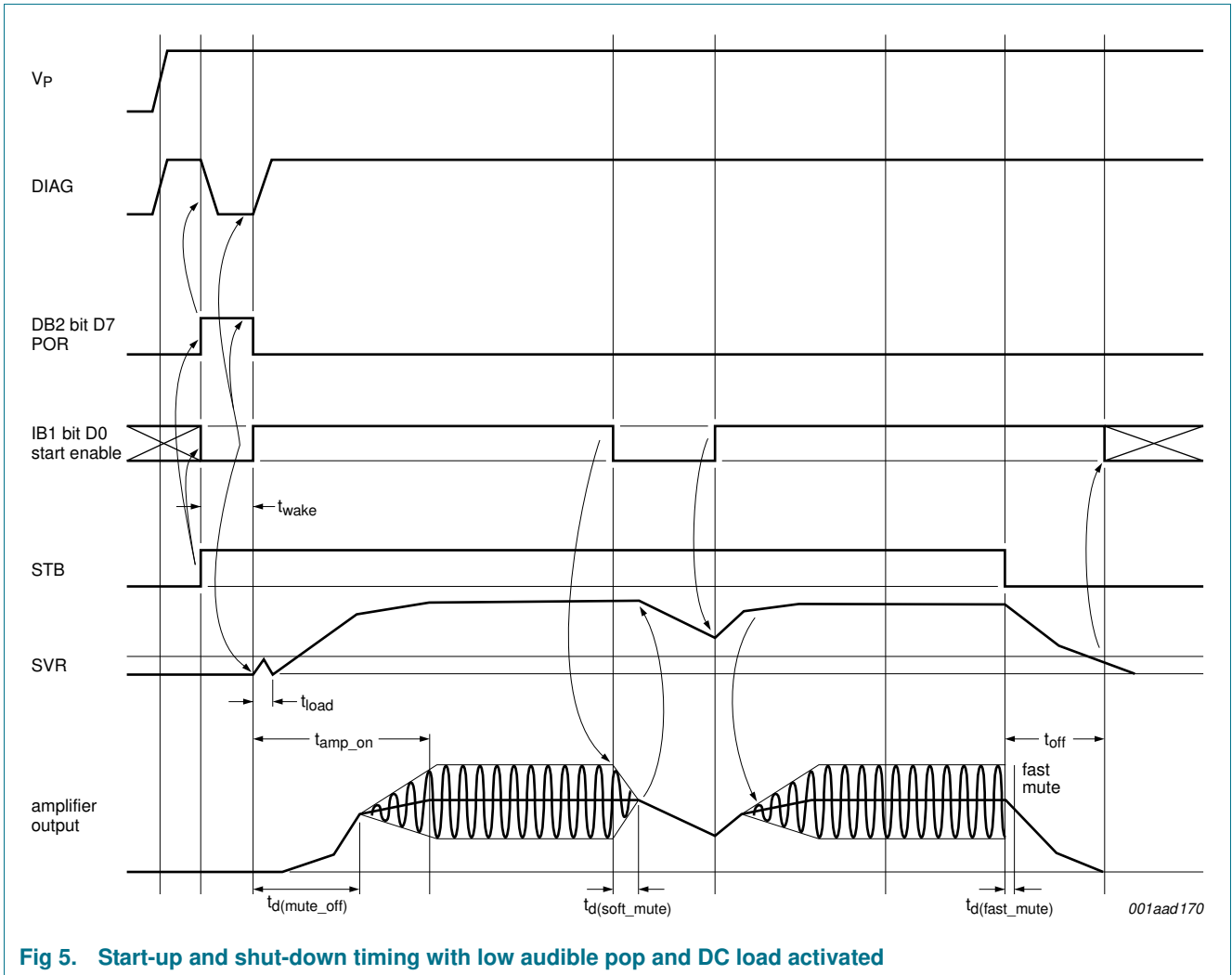
Fig 5. Start-up and shut-down timing with low audible pop and DC load activated

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Fig 6. Start-up and shut-down timing in legacy mode

7.9 Power-on reset and supply voltage spikes

If in I²C-bus mode the supply voltage drops below 5 V (see Figure 9), the content of the I²C-bus latches cannot be guaranteed and the power-on reset will be activated. All latches are reset, the amplifier is switched off and the DIAG pin 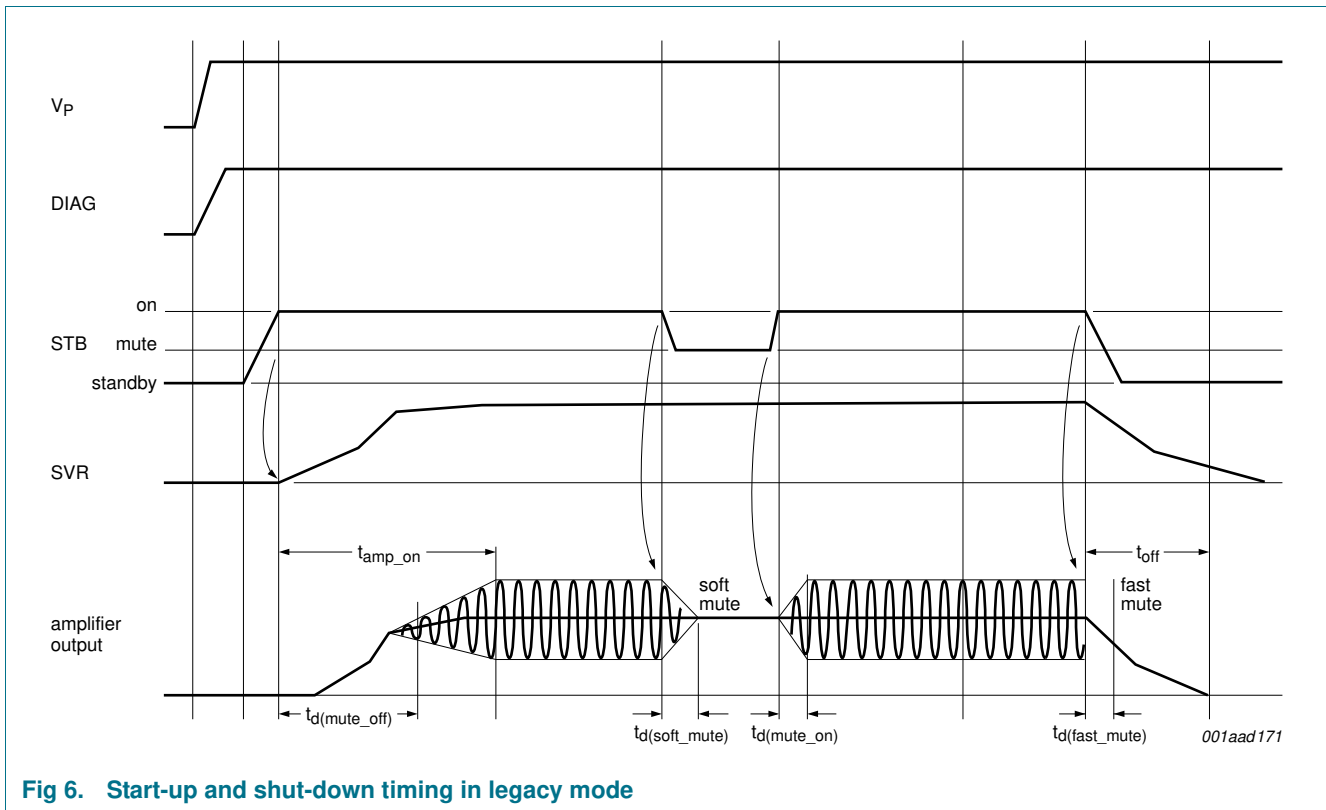is pulled LOW to indicate that a power-on reset has occurred (bit DB2[D7]). When IB1[D0] is set, the power-on flag is reset, the DIAG pin will be released and the amplifier will start up.

In legacy mode a supply voltage drop below 5 V will switch off the amplifier and the DIAG pin will not be pulled LOW.

7.10 Engine start and low voltage operation

The DC output voltage of the amplifier (V_O) is set to half of the supply voltage and is related to the voltage on the SVR pin (see Figure 7; $V_O = V_{SVR} - 1.4$ V). A capacitor is connected on the SVR pin to suppress the ripple on the power supply.

If the supply voltage drops, for instance, during an engine start, the output follows slowly due to the SVR capacitor. The headroom voltage is the voltage needed for good operation of the amplifier and is defined as $V_{hr} = V_P - V_O$ (see Figure 7). If the headroom voltage becomes lower than the headroom protection threshold of 1.6 V, the headroom protection is activated to prevent pop noise at the output. This protection first activates the fast mute and then discharges the capacitors on the SVR and ACGND pins to generate more headroom for the amplifier (see Figure 8).

When the SVR capacitor has discharged, the amplifier starts up again if the V_P voltage is above the low V_P mute threshold, typically 7.5 V. Below the low V_P mute threshold, the outputs of the amplifier remain low. In I^2C-bus mode, a supply voltage drop below $V_{P(reset)}$, typically 5 V, results in setting bit DB2[D7] and not starting of the amplifiers but waiting for an I^2C-bus command to start.

The amplifier prevents audio pops during engine start. To prevent pops on the output caused by the application during an engine start (for instance tuner regulator out of regulation), the STB pin can be made zero when an engine start is detected. The STB pin activates the fast mute and disturbances at the amplifier inputs are suppressed.

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(1) Headroom voltage $V_{hr} = V_P - V_O$.

(2) Steady state output voltage $V_O = V_{SVR} - 1.4$ V.

(3) Headroom protection threshold = $V_O + 1.6$ V.

Fig 7.   Low headroom protection
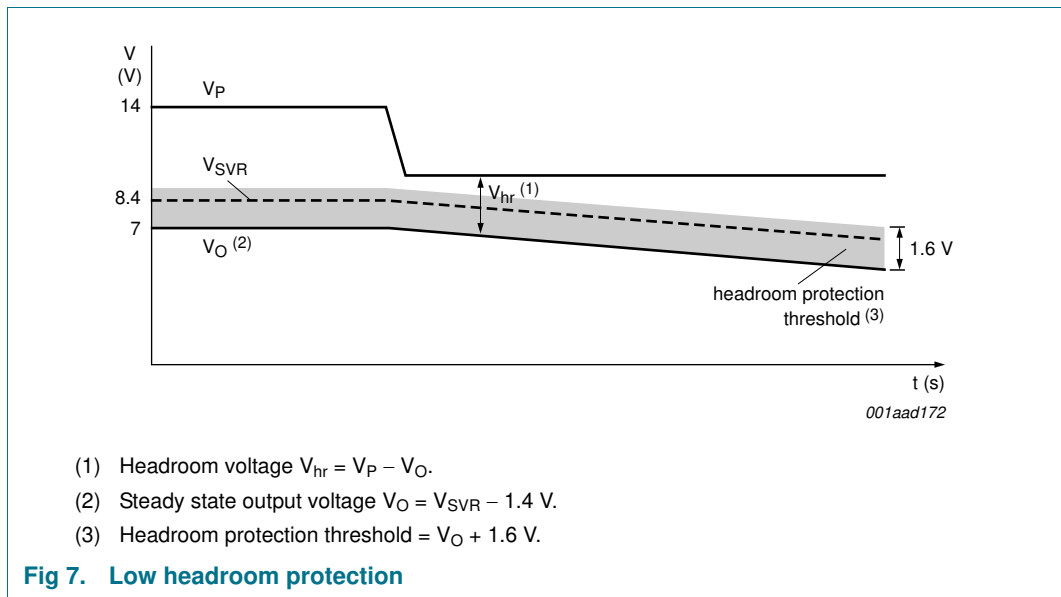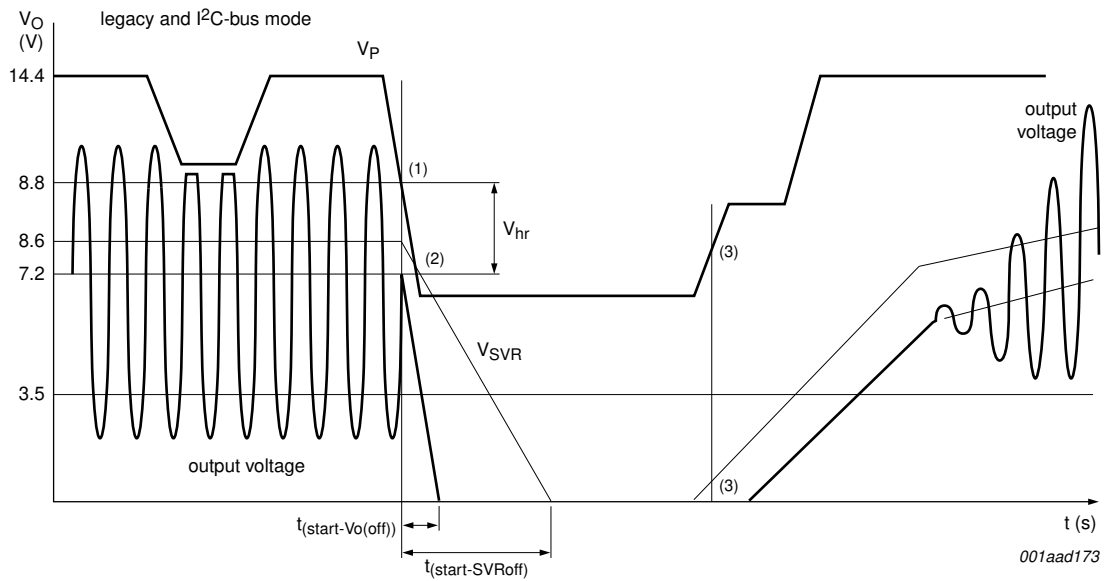
(1) Headroom protection activated:

a) Fast mute

b) Discharge of SVR.

(2) Low V_P mute activated.

(3) Low V_P mute released.

Fig 8. **Low V_P behavior; legacy and I2C-bus modes**

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(1) Low V_P mute activated.

(2) V_{POR}: V_P level at which Power-On Reset (POR) is activated.

Fig 9.   Low V_P behavior; I²C-bus mode only
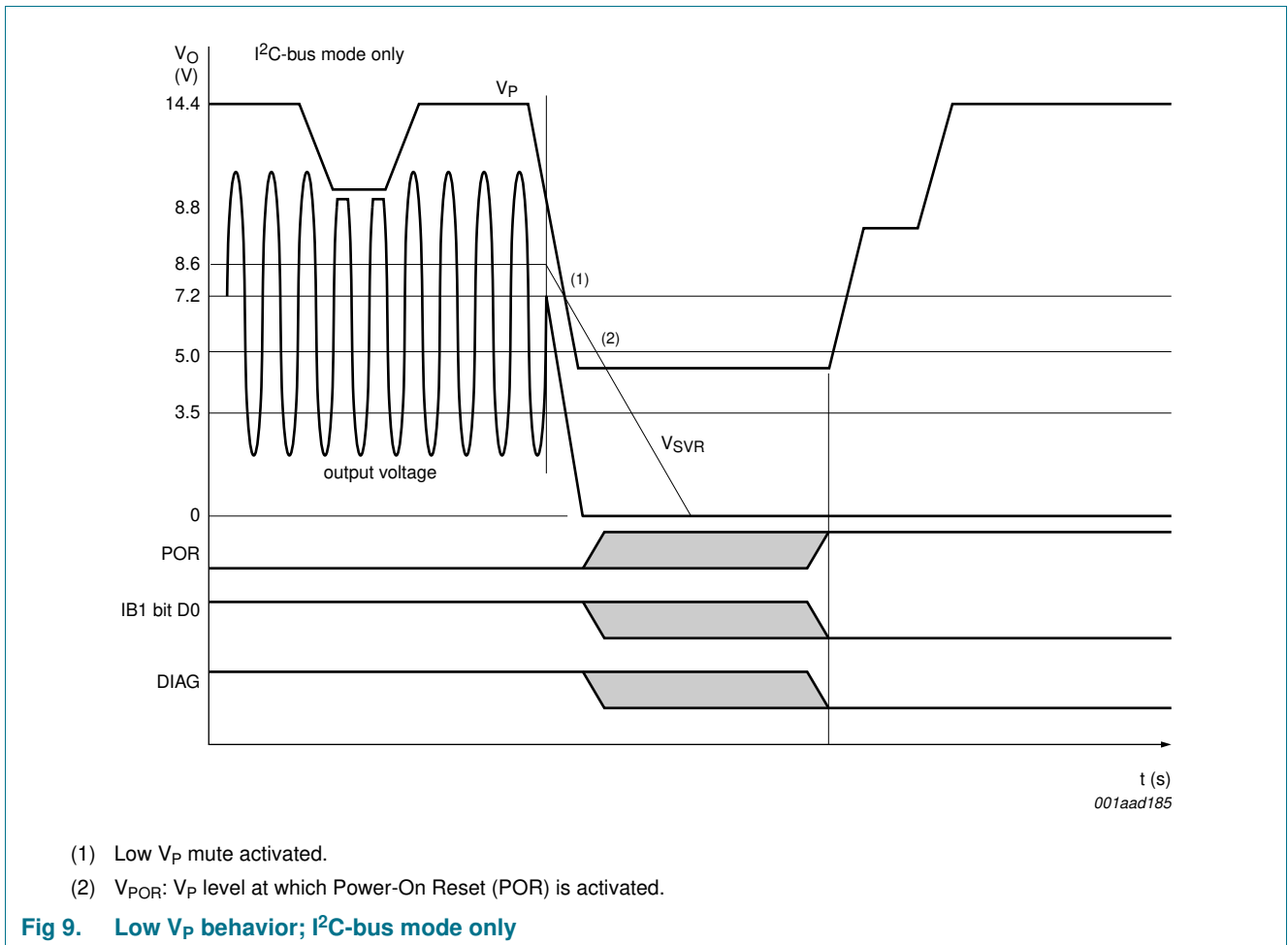
7.11 Overvoltage and load dump protection

When the battery voltage V_P is higher than 22 V, the amplifier stage will be switched to high-impedance. The TDA8594 is protected against load dump voltage with supply voltage up to 50 V.

7.12 Thermal pre-warning and thermal protection

If the average junction temperature reaches a level that is adjustable via the I²C-bus, selected with IB3[D4], the pre-warning will be activated resulting in a LOW level on pin DIAG (if selected) and can be read out via the I²C-bus. The default setting for the thermal pre-warning is IB3[D4] = 0 setting the warning level at 145 °C. In legacy mode the thermal pre-warning is set at 145 °C.

If the temperature increases further, the temperature controlled gain reduction will be activated for all four channels to reduce the output power (see Figure 10). If this does not reduce the average junction temperature, all four channels will be switched off at the absolute maximum temperature T_{off}, typical 175 °C.
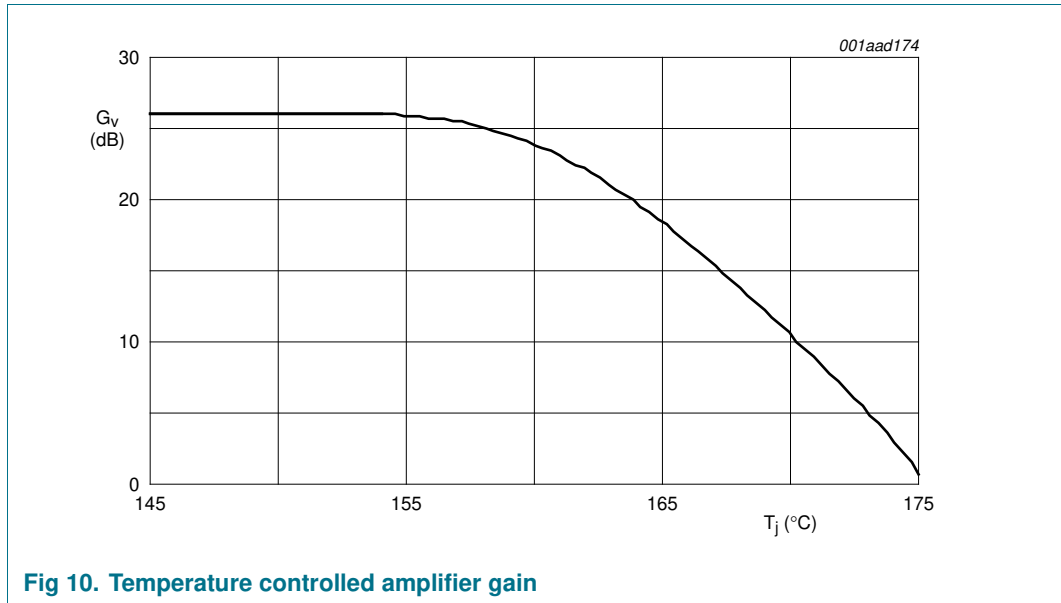
Fig 10. Temperature controlled amplifier gain

7.13 Diagnostics

Diagnostic information can be read via the I²C-bus, and can also be available on the DIAG pin or on the STB pin. The DIAG pin has both fixed information (power-on reset occurred, low battery and high battery) and, via the I²C-bus, selectable information (temperature, load fault and clip). This information will be seen at the DIAG pin as a logic OR. In case of a failure, the DIAG pin remains LOW and the failure information can be read from the microprocessor via the I²C-bus (the DIAG pin can be used as a microprocessor interrupt to minimize I²C-bus traffic). When the failure is removed, the DIAG pin will be released.

To have full control over the clipping information, the STB pin can be programmed as a second clip detection pin. The clip detection level can be selected for all channels at once. It is possible to select whether the clip information is available on the DIAG pin or on the STB pin for each channel separately. It is, for instance, possible to distinguish between clipping of the front and the rear channels.

Diagnostic information selection possibilities are shown in Table 4.

Table 4.   Diagnostic information availability

Diagnostic information	I²C-bus mode		Legacy mode
	DIAG pin	**STB pin**	**DIAG pin**
POR	after power-on reset, DIAG pin will remain LOW until amplifier has been started	no	no
Low battery	yes	no	yes
Clip detection	can be enabled per channel	can be enabled per channel	yes, fixed level for all channels on 2 %
Temperature pre-warning	can be enabled	no	yes, pre-warning level is 145 °C
Short	can be enabled	no	yes
Speaker protection (missing current)	can be enabled	no	yes

Table 4.   **Diagnostic information availability** *…continued*

Diagnostic information	I²C-bus mode		Legacy mode
	DIAG pin	**STB pin**	**DIAG pin**
Offset detection	no	no	no
Load detection	no	no	no
Overvoltage	yes	no	yes

7.14 Offset detection

The offset detection can be performed with no input signal (for instance when the digital signal processor is in mute after a start-up) or with an input signal. In I²C-bus mode, if an I²C-bus read of the output offset is performed, the I²C-bus latches DBx[D2] will be set. When the amplifier BTL output voltage is within a window with a threshold of 1.75 V typical, the latches DBx[D2] are reset and setting is disabled. If, for instance, after 1 second an I²C-bus read is performed again and the offset bits are still set, the output has not crossed the offset threshold during the last 1 second (see Figure 11). This can mean the applied frequency is below 1 Hz (I²C-bus read interval = 1 s) or an output offset of more than 1.75 V is present.
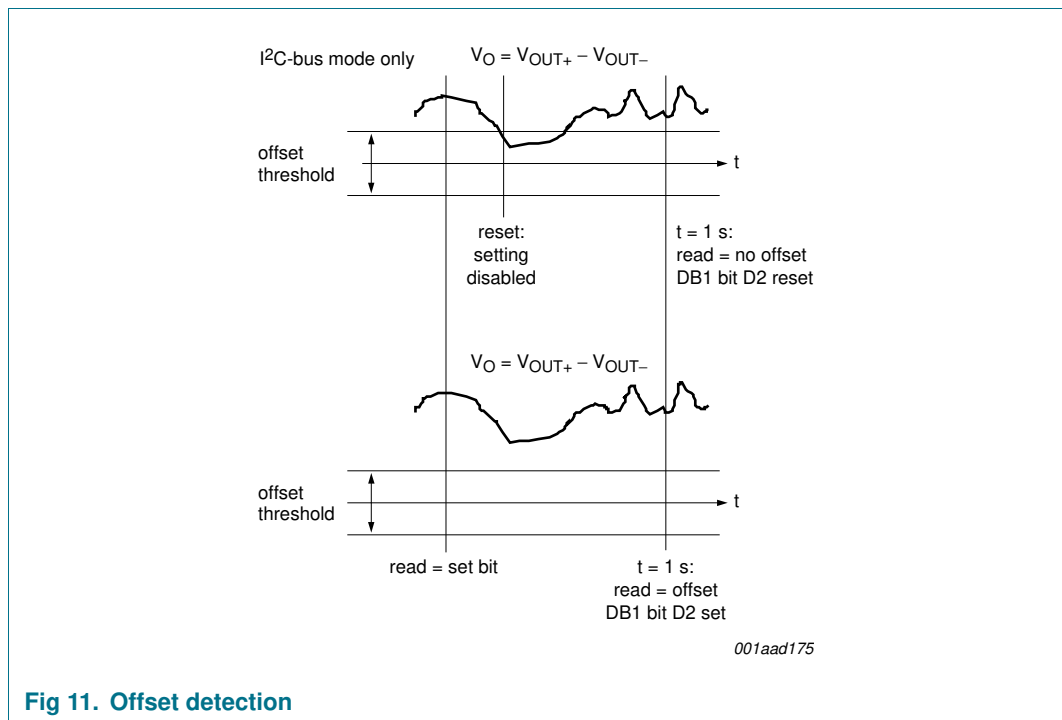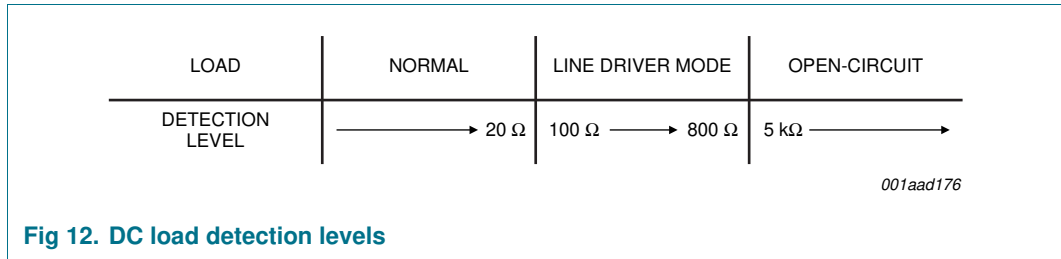

Fig 11. Offset detection

7.15 DC load detection

When the DC load detection is enabled with IB1[D1], a DC offset is slowly applied at the output of the amplifiers during the start-up cycle and the load currents are measured. Different load levels will be detected to differentiate between normal load, line driver load or open load.

Fig 12. DC load detection levels

If the amplifier is used as line driver and the external booster has an input impedance of more than 100 Ω and less than 800 Ω (DC-coupled), the DC load bits will contain DBx[D5:D4] = 10, independent of the gain setting (see Table 5).

Table 5.   DC load detection

DC load bits		Meaning (when IB1[D2] = 0)
DBx[D5]	**DBx[D4]**	
0	0	normal load
1	0	line driver load
1	1	open load
0	1	not valid

By reading the I²C-bus bits the microprocessor can determine, after the start-up of the amplifier, whether a speaker or an external booster is connected.

Depending on these bits, the amplifier gain can be selected, 26 dB for normal mode or 16 dB for line driver mode. If the gain select is performed when the amplifier is muted, the gain select will be pop free.

The DC load bits are combined with the AC load bits and are only valid when the AC load detection is disabled. When the AC load detection is enabled (IB1[D2] = 1), the bits DBx[D4] will show the content of the AC load detection. When the AC load detection is disabled again, bit DBx[D4] will show the content of the DC load measurement, which was stored during the AC load measurement. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection.

7.16 AC load detection

The AC load detection, enabled with IB1[D2] = 1, is used to detect if AC-coupled speakers, for example tweeters, are connected correctly during assembly. The detection is audible because a sine wave of a certain frequency (e.g. 19 kHz) needs to be applied to the inputs of the amplifier. The output voltage over the load impedance will generate an amplifier current. If the amplifier peak current triggers a 460 mA (peak) threshold detector three times, the AC load detection bit will be set. A three 'threshold cross' counter is used to prevent false AC load detection when switching the input signal on or off.

An AC-coupled speaker will reduce the impedance at the output of the amplifier in a certain frequency band. The presence of an AC-coupled speaker can be determined using 460 mA (peak) and 230 mA (peak) threshold current detection. For instance, at an output voltage of 2 V (peak) the total impedance must be less than 4 Ω to detect the AC-coupled load, or more than 8 Ω to guarantee only a DC connection is detected.

The interpretation of line driver and normal mode DC load bit settings for AC load detection is shown in Table 6.

Table 6.   AC load detection

DBx[D4]	Meaning (when IB1[D2] = 1)
0	no AC load detected
1	AC load detected

When bit IB1[D2] = 1, the AC load detection is enabled. The AC load detection can only be performed after the amplifier has completed its start-up cycle and will not conflict with the DC load detection.

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(1) $I_{th(o)det(load)AC}$ < 230 mA (no load detection level)

(2) $I_{th(o)det(load)AC}$ > 460 mA (load detection level)
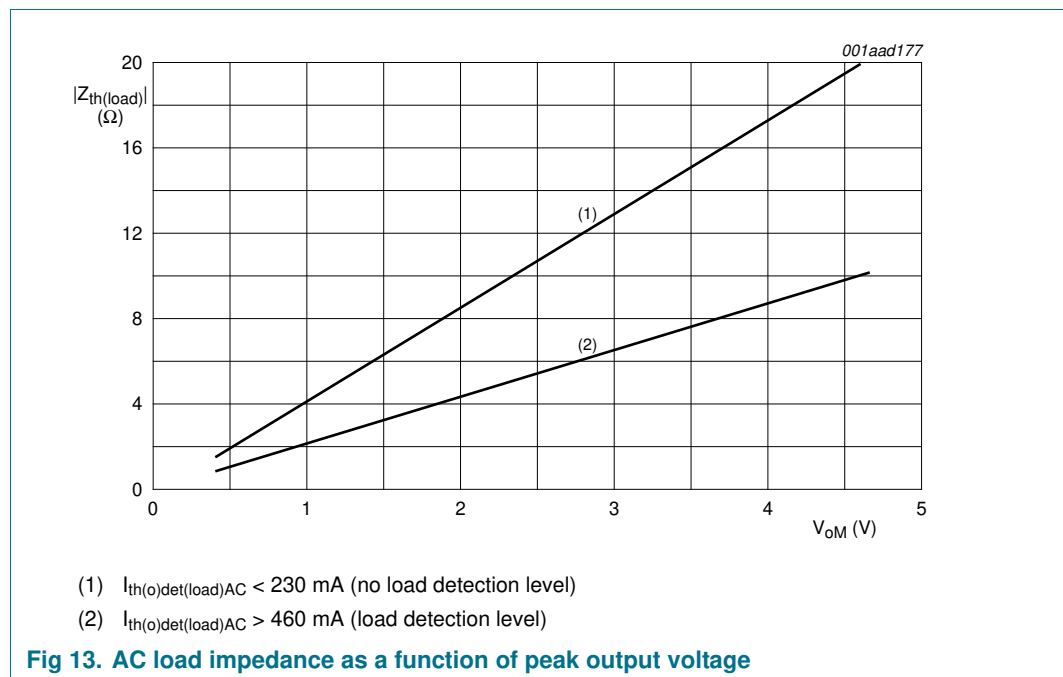
Fig 13. AC load impedance as a function of peak output voltage

7.17 I²C-bus diagnostic readout

The diagnostic information of the amplifier can be read via the I²C-bus. The I²C-bus bits are set on a failure and will be reset with the I²C-bus read command. Even when the failure is removed, the microprocessor will know what was wrong by reading the I²C-bus. The consequence of this procedure is that old information is read during the I²C-bus readout. Most actual information will be gathered after two successive read commands.

The DIAG pin will give actual diagnostic information (when selected). When a failure is removed, the DIAG pin will be released instantly, independently of the I²C-bus latches.

8. I²C-bus specification

Table 7.   TDA8594 hardware address select

Pin ADSEL	A6	A5	A4	A3	A2	A1	A0	R/W̄
Open	1	1	0	1	1	0	0	0 = write to TDA8594
								1 = read from TDA8594
51 kΩ to ground	1	1	0	1	1	0	1	0 = write to TDA8594
								1 = read from TDA8594
10 kΩ to ground	1	1	0	1	1	1	1	0 = write to TDA8594
								1 = read from TDA8594
Ground	no I²C-bus; legacy mode							

Fig 14. Definition of START and STOP conditions

Fig 15. Bit transfer

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I²C-BUS WRITE

To stop the transfer, after the last acknowledge (A)
a STOP condition (P) must be generated

I²C-BUS READ

To stop the transfer, the last byte must not be acknowledged
and a STOP condition (P) must be generated

001aac649

☐ : generated by master (microcontroller)
☐ : generated by slave
S : START
P : STOP
A : acknowledge
NA : not acknowledge
R/W̅ : read / write

Fig 16. I²C-bus read and write modes

8.1 Instruction bytes

I²C-bus mode:

- If bit R/W̅ = 0, the TDA8594 expects three instruction bytes; IB1, IB2 and IB3
- After a power-on reset, all instruction bits are set to zero.

Legacy mode:

- All bits equal to zero define the setting, with the exception of bit IB1[D0] which is ignored; see Table 8.

Table 8.   Instruction byte IB1

Bit	Description
D7	don't care
D6	channel 3 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D5	channel 1 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin

Table 8.   Instruction byte IB1 *…continued*

Bit	Description
D4	channel 4 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D3	channel 2 clip information on DIAG or STB pin
	0 = clip information on DIAG pin
	1 = clip information on STB pin
D2	AC load detection enable
	0 = AC load detection disabled
	1 = AC load detection enabled; DBx[D4] bits not available for DC load detection
D1	DC load detection enable
	0 = DC load detection disabled
	1 = DC load detection enabled
D0	amplifier start enable
	0 = amplifier not enabled, DIAG pin will remain LOW
	1 = amplifier will start up, power-on occurred (DB2[D7] will be reset) and DIAG pin will be released

Table 9.   Instruction byte IB2

Bit	Description
D7 and D6	clip detection level
	00 = clip detection level 2 %
	01 = clip detection level 5 %
	10 = clip detection level 10 %
	11 = clip detection level disabled
D5	temperature information on DIAG pin
	0 = temperature information on DIAG pin
	1 = no temperature information on DIAG pin
D4	load fault information (shorts, missing current) on DIAG pin
	0 = fault information on DIAG pin
	1 = no fault information on DIAG pin
D3	low pop (slow start) enable
	0 = low pop enabled
	1 = low pop disabled
D2	soft mute channel 1 and channel 3 (mute delay 20 ms)
	0 = no mute
	1 = mute
D1	soft mute channel 2 and channel 4 (mute delay 20 ms)
	0 = no mute
	1 = mute

Table 9. Instruction byte IB2 *…continued*

Bit	Description
D0	fast mute all amplifier channels (mute delay 100 μs)
	0 = no mute
	1 = mute

Table 10. Instruction byte IB3

Bit	Description
D7	don't care
D6	amplifier channel 1 and channel 3 gain select
	0 = 26 dB
	1 = 16 dB
D5	amplifier channel 2 and channel 4 gain select
	0 = 26 dB
	1 = 16 dB
D4	temperature pre-warning level
	0 = warning level on 145 °C
	1 = warning level on 122 °C
D3	disable channel 3
	0 = channel 3 enabled
	1 = channel 3 disabled
D2	disable channel 1
	0 = channel 1 enabled
	1 = channel 1 disabled
D1	disable channel 4
	0 = channel 4 enabled
	1 = channel 4 disabled
D0	disable channel 2
	0 = channel 2 enabled
	1 = channel 2 disabled

8.2 Data bytes

I²C-bus mode:

- If bit R/$\overline{W}$ = 1, the TDA8594 sends four data bytes to the microprocessor: DB1, DB2, DB3, and DB4

- All bits except DB1[D7] and DB3[D7] are latched.

- All bits except DBx[D4] and DBx[D5] are reset after a read operation. Bit DBx[D2] is set after a read operation; see Section 7.14

- For explanation of AC and DC load detection bits; see Section 7.15 and Section 7.16.

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Table 11.   Data byte DB1

Bit	Description
D7	temperature pre-warning
	0 = no warning
	1 = junction temperature too high
D6	speaker fault channel 2 (missing current)
	0 = no missing current
	1 = missing current
D5 and D4	channel 2 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning
	0 = no AC load
	1 = AC load detected
	if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 2 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 2 output offset
	0 = no output offset
	1 = output offset
D1	channel 2 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 2 short to ground
	0 = no short to ground
	1 = short to ground

Table 12.   Data byte DB2

Bit	Description
D7	power-on reset and amplifier status
	0 = amplifier on
	1 = power-on reset has occurred; amplifier off
D6	speaker fault channel 4 (missing current)
	0 = no missing current
	1 = missing current

Table 12.   Data byte DB2 *…continued*

Bit	Description
D5 and D4	channel 4 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning
	0 = no AC load
	1 = AC load detected
	if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 4 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 4 output offset
	0 = no output offset
	1 = output offset
D1	channel 4 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 4 short to ground
	0 = no short to ground
	1 = short to ground

Table 13.   Data byte DB3

Bit	Description
D7	maximum temperature protection
	0 = no protection
	1 = maximum temperature protection
D6	speaker fault channel 1 (missing current)
	0 = no missing current
	1 = missing current

Table 13. Data byte DB3 *…continued*

Bit	Description
D5 and D4	channel 1 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning
	0 = no AC load
	1 = AC load detected
	if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load
D3	channel 1 shorted load
	0 = not shorted load
	1 = shorted load
D2	channel 1 output offset
	0 = no output offset
	1 = output offset
D1	channel 1 short to V_P
	0 = no short to V_P
	1 = short to V_P
D0	channel 1 short to ground
	0 = no short to ground
	1 = short to ground

Table 14. Data byte DB4

Bit	Description
D7	reserved
D6	speaker fault channel 3 (missing current)
	0 = no missing current
	1 = missing current
D5 and D4	channel 3 DC load or AC load detection
	if bit IB1[D2] = 1, AC load detection is enabled, bit D5 is don't care, bit D4 has the following meaning
	0 = no AC load
	1 = AC load detected
	if bit IB1[D2] = 0, AC load detection is disabled, bits D5 and D4 are available for DC load detection
	00 = normal load
	01 = not valid
	10 = line driver load
	11 = open load