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TDA8920B

2 × 100 W class-D power amplifier

Rev. 02 — 07 November 2005 **Product data sheet**

1. General description

The TDA8920B is a high efficiency class-D audio power amplifier with very low dissipation. The typical output power is 2 × 100 W.

The device is available in the HSOP24 power package and in the DBS23P through-hole power package. The amplifier operates over a wide supply voltage range from ±12.5 V to ±30 V (±32 V non operating) and consumes a very low quiescent current.

2. Features

- Zero dead time switching
- Advanced current protection: output current limiting
- Smooth start-up: no pop noise due to DC offset
- High efficiency
- Operating supply voltage from ±12.5 V to ±30 V
- Low quiescent current
- Usable as a stereo Single-Ended (SE) amplifier or as a mono amplifier in Bridge-Tied Load (BTL)
- Fixed gain of 30 dB in Single-Ended (SE) and 36 dB in Bridge-Tied Load (BTL)
- High output power
- High supply voltage ripple rejection
- Internal switching frequency can be overruled by an external clock
- Full short-circuit proof across load and to supply lines
- Thermally protected

3. Applications

- Television sets
- Home-sound sets
- Multimedia systems
- All mains fed audio systems
- Car audio (boosters)

4. Quick reference data

Table 1: Quick reference data

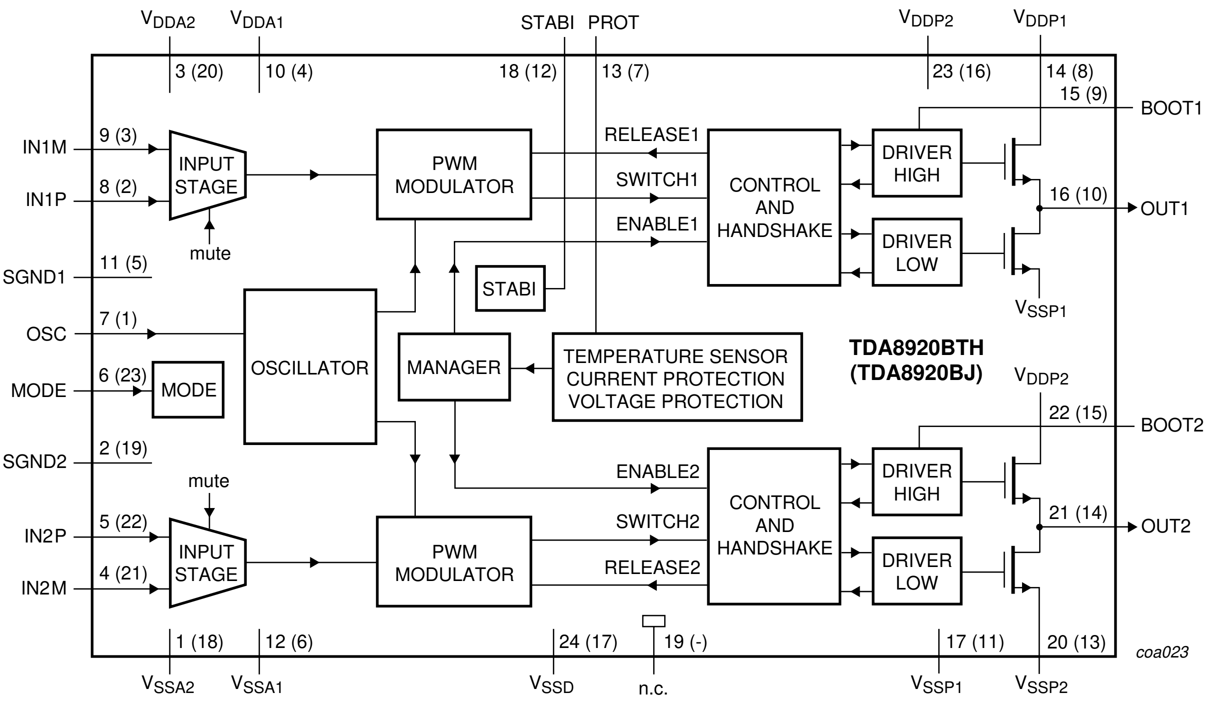
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; $V_P = \pm 27$ V						
V_P	supply voltage		±12.5	±27	±30	V
$I_{q(tot)}$	total quiescent supply current	no load; no filter; no RC-snubber network connected	-	50	65	mA
Stereo single-ended configuration						
P_o	output power	$R_L = 3\ \Omega$; THD = 10 %; $V_P = \pm 27$ V	-	110	-	W
		$R_L = 4\ \Omega$; THD = 10 %; $V_P = \pm 27$ V	-	86	-	W
Mono bridge-tied load configuration						
P_o	output power	$R_L = 6\ \Omega$; THD = 10 %; $V_P = \pm 27$ V	-	210	-	W

5. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TDA8920BTH	HSOP24	plastic, heatsink small outline package; 24 leads; low stand-off height	SOT566-3
TDA8920BJ	DBS23P	plastic DIL-bent-SIL power package; 23 leads (straight lead length 3.2 mm)	SOT411-1

6. Block diagram



Pin numbers in parenthesis refer to the TDA8920BJ.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

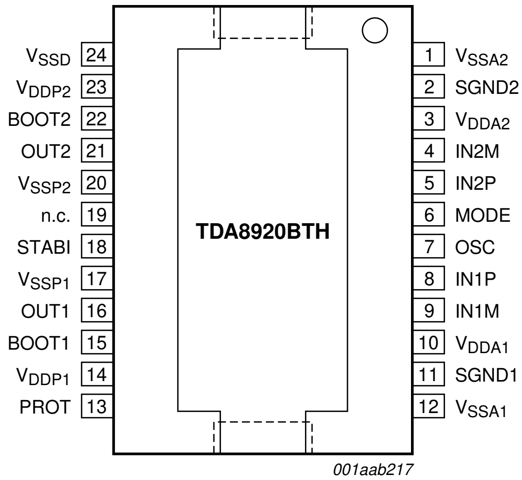


Fig 2. Pin configuration TDA8920BTH

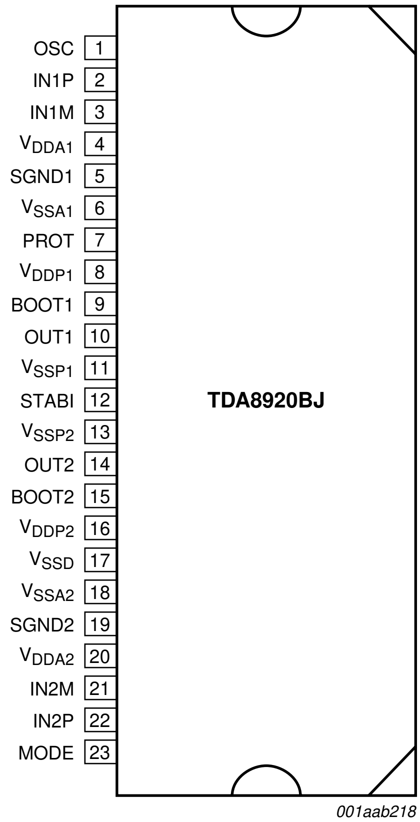


Fig 3. Pin configuration TDA8920BJ

7.2 Pin description

Table 3: Pin description

Symbol	Pin		Description
	TDA8920BTH	TDA8920BJ	
V_{SSA2}	1	18	negative analog supply voltage for channel 2
SGND2	2	19	signal ground for channel 2
V_{DDA2}	3	20	positive analog supply voltage for channel 2
IN2M	4	21	negative audio input for channel 2
IN2P	5	22	positive audio input for channel 2
MODE	6	23	mode selection input: Standby, Mute or Operating mode
OSC	7	1	oscillator frequency adjustment or tracking input
IN1P	8	2	positive audio input for channel 1
IN1M	9	3	negative audio input for channel 1
V_{DDA1}	10	4	positive analog supply voltage for channel 1

Table 3: Pin description *…continued*

Symbol	Pin		Description
	TDA8920BTH	TDA8920BJ	
SGND1	11	5	signal ground for channel 1
V_{SSA1}	12	6	negative analog supply voltage for channel 1
PROT	13	7	decoupling capacitor for protection (OCP)
V_{DDP1}	14	8	positive power supply voltage for channel 1
BOOT1	15	9	bootstrap capacitor for channel 1
OUT1	16	10	PWM output from channel 1
V_{SSP1}	17	11	negative power supply voltage for channel 1
STABI	18	12	decoupling of internal stabilizer for logic supply
n.c.	19	-	not connected
V_{SSP2}	20	13	negative power supply voltage for channel 2
OUT2	21	14	PWM output from channel 2
BOOT2	22	15	bootstrap capacitor for channel 2
V_{DDP2}	23	16	positive power supply voltage for channel 2
V_{SSD}	24	17	negative digital supply voltage

8. Functional description

8.1 General

The TDA8920B is a two channel audio power amplifier using class-D technology.

The audio input signal is converted into a digital pulse width modulated signal via an analog input stage and Pulse Width Modulation (PWM) modulator. To enable the output power transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. In this way a level shift is performed from the low power digital PWM signal (at logic levels) to a high power PWM signal which switches between the main supply lines.

A 2nd-order low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8920B one-chip class-D amplifier contains high power D-MOS switches, drivers, timing and handshaking between the power switches and some control logic. For protection a temperature sensor and a maximum current detector are built-in.

The two audio channels of the TDA8920B contain two PWM modulators, two analog feedback loops and two differential input stages. It also contains circuits common to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager.

The TDA8920B contains two independent amplifier channels with high output power, high efficiency, low distortion and a low quiescent current. The amplifier channels can be connected in the following configurations:

- Mono Bridge-Tied Load (BTL) amplifier
- Stereo Single-Ended (SE) amplifiers

The amplifier system can be switched to one of three operating modes by pin MODE:

- Standby mode; with a very low supply current
- Mute mode; the amplifiers are operational; but the audio signal at the output is suppressed by disabling the VI-converter input stages
- Operating mode; the amplifiers are fully operational with output signal

To ensure pop noise-free start-up, the DC output offset voltage is applied gradually to the output at a level between Mute mode and Operating mode levels. The bias current setting of the VI converters is related to the voltage on the MODE pin; in Mute mode the bias current setting of the VI converters is zero (VI converters disabled) and in Operating mode the bias current is at maximum. The time constant required to apply the DC output offset voltage gradually between Mute and Operating mode levels can be generated via an RC-network on the MODE pin. An example of a switching circuit for driving pin MODE is illustrated in Figure 4. If the capacitor C is left out of the application the voltage on the MODE pin will be applied with a much smaller time-constant, which might result in audible pop noises during start-up (depending on DC output offset voltage and loudspeaker used).

In order to fully charge the coupling capacitors at the inputs, the amplifier will remain automatically in the Mute mode before switching to the Operating mode. A complete overview of the start-up timing is given in Figure 5.

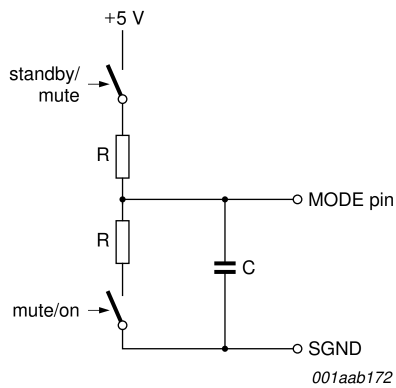
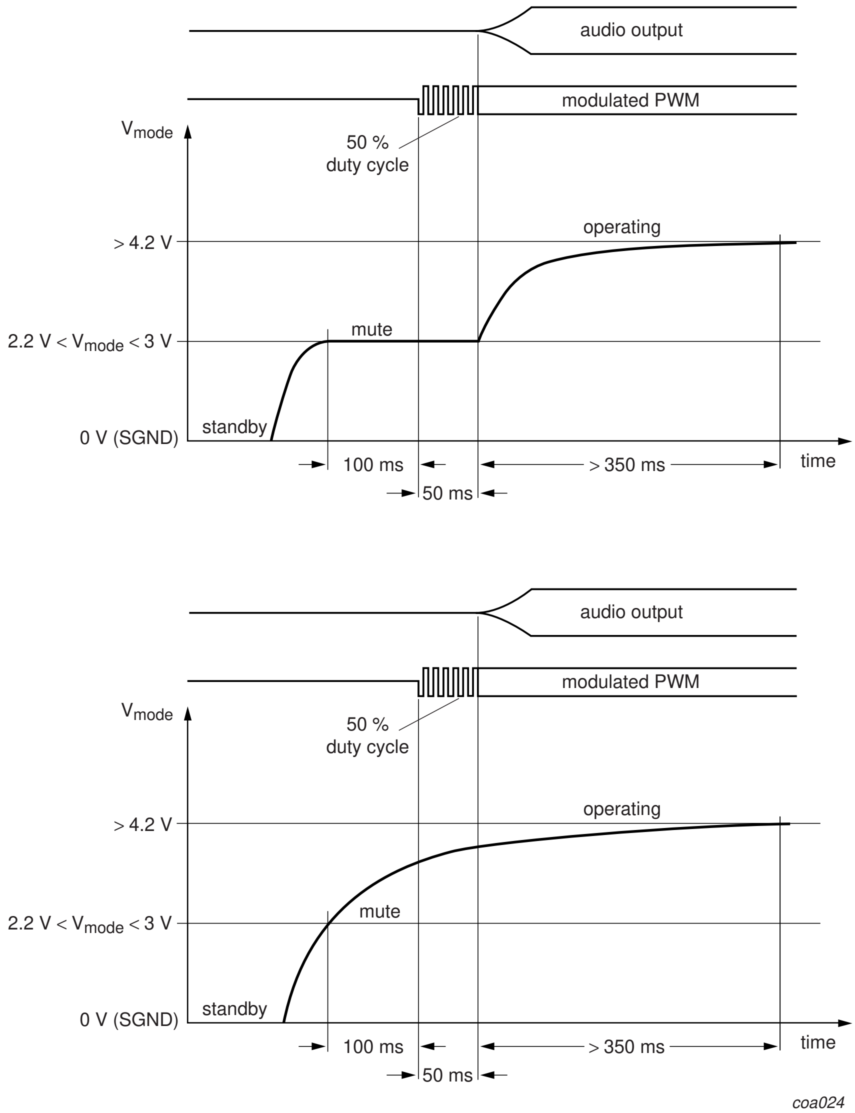


Fig 4. Example of mode selection circuit



Upper diagram: When switching from standby to mute, there is a delay of 100 ms before the output starts switching. The audio signal is available after V_{mode} has been set to operating, but not earlier than 150 ms after switching to mute. For pop noise-free start-up it is recommended that the time constant applied to the MODE pin is at least 350 ms for the transition between mute and operating.

Lower diagram: When switching directly from standby to operating, there is a first delay of 100 ms before the outputs starts switching. The audio signal is available after a second delay of 50 ms. For pop noise-free start-up it is recommended that the time constant applied to the MODE pin is at least 500 ms for the transition between standby and operating.

Fig 5. Timing on mode selection input

8.2 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 317 kHz. Using a 2nd-order LC demodulation filter in the application results in an analog audio signal across the loudspeaker. This switching frequency is fixed by an external resistor R_{OSC} connected between pin OSC and V_{SSA}. An optimal setting for the carrier frequency is between 300 kHz and 350 kHz.

Using an external resistor of 30 kΩ on the OSC pin, the carrier frequency is set to 317 kHz.

If two or more class-D amplifiers are used in the same audio application, it is advisable to have all devices operating at the same switching frequency by using an external clock circuit.

8.3 Protections

The following protections are included in TDA8920B:

- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protections:
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)

The reaction of the device to the different fault conditions differs per protection.

8.3.1 OverTemperature Protection (OTP)

If the junction temperature $T_j > 150$ °C, then the power stage will shut-down immediately. The power stage will start switching again if the temperature drops to approximately 130 °C, thus there is a hysteresis of approximately 20 °C.

8.3.2 OverCurrent Protection (OCP)

When the loudspeaker terminals are short-circuited or if one of the demodulated outputs of the amplifier is short-circuited to one of the supply lines, this will be detected by the OverCurrent Protection (OCP). If the output current exceeds the maximum output current of 8 A, this current will be limited by the amplifier to 8 A while the amplifier outputs remain switching (the amplifier is NOT shut-down completely).

The amplifier can distinguish between an impedance drop of the loudspeaker and a low-ohmic short across the load. In the TDA8920B this impedance threshold (Z_{th}) depends on the supply voltage used.

When a short is made across the load causing the impedance to drop below the threshold level ($< Z_{th}$) then the amplifier is switched off completely and after a time of 100 ms it will try to restart again. If the short circuit condition is still present after this time this cycle will be repeated. The average dissipation will be low because of this low duty cycle.

In case of an impedance drop (e.g. due to dynamic behavior of the loudspeaker) the same protection will be activated; the maximum output current is again limited to 8 A, but the amplifier will NOT switch-off completely (thus preventing audio holes from occurring). Result will be a clipping output signal without any artefacts.

See also Section 13.6 for more information on this maximum output current limiting feature.

8.3.3 Window Protection (WP)

During the start-up sequence, when pin MODE is switched from standby to mute, the conditions at the output terminals of the power stage are checked. In the event of a short-circuit at one of the output terminals to V_{DD} or V_{SS} the start-up procedure is interrupted and the system waits for open-circuit outputs. Because the test is done before enabling the power stages, no large currents will flow in the event of a short-circuit. This system is called Window Protection (WP) and protects for short-circuits at both sides of the output filter to both supply lines. When there is a short-circuit from the power PWM output of the power stage to one of the supply lines (before the demodulation filter) it will also be detected by the start-up safety test. Practical use of this test feature can be found in detection of short-circuits on the printed-circuit board.

Remark: This test is operational during (every) start-up sequence at a transition between Standby and Mute mode. However when the amplifier is completely shut-down due to activation of the OverCurrent Protection (OCP) because a short to one of the supply lines occurred, then during restart (after 100 ms) the window protection will be activated. As a result the amplifier will not start-up until the short to the supply line is removed.

8.3.4 Supply voltage protections

If the supply voltage drops below ±12.5 V, the UnderVoltage Protection (UVP) circuit is activated and the system will shut-down correctly. If the internal clock is used, this switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system is restarted again after 100 ms. If the supply voltage exceeds ±33 V the OverVoltage Protection (OVP) circuit is activated and the power stages will shut-down. It is re-enabled as soon as the supply voltage drops below the threshold level. So in this case no timer of 100 ms is started.

An additional UnBalance Protection (UBP) circuit compares the positive analog (V_{DDA}) and the negative analog (V_{SSA}) supply voltages and is triggered if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. An expression for the unbalanced threshold level is as follows: $V_{th(ub)} \approx 0.15 \times (V_{DDA} + V_{SSA})$.

When the supply voltage difference drops below the threshold level, the system is restarted again after 100 ms.

Example: With a symmetrical supply of ±30 V, the protection circuit will be triggered if the unbalance exceeds approximately 9 V; see also Section 13.7.

In Table 4 an overview is given of all protections and the effect on the output signal.

Table 4: Overview of TDA8920B protections

Protection name	Complete shut-down	Restart directly	Restart every 100 ms
OTP	Y	Y [1]	N [1]
OCP	N [2]	Y [2]	N [2]
WP	Y [3]	Y	N
UVP	Y	N	Y
OVP	Y	Y	N
UBP	Y	N	Y

[1] Hysteresis of 20 °C will influence restart timing depending on heatsink size.

[2] Only complete shut-down of amplifier if short-circuit impedance is below threshold of 1 Ω. In all other cases current limiting: resulting in clipping output signal.

[3] Fault condition detected during (every) transition between standby-to-mute and during restart after activation of OCP (short to one of the supply lines).

8.4 Differential audio inputs

For a high common mode rejection ratio and a maximum of flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the channels can be inverted, so that a load can be connected between the two output filters. In this case the system operates as a mono BTL amplifier and with the same loudspeaker impedance an approximately four times higher output power can be obtained.

The input configuration for a mono BTL application is illustrated in Figure 6.

In the stereo single-ended configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies.

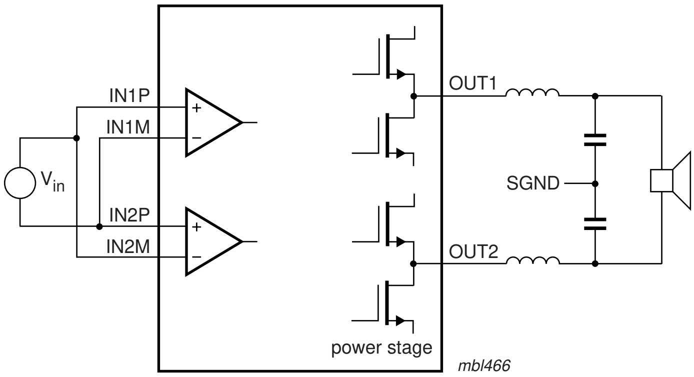


Fig 6. Input configuration for mono BTL application

9. Limiting values

Table 5: Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage					
		operating		-	±30	V
		non operating	[1]	-	±32	V
I_{ORM}	repetitive peak current in output pin	maximum output current limiting	[2]	8	-	A
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
T_j	junction temperature			-	150	°C

[1] Overvoltage protection might be activated.

[2] Current limiting concept. See also Section 13.6.

10. Thermal characteristics

Table 6: Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]		
	TDA8920BTH	in free air		35	K/W
	TDA8920BJ	in free air		35	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]		
	TDA8920BTH			1.3	K/W
	TDA8920BJ			1.3	K/W

[1] See also Section 13.5.

11. Static characteristics

Table 7: Static characteristics

V_P = ±27 V; f_{osc} = 317 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_P	supply voltage		[1]	±12.5	±27	±30	V
$I_{q(tot)}$	total quiescent supply current	no load, no filter; no RC-snubber network connected		-	50	65	mA
I_{stb}	standby supply current			-	150	500	μA
Mode select input; pin MODE							
V_I	input voltage		[2]	0	-	6	V
I_I	input current	V_I = 5.5 V		-	100	300	μA
V_{stb}	input voltage for Standby mode		[2] [3]	0	-	0.8	V
V_{mute}	input voltage for Mute mode		[2] [3]	2.2	-	3.0	V
V_{on}	input voltage for Operating mode		[2] [3]	4.2	-	6	V
Audio inputs; pins IN1M, IN1P, IN2P and IN2M							
V_I	DC input voltage		[2]	-	0	-	V
Amplifier outputs; pins OUT1 and OUT2							
$\|V_{OO(SE)(mute)}\|$	mute SE output offset voltage			-	-	15	mV
$\|V_{OO(SE)(on)}\|$	operating SE output offset voltage		[4]	-	-	150	mV
$\|V_{OO(BTL)(mute)}\|$	mute BTL output offset voltage			-	-	21	mV
$\|V_{OO(BTL)(on)}\|$	operating BTL output offset voltage		[4]	-	-	210	mV
Stabilizer output; pin STABI							
$V_{o(stab)}$	stabilizer output voltage	mute and operating; with respect to V_{SSP1}		11	12.5	15	V

Table 7: Static characteristics *…continued*
V_P = ±27 V; f_{osc} = 317 kHz; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Temperature protection						
T_{prot}	temperature protection activation		-	150	-	°C
T_{hys}	hysteresis of temperature protection		-	20	-	°C

[1] The circuit is DC adjusted at V_P = ±12.5 V to ±30 V.

[2] With respect to SGND (0 V).

[3] The transition between Standby and Mute mode has hysteresis, while the slope of the transition between Mute and Operating mode is determined by the time-constant of the RC-network on the MODE pin; see Figure 7.

[4] DC output offset voltage is applied to the output during the transition between Mute and Operating mode in a gradual way. The slope of the dV/dt caused by any DC output offset is determined by the time-constant of the RC-network on the MODE pin.

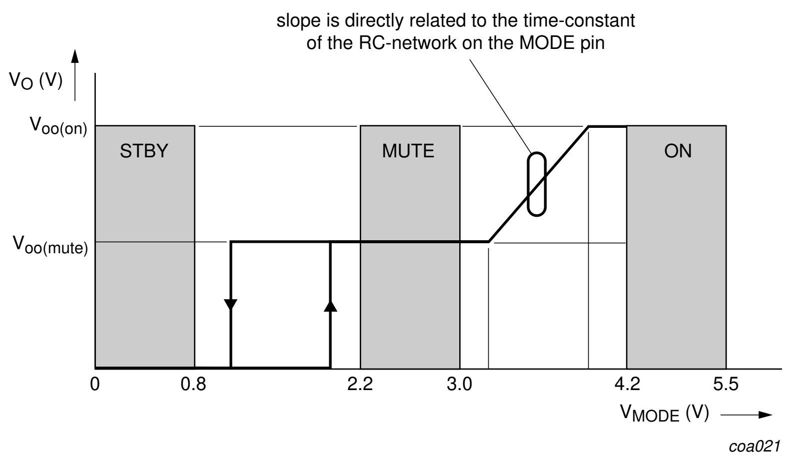


Fig 7. Behavior of mode selection pin MODE

12. Dynamic characteristics

12.1 Switching characteristics

Table 8: Switching characteristics
V_{DD} = ±27 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	typical internal oscillator frequency	R_{OSC} = 30.0 kΩ	290	317	344	kHz
$f_{osc(int)}$	internal oscillator frequency range		210	-	600	kHz
External oscillator or frequency tracking						
V_{OSC}	high-level voltage on pin OSC		SGND + 4.5	SGND + 5	SGND + 6	V
$V_{OSC(trip)}$	trip level for tracking on pin OSC		-	SGND + 2.5	-	V
f_{track}	frequency range for tracking		210	-	600	kHz

12.2 Stereo and dual SE application

Table 9: Stereo and dual SE application characteristics

V_P = ±27 V; R_L = 4 Ω; f_i = 1 kHz; f_{osc} = 317 kHz; R_{sL} < 0.1 Ω [1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	R_L = 3 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	87	-	W
		THD = 10 %		-	110	-	W
		R_L = 4 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	69	-	W
		THD = 10 %		-	86	-	W
		R_L = 6 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	48	-	W
		THD = 10 %		-	60	-	W
		R_L = 8 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	36	-	W
		THD = 10 %		-	45	-	W
THD	total harmonic distortion	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.02	0.05	%
		f_i = 6 kHz		-	0.03	-	%
$G_{v(cl)}$	closed loop voltage gain			29	30	31	dB
SVRR	supply voltage ripple rejection	operating	[4]				
		f_i = 100 Hz		-	55	-	dB
		f_i = 1 kHz		40	50	-	dB
		mute; f_i = 100 Hz	[4]	-	55	-	dB
		standby; f_i = 100 Hz	[4]	-	80	-	dB
$\|Z_i\|$	input impedance			45	68	-	kΩ
$V_{n(o)}$	noise output voltage	operating					
		R_s = 0 Ω	[5]	-	210	-	μV
		mute	[6]	-	160	-	μV
α_{cs}	channel separation		[7]	-	70	-	dB
$\|\Delta G_v\|$	channel unbalance			-	-	1	dB
$V_{o(mute)}$	output signal in mute		[8]	-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB

[1] R_{sL} is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement. See also Section 13.3.

[3] Total harmonic distortion is measured in a bandwidth of 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter. Maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[5] B = 22 Hz to 20 kHz, using AES17 20 kHz brickwall filter.

[6] B = 22 Hz to 22 kHz, using AES17 20 kHz brickwall filter; independent of R_s.

[7] P_o = 1 W; R_s = 0 Ω; f_i = 1 kHz.

[8] $V_i = V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

12.3 Mono BTL application

Table 10: Mono BTL application characteristics

V_P = ±27 V; R_L = 8 Ω; f_i = 1 kHz; f_{osc} = 317 kHz; R_{sL} < 0.1 Ω [1]; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	R_L = 6 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	174	-	W
		THD = 10 %		-	210	-	W
		R_L = 8 Ω; V_P = ±27 V	[2]				
		THD = 0.5 %		-	138	-	W
		THD = 10 %		-	173	-	W
THD	total harmonic distortion	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.02	0.05	%
		f_i = 6 kHz		-	0.03	-	%
$G_{v(cl)}$	closed loop voltage gain			35	36	37	dB
SVRR	supply voltage ripple rejection	operating	[4]				
		f_i = 100 Hz		-	80	-	dB
		f_i = 1 kHz		70	80	-	dB
		mute; f_i = 100 Hz	[4]	-	80	-	dB
		standby; f_i = 100 Hz	[4]	-	80	-	dB
$\|Z_i\|$	input impedance			22	34	-	kΩ
$V_{n(o)}$	noise output voltage	operating					
		R_s = 0 Ω	[5]	-	300	-	μV
		mute	[6]	-	220	-	μV
$V_{o(mute)}$	output signal in mute		[7]	-	200	-	μV
CMRR	common mode rejection ratio	$V_{i(CM)}$ = 1 V (RMS)		-	75	-	dB

[1] R_{sL} is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement. See also Section 13.3.

[3] Total harmonic distortion is measured in a bandwidth of 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter. Maximum limit is guaranteed but may not be 100 % tested.

[4] $V_{ripple} = V_{ripple(max)}$ = 2 V (p-p); R_s = 0 Ω.

[5] B = 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter.

[6] B = 22 Hz to 20 kHz, using an AES17 20 kHz brickwall filter; independent of R_s.

[7] $V_i = V_{i(max)}$ = 1 V (RMS); f_i = 1 kHz.

13. Application information

13.1 BTL application

When using the power amplifier in a mono BTL application the inputs of both channels must be connected in parallel and the phase of one of the inputs must be inverted (see Figure 6). In principle the loudspeaker can be connected between the outputs of the two single-ended demodulation filters.

13.2 MODE pin

For pop noise-free start-up an RC time-constant must be applied on the MODE pin. The bias-current setting of the VI-converter input is directly related to the voltage on the MODE pin. In turn the bias-current setting of the VI converters is directly related to the DC output offset voltage. Thus a slow dV/dt on the MODE pin results in a slow dV/dt for the DC output offset voltage, resulting in pop noise-free start-up. A time-constant of 500 ms is sufficient to guarantee pop noise-free start-up (see also Figure 4, 5 and 7).

13.3 Output power estimation

The achievable output powers in several applications (SE and BTL) can be estimated using the following expressions:

SE:

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{R_L + 0.4} \times V_P \times (1 - t_{min} \times f_{osc})\right]^2}{2 \times R_L} \quad (1)$$

Maximum current (internally limited to 8 A):

$$I_{o(peak)} = \frac{V_P \times (1 - t_{min} \times f_{osc})}{R_L + 0.4} \quad (2)$$

BTL:

$$P_{o(1\%)} = \frac{\left[\frac{R_L}{R_L + 0.8} \times 2V_P \times (1 - t_{min} \times f_{osc})\right]^2}{2 \times R_L} \quad (3)$$

Maximum current (internally limited to 8 A):

$$I_{o(peak)} = \frac{2V_P \times (1 - t_{min} \times f_{osc})}{R_L + 0.8} \quad (4)$$

Variables:

R_L = load impedance

f_{osc} = oscillator frequency

t_{min} = minimum pulse width (typically 150 ns)

V_P = single-sided supply voltage (so, if supply is ±30 V symmetrical, then V_P = 30 V)

$P_{o(1\%)}$ = output power just at clipping

$P_{o(10\%)}$ = output power at THD = 10 %

$P_{o(10\%)} = 1.24 \times P_{o(1\%)}$.

13.4 External clock

When using an external clock the following accuracy of the duty cycle of the external clock has to be taken into account: 47.5 % < δ < 52.5 %.

If two or more class-D amplifiers are used in the same audio application, it is strongly recommended that all devices run at the same switching frequency. This can be realized by connecting all OSC pins together and feed them from an external central oscillator. Using an external oscillator it is necessary to force pin OSC to a DC-level above SGND for switching from the internal to an external oscillator. In this case the internal oscillator is disabled and the PWM modulator will be switched on the external frequency. The frequency range of the external oscillator must be in the range as specified in the switching characteristics; see Section 12.1.

In an application circuit:

- Internal oscillator: R_{OSC} connected between pin OSC and V_{SSA}
- External oscillator: connect the oscillator signal between pins OSC and SGND; R_{OSC} and C_{OSC} removed

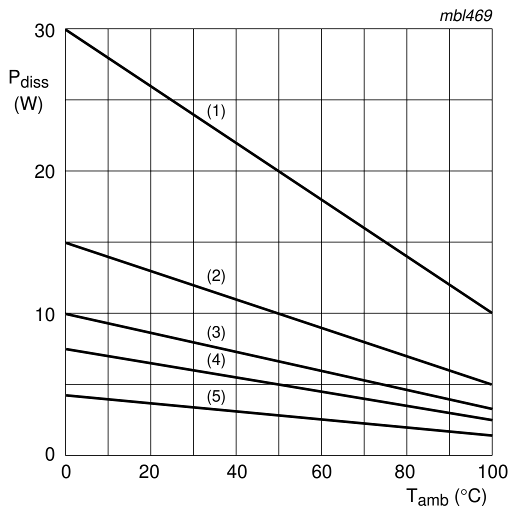
13.5 Heatsink requirements

In some applications it may be necessary to connect an external heatsink to the TDA8920B. Limiting factor is the 150 °C maximum junction temperature $T_{j(max)}$ which cannot be exceeded. The expression below shows the relationship between the maximum allowable power dissipation and the total thermal resistance from junction to ambient:

$$R_{th(j-a)} = \frac{T_{j(max)} - T_{amb}}{P_{diss}} \quad (5)$$

P_{diss} is determined by the efficiency (η) of the TDA8920B. The efficiency measured in the TDA8920B as a function of output power is given in Figure 21. The power dissipation can be derived as a function of output power (see Figure 20).

The derating curves (given for several values of $R_{th(j-a)}$) are illustrated in Figure 8. A maximum junction temperature T_j = 150 °C is taken into account. From Figure 8 the maximum allowable power dissipation for a given heatsink size can be derived or the required heatsink size can be determined at a required dissipation level.



(1) $R_{th(j-a)}$ = 5 K/W.

(2) $R_{th(j-a)}$ = 10 K/W.

(3) $R_{th(j-a)}$ = 15 K/W.

(4) $R_{th(j-a)}$ = 20 K/W.

(5) $R_{th(j-a)}$ = 35 K/W.

Fig 8. Derating curves for power dissipation as a function of maximum ambient temperature

13.6 Output current limiting

To guarantee the robustness of the class-D amplifier the maximum output current which can be delivered by the output stage is limited. An advanced OverCurrent Protection (OCP) is included for each output power switch.

When the current flowing through any of the power switches exceeds the defined internal threshold of 8 A (e.g. in case of a short-circuit to the supply lines or a short-circuit across the load) the maximum output current of the amplifier will be regulated to 8 A.

The TDA8920B amplifier can distinguish between a low-ohmic short circuit condition and other overcurrent conditions like dynamic impedance drops of the loudspeakers used. The impedance threshold (Z_{th}) depends on the supply voltage used.

Depending on the impedance of the short circuit the amplifier will react as follows:

1. Short-circuit impedance > Z_{th}:

   the maximum output current of the amplifier is regulated to 8 A, but the amplifier will not shut-down its PWM outputs. Effectively this results in a clipping output signal across the load (behavior is very similar to voltage clipping).

2. Short-circuit impedance < Z_{th}:

   the amplifier will limit the maximum output current to 8 A and at the same time the capacitor on the PROT pin is discharged. When the voltage across this capacitor drops below an internal threshold voltage the amplifier will shut-down completely and an internal timer will be started.

A typical value for the capacitor on the PROT pin is 220 pF. After a fixed time of 100 ms the amplifier is switched on again. If the requested output current is still too high the amplifier will switch-off again. Thus the amplifier will try to switch to the Operating mode every 100 ms. The average dissipation will be low in this situation because of this low duty cycle. If the overcurrent condition is removed the amplifier will remain in Operating mode once restarted.

In this way the TDA8920B amplifier is fully robust against short circuit conditions while at the same time so-called audio holes as a result of loudspeaker impedance drops are eliminated.

13.7 Pumping effects

In a typical stereo half-bridge SE application the TDA8920B class-D amplifier is supplied by a symmetrical voltage (e.g V_{DD} = +27 V and V_{SS} = −27 V). When the amplifier is used in a SE configuration, a so-called 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DD}), while a part of that energy is delivered back to the other supply line (e.g. V_{SS}) and visa versa. When the voltage supply source cannot sink energy, the voltage across the output capacitors of that voltage supply source will increase: the supply voltage is pumped to higher levels. The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels

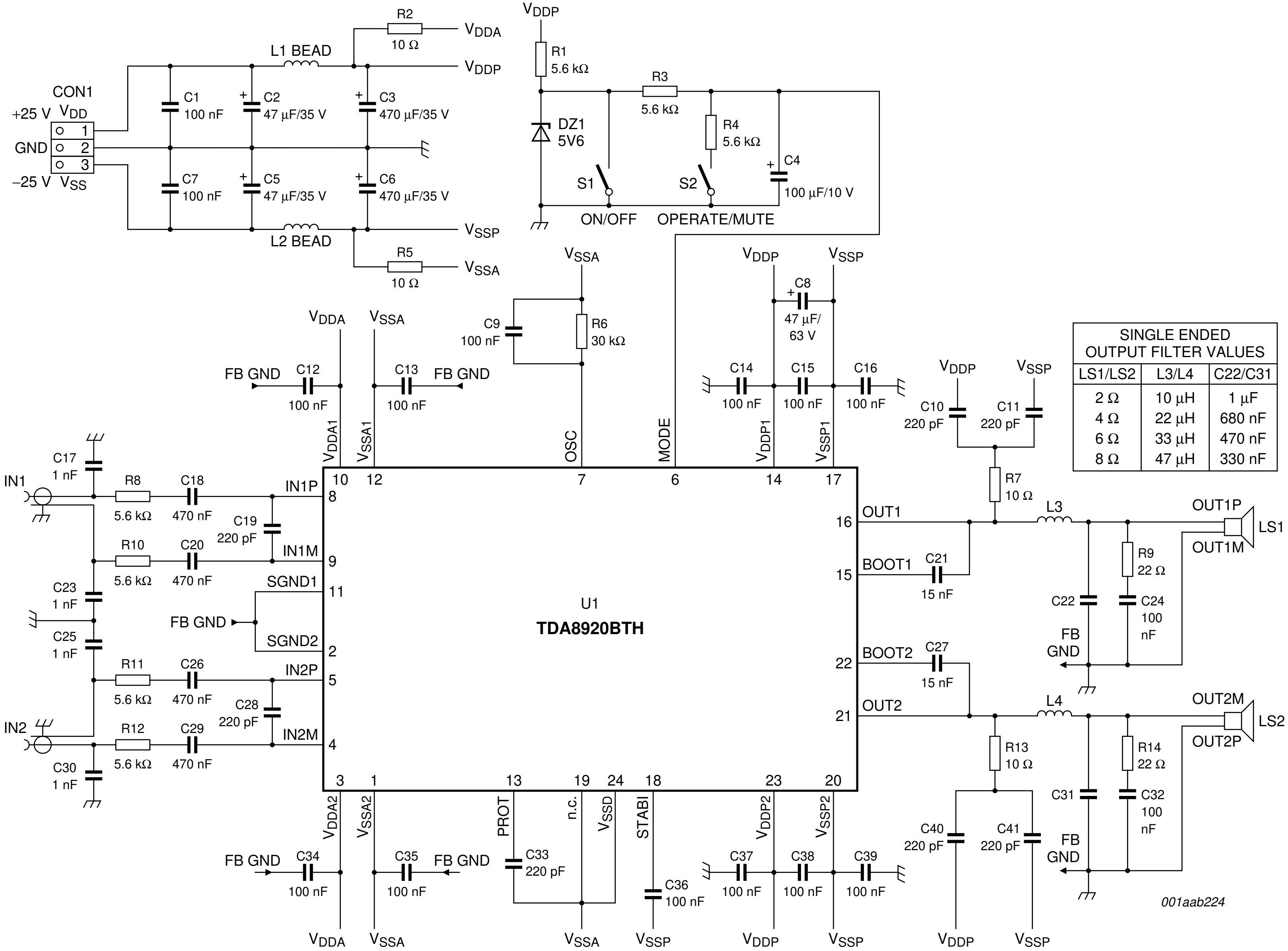
The pumping effect should not cause a malfunction of either the audio amplifier and/or the voltage supply source. For instance, this malfunction can be caused by triggering of the undervoltage or overvoltage protection or unbalance protection of the amplifier.

Best remedy for pumping effects is to use the TDA8920B in a mono full-bridge application or in case of stereo half-bridge application adapt the power supply (e.g. increase supply decoupling capacitors).

13.8 Application schematic

Notes for the application schematic:

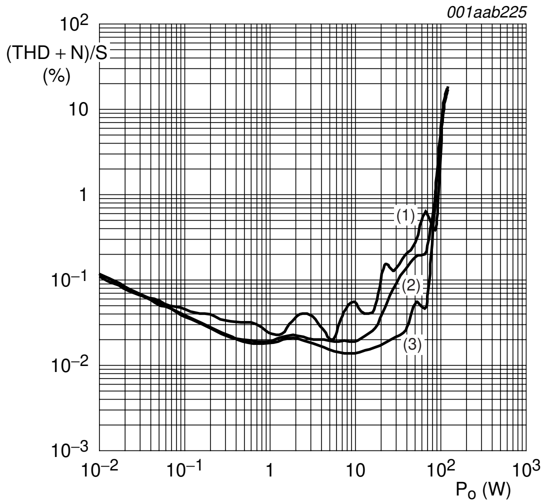
- A solid ground plane around the switching amplifier is necessary to prevent emission
- 100 nF capacitors must be placed as close as possible to the power supply pins of the TDA8920BTH
- The internal heat spreader of the TDA8920BTH is internally connected to V_{SS}
- The external heatsink must be connected to the ground plane
- Use a thermal conductive electrically non-conductive Sil-Pad between the backside of the TDA8920BTH and a small external heatsink
- The differential inputs enable the best system level audio performance with unbalanced signal sources. In case of hum due to floating inputs, connect the shielding or source ground to the amplifier ground. Jumpers J1 and J2 are open on set level and are closed on the stand-alone demo board
- Minimum total required capacitance per power supply line is 3300 μF



SINGLE ENDED OUTPUT FILTER VALUES		
LS1/LS2	L3/L4	C22/C31
2 Ω	10 µH	1 µF
4 Ω	22 µH	680 nF
6 Ω	33 µH	470 nF
8 Ω	47 µH	330 nF

Fig 9. TDA8920BTH application schematic

13.9 Curves measured in reference design



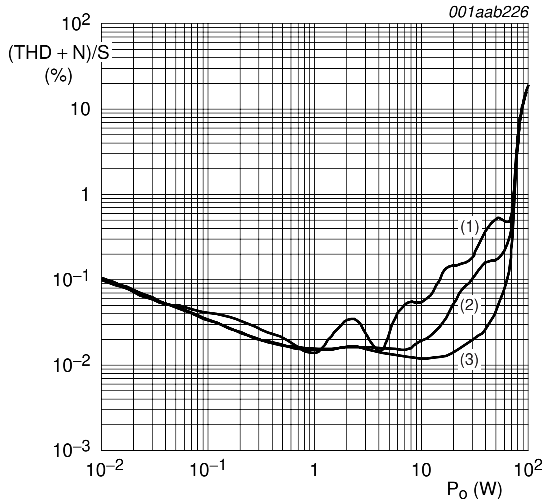
$V_P = \pm 27$ V; 2 × 3 Ω SE configuration.

(1) f = 6 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 10. (THD + N)/S as a function of output power; SE configuration with 2 × 3 Ω load



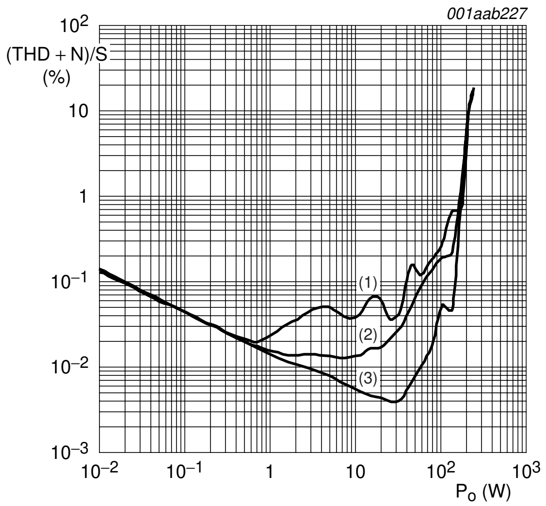
$V_P = \pm 27$ V; 2 × 4 Ω SE configuration.

(1) f = 6 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 11. (THD + N)/S as a function of output power; SE configuration with 2 × 4 Ω load



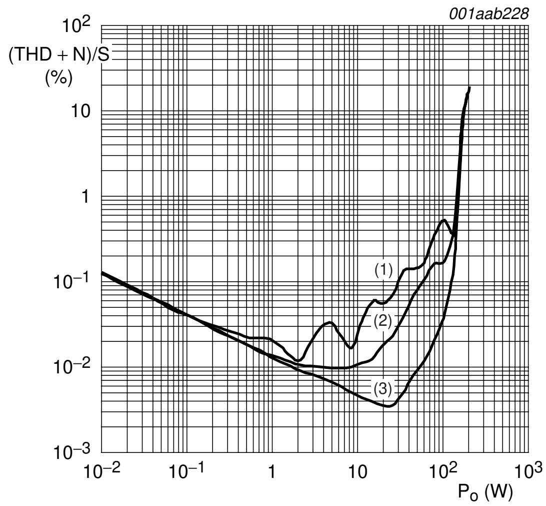
$V_P = \pm 27$ V; 1 × 6 Ω BTL configuration.

(1) f = 6 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 12. (THD + N)/S as a function of output power; BTL configuration with 1 × 6 Ω load



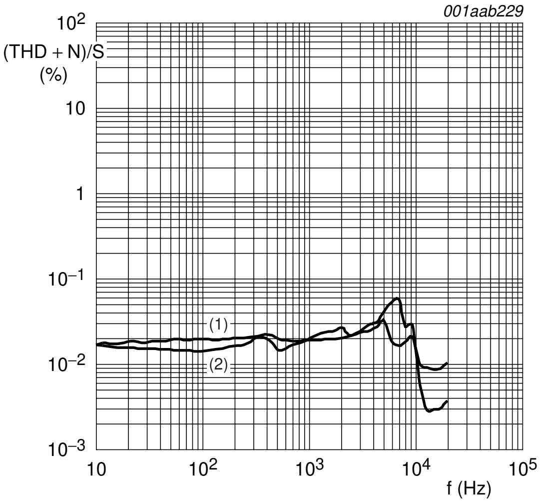
$V_P = \pm 27$ V; 1 × 8 Ω BTL configuration.

(1) f = 6 kHz.

(2) f = 1 kHz.

(3) f = 100 Hz.

Fig 13. (THD + N)/S as a function of output power; BTL configuration with 1 × 8 Ω load

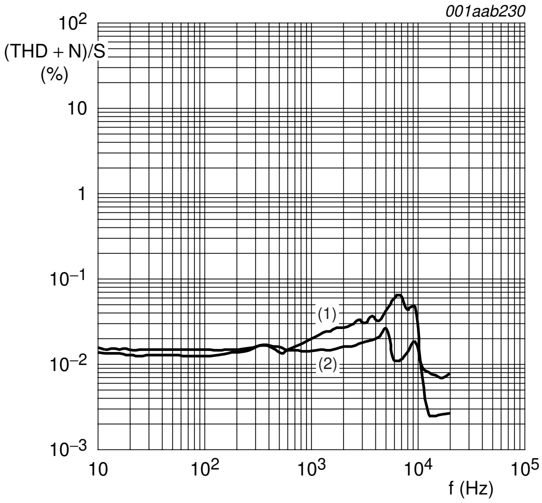


V_P = ±27 V; 2 × 3 Ω SE configuration.

(1) P_{out} = 1 W.

(2) P_{out} = 10 W.

Fig 14. (THD + N)/S as a function of frequency; SE configuration with 2 × 3 Ω load

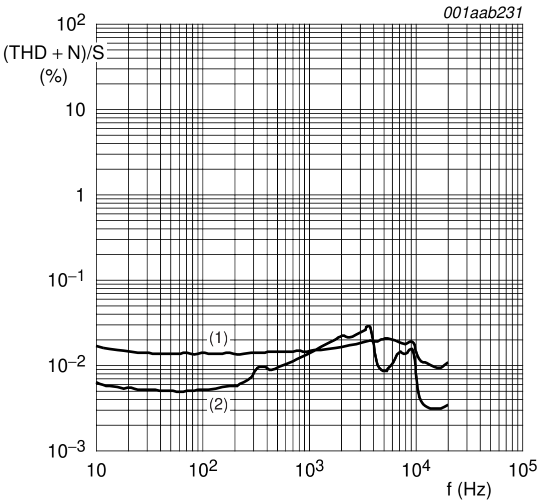


V_P = ±27 V; 2 × 4 Ω SE configuration.

(1) P_{out} = 1 W.

(2) P_{out} = 10 W.

Fig 15. (THD + N)/S as a function of frequency; SE configuration with 2 × 4 Ω load

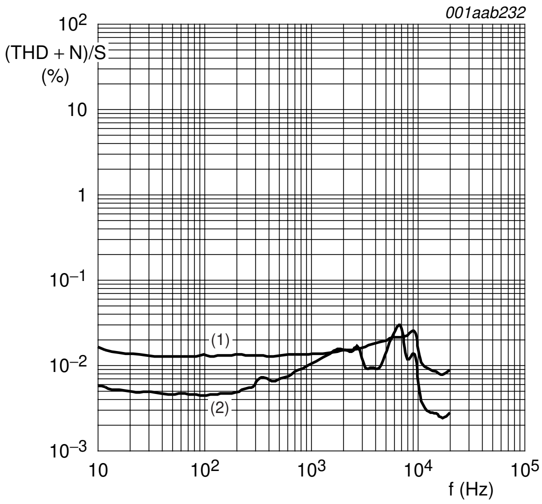


V_P = ±27 V; 1 × 6 Ω BTL configuration.

(1) P_{out} = 1 W.

(2) P_{out} = 10 W.

Fig 16. (THD + N)/S as a function of frequency; BTL configuration with 1 × 6 Ω load

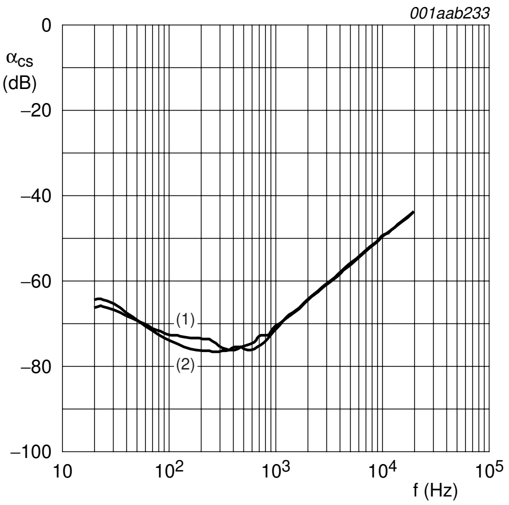


V_P = ±27 V; 1 × 8 Ω BTL configuration.

(1) P_{out} = 1 W.

(2) P_{out} = 10 W.

Fig 17. (THD + N)/S as a function of frequency; BTL configuration with 1 × 8 Ω load

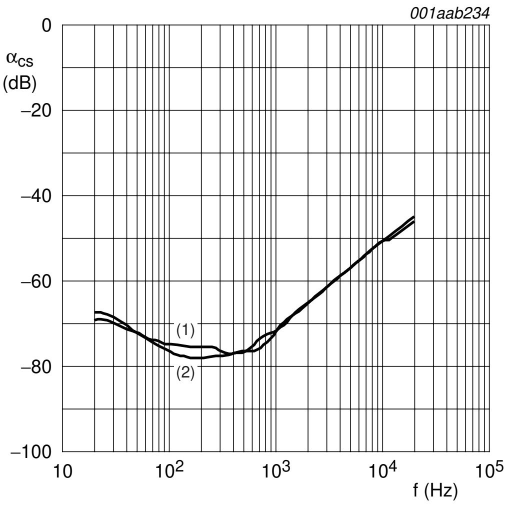


V_P = ±27 V; 2 × 3 Ω SE configuration.

(1) P_{out} = 10 W.

(2) P_{out} = 1 W.

Fig 18. Channel separation as a function of frequency; SE configuration with 2 × 3 Ω load

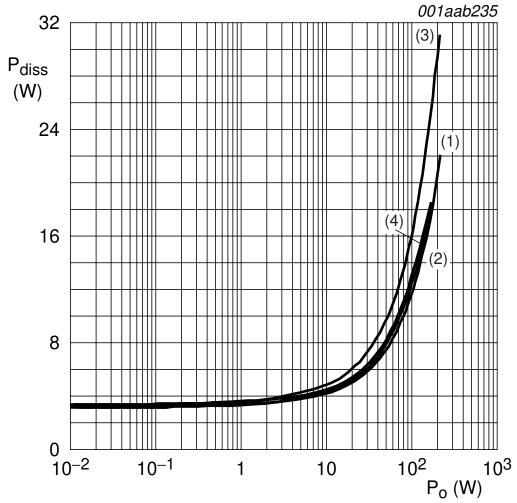


V_P = ±27 V; 2 × 4 Ω SE configuration.

(1) P_{out} = 10 W.

(2) P_{out} = 1 W.

Fig 19. Channel separation as a function of frequency; SE configuration with 2 × 4 Ω load



V_P = ±27 V; f = 1 kHz.

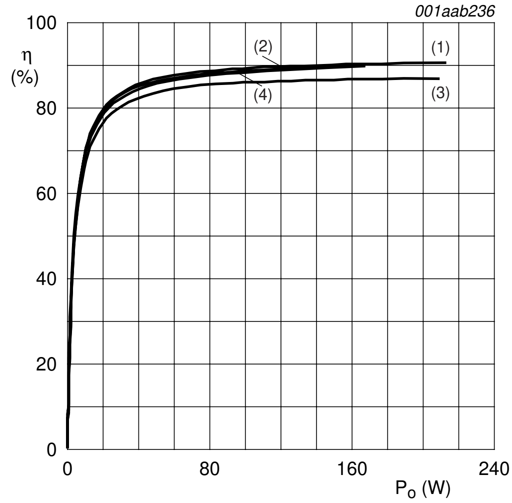
(1) 2 × 3 Ω SE configuration.

(2) 2 × 4 Ω SE configuration.

(3) 1 × 6 Ω BTL configuration.

(4) 1 × 8 Ω BTL configuration.

Fig 20. Power dissipation as a function of total output power



V_P = ±27 V; f = 1 kHz.

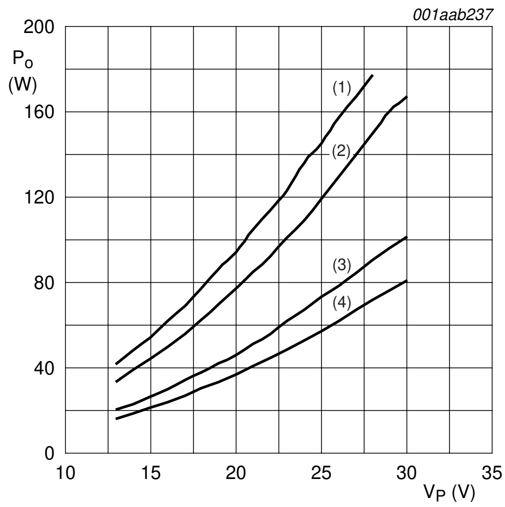
(1) 2 × 3 Ω SE configuration.

(2) 2 × 4 Ω SE configuration.

(3) 1 × 6 Ω BTL configuration.

(4) 1 × 8 Ω BTL configuration.

Fig 21. Efficiency as a function of total output power



f = 1 kHz.

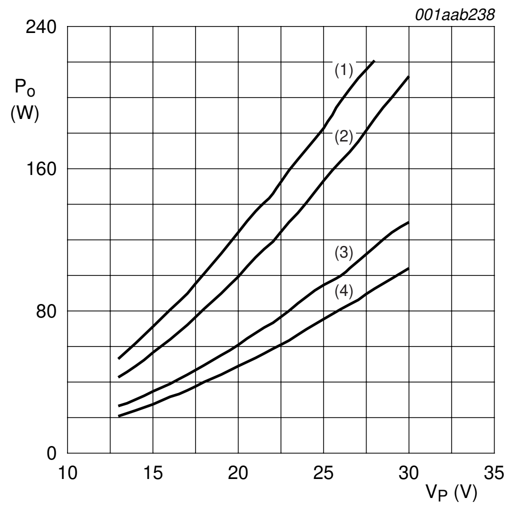
(1) 1 × 6 Ω BTL configuration.

(2) 1 × 8 Ω BTL configuration.

(3) 2 × 3 Ω SE configuration.

(4) 2 × 4 Ω SE configuration.

Fig 22. Output power as a function of supply voltage; THD + N = 0.5 %



f = 1 kHz.

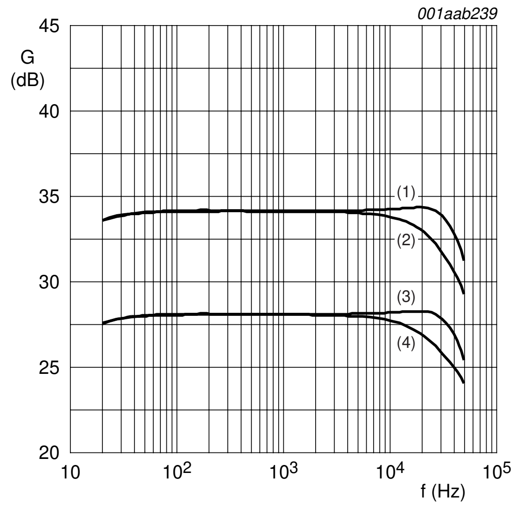
(1) 1 × 6 Ω BTL configuration.

(2) 1 × 8 Ω BTL configuration.

(3) 2 × 3 Ω SE configuration.

(4) 2 × 4 Ω SE configuration.

Fig 23. Output power as a function of supply voltage; THD + N = 10 %



V_i = 100 mV; R_s = 5.6 kΩ; C_i = 330 pF; V_P = ±27 V.

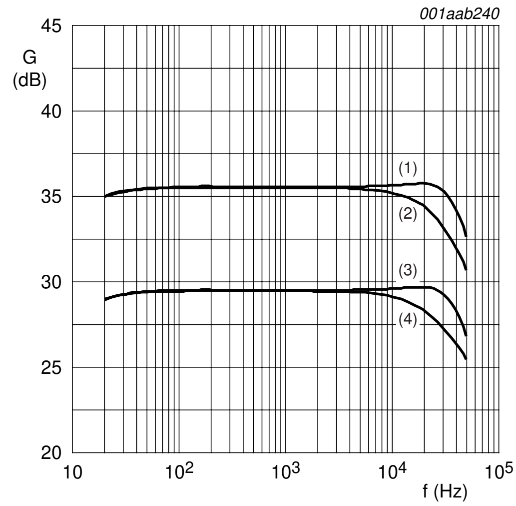
(1) 1 × 8 Ω BTL configuration.

(2) 1 × 6 Ω BTL configuration.

(3) 2 × 4 Ω BTL configuration.

(4) 2 × 3 Ω BTL configuration.

Fig 24. Gain as a function of frequency; R_s = 5.6 kΩ and C_i = 330 pF



V_i = 100 mV; R_s = 0 Ω; C_i = 330 pF; V_P = ±27 V.

(1) 1 × 8 Ω BTL configuration.

(2) 1 × 6 Ω BTL configuration.

(3) 2 × 4 Ω BTL configuration.

(4) 2 × 3 Ω BTL configuration.

Fig 25. Gain as a function of frequency; R_s = 0 Ω and C_i = 330 pF