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TDA8933B

Class D audio amplifier

Rev. 01 — 23 October 2008 Preliminary data sheet

1. General description

The TDA8933B is a high-efficiency class D amplifier with low power dissipation.

The continuous time output power is 2×10 W in a stereo half-bridge application (R_L = 8 Ω) or 1×20 W in a mono full-bridge application (R_L =16 Ω). Due to the low power dissipation the device can be used without any external heat sink when playing music. Due to the implementation of Thermal Foldback (TF) the device remains operating with considerable music output power without the need for an external heat sink, even for high supply voltages and/or lower load impedances.

The device has two full differential inputs driving two independent outputs. It can be used in a mono full-bridge configuration (Bridge-Tied Load (BTL)) or as stereo half-bridge configuration (Single-Ended (SE)).

2. Features

- Operating voltage from 10 V to 36 V asymmetrical or ±5 V to ±18 V symmetrical
- Mono bridge-tied load (full-bridge) or stereo single-ended (half-bridge) application
- Application without heat sink using thermally enhanced small outline package
- High efficiency and low-power dissipation
- Thermal foldback to avoid audio holes
- Current limiting to avoid audio holes
- Full short circuit proof across load and to supply lines (using advanced current protection)
- Internal or external oscillator (master-slave setting) that can be switched
- No pop noise
- Full differential inputs

3. Applications

- Flat-panel television sets
- Flat-panel monitor sets
- Multimedia systems
- Wireless speakers
- Mini/micro systems
- Home sound sets

4. Quick reference data

Table 1. Quick reference data

General; V_p = 25 V, f_{osc} = 320 kHz, T_{amb} = 25 °C unless specified otherwise

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_P	supply voltage	asymmetrical supply	10	25	36	V
I_P	supply current	Sleep mode	-	0.6	1.0	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load; no snubbers or filter connected	-	40	50	mA
Stereo SE channel; R_s < 0.1 Ω[1]						
$P_{o(RMS)}$	RMS output power	continuous time output power per channel[2]				
		R_L = 4 Ω; V_P = 17 V				
		THD+N = 10 %, f_i = 1 kHz	7.5	8.5	-	W
		R_L = 8 Ω; V_P = 25 V				
		THD+N = 10 %, f_i = 1 kHz	9.3	10.3	-	W
Mono BTL channel; R_s < 0.1 Ω[1]						
$P_{o(RMS)}$	RMS output power	continuous time output power[2]				
		R_L = 8 Ω; V_P = 17 V				
		THD+N = 10 %, f_i = 1 kHz	15.4	17.1	-	W
		R_L = 16 Ω; V_P = 25 V				
		THD+N = 10 %, f_i = 1 kHz	18.9	20.6	-	W

[1] R_s is the total series resistance of an inductor and an ESR single-ended capacitor in the application.

[2] Output power is measured indirectly, based on R_{DSon} measurement.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8933BTW	HTSSOP32	plastic thermal enhanced thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm; exposed die pad	SOT549-1

6. Block diagram

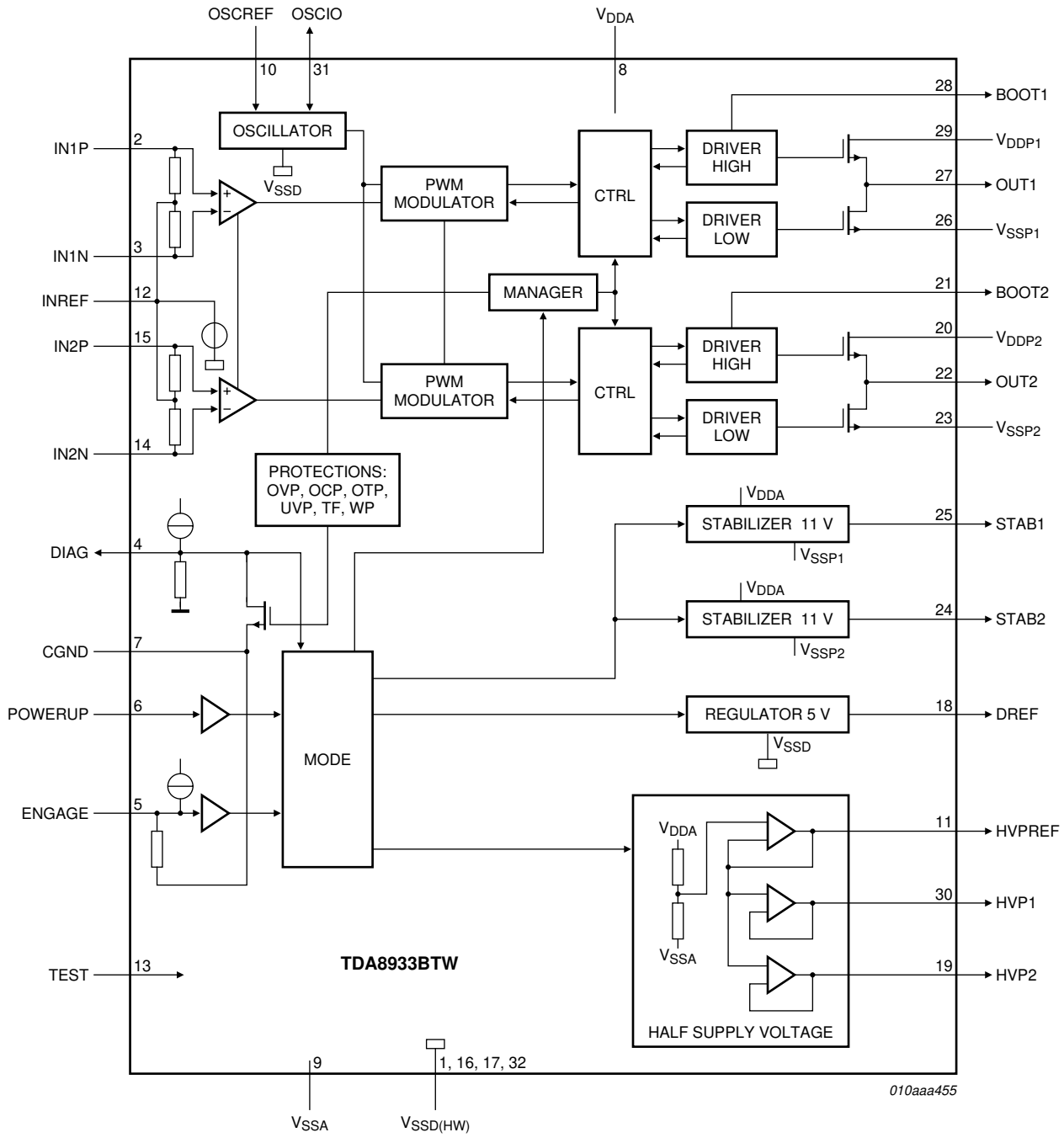


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

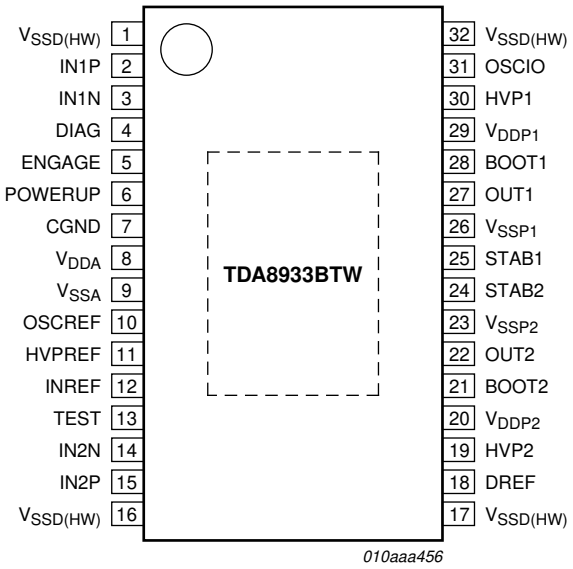


Fig 2. Pin configuration diagram (HTSSOP32 package)

7.2 Pin description

Table 3. Pinning description

Symbol	Pin	Description
$V_{SSD(HW)}$	1	negative digital supply voltage and handle wafer connection
IN1P	2	positive audio input for channel 1
IN1N	3	negative audio input for channel 1
DIAG	4	diagnostic output; open-drain
ENGAGE	5	engage input to switch between Mute mode and Operating mode
POWERUP	6	power-up input to switch between Sleep mode and Mute mode
CGND	7	control ground; reference for POWERUP, ENGAGE and DIAG
V_{DDA}	8	positive analog supply voltage
V_{SSA}	9	negative analog supply voltage
OSCREF	10	input internal oscillator setting (only master setting)
HVPREF	11	decoupling of internal half supply voltage reference
INREF	12	decoupling for input reference voltage
TEST	13	test signal input; for testing purpose only
IN2N	14	negative audio input for channel 2
IN2P	15	positive audio input for channel 2
$V_{SSD(HW)}$	16	negative digital supply voltage and handle wafer connection
$V_{SSD(HW)}$	17	negative digital supply voltage and handle wafer connection
DREF	18	decoupling of internal (reference) 5 V regulator for logic supply

Table 3. Pinning description *...continued*

Symbol	Pin	Description
HVP2	19	half supply output voltage 2 for charging single-ended capacitor for channel 2
V_{DDP2}	20	positive power supply voltage for channel 2
BOOT2	21	bootstrap high-side driver channel 2
OUT2	22	Pulse Width Modulated (PWM) output channel 2
V_{SSP2}	23	negative power supply voltage for channel 2
STAB2	24	decoupling of internal 11 V regulator for channel 2 drivers
STAB1	25	decoupling of internal 11 V regulator for channel 1 drivers
V_{SSP1}	26	negative power supply voltage for channel 1
OUT1	27	PWM output channel 1
BOOT1	28	bootstrap high-side driver for channel 1
V_{DDP1}	29	positive power supply voltage for channel 1
HVP1	30	half supply output voltage 1 for charging single-ended capacitor for channel 1
OSCIO	31	oscillator input in slave configuration or oscillator output in master configuration
$V_{SSD(HW)}$	32	negative digital supply voltage and handle wafer connection
Exposed die pad[1]	-	

[1] The exposed die pad has to be connected to $V_{SSD(HW)}$.

8. Functional description

8.1 General

The TDA8933B is a mono full-bridge or stereo half-bridge audio power amplifier using class D technology. The audio input signal is converted into a PWM signal via an analog input stage and a PWM modulator. To enable the output power Diffusion Metal Oxide Semiconductor (DMOS) transistors to be driven, this digital PWM signal is applied to a control and handshake block and driver circuits for both the high side and low side. A 2nd-order low-pass filter in the application converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8933B contains two independent half bridges with full differential input stages. The loudspeakers can be connected in the following configurations:

- Mono full-bridge: Bridge-Tied Load (BTL)
- Stereo half-bridge: Single-Ended (SE)

The TDA8933B contains circuits common to both channels such as the oscillator, all reference sources, the mode functionality and a digital timing manager. The following protections are built-in: thermal foldback and overtemperature, current and voltage protections.

8.2 Mode selection and interfacing

The TDA8933B can be switched to one of four operating modes using pins POWERUP and ENGAGE:

- Sleep mode: with low supply current.
- Mute mode: the amplifiers are switching to idle (50 % duty cycle), but the audio signal at the output is suppressed by disabling the V_I-converter input stages. The capacitors on pins HVP1 and HVP2 have been charged to half the supply voltage (asymmetrical supply only)
- Operating mode: the amplifiers are fully operational with an output signal
- Fault mode

Both pins POWERUP and ENGAGE refer to pin CGND.

Table 4 shows the different modes as a function of the voltages on the POWERUP and ENGAGE pins.

Table 4. Mode selection for the TDA8933B

Mode	Pin		
	POWERUP[1]	ENGAGE[1]	DIAG
Sleep	< 0.8 V	< 0.8 V	undefined
Mute	2 V to 6 V	< 0.8 V	> 2 V
Operating	2 V to 6 V	2.4 V to 6 V	> 2 V
Fault	2 V to 6 V	undefined	< 0.8 V

[1] When there are symmetrical supply conditions, the voltage applied to pins POWERUP and ENGAGE must never exceed the supply voltage (V_{DDA}, V_{DDP1} or V_{DDP2}).

If the transition between Mute mode and Operating mode is controlled via a time constant, the start-up will be pop-free since the DC output offset voltage is applied gradually to the output. The bias current setting of the V/I-converters is related to the voltage on pin ENGAGE.

- Mute mode: the bias current setting of the V/I-converters is zero (V/I-converters disabled).
- Operating mode: the bias current is at maximum.

The time constant required to apply the DC output offset voltage gradually between Mute mode and Operating mode can be generated by applying a capacitor on pin ENGAGE. The value of the capacitor on pin ENGAGE should be 470 nF.

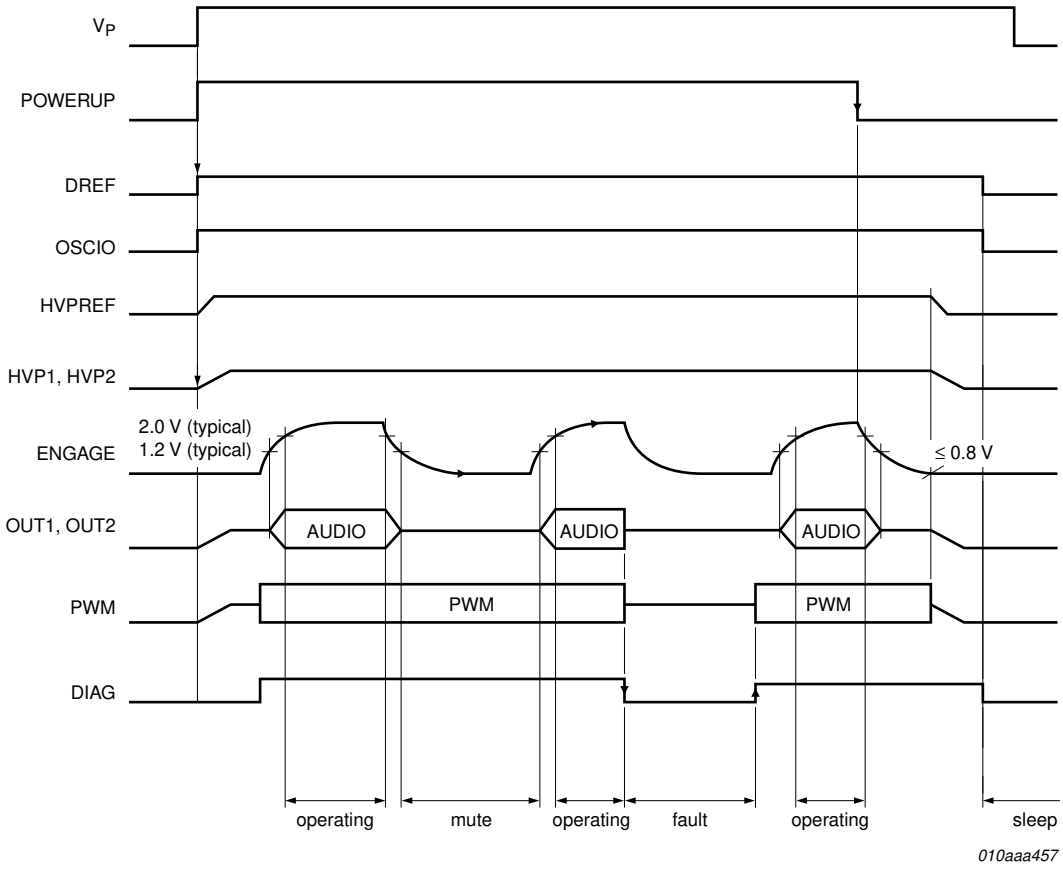


Fig 3. Start-up sequence

8.3 Pulse Width Modulation (PWM) frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 320 kHz. Using a 2nd-order low-pass filter in the application results in an analog audio signal across the loudspeaker. The PWM switching frequency can be set by an external resistor R_{osc} connected between pin OSCREF and $V_{SSD(HW)}$. The carrier frequency can be set between 300 kHz and 500 kHz. Using an external resistor of 39 kΩ, the carrier frequency is set to a typical value of 320 kHz (see Figure 4).

If two or more TDA8933B devices are used in the same audio application, it is recommended to synchronize the switching frequency of all devices. See Section 14.6 for more information.

The value of the resistor also sets the frequency of the carrier and can be calculated with Equation 1:

$$f_{osc} = \frac{12.45 \times 10^{9}}{R_{osc}} \quad (1)$$

Where:

f_{osc} = oscillator frequency (Hz)

R_{osc} = oscillator resistor (Ω) (on pin OSCREF)

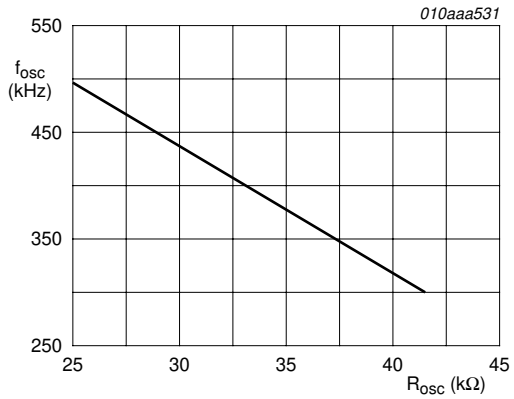


Fig 4. Oscillation frequency as a function of R_{osc}

Table 5 summarizes how to configure the TDA8933B in master or slave configuration.

For device synchronization see Section 14.6.

Table 5. Master or slave configuration

Configuration	Pin	
	OSCREF	OSCIO
Master	R_{osc} > 25 kΩ to $V_{SSD(HW)}$	output
Slave	R_{osc} = 0 Ω; shorted to $V_{SSD(HW)}$	input

8.4 Protections

The following protections are implemented in the TDA8933B:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protections
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)
- Electro Static Discharge (ESD)

The behavior of the device under the different fault conditions differs according to the protection activated and is described in the following sections.

8.4.1 Thermal Foldback (FT)

If the junction temperature of the TDA8933B exceeds the threshold level (T_j > 140 °C), the gain of the amplifier is decreased gradually to a level where the combination of dissipation (P) and the thermal resistance from junction to ambient ($R_{th(j-a)}$) results in a junction temperature of around the threshold level.

This means that the device will not switch off completely, but remains operational at lower output power levels. With music output signals, this feature enables high peak output powers while still operating without any external heat sink other than the copper area on the Printed-Circuit Board (PCB).

If the junction temperature still increases due to external causes the OTP shuts down the amplifier completely.

8.4.2 OverTemperature Protection (OTP)

If the junction temperature T_j > 155 °C the power stage will shut down immediately.

8.4.3 OverCurrent Protection (OCP)

The OCP can distinguish between an impedance drop of the loudspeaker and a low-ohmic short circuit.

If an impedance drop causes the output current to exceed 2 A, e.g. due to dynamic behavior of the loudspeaker, the amplifier will start limiting the current above 2 A. Therefore the current limiting feature will avoid audio interruption (audio holes) due to a loudspeaker impedance drop.

If a fault condition causes the output current to exceed 2 A, like a short circuit between the loudspeaker terminals or from the loudspeaker terminal to the supply lines or ground, the amplifier is switched off and a timer of 100 ms is started. The DIAG is set low for the first 50 ms of the timer. The timer will keep the power stage disabled for at least 100 ms.

Every 100 ms the amplifier will try to restart as long as the short circuit between the loudspeaker terminals remains. The average power dissipation in the TDA8933B will be low because the short circuit current will flow only during a very short time every 100 ms. If a short circuit occurs between a loudspeaker terminal and the supply lines or ground, the activated WP will keep the power stage disabled (no restart every 100 ms). Restart will take place after removing this short.

8.4.4 Window Protection (WP)

The window protection protects the amplifier against the following fault conditions:

- During the start-up sequence, when pin POWERUP is switched from Sleep mode to Mute mode. In the event of a short circuit at one of the output terminals to V_{DDP1}, V_{SSP1}, V_{DDP2} or V_{SSP2} the start-up procedure is interrupted and the TDA8933B waits for open circuit outputs. Because the check is done before enabling the power stages no large currents will flow in the event of a short circuit.
- When the amplifier is shut down completely due to activation of the OCP or because of a short circuit to one of the supply lines, then during restart (i.e. after 100 ms) the window protection will be activated. As a result the amplifier will not start up until the short circuit to the supply lines has been removed.

8.4.5 Supply voltage protection

If the supply voltage drops below 10 V the UnderVoltage Protection (UVP) circuit is activated and the system will shut down directly. This switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level the power stage is restarted after 100 ms.

If the supply voltage exceeds 36 V the OVP circuit is activated and the power stages will shut down. It is enabled again as soon as the supply voltage drops below the threshold level. The power stage is restarted after 100 ms.

Supply voltages > 40 V may damage the TDA8933B. Two conditions should be distinguished here:

- If the supply voltage is pumped to higher values by the TDA8933B application itself (see also Section 14.8), the OVP is triggered and the TDA8933B is shut down. The supply voltage will decrease and the TDA8933B is thus protected against any overstress.
- If a supply voltage > 40 V is caused by other or by external causes the TDA8933B will shut down, but the device can still be damaged since the supply voltage in this case will remain > 40 V. The OVP protection is not a supply clamp.

An additional UnBalance Protection (UBP) circuit compares the positive analog supply voltage V_{DDA} with the negative analog supply voltage V_{SSA} and is triggered if the difference between them exceeds a certain level. This level depends on the sum of both supply voltages. The UBP threshold levels can be defined as follows:

- LOW-level threshold: $V_{P(th)(ubp)l} < 8/5 \times V_{HVPREF}$
- HIGH-level threshold: $V_{P(th)(ubp)h} > 8/3 \times V_{HVPREF}$

In a symmetrical supply the UBP is released when the unbalance of the supply voltage is within 6 % of its starting value.

Table 6 shows an overview of all protections and their effect on the output signal.

Table 6. Overview of protections for the TDA8933B

Protection	Restart	
	When fault is removed	Every 100 ms
OTP	no	yes
OCP	yes	no
WP	yes	no
UVP	no	yes
OVP	no	yes
UBP	no	yes

8.5 Diagnostic input and output

Except for TF, whenever one of the protections is triggered pin DIAG is activated to LOW level (see Table 6). An internal current source will pull up the open-drain DIAG output to approximately 2.5 V. This current source can deliver approximately 50 μA. The DIAG pin refers to pin CGND. The diagnostic output signal during different short circuit conditions is illustrated in Figure 5. Using pin DIAG as input, a voltage < 0.8 V will put the device into Fault mode.

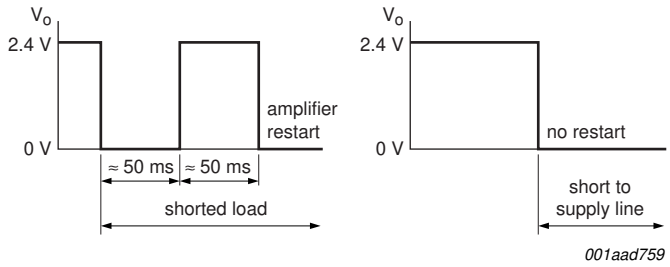


Fig 5. Diagnostic output for different short circuit conditions

8.6 Differential inputs

For a high common-mode rejection ratio and for maximum flexibility in the application the audio inputs are fully differential. By connecting the inputs anti-parallel the phase of one of the two channels can be inverted so that the amplifier can then operate as a mono BTL amplifier. The input configuration for a mono BTL application is illustrated in Figure 6.

In the SE configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies and minimizes supply pumping (see also Section 14.8).

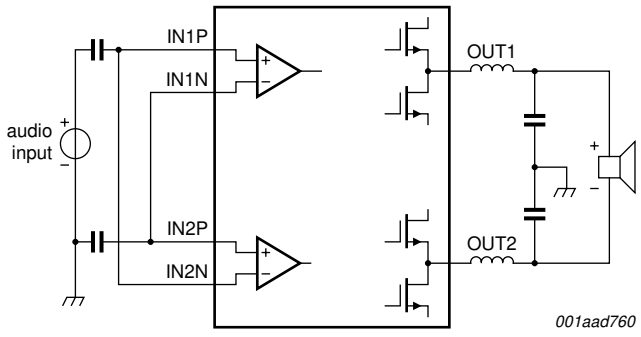


Fig 6. Input configuration for a mono BTL application

8.7 Output voltage buffers

When pin POWERUP is set HIGH the half-supply output voltage buffers are switched on in asymmetrical configuration. The start-up will then be pop-free because the device starts switching when the capacitor on pin HVPREF and the SE capacitors are completely charged.

Output voltage buffer pins:

- Pins HVP1 and HVP2: The time required for charging the SE capacitor depends on its value. The half-supply voltage output is disabled when the TDA8933B is used in a symmetrical supply application.
- Pin HVPREF: This output voltage reference buffer charges the capacitor on pin HVPREF.
- Pin INREF: This output voltage reference buffer charges the input reference capacitor on pin INREF, which applies the bias voltage for the inputs.

9. Internal circuitry

Table 7. Internal circuitry

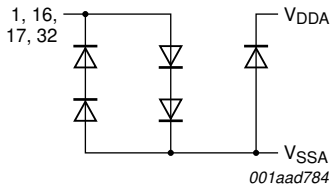
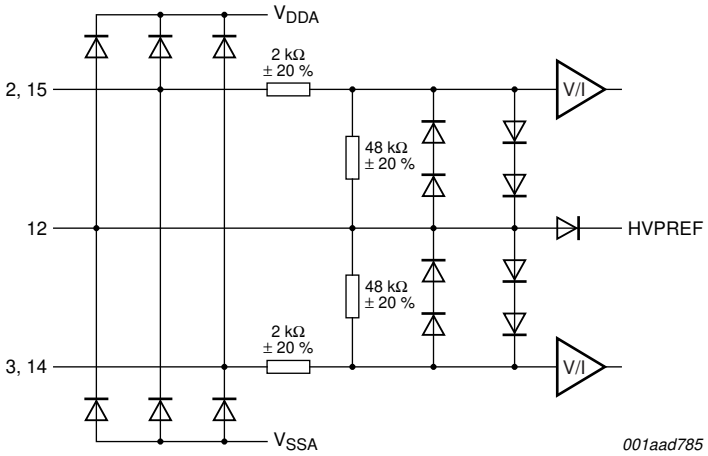
Pin	Symbol	Equivalent circuit
1	$V_{SSD(HW)}$	
16		
17		
32		
2	IN1P	
3	IN1N	
12	INREF	
14	IN2N	
15	IN2P	

Table 7. Internal circuitry

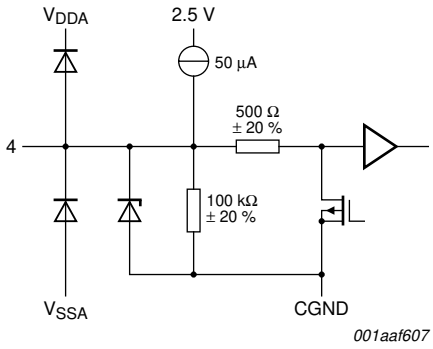
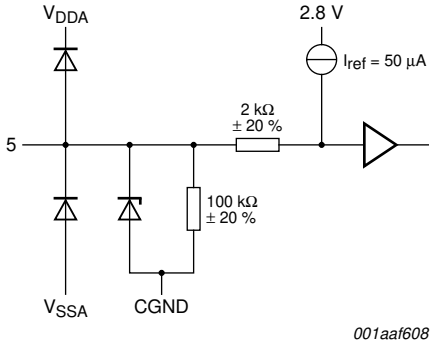
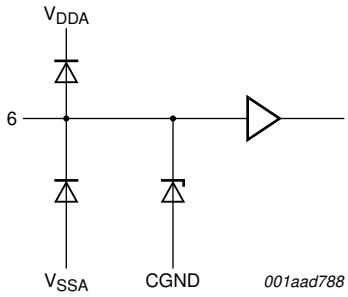
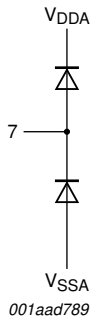
Pin	Symbol	Equivalent circuit
4	DIAG	
5	ENGAGE	
6	POWERUP	
7	CGND	

Table 7. Internal circuitry

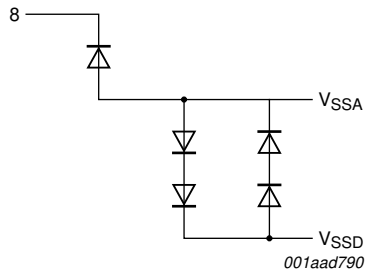
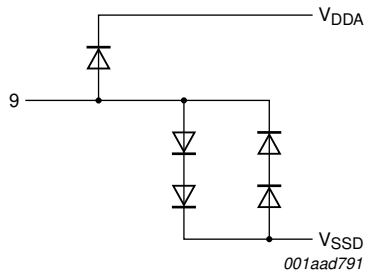
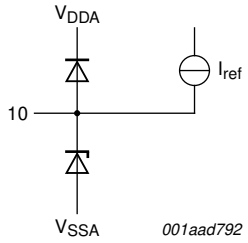
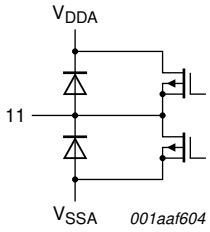
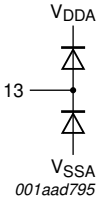
Pin	Symbol	Equivalent circuit
8	V_{DDA}	
9	V_{SSA}	
10	OSCREF	
11	HVPREF	
13	TEST	

Table 7. Internal circuitry

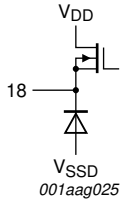
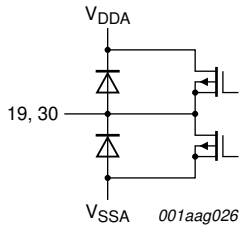
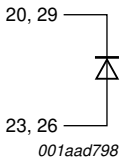
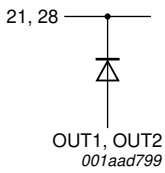
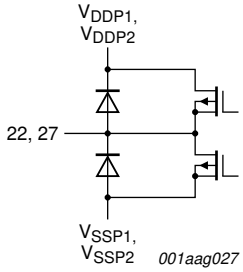
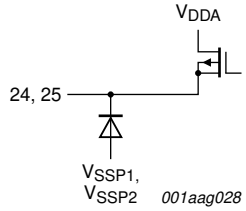
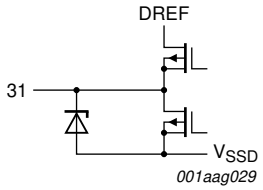
Pin	Symbol	Equivalent circuit
18	DREF	
19	HVP2	
30	HVP1	
20	V_{DDP2}	
23	V_{SSP2}	
26	V_{SSP1}	
29	V_{DDP1}	
21	BOOT2	
28	BOOT1	
22	OUT2	
27	OUT1	

Table 7. Internal circuitry

Pin	Symbol	Equivalent circuit
24	STAB2	
25	STAB1	
31	OSCIO	

10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	asymmetrical supply[1]		–0.3	+40.1	V
V_x	voltage on pin x					
	IN1P, IN1N, IN2P, IN2N		[2]	–5	+5	V
	OSCREF, OSCIO, TEST		[3]	$V_{SSD(HW)}$ – 0.3	5	V
	POWERUP, ENGAGE, DIAG		[4]	V_{CGND} – 0.3	6	V
	all other pins		[5]	V_{SS} – 0.3	V_{DD} + 0.3	V
I_{ORM}	repetitive peak output current	maximum output current limiting	[6]	2	-	A
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P	power dissipation			-	5	W
V_{esd}	electrostatic discharge voltage	human body model	[7]	–2000	+2000	V
		machine model	[8]	–200	+200	V

[1] $V_P = V_{DDP1} - V_{SSP1} = V_{DDP2} - V_{SSP2}$

[2] Measured with respect to pin INREF; $V_x < V_{DD} + 0.3$ V.

[3] Measured with respect to pin $V_{SSD(HW)}$; $V_x < V_{DD} + 0.3$ V.

[4] Measured with respect to pin CGND; $V_x < V_{DD} + 0.3$ V.

[5] $V_{SS} = V_{SSP1} = V_{SSP2}$; $V_{DD} = V_{DDP1} = V_{DDP2}$.

[6] Current limiting concept.

[7] Human Body Model (HBM); R_s = 1500 Ω; C = 100 pF. For pins 2, 3, 11, 14 and 15 V_{esd} = 1800V.

[8] Machine Model (MM); R_s = 0 Ω; C = 200 pF; L = 0.75 µH.

11. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	free air natural convection					
		JEDEC test board	[1]	-	47	50	K/W
		Two-layer application board	[2]	-	48	-	K/W
		Three-layer application board	[3]	-	30	-	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead			-	-	30	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		[4]	-	-	2	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	free-air natural convection		-	4.0	-	K/W

[1] Measured on a JEDEC high K-factor test board (standard EIA/JESO 51-7) in free air with natural convection.

[2] Measured on a two-layer application board (55 mm × 40 mm), 35 µm copper, FR4 base material in free air with natural convection.

[3] Measured on a three-layer application board (70 mm × 50 mm), 35 µm copper, FR4 base material in free air with natural convection.

[4] Strongly dependent on where the measurement is taken on the package.

12. Static characteristics

Table 10. Characteristics

V_P = 25 V, f_{osc} = 320 kHz and T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_P	supply voltage	asymmetrical supply	10	25	36	V
		symmetrical supply	±5	±12.5	±18	V
I_P	supply current	Sleep mode	-	0.6	1.0	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers or filter connected	-	40	50	mA
Series resistance output switches						
R_{DSon}	drain-source on-state resistance	T_j = 25 °C	-	380	-	mΩ
		T_j = 125 °C	-	545	-	mΩ
Power-up input: pin POWERUP[1]						
V_I	input voltage		0	-	6.0	V
I_I	input current	V_I = 3 V	-	1	20	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	6.0	V

Table 10. Characteristics *...continued*

V_P = 25 V, f_{osc} = 320 kHz and T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Engage input: pin ENGAGE[1]						
V_O	output voltage		2.4	2.8	3.1	V
V_I	input voltage		0	-	6.0	V
I_O	output current	V_I = 3 V	-	50	60	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2.4	-	6.0	V
Diagnostic output: pin DIAG[1]						
V_O	output voltage	protection activated; see Table 6	-	-	0.8	V
		Operating mode	2	2.5	3.3	V
Bias voltage for inputs: pin INREF						
$V_{O(bias)}$	bias output voltage	Reference to V_{SSA}	-	2.1	-	V
Half-supply voltage						
Pins HVP1 and HVP2						
V_O	output voltage	half-supply voltage to charge SE capacitor	$0.5V_P - 0.2$ V	$0.5V_P$	$0.5V_P + 0.2$ V	V
I_O	output current	$V_{HVP1} = V_{HVP2} = V_O - 1$ V	-	50	-	mA
Pin HVPREF						
V_O	output voltage	half-supply reference voltage in Mute mode	$0.5V_P - 0.2$ V	$0.5V_P$	$0.5V_P + 0.2$ V	V
Reference voltage for internal logic: pin DREF						
V_O	output voltage	reference to V_{SSA}	4.5	4.8	5.1	V
Amplifier outputs: pins OUT1 and OUT2						
$V_{O(offset)}$	output offset voltage	SE; with respect to HVPREF				
		Mute mode	-	-	15	mV
		Operating mode	-	-	100	mV
		BTL				
		Mute mode	-	-	20	mV
		Operating mode	-	-	150	mV
Stabilizer output: pins STAB1, STAB2						
V_O	output voltage	Mute mode and Operating mode; with respect to pins V_{SSP1} and V_{SSP2}	10	11	12	V
Voltage protections						
$V_{P(uvp)}$	undervoltage protection supply voltage		8.0	9.5	9.9	V
$V_{P(ovp)}$	overvoltage protection supply voltage		36.1	38.5	40	V

Table 10. Characteristics *...continued*

V_P = 25 V, f_{osc} = 320 kHz and T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{P(th)(ubp)l}$	low unbalance protection threshold supply voltage	V_P = 22 V; V_{HVPREF} = 11 V	-	-	18	V
$V_{P(th)(ubp)h}$	high unbalance protection threshold supply voltage	V_P = 22 V; V_{HVPREF} = 11 V	29	-	-	V
Current protections						
$I_{O(ocp)}$	overcurrent protection output current	current limiting	2.0	2.5	-	A
Temperature protection						
$T_{act(th\_prot)}$	thermal protection activation temperature		155	-	160	°C
$T_{act(th\_fold)}$	thermal foldback activation temperature		140	-	150	°C
Oscillator reference: pin OSCIO[2]						
V_{IH}	HIGH-level input voltage		4.0	-	5.0	V
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{OH}	HIGH-level output voltage		4.0	-	5.0	V
V_{OL}	LOW-level output voltage		0	-	0.8	V
$N_{slave(max)}$	maximum number of slaves	driven by one master	12	-	-	-

[1] Measured with respect to pin CGND.

[2] Measured with respect to pin $V_{SSD(HW)}$.

13. Dynamic characteristics

Table 11. Switching characteristics

V_P = 25 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	R_{osc} = 39 kΩ	-	320	-	kHz
		range	300	-	500	kHz
Timing PWM output: pins OUT1 and OUT2						
t_r	rise time	I_O = 0 A	-	10	-	ns
t_f	fall time	I_O = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_O = 0 A	-	80	-	ns

Table 12. SE characteristics

V_P = 25 V, R_L = 2 × 8 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [1] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power per channel[2]				
		R_L = 4 Ω; V_P = 17 V				
		THD+N = 0.5 %, f_i = 1 kHz	5.9	6.8	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	6.8	-	W
		THD+N = 10 %, f_i = 1 kHz	7.5	8.5	-	W
		THD+N = 10 %, f_i = 100 Hz	-	8.5	-	W
		R_L = 8 Ω; V_P = 25 V				
		THD+N = 0.5 %, f_i = 1 kHz	7.3	8.2	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	8.2	-	W
		THD+N = 10 %, f_i = 1 kHz	9.3	10.3	-	W
		THD+N = 10 %, f_i = 100 Hz	-	10.3	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W [3]				
		f_i = 1 kHz	-	0.014	0.1	%
		f_i = 6 kHz	-	0.05	0.1	%
$G_{v(cl)}$	closed-loop voltage gain	V_i =100 mV; no load	29	30	31	dB
$\lvert\Delta G_V\rvert$	voltage gain difference		-	0.5	1	dB
α_{cs}	channel separation	P_o = 1 W; f_i = 1 kHz	70	80	-	dB
SVRR	supply voltage ripple rejection	Operating mode [4]				
		f_i = 100 Hz	-	60	-	dB
		f_i = 1 kHz	40	50	-	dB
$\lvert Z_i\rvert$	input impedance	differential	70	100	-	kΩ
$V_{n(o)}$	output noise voltage	Operating mode; R_i = 0 Ω [5]	-	100	150	μV
		Mute mode [5]	-	70	100	μV
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS)	-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)	-	75	-	dB
η_{po}	output power efficiency	V_P = 17 V; R_L = 4 Ω; P_o = 8 W/channel	86	89	-	%
		V_P = 25 V; R_L = 8 Ω; P_o = 10 W/channel	89	92	-	%

[1] R_S is the total series resistance of an inductor and a ESR single ended capacitor in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] V_{ripple} = 2 V (p-p); R_i = 0 Ω.

[5] B = 20 Hz to 20 kHz, AES17 brick wall.

Table 13. BTL characteristics

V_P = 25 V, R_L = 16 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [1] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power[2]					
		R_L = 8 Ω; V_P = 17 V					
		THD+N = 0.5 %, f_i = 1 kHz		11.9	13.7	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	13.7	-	W
		THD+N = 10 %, f_i = 1 kHz		15.4	17.1	-	W
		THD+N = 10 %, f_i = 100 Hz		-	17.1	-	W
		R_L = 16 Ω; V_P = 25 V					
		THD+N = 0.5 %, f_i = 1 kHz		14.9	16.5	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	16.5	-	W
		THD+N = 10 %, f_i = 1 kHz		18.9	20.6	-	W
		THD+N = 10 %, f_i = 100 Hz		-	20.6	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.01	0.1	%
		f_i = 6 kHz		-	0.04	0.1	%
$G_{v(cl)}$	closed-loop voltage gain			35	36	37	dB
$\|Z_i\|$	input impedance	differential		35	50	-	kΩ
$V_{n(o)}$	output noise voltage	R_i = 0 Ω					
		Operating mode	[4]	-	100	150	μV
		Mute mode	[4]	-	70	100	μV
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS)		-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	P_o = 17 W; V_P = 17 V; R_L = 8 Ω	[5]	89	91	-	%
		P_o = 21 W; V_P = 25 V; R_L = 16 Ω		92	94	-	%

[1] R_S is the total series resistance of an inductor and a ESR single ended capacitor in the application.

[2] Output power is measured indirectly; based on R_{DSon} measurement.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] B = 22 Hz to 20 kHz, AES17 brick wall.

[5] $$\eta_{po} = \frac{2 \cdot P_o}{2 \cdot P_o + P}$$

14. Application information

14.1 Output power estimation

The output power P_o at THD+N = 0.5 %, just before clipping, for the SE and the BTL configurations can be estimated using Equation 2 and Equation 3.

SE configuration:

$$P_{o(0.5\%)} = \frac{\left[\left(\frac{R_L}{R_L + R_{DSon} + R_s + R_{ESR}}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{8 \times R_L} \quad (2)$$

BTL configuration:

$$P_{o(0.5\%)} = \frac{\left[\left(\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{2 \times R_L} \quad (3)$$

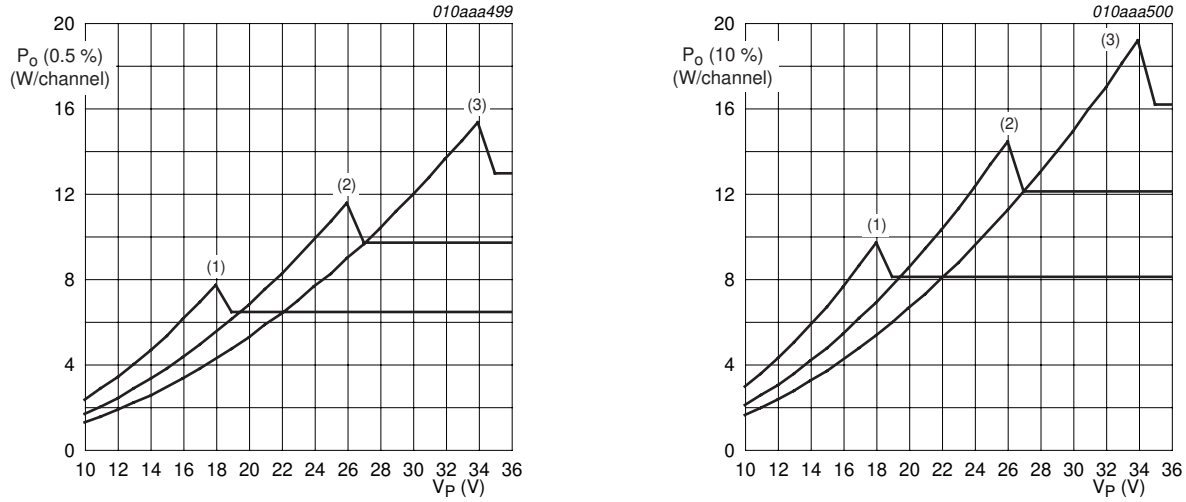
Where:

- V_P = supply voltage $V_{DDP1} - V_{SSP1}$ (V) or $V_{DDP2} - V_{SSP2}$ (V)
- R_L = load resistance (Ω)
- R_{DSon} = drain-source on-state resistance (Ω)
- R_s = series resistance output inductor (Ω)
- R_{ESR} = Equivalent Series Resistance SE capacitance (Ω)
- $t_{w(min)}$ = minimum pulse width(s); 80 ns typical
- f_{osc} = oscillator frequency (Hz); 320 kHz typical with R_{osc} = 39 kΩ

The output power P_o at THD+N = 10 % can be estimated by:

$$P_{o(10\%)} = 1.25 \times P_{o(0.5\%)} \quad (4)$$

Figure 7 and Figure 8 show the estimated output power at THD+N = 0.5 % and THD+N = 10 % as a function of the supply voltage for SE and BTL configurations at different load impedances. The output power is calculated with: R_{DSon} = 0.38 Ω (at T_j = 25 °C), R_s = 0.05 Ω, R_{ESR} = 0.05 Ω and $I_{O(ocp)}$ = 2 A (minimum).



a. THD+N = 0.5 %

b. THD+N = 10 %

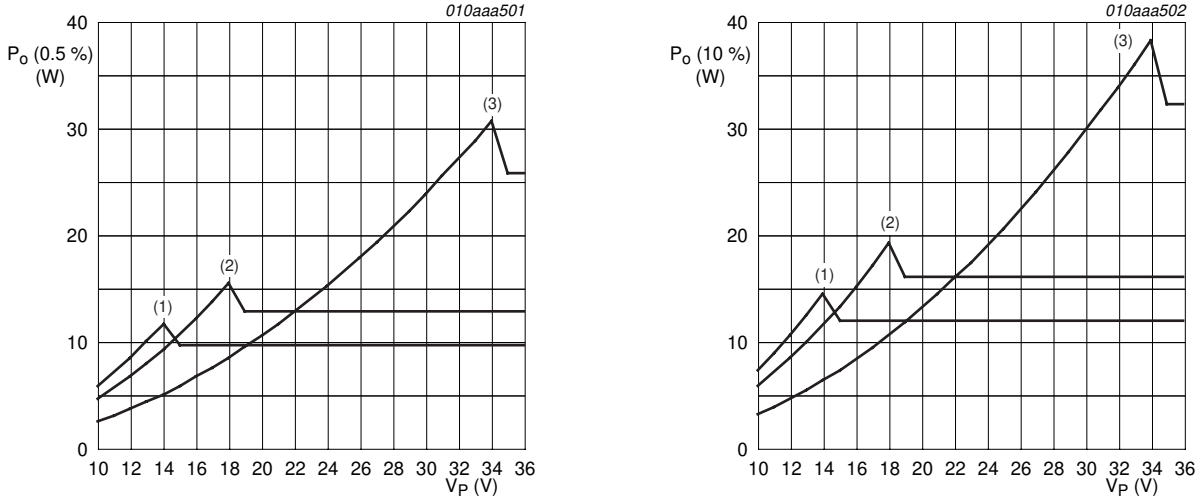
(1) R_L = 4 Ω

(2) R_L = 6 Ω

(3) R_L = 8 Ω

When the maximum current of 2 A is reached, the current limitation feature becomes active. See also Section 8.4.3 for OCP details.

Fig 7. SE output power as a function of supply voltage



a. THD+N = 0.5 %

b. THD+N = 10 %

(1) R_L = 6 Ω

(2) R_L = 8 Ω

(3) R_L = 16 Ω

When the maximum current of 2 A is reached, the current limitation feature becomes active. See also Section 8.4.3 for OCP details.

Fig 8. BTL output power as a function of supply voltage

14.2 Output current limitation

The peak output current $I_{O(max)}$ is internally limited to a minimum value of 2 A. During normal operation the output current should not exceed this threshold level, otherwise the signal will be distorted. The peak output current in SE or BTL configurations can be calculated using Equation 5 and Equation 6.

SE configuration:

$$I_{O(max)} \leq \frac{0.5 \times V_P}{R_L + R_{DSon} + R_s + R_{ESR}} \leq 2A \quad (5)$$

BTL configuration:

$$I_{O(max)} \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 2A \quad (6)$$

Where:

- V_P = supply voltage $V_{DDP1} - V_{SSP1}$ (V) or $V_{DDP2} - V_{SSP2}$ (V)
- R_L = load resistance (Ω)
- R_{DSon} = drain-source on-state resistance (Ω)
- R_s = series resistance output inductor (Ω)
- R_{ESR} = Equivalent Series Resistance SE capacitance (Ω)

Example:

An 8 Ω speaker in the BTL configuration can be used up to a supply voltage of 18 V without running into current limiting. Current limiting (clipping) will avoid audio holes but produces a similar distortion to voltage clipping.

14.3 Speaker configuration and impedance

For a flat frequency response (second-order Butterworth filter with an output frequency of 40 kHz) it is necessary to change the low-pass filter components L_{LC} and C_{LC} according to the speaker configuration and impedance. Table 14 shows the values required in practice.

Table 14. Filter component values

Configuration	R_L (Ω)	L_{LC} (μH)	C_{LC} (nF)
SE	4	22	680
	6	33	470
	8	47	330
BTL	8	22	680
	16	47	330

14.4 Single-ended capacitor

The SE capacitor forms a high-pass filter with the speaker impedance. This means that the frequency response will roll off with 20 dB per decade below f_{-3dB} and a cut-off frequency of 3 dB.

The 3 dB cut-off frequency is equal to:

$$f_{-3dB} = \frac{1}{2\pi \times R_L \times C_{SE}} \quad (7)$$

Where:

- f_{-3dB} = 3 dB cut-off frequency (Hz)
- R_L = load resistance (W)
- C_{SE} = single-ended capacitance (F); see Figure 32

Table 15 shows an overview of the required SE capacitor values in the case of a 60 Hz, 40 Hz or 20 Hz 3 dB cut-off frequency.

Table 15. SE capacitor values

Impedance (Ω)	C_{SE} (μF)		
	f_{-3dB} = 60 Hz	f_{-3dB} = 40 Hz	f_{-3dB} = 20 Hz
4	680	1000	2200
6	470	680	1500
8	330	470	1000

14.5 Gain reduction

The gain of the TDA8933B is internally fixed at 30 dB for SE and 36 dB for BTL. The gain can be reduced by a resistive voltage divider at the input (see Figure 9).

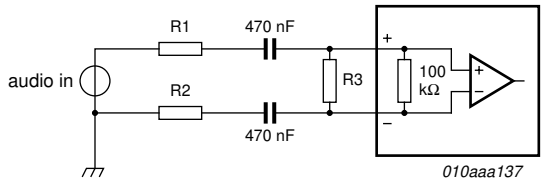


Fig 9. Input configuration for reducing gain

When applying a resistive divider, the total voltage gain $G_{v(tot)}$ can be calculated using Equation 8 and Equation 9:

$$G_{v(tot)} = G_{v(cl)} + 20log\left[\frac{R_{EQ}}{R_{EQ} + (R1 + R2)}\right] \quad (8)$$

Where:

- $G_{v(tot)}$ = total voltage gain (dB)
- $G_{v(cl)}$ = closed-loop voltage gain, fixed at 30 dB for SE (dB)
- R_{EQ} = equivalent resistance, R3 and Z_i (Ω)