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# DATA SHEET

## **TDA9855**

**I<sup>2</sup>C-bus controlled BTSC  
stereo/SAP decoder and audio  
processor**

Product specification  
Supersedes data of July 1994  
File under Integrated Circuits, IC02

1997 Nov 04

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

## TDA9855

### FEATURES

- Quasi alignment-free BTSC stereo decoder due to automatic adjustment of channel separation via I<sup>2</sup>C-bus
- High integration level with automatically tuned integrated filters
- Input level adjustment I<sup>2</sup>C-bus controlled
- Alignment-free SAP processing
- dbx noise reduction circuit
- I<sup>2</sup>C-bus transceiver.



### GENERAL DESCRIPTION

The TDA9855 is a bipolar-integrated BTSC stereo/SAP decoder with hi-fi audio processor (I<sup>2</sup>C-bus controlled) for application in TV sets.

### Audio processor

- Selector for internal and external signals (line in)
- Automatic volume level control
- Subwoofer or surround output with separate volume control
- Volume control
- Special loudness characteristic automatically controlled in combination with volume setting
- Bass and treble control
- Audio signal zero-crossing detection between any volume step switching
- Mute control at audio signal zero-crossing.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9855	SDIP52	plastic shrink dual in-line package; 52 leads (600 mil)	SOT247-1
TDA9855WP	PLCC68	plastic leaded chip carrier; 68 leads	SOT188-2

### LICENSE INFORMATION

A license is required for the use of this product. For further information, please contact

COMPANY	BRANCH	ADDRESS
THAT Corporation	Licensing Operations	734 Forest St. Marlborough, MA 01752 USA Tel.: (508) 229-2500 Fax: (508) 229-2590
	Tokyo Office	405 Palm House, 1-20-2 Honmachi Shibuya-ku, Tokyo 151 Japan Tel.: (03) 3378-0915 Fax: (03) 3374-5191

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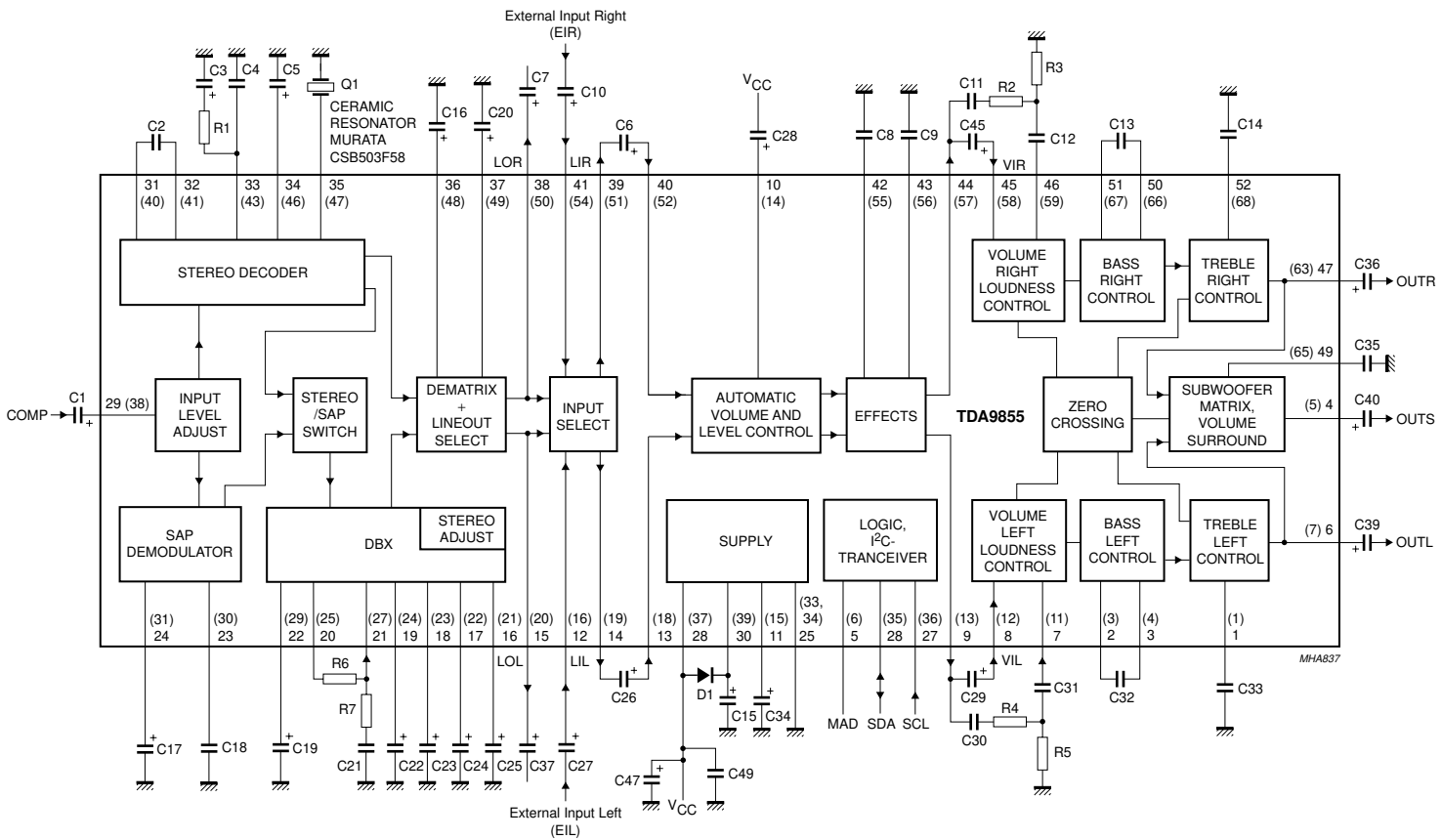
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		8.0	8.5	9.0	V
I <sub>CC</sub>	supply current		50	75	95	mA
V <sub>COMP(rms)</sub>	input signal voltage (RMS value)	100% modulation L + R; f <sub>i</sub> = 300 Hz	–	250	–	mV
V <sub>oR,L(rms)</sub>	output signal voltage (RMS value)	100% modulation L + R; f <sub>i</sub> = 300 Hz	–	500	–	mV
G <sub>LA</sub>	input level adjustment control	maximum gain	–	4	–	dB
		maximum attenuation	–	–3.5	–	dB
α <sub>CS</sub>	stereo channel separation	f <sub>L</sub> = 300 Hz; f <sub>R</sub> = 3 kHz	25	35	–	dB
THD <sub>L,R</sub>	total harmonic distortion L + R	f <sub>i</sub> = 1 kHz	–	0.2	–	%
V <sub>I, O(rms)</sub>	signal handling (RMS value)	THD < 0.5%	2	–	–	V
AVL	control range		–15	–	+6	dB
G <sub>c</sub>	volume control range		–71	–	+16	dB
L <sub>B</sub>	maximum loudness boost	f <sub>i</sub> = 40 Hz	–	17	–	dB
G <sub>bass</sub>	bass control range	f <sub>i</sub> = 40 Hz	–12	–	+16.5	dB
G <sub>treble</sub>	treble control range	f <sub>i</sub> = 15 kHz	–12	–	+12	dB
G <sub>s</sub>	subwoofer control range	f <sub>i</sub> = 40 Hz	–14	–	+14	dB
S/N	signal-to-noise ratio	line out (mono); V <sub>o</sub> = 0.5 V (RMS)				
		CCIR noise weighting filter (peak value)	–	60	–	dB
		DIN noise weighting filter (RMS value)	–	73	–	dBA
		audio section; V <sub>o</sub> = 2 V (RMS); gain = 0 dB				
CCIR noise weighting filter (peak value)	–	94	–	dB		
DIN noise weighting filter (RMS value)	–	107	–	dBA		

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## BLOCK DIAGRAM



The numbers given in parenthesis refer to the TDA9855WP version.

Fig.1 Block diagram.

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## Component list

Electrolytic capacitors  $\pm 20\%$ ; foil or ceramic capacitors  $\pm 10\%$ ; resistors  $\pm 5\%$ ; unless otherwise specified; see Fig.1.

COMPONENTS	VALUE	TYPE	REMARK
C1	10 $\mu$ F	electrolytic	63 V
C2	470 nF	foil	–
C3	4.7 $\mu$ F	electrolytic	63 V
C4	220 nF	foil	–
C5	10 $\mu$ F	electrolytic	63 V; $I_{leak} < 1.5 \mu$ A
C6	2.2 $\mu$ F	electrolytic	16 V
C7	4.7 $\mu$ F	electrolytic	16 V
C8	15 nF	foil	$\pm 5\%$
C9	15 nF	foil	$\pm 5\%$
C10	2.2 $\mu$ F	electrolytic	63 V
C11	8.2 nF	foil or ceramic	$\pm 5\%$ SMD 2220/1206
C12	150 nF	foil	$\pm 5\%$
C13	33 nF	foil	$\pm 5\%$
C14	5.6 nF	foil or ceramic	$\pm 5\%$ SMD 2220/1206
C15	100 $\mu$ F	electrolytic	16 V
C16	4.7 $\mu$ F	electrolytic	63 V
C17	4.7 $\mu$ F	electrolytic	63 V
C18	100 nF	foil	
C19	10 $\mu$ F	electrolytic	63 V
C20	4.7 $\mu$ F	electrolytic	63 V
C21	47 nF	foil	$\pm 5\%$
C22	1 $\mu$ F	electrolytic	63 V
C23	1 $\mu$ F	electrolytic	63 V
C24	10 $\mu$ F	electrolytic	63 V $\pm 10\%$
C25	10 $\mu$ F	electrolytic	63 V $\pm 10\%$
C26	2.2 $\mu$ F	electrolytic	16 V
C27	2.2 $\mu$ F	electrolytic	63 V
C28	4.7 $\mu$ F	electrolytic	63 V $\pm 10\%$
C29	2.2 $\mu$ F	electrolytic	16 V
C30	8.2 nF	foil or ceramic	$\pm 5\%$ SMD 2220/1206
C31	150 nF	foil	$\pm 5\%$
C32	33 nF	foil	$\pm 5\%$
C33	5.6 nF	foil or ceramic	$\pm 5\%$ SMD 2220/1206
C34	100 $\mu$ F	electrolytic	16 V
C35	150 nF	foil	$\pm 5\%$
C36	4.7 $\mu$ F	electrolytic	16 V
C37	4.7 $\mu$ F	electrolytic	16 V
C39	4.7 $\mu$ F	electrolytic	16 V
C40	4.7 $\mu$ F	electrolytic	16 V

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COMPONENTS	VALUE	TYPE	REMARK
C45	2.2 $\mu$ F	electrolytic	16 V
C47	220 $\mu$ F	electrolytic	25 V
C49	100 nF	foil or ceramic	SMD 1206
D1	–	–	general purpose diode
R1	2.2 k $\Omega$	–	–
R2	20 k $\Omega$	–	–
R3	2.2 k $\Omega$	–	–
R4	20 k $\Omega$	–	–
R5	2.2 k $\Omega$	–	–
R6	8.2 k $\Omega$	–	$\pm 2\%$
R7	160 $\Omega$	–	$\pm 2\%$
Q1		CSB503F58	radial leads
		CSB503JF958	alternative as SMD

## PINNING

SYMBOL	PINS		DESCRIPTION
	PLCC68	SDIP52	
TL	1	1	treble control capacitor, left channel
n.c.	2	–	not connected
B1L	3	2	bass control capacitor, left channel
B2L	4	3	bass control capacitor, left channel
OUTS	5	4	output subwoofer or output surround sound
MAD	6	5	programmable address bit (module address)
OUTL	7	6	output, left channel
n.c.	8 to 10	–	not connected
LDL	11	7	input loudness, left channel
VIL	12	8	input volume control, left channel
EOL	13	9	output effects, left channel
C <sub>AV</sub>	14	10	automatic volume control capacitor
V <sub>ref</sub>	15	11	reference voltage 0.5V <sub>CC</sub>
LIL	16	12	input line, left channel
n.c.	17	–	not connected
AVL	18	13	input automatic volume control, left channel
SOL	19	14	output selector, left channel
LOL	20	15	output line control, left channel
C <sub>TW</sub>	21	16	capacitor timing wideband for dbx
C <sub>TS</sub>	22	17	capacitor timing spectral for dbx
C <sub>W</sub>	23	18	capacitor wideband for dbx
C <sub>S</sub>	24	19	capacitor spectral for dbx
VEO	25	20	variable emphasis output for dbx

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SYMBOL	PINS		DESCRIPTION
	PLCC68	SDIP52	
n.c.	26	–	not connected
VEI	27	21	variable emphasis input for dbx
n.c.	28	–	not connected
C <sub>NR</sub>	29	22	capacitor noise reduction for dbx
C <sub>M</sub>	30	23	capacitor mute for SAP
C <sub>DEC</sub>	31	24	capacitor DC-decoupling for SAP
n.c.	32	–	not connected
AGND	33	–	analog ground
DGND	34	–	digital ground
GND	–	25	ground
SDA	35	26	serial data input/output (I <sup>2</sup> C-bus)
SCL	36	27	serial clock input (I <sup>2</sup> C-bus)
V <sub>CC</sub>	37	28	supply voltage
COMP	38	29	composite input signal
V <sub>CAP</sub>	39	30	capacitor for electronic filtering of supply
C <sub>P1</sub>	40	31	capacitor for pilot detector
C <sub>P2</sub>	41	32	capacitor for pilot detector
n.c.	42	–	not connected
C <sub>PH</sub>	43	33	capacitor for phase detector
n.c.	44, 45	–	not connected
C <sub>ADJ</sub>	46	34	capacitor for filter adjustment
CER	47	35	ceramic resonator
C <sub>MO</sub>	48	36	capacitor DC-decoupling mono
C <sub>SS</sub>	49	37	capacitor DC-decoupling stereo/SAP
LOR	50	38	output line control, right channel
SOR	51	39	output selector, right channel
AVR	52	40	input automatic volume control, right channel
n.c.	53	–	not connected
LIR	54	41	input line control, right channel
C <sub>PS2</sub>	55	42	capacitor 2 pseudo function
C <sub>PS1</sub>	56	43	capacitor 1 pseudo function
EOR	57	44	output effects, right channel
VIR	58	45	input volume control, right channel
LDR	59	46	input loudness, right channel
n.c.	60 to 62	–	not connected
OUTR	63	47	output, right channel
n.c.	64	48	not connected
SW	65	49	filter capacitor for subwoofer



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SYMBOL	PINS		DESCRIPTION
	PLCC68	SDIP52	
B2R	66	50	bass control capacitor, right channel
B1R	67	51	bass control capacitor, right channel
TR	68	52	treble control capacitor

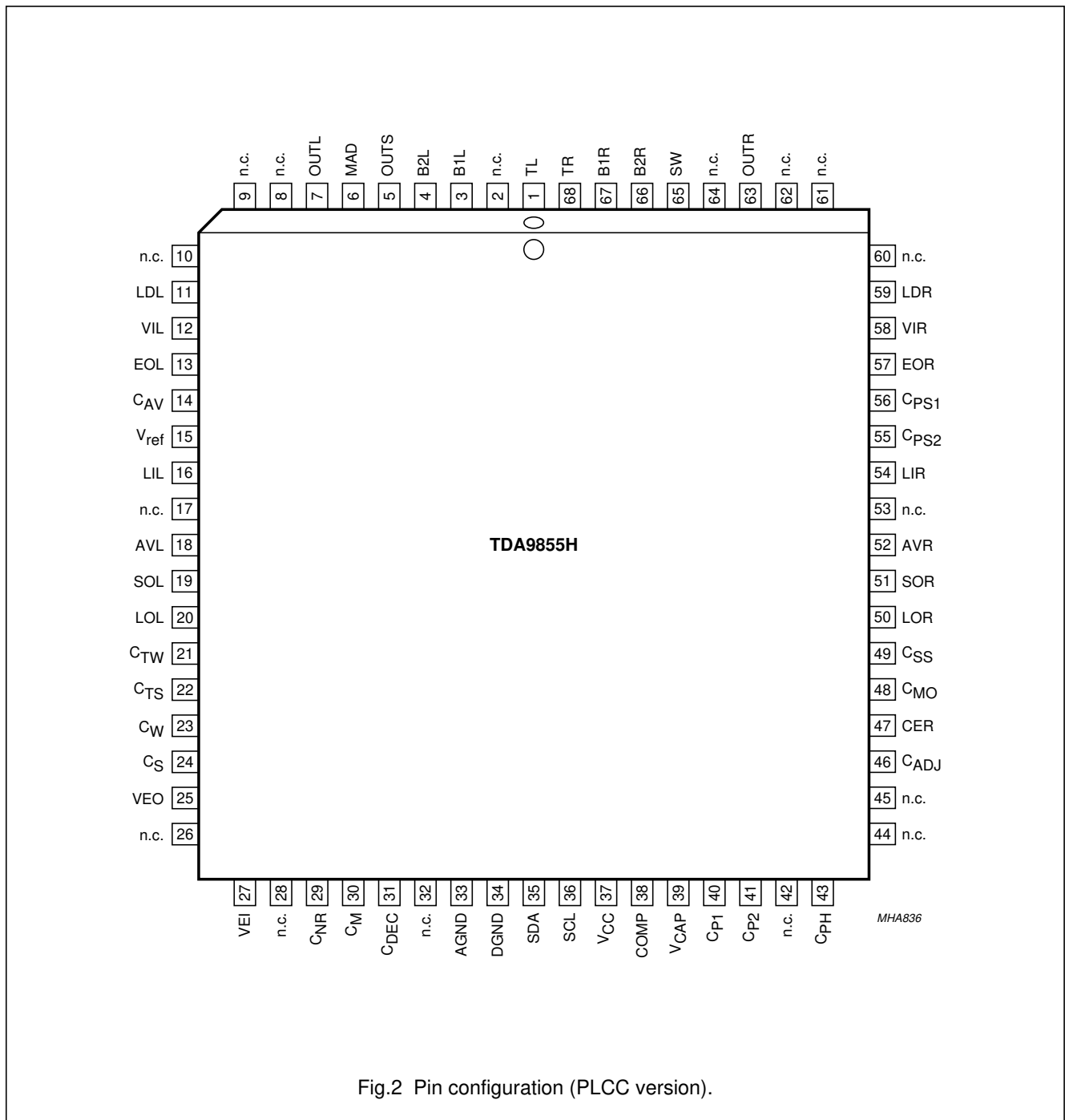


Fig.2 Pin configuration (PLCC version).

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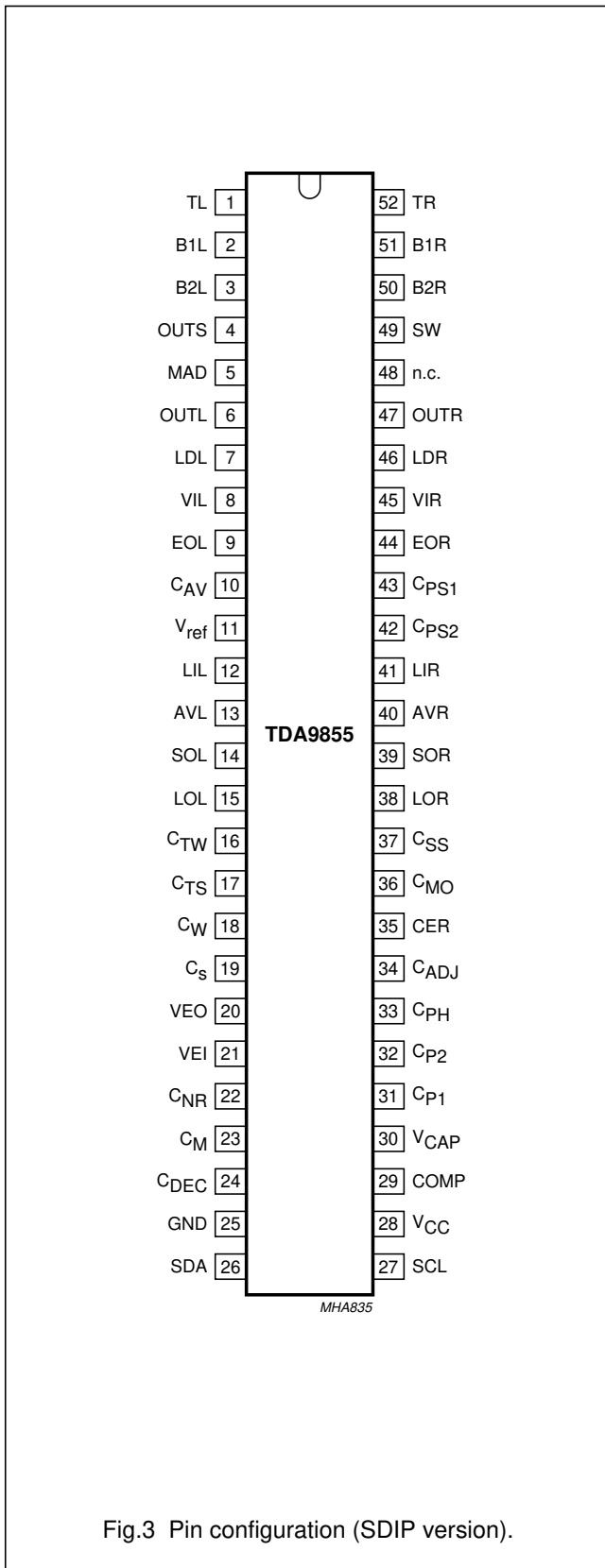


Fig.3 Pin configuration (SDIP version).

FUNCTIONAL DESCRIPTION

Decoder

INPUT LEVEL ADJUSTMENT

The composite input signal is fed to the input level adjustment stage. In order to compensate tolerances of the FM demodulator which supplied the composite input signal, the TDA9855 provides an input level adjustment stage. The control range is from -3.5 to +4.0 dB in steps of 0.5 dB. The subaddress control 3 of Tables 5 and 6 and the level adjust setting of Table 22 allows an optimum signal adjustment during the set alignment in the production line. This value has to be stored in a non-volatile memory. The maximum input signal voltage is 2 V (RMS).

STEREO DECODER

The output signal of the level adjustment stage is coupled to a low-pass filter which suppresses the baseband noise above 125 kHz. The composite signal is then fed into a pilot detector/pilot cancellation circuit and into the MPX demodulator. The main L + R signal passes a 75 μs fixed de-emphasis filter and is fed into the dematrix circuit. The decoded sub-signal L - R is sent to the stereo/SAP switch. To generate the pilot signal the stereo demodulator uses a PLL circuit including a ceramic resonator. The stereo channel separation can be adjusted by an automatic procedure or manually. For a detailed description see Section "Adjustment procedure". The stereo identification can be read by the I<sup>2</sup>C-bus (see Table 2). Two different pilot thresholds can be selected via the I<sup>2</sup>C-bus (see Table 24).

SAP DEMODULATOR

The composite signal is fed from the output of the input level adjustment stage to the SAP demodulator circuit through a 5f<sub>H</sub> (f<sub>H</sub> = horizontal frequency) band-pass filter. The demodulator level is automatically controlled. The SAP demodulator includes internal noise and field strength detectors that mute the SAP output in the event of insufficient signal conditions. The SAP identification signal can be read by the I<sup>2</sup>C-bus (see Table 2).

SWITCH

The stereo/SAP switch feeds either the L - R signal or the SAP demodulator output signal via the internal dbx noise reduction circuit to the dematrix/line out select circuit. Table 21 shows the different switch modes provided at the output pins LOR and LOL.

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### dbx DECODER

The circuit includes all blocks required for the noise reduction system in accordance with the BTSC system specification. The output signal is fed through a 73  $\mu$ s fixed de-emphasis circuit to the dematrix block.

### INTEGRATED FILTERS

The filter functions necessary for stereo and SAP demodulation and part of the dbx filter circuits are provided on-chip using transistor circuits. The required filter accuracy is attained by an automatic filter alignment circuit.

### Audio processor

#### SELECTOR

The selector allows selecting either the internal line out signals LOR or LOL (dematrix output) or the external line in signals LIR and LIL and combines the left and right signals in several modes (see Table 12). The input signal capability of the line inputs (LIR/LIL) is 2 V (RMS). The output of the selector is AC-coupled to the automatic volume level control circuit via pins SOR/SOL and AVR/AVL to avoid offset voltages.

#### AUTOMATIC VOLUME LEVEL CONTROL

The automatic volume level stage controls its output voltage to a constant level of typically 200 mV (RMS) from an input voltage range of 0.1 to 1.1 V (RMS). The circuit adjusts variations in modulation during broadcasting and due to changes in the programme material. The function can be switched **off**. To avoid audible 'plops' during the permanent operation of the AVL circuit a soft blending scheme has been applied between the different gain stages. A capacitor (4.7  $\mu$ F) at pin C<sub>AV</sub> determines the attack and decay time constants. In addition the ratio of attack and decay time can be changed via the I<sup>2</sup>C-bus (see notes 7 and 8 of Chapter "Characteristics").

#### EFFECTS

The audio processor section offers the following mode selections: linear stereo, pseudo stereo, spatial stereo and forced mono. The spatial mode provides an antiphase crosstalk of 30% or 52% (switchable via the I<sup>2</sup>C-bus; see Table 18).

#### VOLUME/LOUDNESS

The volume control range is from +16 dB to -71 dB in steps of 1 dB and ends with a mute step (see Table 8). Balance control is achieved by the independent volume

control of each channel. The volume control blocks operate in combination with the loudness control. The filter is linear when maximum gain for volume control is selected. The filter characteristic changes automatically over a range of 28 dB down to a setting of -12 dB. At -12 dB volume control the maximum loudness boost is obtained. The filter characteristic is determined by external components. The proposed application provides a maximum boost of 17 dB for bass and 4.5 dB for treble. The loudness may be switched **on** or **off** via I<sup>2</sup>C-bus control (see Table 14). The left and right volume control stages include two independent zero-crossing detectors. In the zero-crossing mode a change in volume is automatically activated but not executed. The execution is enabled at the next zero-crossing of the signal. If a new volume step is activated before the previous one has been processed, the previous value will be executed first, and then the new value will be activated. If no zero-crossing occurs the next volume transmission will enforce the last activated volume setting.

The zero-crossing mode is realized between adjoining steps and between any steps, but not from any step to mute. In this case the GMU bit is required for use. In case only one channel has to be muted, two steps are necessary. The first step is a transmission of any step to -71 dB and the second step is the -71 dB step to mute mode. The step of -71 dB to mute mode has no zero-crossing but this is not relevant. This procedure has to be provided by software.

#### BASS CONTROL

A single external 33 nF capacitor for each channel in combination with a linear operational amplifier and internal resistors provides a bass control range of +16.5 to -12 dB in steps of 1.5 dB at low frequencies (40 Hz). Internally the basic step width is 3 dB, with intermediate steps obtained by a toggle function that provides an additional 1.5 dB boost or attenuation (see Table 9). It should be noted that both loudness and bass control together result in a maximum bass boost of 34.5 dB for low volume steps.

#### TREBLE CONTROL

The adjustable range of the treble control stage is from -12 to +12 dB in steps of 3 dB. The filter characteristic is determined by an external 5.6 nF capacitor for each channel. The logic circuitry is arranged in a way that the same data words (06H to 16H) can be used for both tone controls if a bass control range from -12 to +12 dB and a treble control range from -12 to +12 dB with 3 dB steps are used (see Tables 9 and 10).

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### SUBWOOFER; SURROUND SOUND CONTROL

The subwoofer or the surround mode can be activated with the control bit SUR (see Table 6). A low bit provides an output signal  $\frac{1}{2}(L + R)$  in subwoofer mode, a high bit selects surround mode and provides an output signal  $\frac{1}{2}(L - R)$ . The signal is fed through a volume control stage with a range from +14 to -14 dB in 2 dB steps on top of the main channel control to the output pin OUTS. The last setting is the mute position (see Table 11). The capacitor C35 at pin SW provides a 230 Hz low-pass filter in subwoofer mode. In surround mode this capacitor should be disconnected. If balance is not in mid position the selected left and right output levels will be combined.

### MUTE

The mute function can be activated independently with the last step of volume or subwoofer/surround control at the left, right or centre output. By setting the general mute bit GMU via the I<sup>2</sup>C-bus all audio part outputs are muted. All channels include an independent zero-crossing detector. The zero-crossing mute feature can be selected via bit TZCM:

TZCM = 0: forced mute with direct execution

TZCM = 1: execution in time with signal zero-crossing.

In the zero-crossing mode a change of the GMU bit is activated but not executed. The execution is enabled at the next zero-crossing of the signal. To avoid a large delay of mute switching, when very low frequencies are processed, or the output signal amplitude is lower than the DC offset voltage, the following I<sup>2</sup>C-bus transmissions are needed:

A first transmission for mute execution

A second transmission approximately 100 ms later, which must switch the zero-crossing mode to forced mute (TZCM = 0)

A third transmission to reactivate the zero-crossing mode (TZCM = 1). This transmission can take place immediately, but must follow before the next mute execution.

### Adjustment procedure

#### COMPOSITE INPUT LEVEL ADJUSTMENT

Apply the composite signal (from the FM demodulator) with 100% modulation (25 kHz deviation) L + R;  $f_i = 300$  Hz. Set input level control via the I<sup>2</sup>C-bus monitoring line output (500 mV  $\pm$  20 mV). Store the setting in a non-volatile memory. Adjustment of the spectral and

wideband expander is performed via the stereo channel separation adjust.

#### AUTOMATIC ADJUSTMENT PROCEDURE

- Capacitors of external inputs EIL and EIR must be grounded
- Composite input signal L = 300 Hz, R = 3.1 kHz, 14% modulation for each channel; volume gain +16 dB via the I<sup>2</sup>C-bus; to avoid annoying sound level set GMU bit to logic 1 during adjustment procedure
- Effects, AVL, loudness **off**
- Selector setting SC0, SC1 and SC2 = 0, 0, 0 (see Table 12)
- Line out setting bits: STEREO = 1, SAP = 0 (see Table 21)
- Start adjustment by transmission ADJ = 1 in register ALI3; the decoder will align itself
- After 1 second, stop alignment by transmitting ADJ = 0 in register ALI3 read the alignment data by an I<sup>2</sup>C-bus read operation from ALR1 and ALR2 (see Chapter "I<sup>2</sup>C-bus protocol") and store it in a non-volatile memory; the alignment procedure overwrites the previous data stored in ALI1 and ALI2
- Disconnect the capacitors of external inputs from ground.

#### MANUAL ADJUSTMENT

Manual adjustment is necessary when no dual tone generator is available (e.g. for service).

- Spectral and wideband data have to be set to 10000 (middle position for adjustment range)
- Composite input L = 300 Hz; 14% modulation
- Adjust channel separation by varying wideband data
- Composite input L = 3 kHz; 14% modulation
- Adjust channel separation by varying spectral data
- Iterative spectral/wideband operation for optimum adjustment
- Store data in non-volatile memory.

After every power-on, the alignment data and the input level adjustment data must be loaded from the non-volatile memory.

#### TIMING CURRENT FOR RELEASE RATE

Due to possible internal and external spreading, the timing current can be adjusted via the I<sup>2</sup>C-bus (see Table 25) as recommended by dbx.

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## Requirements for the composite input signal to ensure correct system performance

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
COMP <sub>L+R(rms)</sub>	composite input level for 100% modulation L + R; 25 kHz deviation; f <sub>i</sub> = 300 Hz; RMS value	measured at pin COMP	162	250	363	mV
ΔCOMP	composite input level spreading under operating conditions	T <sub>amb</sub> = -20 to +70 °C; aging; power supply influence	-0.5	-	+0.5	dB
Z <sub>o</sub>	output impedance	note 1	-	low-ohmic	5	kΩ
f <sub>lf</sub>	low frequency roll-off	25 kHz deviation L + R; -2 dB	-	-	5	Hz
f <sub>hf</sub>	high frequency roll-off	25 kHz deviation L + R; -2 dB	100	-	-	kHz
THD <sub>L,R</sub>	total harmonic distortion L + R	f <sub>i</sub> = 1 kHz; 25 kHz deviation	-	-	0.5	%
		f <sub>i</sub> = 1 kHz; 125 kHz deviation; note 2	-	-	1.5	%
S/N	signal-to-noise ratio L + R/noise	CCIR 468-2 weighted quasi peak; L + R; 25 kHz deviation; f <sub>i</sub> = 1 kHz; 75 μs de-emphasis critical picture modulation with sync only	44	-	-	dB
			54	-	-	dB
α <sub>SB</sub>	side band suppression mono into unmodulated SAP carrier; SAP carrier/side band	mono signal: 25 kHz deviation, f <sub>i</sub> = 1 kHz; side band: SAP carrier frequency ±1 kHz	46	-	-	dB
α <sub>SP</sub>	spectral spurious attenuation L + R/spurious	50 Hz to 100 kHz; mainly n × f <sub>H</sub> ; no de-emphasis; L + R; 25 kHz deviation, f = 1 kHz as reference	40	-	-	dB

### Notes

1. Low-ohmic preferred, otherwise the signal loss and spreading at COMP, caused by Z<sub>o</sub> and the composite input impedance (see Chapter "Characteristics", Section INPUT LEVEL ADJUSTMENT CONTROL) must be taken into account.
2. In order to prevent clipping at over-modulation (maximum deviation in the BTSC system for 100% modulation is 73 kHz).

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## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		0	9.5	V
V <sub>n</sub>	voltage of all other pins with respect to pin GND		0	V <sub>CC</sub>	V
T <sub>amb</sub>	operating ambient temperature		-20	+70	°C
T <sub>stg</sub>	storage temperature		-65	+150	°C
V <sub>esd</sub>	electrostatic handling	note 1	-2000	+2000	V
		note 2	-300	+300	V

## Notes

- Human body model: C = 100 pF; R = 1.5 kΩ.
- Charge device model: C = 200 pF; R = 0 Ω.

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air		
	SOT247-1		43	K/W
	SOT188-2		38	K/W

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## CHARACTERISTICS

All voltages are measured relative to GND;  $V_{CC} = 8.5\text{ V}$ ; source resistance  $R_s \leq 600\ \Omega$ ; output load  $R_L \geq 10\ \text{k}\Omega$ ;  $C_L \leq 2.5\ \text{nF}$ ; AC-coupled;  $f_i = 1\ \text{kHz}$ ;  $T_{\text{amb}} = 25\ \text{°C}$ ; volume gain control  $G_c = 0\ \text{dB}$ ; bass linear; treble linear; loudness **off**; AVL **off**; effects linear; composite input signal in accordance with BTSC standard; see Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>General</b>						
$V_{CC}$	supply voltage		8.0	8.5	9.0	V
$I_{CC}$	supply current		50	75	95	mA
$V_{DC}$	DC voltage at signal handling pins		–	$\frac{1}{2}V_{CC}$	–	V
<b>Decoder section</b>						
INPUT LEVEL ADJUSTMENT CONTROL						
$G_{LA}$	input level adjustment control	maximum gain	–	4.0	–	dB
		maximum attenuation	–	–3.5	–	dB
$G_{\text{step}}$	step resolution		–	0.5	–	dB
$V_{i(\text{rms})}$	maximum input voltage level (RMS value)		2	–	–	V
$Z_i$	input impedance		29.5	35	40.5	k $\Omega$
STEREO DECODER						
$MPX_{L+R(\text{rms})}$	input voltage level for 100% modulation L + R; 25 kHz deviation (RMS value)	input level adjusted via I <sup>2</sup> C-bus (L + R; $f_i = 300\ \text{Hz}$ ); monitoring line out	–	250	–	mV
$MPX_{L-R}$	input voltage level for 100% modulation L – R; 50 kHz deviation (peak value)		–	707	–	mV
$MPX_{(\text{max})}$	maximum headroom for L + R, L, R	$f_{\text{mod}} < 15\ \text{kHz}$ ; THD < 15% for 75 $\mu\text{s}$ equivalent input modulation	9	–	–	dB
$MPX_{\text{pilot}(\text{rms})}$	nominal stereo pilot voltage level (RMS value)		–	50	–	mV
$ST_{\text{on}(\text{rms})}$	pilot threshold voltage stereo <b>on</b> (RMS value)	data STS = 1	–	–	35	mV
		data STS = 0	–	–	30	mV
$ST_{\text{off}(\text{rms})}$	pilot threshold voltage stereo <b>off</b> (RMS value)	data STS = 1	15	–	–	mV
		data STS = 0	10	–	–	mV
$\text{hys}$	hysteresis		–	2.5	–	dB
$OUT_{L+R}$	output voltage level for 100% modulation L + R at LINE OUT	input level adjusted via I <sup>2</sup> C-bus (L + R; $f_i = 300\ \text{Hz}$ ); monitoring LINE OUT	480	500	520	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\alpha_{CS}$	stereo channel separation L/R at LINE OUT	aligned with dual tone 14% modulation; see Section "Adjustment procedure" in Chapter "Functional description"				
		$f_L = 300 \text{ Hz}; f_R = 3 \text{ kHz}$	25	35	–	dB
		$f_L = 300 \text{ Hz}; f_R = 8 \text{ kHz}$	20	30	–	dB
		$f_L = 300 \text{ Hz}; f_R = 10 \text{ kHz}$	15	25	–	dB
$f_{L,R}$	L, R frequency response	14% modulation; $f_{ref} = 300 \text{ Hz L or R}$				
		$f_i = 50 \text{ Hz to } 11 \text{ kHz}$	–3	–	–	dB
		$f_i = 12 \text{ kHz}$	–	–3	–	dB
$THD_{L,R}$	total harmonic distortion L, R at LINE OUT	modulation L or R 1% to 100%; $f_i = 1 \text{ kHz}$	–	0.2	1.0	%
S/N	signal-to-noise ratio	mono mode; CCIR 468-2 weighted; quasi peak; 500 mV output signal	50	60	–	dB
STEREO DECODER, OSCILLATOR (VCXO); note 1						
$f_o$	nominal VCXO output frequency ( $32f_H$ )	with nominal ceramic resonator	–	503.5	–	kHz
$f_{of}$	spread of free-running frequency	with nominal ceramic resonator	500.0	–	507.0	kHz
$\Delta f_H$	capture range frequency (nominal pilot)		$\pm 190$	$\pm 265$	–	Hz
SAP DEMODULATOR; note 2						
$SAP_{i(rms)}$	nominal SAP carrier input voltage level (RMS value)	15 kHz frequency deviation of intercarrier	–	150	–	mV
$SAP_{on(rms)}$	pilot threshold voltage SAP <b>on</b> (RMS value)		–	–	85	mV
$SAP_{off(rms)}$	pilot threshold voltage SAP <b>off</b> (RMS value)		35	–	–	mV
$SAP_{hys}$	hysteresis		–	2	–	dB
$SAP_{LEV}$	SAP output voltage level at LINE OUT	LINE OUT (LOL, LOR) in position SAP/SAP; $f_{mod} = 300 \text{ Hz};$ 100% modulation	–	500	–	mV
$f_{res}$	frequency response	14% modulation; 50 Hz to 8 kHz; $f_{ref} = 300 \text{ Hz}$	–3	–	–	dB
THD	total harmonic distortion	$f_i = 1 \text{ kHz}$	–	0.5	2.0	%



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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LINE OUT AT PINS LOL AND LOR						
$V_{o(rms)}$	nominal output voltage (RMS value)	100% modulation	–	500	–	mV
HEAD <sub>o</sub>	output headroom		9	–	–	dB
Z <sub>o</sub>	output impedance		–	80	120	Ω
V <sub>O</sub>	DC output voltage		0.45V <sub>CC</sub>	0.5V <sub>CC</sub>	0.55V <sub>CC</sub>	V
R <sub>L</sub>	output load resistance		5	–	–	kΩ
C <sub>L</sub>	output load capacitance		–	–	2.5	nF
$\alpha_{ct}$	idle crosstalk L, R into SAP	100% modulation; f <sub>i</sub> = 1 kHz; L or R; line out switched to SAP/SAP	50	–	–	dB
	idle crosstalk SAP into L, R	100% modulation; f <sub>i</sub> = 1 kHz; SAP; line out switched to stereo	50	–	–	dB
$\Delta V_{ST-SAP}$	output voltage difference if switched from L, R to SAP	250 Hz to 6.3 kHz	–	–	3	dB
dbx NOISE REDUCTION CIRCUIT						
t <sub>adj</sub>	stereo adjustment time	see Section “Adjustment procedure” in Chapter “Functional description”	–	–	1	s
I <sub>s</sub>	nominal timing current for nominal release rate of spectral RMS detector	I <sub>s</sub> can be measured at pin 17 (pin 22) via current meter connected to ½V <sub>CC</sub> + 1 V	–	24	–	μA
ΔI <sub>s</sub>	spread of timing current		–	–	15	%
I <sub>s(range)</sub>	timing current adjustment range	7 steps via I <sup>2</sup> C-bus	–	±30	–	%
I <sub>t</sub>	timing current for release rate of wideband RMS detector		–	1/3 I <sub>s</sub>	–	μA
Rel <sub>rate</sub>	nominal RMS detector release rate	nominal timing current and external capacitor values				
		wideband	–	125	–	dB/s
		spectral	–	381	–	dB/s

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Audio part</b>						
CIRCUIT SECTION FROM PINS LIL AND LIR TO PINS OUTL, OUTR AND OUTS; note 3						
B	roll-off frequencies	C <sub>6</sub> , C <sub>7</sub> , C <sub>10</sub> , C <sub>26</sub> , C <sub>27</sub> and C <sub>29</sub> = 2.2 μF; Z <sub>i</sub> = Z <sub>i(min)</sub> low frequency (-3 dB) high frequency (-0.5 dB)	- 20	- -	20 -	Hz kHz
THD	total harmonic distortion	V <sub>i</sub> = 1 V (RMS); G <sub>c</sub> = 0 dB; AVL <b>on</b>	-	0.2	0.5	%
		V <sub>i</sub> = 2 V (RMS); G <sub>c</sub> = 0 dB; AVL <b>on</b>	-	0.2	0.5	%
		V <sub>i</sub> = 1 V (RMS); G <sub>c</sub> = 0 dB; AVL <b>off</b>	-	0.05	-	%
		V <sub>i</sub> = 2 V (RMS); G <sub>c</sub> = 0 dB; AVL <b>off</b>	-	0.02	-	%
PSRR	power supply ripple rejection	V <sub>r(rms)</sub> < 200 mV; f <sub>i</sub> = 100 Hz	47	50	-	dB
α <sub>B</sub>	crosstalk between bus inputs and signal outputs	notes 4 and 5	-	110	-	dB
V <sub>no</sub>	noise output voltage	CCIR 468-2 weighted; quasi peak	-	40	80	μV
		measured in dBA	-	8	-	μV
α <sub>cs</sub>	channel separation	V <sub>i</sub> = 1 V; f <sub>i</sub> = 1 kHz	75	-	-	dB
		V <sub>i</sub> = 1 V; f <sub>i</sub> = 12.5 kHz	75	-	-	dB
SELECTOR (FROM PINS LOL, LOR, LIL AND LIR TO PINS SOL AND SOR)						
Z <sub>i</sub>	input impedance		16	20	24	kΩ
α <sub>s</sub>	input isolation of one selected source to any other input	f = 1 kHz; V <sub>i</sub> = 1 V	86	96	-	dB
		f = 12.5 kHz; V <sub>i</sub> = 1 V	80	96	-	dB
V <sub>i(rms)</sub>	maximum input voltage (RMS value)	THD < 0.5%	2	2.3	-	V
V <sub>offset</sub>	DC offset voltage at selector output by selection of any inputs		-	-	25	mV
Z <sub>o</sub>	output impedance		-	80	120	Ω
R <sub>L</sub>	output load resistance (AC)		5	-	-	kΩ
C <sub>L</sub>	output load capacitance		-	-	2.5	nF
G <sub>c</sub>	voltage gain, selector		-	0	-	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AUTOMATIC VOLUME LEVEL CONTROL (AVL)						
Z <sub>i</sub>	input impedance		8.8	11.0	13.2	kΩ
V <sub>i(rms)</sub>	maximum input voltage (RMS value)	THD < 0.2%	2	–	–	V
G <sub>v</sub>	gain, maximum boost		5	6	7	dB
	maximum attenuation		14	15	16	dB
G <sub>step</sub>	equivalent step width between the input stages (soft switching system)		–	1.5	–	dB
V <sub>i(rms)</sub>	input level at maximum boost (RMS value)	see Fig.4	–	0.1	–	V
	input level at maximum attenuation (RMS value)	see Fig.4	–	1.125	–	V
V <sub>o(rms)</sub>	output level in AVL operation (RMS value)	see Fig.4	160	200	250	mV
V <sub>DC(OFF)</sub>	DC offset between different gain steps	voltage at pin C <sub>AV</sub> 6.50 to 6.33 V or 6.33 to 6.11 V or 6.11 to 5.33 V or 5.33 to 2.60 V; note 6	–	–	6	mV
R <sub>att</sub>	discharge resistors for attack time constant	AT1 = 0; AT2 = 0; note 7	340	420	520	Ω
		AT1 = 1; AT2 = 0; note 7	590	730	910	Ω
		AT1 = 0; AT2 = 1; note 7	0.96	1.2	1.5	kΩ
		AT1 = 1; AT2 = 1; note 7	1.7	2.1	2.6	kΩ
I <sub>dec</sub>	charge current for decay time	normal mode; CCD = 0; note 8	1.6	2.0	2.4	μA
EFFECT CONTROLS						
α <sub>spat1</sub>	anti-phase crosstalk by spatial effect		–	52	–	%
α <sub>spat2</sub>			–	30	–	%
φ	phase shift by pseudo-stereo	see Fig.5	–	–	–	–
VOLUME TONE CONTROL PART (INPUT PINS VIL AND VIR TO PINS OUTX AND OUTS)						
Z <sub>i</sub>	volume input impedance		8.0	10.0	12.0	kΩ
Z <sub>o</sub>	output impedance		–	80	120	Ω
R <sub>L</sub>	output load resistance (AC)		5	–	–	kΩ
C <sub>L</sub>	output load capacitance		–	–	2.5	nF
V <sub>i(rms)</sub>	maximum input voltage (RMS value)	THD < 0.5%	2.0	2.15	–	V
V <sub>no</sub>	noise output voltage	CCIR 468-2 weighted; quasi peak	–	–	–	–
		G <sub>c</sub> = 16 dB	–	110	220	μV
		G <sub>c</sub> = 0 dB	–	33	50	μV
		mute position	–	10	–	μV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G <sub>c</sub>	total continuous control range	maximum boost	–	16	–	dB
		maximum attenuation	–	71	–	dB
G <sub>step</sub>	step resolution		–	1	–	dB
	step error between any adjoining step		–	–	0.5	dB
ΔG <sub>a</sub>	attenuator set error	G <sub>c</sub> = +16 to –50 dB	–	–	2	dB
		G <sub>c</sub> = –51 to –71 dB	–	–	3	dB
ΔG <sub>t</sub>	gain tracking error	G <sub>c</sub> = +16 to –50 dB	–	–	2	dB
α <sub>m</sub>	mute attenuation		80	–	–	dB
V <sub>DC(OFF)</sub>	DC step offset between any adjacent step	G <sub>c</sub> = +16 to 0 dB	–	0.2	10.0	mV
		G <sub>c</sub> = 0 to –71 dB	–	–	5	mV
	DC step offset between any step to mute	G <sub>c</sub> = +16 to +1 dB	–	2	15	mV
		G <sub>c</sub> = 0 to –71 dB	–	1	10	mV
LOUDNESS CONTROL PART						
L <sub>B</sub>	maximum loudness boost	loudness <b>on</b> ; referred to loudness <b>off</b> ; boost is determined by external components; see Fig.6  f <sub>i</sub> = 40 Hz f <sub>i</sub> = 10 kHz				
			–	17	–	dB
			–	4.5	–	dB
BASS CONTROL (see Fig.7)						
G <sub>bass</sub>	bass control maximum boost	f <sub>i</sub> = 40 Hz	15.5	16.5	17.5	dB
	maximum attenuation	f <sub>i</sub> = 40 Hz	11	12	13	dB
G <sub>step</sub>	step resolution	f <sub>i</sub> = 40 Hz	–	1.5	–	dB
	step error between any adjoining step		–	–	0.5	dB
V <sub>DC(OFF)</sub>	DC step offset between any adjacent step		–	–	15	mV
TREBLE CONTROL (see Fig.8)						
G <sub>treble</sub>	treble control maximum boost	f <sub>i</sub> = 15 kHz	11	12	13	dB
	maximum attenuation	f <sub>i</sub> = 15 kHz	11	12	13	dB
	maximum boost	f <sub>i</sub> > 15 kHz	–	–	15	dB
G <sub>step</sub>	step resolution	f <sub>i</sub> = 15 kHz	–	3	–	dB
	step error between any adjoining step		–	–	0.5	dB
V <sub>DC(OFF)</sub>	DC step offset between any adjacent step		–	–	10	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SUBWOOFER OR SURROUND CONTROL						
G <sub>s</sub>	subwoofer control	maximum boost; f <sub>i</sub> = 40 Hz	12	14	16	dB
		maximum attenuation; f <sub>i</sub> = 40 Hz	12	14	16	dB
G <sub>step</sub>	step resolution		–	2	–	dB
α <sub>m</sub>	mute attenuation		60	–	–	dB
V <sub>DC(OFF)</sub>	DC step offset between any adjacent step	G <sub>s</sub> = 0 to +14 dB	–	–	10	mV
		G <sub>s</sub> = 0 to –14 dB	–	–	5	mV
	DC step offset between any step to mute	G <sub>s</sub> = +2 to +14 dB without input offset (pin SW connected to V <sub>ref</sub> )	–	–	15	mV
		G <sub>s</sub> = +2 to +14 dB inclusive offset from OUTR, OUTL	–	–	50	mV
		G <sub>s</sub> = 0 to –14 dB	–	–	10	mV
R <sub>F</sub>	internal resistor for low-pass filter with external capacitor at pin SW		4	5	6	kΩ
L + R <sub>REJ</sub>	common mode rejection in surround sound at pin OUTS	mono signal at VIL/VIR; f = 1 kHz; V <sub>i</sub> = 1 V; balance = 0 dB	26	36	–	dB
MUTING AT POWER SUPPLY DROP FOR OUTL, OUTR AND OUTS						
V <sub>CC-DROP</sub>	supply drop for mute active		–	V <sub>CAP</sub> – 0.7	–	V
POWER-ON RESET; note 9						
V <sub>RESET(STA)</sub>	start of reset voltage	increasing supply voltage	–	–	2.5	V
		decreasing supply voltage	4.2	5	5.8	V
V <sub>RESET(END)</sub>	end of reset voltage	increasing supply voltage	5.2	6	6.8	V
<b>Digital part (I<sup>2</sup>C-bus pins); note 10</b>						
V <sub>IH</sub>	HIGH-level input voltage		3	–	V <sub>CC</sub>	V
V <sub>IL</sub>	LOW-level input voltage		–0.3	–	+1.5	V
I <sub>IH</sub>	HIGH-level input current		–10	–	+10	μA
I <sub>IL</sub>	LOW-level input current		–10	–	+10	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>IL</sub> = 3 mA	–	–	0.4	V

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## Notes to the characteristics

1. The oscillator is designed to operate together with a MURATA resonator CSB503F58 for TDA9855. Change of the resonator supplier is possible, but the resonator specification must be close to CSB503F58 for TDA9855.
2. The internal SAP carrier level is determined by the composite input level and the level adjustment gain.
3. Select in to input line control.

4. Crosstalk:  $20 \log \frac{V_{\text{bus(p-p)}}}{V_{\text{o(rms)}}}$

5. The transmission contains:
  - a) Total initialization with MAD and SAD for volume and 11 DATA words, see also definition of characteristics
  - b) Clock frequency = 50 kHz
  - c) Repetition burst rate = 400 Hz
  - d) Maximum bus signal amplitude = 5 V (p-p).
6. The listed pin voltage corresponds with typical gain steps of +6 dB, +3 dB, 0 dB, -6 dB and -15 dB.
7. Attack time constant =  $C_{AV} \times R_{att}$ .

8. Decay time = 
$$\frac{C_{AV} \times 0.76 \text{ V} \left( 10^{\frac{-G_{V1}}{20}} - 10^{\frac{-G_{V2}}{20}} \right)}{I_{dec}}$$

Example:  $C_{AV} = 4.7 \mu\text{F}$ ;  $I_{dec} = 2 \mu\text{A}$ ;  $G_{V1} = -9 \text{ dB}$ ;  $G_{V2} = +6 \text{ dB}$  → decay time results in 4.14 s.

9. When reset is active the GMU-bit (general mute) and the LMU-bit (LINE OUT mute) is set and the I<sup>2</sup>C-bus receiver is in the reset position.
10. The AC characteristics are in accordance with the I<sup>2</sup>C-bus specification. The maximum clock frequency is 100 kHz. Information about the I<sup>2</sup>C-bus can be found in the brochure "*The I<sup>2</sup>C-bus and how to use it*" (order number 9398 393 40011).

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## I<sup>2</sup>C-BUS PROTOCOL

### I<sup>2</sup>C-bus format to read (slave transmits data)

S	SLAVE ADDRESS	R/ $\bar{W}$	A	DATA	MA	DATA	P
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**Table 1** Explanation of I<sup>2</sup>C-bus format to read (slave transmits data)

NAME	DESCRIPTION
S	START condition; generated by the master
Standard SLAVE ADDRESS	101 101 1 pin MAD not connected
Pin programmable SLAVE ADDRESS	101 101 0 pin MAD connected to ground
R/ $\bar{W}$	logic 1 (read); generated by the master
A	acknowledge; generated by the slave
DATA	slave transmits an 8-bit data word
MA	acknowledge; generated by the master
P	STOP condition; generated by the master

**Table 2** Definition of the transmitted bytes after read condition

FUNCTION	BYTE	MSB								LSB	
		D7	D6	D5	D4	D3	D2	D1	D0		
Alignment read 1	ALR1	Y	SAPP	STP	A14	A13	A12	A11	A10		
Alignment read 2	ALR2	Y	SAPP	STP	A24	A23	A22	A21	A20		

**Table 3** Function of the bits in Table 2

BITS	FUNCTION
STP	stereo pilot identification (stereo received = 1)
SAPP	SAP pilot identification (SAP received = 1)
A1X to A2X	stereo alignment read data
A1X	for wideband expander
A2X	for spectral expander
Y	indefinite

The master generates an acknowledge when it has received the first data word ALR1, then the slave transmits the next data word ALR2. Afterwards the master generates an acknowledge, then the slave begins transmitting the first data word ALR1 etc. until the master generates no acknowledge and transmits a STOP condition.

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## I<sup>2</sup>C-bus format to write (slave receives data)

S	SLAVE ADDRESS	R/W	A	SUBADDRESS	A	DATA	A	P
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**Table 4** Explanation of I<sup>2</sup>C-bus format to write (slave receives data)

NAME	DESCRIPTION
S	START condition
Standard SLAVE ADDRESS	101 101 1 pin MAD not connected
Pin programmable SLAVE ADDRESS	101 101 0 pin MAD connected to ground
R/W	logic 0 (write)
A	acknowledge; generated by the slave
SUBADDRESS (SAD)	see Table 5
DATA	see Table 6
P	STOP condition

If more than 1 byte of DATA is transmitted, then auto-increment is performed, starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 5 is performed.

**Table 5** Subaddress second byte after slave address

FUNCTION	REGISTER	MSB								LSB	HEX
		D7	D6	D5	D4	D3	D2	D1	D0		
Volume right	VR	0	0	0	0	0	0	0	0	0	00
Volume left	VL	0	0	0	0	0	0	0	0	1	01
Bass	BA	0	0	0	0	0	0	0	1	0	02
Treble	TR	0	0	0	0	0	0	0	1	1	03
Subwoofer	SW	0	0	0	0	0	0	1	0	0	04
Control 1	CON1	0	0	0	0	0	0	1	0	1	05
Control 2	CON2	0	0	0	0	0	0	1	1	0	06
Control 3	CON3	0	0	0	0	0	0	1	1	1	07
Alignment 1	ALI1	0	0	0	0	1	0	0	0	0	08
Alignment 2	ALI2	0	0	0	0	1	0	0	0	1	09
Alignment 3	ALI3	0	0	0	0	1	0	1	0	0	0A



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**Table 6** Definition of third byte after slave address

FUNCTION	REGISTER	MSB								LSB	
		D7	D6	D5	D4	D3	D2	D1	D0		
Volume right	VR	0	VR6	VR5	VR4	VR3	VR2	VR1	VR0		
Volume left	VL	0	VL6	VL5	VL4	VL3	VL2	VL1	VL0		
Bass	BA	0	0	0	BA4	BA3	BA2	BA1	BA0		
Treble	TR	0	0	0	TR4	TR3	TR2	TR1	0		
Subwoofer	SW	0	0	SW5	SW4	SW3	SW2	0	0		
Control 1	CON1	GMU	AVLON	LOFF	X	SUR	SC2	SC1	SC0		
Control 2	CON2	SAP	STEREO	TZCM	VZCM	LMU	EF2	EF1	EF0		
Control 3	CON3	0	0	0	0	L3	L2	L1	L0		
Alignment 1	ALI1	0	0	0	A14	A13	A12	A11	A10		
Alignment 2	ALI2	STS	0	0	A24	A23	A22	A21	A20		
Alignment 3	ALI3	ADJ	AT1	AT2	0	1	TC2	TC1	TC0		

**Table 7** Function of the bits in Table 6

BITS	FUNCTION
VR0 to VR6	volume control right
VL0 to VL6	volume control left
BA0 to BA4	bass control
TR1 to TR3	treble control
SW2 to SW5	subwoofer, surround control
GMU	mute control for outputs OUTL, OUTR and OUTS (generate mute)
AVLON	<b>AVL on/off</b>
LOFF	switch loudness <b>on/off</b>
X	don't care bit
SUR	surround/subwoofer SUR = 1 → $\frac{1}{2}(L - R)$ ; SUR = 0 → $\frac{1}{2}(L + R)$
SC0 to SC2	selection between line in and line out
STEREO, SAP	mode selection for line out
TZCM	zero-crossing mode in mute operation (treble and subwoofer/surround output stage)
VZCM	zero-crossing mode in volume operation
LMU	mute control for dematrix + line out select
EF0 to EF2	selection between mono, stereo linear, spatial stereo and pseudo mode
L0 to L3	input level adjustment
ADJ	stereo adjustment <b>on/off</b>
A1X	stereo alignment data for wideband expander
A2X	stereo alignment data for spectral expander
AT1 and AT2	attack time at AVL
TC0 to TC2	timing current alignment data
STS	stereo level switch

# I<sup>2</sup>C-bus controlled BTSC stereo/SAP decoder and audio processor

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**Table 8** Volume setting in registers VR and VL

G <sub>c</sub> (dB)	DATA							HEX
	D6 V6	D5 V5	D4 V4	D3 V3	D2 V2	D1 V1	D0 V0	
16	1	1	1	1	1	1	1	7F
15	1	1	1	1	1	1	0	7E
14	1	1	1	1	1	0	1	7D
13	1	1	1	1	1	0	0	7C
12	1	1	1	1	0	1	1	7B
11	1	1	1	1	0	1	0	7A
10	1	1	1	1	0	0	1	79
9	1	1	1	1	0	0	0	78
8	1	1	1	0	1	1	1	77
7	1	1	1	0	1	1	0	76
6	1	1	1	0	1	0	1	75
5	1	1	1	0	1	0	0	74
4	1	1	1	0	0	1	1	73
3	1	1	1	0	0	1	0	72
2	1	1	1	0	0	0	1	71
1	1	1	1	0	0	0	0	70
0	1	1	0	1	1	1	1	6F
-1	1	1	0	1	1	1	0	6E
-2	1	1	0	1	1	0	1	6D
-3	1	1	0	1	1	0	0	6C
-4	1	1	0	1	0	1	1	6B
-5	1	1	0	1	0	1	0	6A
-6	1	1	0	1	0	0	1	69
-7	1	1	0	1	0	0	0	68
-8	1	1	0	0	1	1	1	67
-9	1	1	0	0	1	1	0	66
-10	1	1	0	0	1	0	1	65
-11	1	1	0	0	1	0	0	64
-12	1	1	0	0	0	1	1	63
-13	1	1	0	0	0	1	0	62
-14	1	1	0	0	0	0	1	61
-15	1	1	0	0	0	0	0	60
-16	1	0	1	1	1	1	1	5F
-17	1	0	1	1	1	1	0	5E
-18	1	0	1	1	1	0	1	5D
-19	1	0	1	1	1	0	0	5C
-20	1	0	1	1	0	1	1	5B
-21	1	0	1	1	0	1	0	5A