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DATA SHEET

TDA9874A
Digital TV sound demodulator/decoder

Product specification
Supersedes data of 1999 Dec 03
File under Integrated Circuits, IC02

2000 Aug 04

CONTENTS

1 FEATURES

- Sound IF (SIF) input switch
- SIF Automatic Gain Control (AGC) with 24 dB control range
- Switchable 10 dB SIF input attenuator
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Easy TV standard programming option
- Differential Quadrature Phase Shift Keying (DQPSK) demodulation for different standards, simultaneously with 1-channel FM demodulation
- Near Instantaneous Companded Audio Multiplex (NICAM) decoding (B/G, D/K, I and L standard)
- 2-carrier multi-standard FM demodulation (B/G, D/K, I and M standard)
- Single carrier high deviation FM mono demodulation mode
- Decoding for three analog multi-channel systems (A2) and satellite sound
- Adaptive de-emphasis for satellite
- Programmable identification (B/G, D/K and M standard) and different identification times
- FM pilot carrier presence detector
- Optional AM demodulation for L standard, simultaneously with NICAM
- Monitor selection for FM/AM demodulator outputs and FM and NICAM signals with peak option
- Automatic FM dematrixing option
- Digital crossbar switch
- I^2S-bus serial audio output with matrix, level adjust and mute
- Dual audio Digital-to-Analog Converter (DAC) from digital crossbar switch to analog crossbar switch, bandwidth 15 kHz
- Automatic Volume Level (AVL) control
- Analog crossbar switch with inputs for mono and stereo
- Output selection of mono, stereo, dual, dual A or dual B
- Additional mono output with automatic select
- 20 kHz bandwidth for analog path
- Standby mode
- Automatic output selection for TV applications.

2 GENERAL DESCRIPTION

The TDA9874A is a single-chip Digital TV Sound Demodulator/Decoder (DTVSD) for analog and digital multi-channel sound systems in TV/VCR sets and satellite receivers.

2.1 Supported standards

The multi-standard/multi-stereo capability of the TDA9874A is of interest in Europe, Hong Kong/PR China and South East Asia. This includes B/G, D/K, I, M and L standards. In other application areas there exist subsets of the standard combinations or only single standards are transmitted.

All A2 (analog 2-carrier) and NICAM systems are supported. M standard (with mono or BTSC stereo sound) can be received and processed in mono sound mode.

The AM sound of L/L' standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9874A. A second possibility is to use the internal AM demodulator stage (with 6.5 MHz intercarrier), which gives limited performance.

Korea has a stereo sound system similar to Europe which is supported by the TDA9874A. Differences include deviation, modulation contents and identification. It is based on M standard.

For all FM standards a high deviation mode for a single carrier monaural sound demodulation is selectable.

An overview of the supported standards, sound systems and their key parameters is given in Tables 1 to 3.

The analog multi-channel systems are sometimes also referred to as 2-carrier systems (2CS).

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz)			MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/µs)
			NOM.	MAX.	OVER.	SC1	SC2	
M	mono	4.5	15	25	50	mono	–	15/75
M	A2	4.5/4.724	15	25	50	½(L + R)	½(L – R)	15/75 (Korea)
B/G	A2	5.5/5.742	27	50	80	½(L + R)	R	15/50
I	mono	6.0	27	50	80	mono	–	15/50
D/K (2)	A2	6.5/6.742	27	50	80	½(L + R)	R	15/50
D/K (1)	A2	6.5/6.258	27	50	80	½(L + R)	R	15/50
D/K (3)	A2	6.5/5.742	27	50	80	½(L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2; A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 × line frequency	55.0699 kHz = 3.5 × line frequency
Stereo identification frequency	$117.5\text{ Hz} = \frac{\text{line frequency}}{133}$	$149.9\text{ Hz} = \frac{\text{line frequency}}{105}$
Dual identification frequency	$274.1\text{ Hz} = \frac{\text{line frequency}}{57}$	$276.0\text{ Hz} = \frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 2-CARRIER SYSTEMS WITH NICAM

Table 3 NICAM

STANDARD	SC1						SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION							
			INDEX (%)		DEVIATION (kHz)					
			NOM.	MAX.	NOM.	MAX.				
B/G	5.5	FM	–	–	27	50	5.85	J17	40	note 1
I	6.0	FM	–	–	27	50	6.552	J17	100	note 1
D/K	6.5	FM	–	–	27	50	5.85	J17	40	note 2
L	6.5	AM	54	100	–	–	5.85	J17	40	note 1

Notes

1. See *"EBU NICAM 728 specification"* or equivalent specification.
2. Not yet officially defined.

2.1.3 SATELLITE SYSTEMS

An important specification for satellite TV reception is the Astra specification. The TDA9874A is suitable for the reception of Astra and other satellite signals, with sound carrier frequencies from 4 to 9.2 MHz.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/μs)
Main	6.50(1)	0.26	85(2)	mono	15/50(3)
Sub	7.02/7.20	0.15	50	m/st/d(4)	15/adaptive(5)
	7.38/7.56				
	7.74/7.92				
	8.10/8.28				

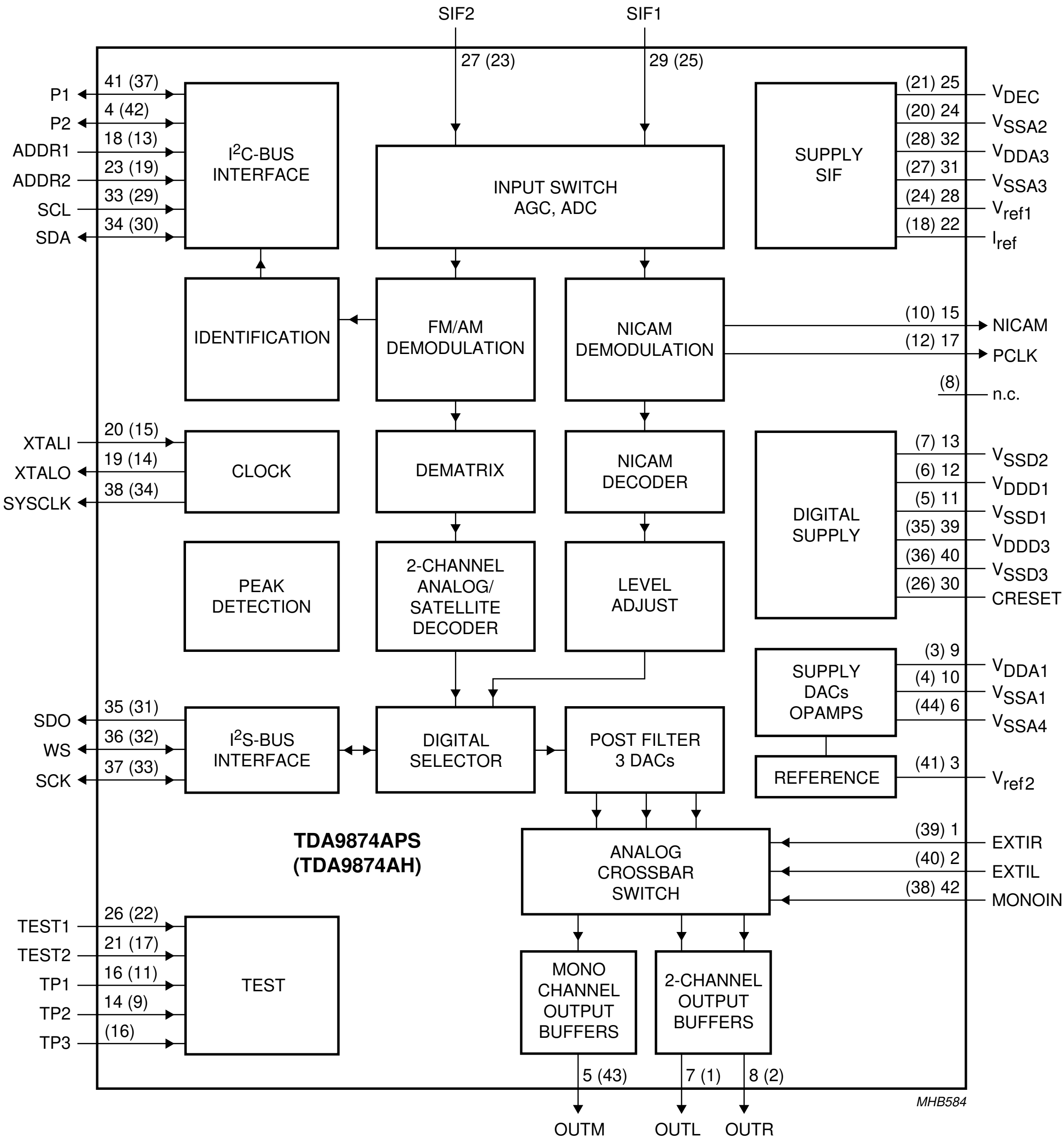
Notes

1. For other satellite systems, frequencies of e.g. 5.80, 6.60 or 6.65 MHz can also be received.
2. Main channels with high deviation can also be handled.
3. A de-emphasis of 60 μs, or in accordance with J17, is available.
4. m/st/d = mono or stereo or dual language sound.
5. Adaptive de-emphasis is compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9874APS	SDIP42	plastic shrink dual in-line package; 42 leads (600 mil)	SOT270-1
TDA9874AH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1

4 BLOCK DIAGRAM



The pin numbers given in parenthesis refer to the TDA9874AH.

Fig.1 Block diagram.

5 PINNING

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
EXTIR	1	39	external audio input right channel
EXTIL	2	40	external audio input left channel
V_{ref2}	3	41	analog reference voltage for DAC and operational amplifiers
P2	4	42	second general purpose I/O pin
OUTM	5	43	analog output mono
V_{SSA4}	6	44	analog ground supply 4 for analog back-end circuitry
OUTL	7	1	analog output left
OUTR	8	2	analog output right
V_{DDA1}	9	3	analog supply voltage 1; back-end circuitry 5 V
V_{SSA1}	10	4	analog ground supply 1; back-end circuitry
V_{SSD1}	11	5	digital ground supply 1; core circuitry
V_{DDD1}	12	6	digital supply voltage 1; core voltage regulator circuitry
V_{SSD2}	13	7	digital ground supply 2; core circuitry
n.c.	–	8	not connected
TP2	14	9	additional test pin 2; connected to V_{SSD} for normal operation
NICAM	15	10	serial NICAM data output (at 728 kHz)
TP1	16	11	additional test pin 1; connected to V_{SSD} for normal operation
PCLK	17	12	NICAM clock output (at 728 kHz)
ADDR1	18	13	first I^2C-bus slave address modifier input
XTALO	19	14	crystal oscillator output
XTALI	20	15	crystal oscillator input
TP3	–	16	additional test pin 3; connected to V_{SSD} for normal operation
TEST2	21	17	test pin 2; connected to V_{SSD} for normal operation
I_{ref}	22	18	resistor for reference current generation; front-end circuitry
ADDR2	23	19	second I^2C-bus slave address modifier input
V_{SSA2}	24	20	analog ground supply 2; analog front-end circuitry
V_{DEC}	25	21	analog front-end circuitry supply voltage decoupling
TEST1	26	22	test pin 1; connected to V_{SSD} for normal operation
SIF2	27	23	sound IF input 2
V_{ref1}	28	24	reference voltage; for analog front-end circuitry
SIF1	29	25	sound IF input 1
CRESET	30	26	capacitor for Power-on reset
V_{SSA3}	31	27	digital ground supply 3; front-end circuitry
V_{DDA3}	32	28	analog front-end circuitry regulator supply voltage 3 (5 V)
SCL	33	29	I^2C-bus serial clock input
SDA	34	30	I^2C-bus serial data input/output
SDO	35	31	I^2S-bus serial data output
WS	36	32	I^2S-bus word select input/output

SYMBOL	PIN		DESCRIPTION
	SDIP42	QFP44	
SCK	37	33	I^2S-bus clock input/output
SYSCLK	38	34	system clock output
V_{DDD3}	39	35	digital supply voltage 3; digital I/O pads
V_{SSD3}	40	36	digital ground supply 3; digital I/O pads
P1	41	37	first general purpose I/O pin
MONOIN	42	38	analog mono input

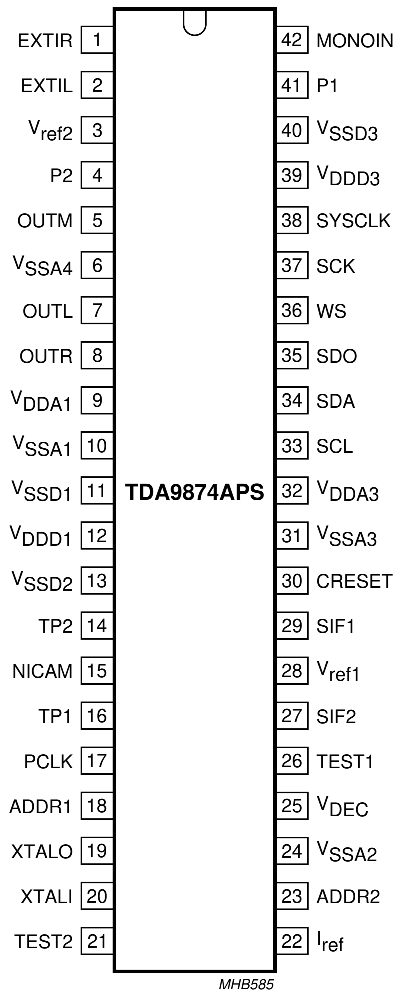


Fig.2 Pin configuration (SDIP42).

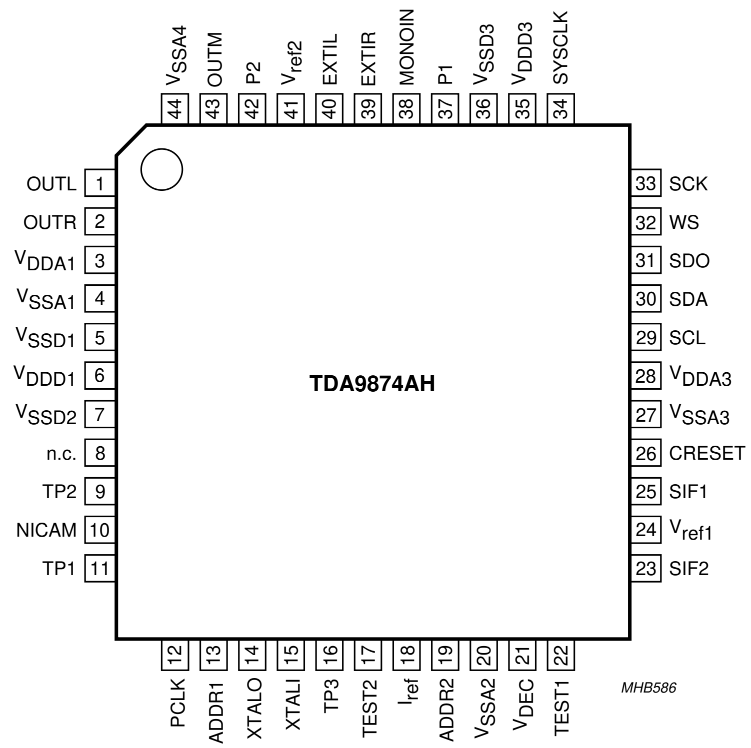


Fig.3 Pin configuration (QFP44).

6 FUNCTIONAL DESCRIPTION

6.1 Description of the demodulator and decoder section

6.1.1 SIF INPUTS

Two inputs are provided, pin SIF1 and pin SIF2. For higher SIF signal levels the SIF input can be attenuated with an internal switchable −10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads, and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen (see Table 14).

The AGC can be controlled via the I^{2}C-bus; details are given in Sections 7.3.2, 7.3.3 and 7.4.6.

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I^{2}C-bus (see Sections 7.3.5 and 7.3.6) or via Easy Standard Programming (ESP, see Section 7.3.23). When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed through a switchable band-limiting filter into a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

6.1.5 FM DECODING

A 2-carrier stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

Automatic FM dematrixing is also supported, which means that the FM sound mode identification (mono, stereo or dual) switches the FM dematrix directly. No loop via the microcontroller is needed.

For highly overmodulated signals, a high deviation mode for monaural audio sound single carrier demodulation can be selected.

NICAM decoding is still possible in high deviation mode.

6.1.6 FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standards, and for three different time constants that represent different trade-offs between speed and reliability of identification. A pilot detector allows the control software to identify an analog 2-carrier (A2) transmission within approximately 0.1 s.

Automatic FM dematrixing, depending on the identification, is possible.

6.1.7 NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbits/s. The NICAM demodulator performs DQPSK demodulation and passes the resulting bitstream and clock signal to the NICAM decoder and, for evaluation purposes, to various pins.

A timing loop controls the frequency of the crystal oscillator to lock the sampling instants to the symbol timing of the NICAM data.

6.1.8 NICAM DECODING

The device performs all decoding functions in accordance with the *“EBU NICAM 728 specification”*. After locking to the frame alignment word, the data is descrambled by applying the defined pseudo-random binary sequence. The device then synchronizes to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM status register by the user (see Section 7.4.2). The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel.

The error byte contains the number of sound sample errors (resulting from parity checking) that occurred in the past 128 ms period. The Bit Error Rate (BER) can be calculated using the following equation:

$$\mathrm{BER} = \frac{\text{bit errors}}{\text{total bits}} \approx \text{error byte} \times 1.74 \times 10^{-5}$$

6.1.9 NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE to logic 0 (see Section 7.3.12). Upper and lower error limits may be defined by writing appropriate values to two registers in the I^2C-bus section (see Sections 7.3.14 and 7.3.15). When the number of errors in a 128 ms period exceeds the upper error limit, the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM or AM) or to the analog mono input. When the error count is smaller than the lower error limit, the NICAM sound is restored.

The auto-mute function can be disabled by setting bit AMUTE to logic 1. In this case clicks become audible when the error count increases. The user will hear a signal of degrading quality.

If no NICAM sound is received, the outputs are switched from the NICAM channel to the 1st sound carrier.

A decision to enable or disable the auto-mute is taken by the microprocessor based on an interpretation of the application control bits C1, C2, C3 and C4, and possibly any additional strategy implemented by the user in the microcontroller software.

When the AM sound in NICAM L systems is demodulated in the 1st sound IF and the audio signal connected to the mono input of the TDA9874A, the controlling microprocessor has to ensure switching from NICAM reception to mono input, if auto-muting is desired. This can be achieved by setting bit AMSEL = 1 and bit AMUTE = 0.

6.1.10 CRYSTAL OSCILLATOR

The digital controlled crystal oscillator (DCXO) is fully integrated. Only an external 24.576 MHz crystal is required.

6.1.11 TEST PINS

All test pins are active HIGH. In normal operation of the device they can be left open-circuit, as they have internal pull-down resistors. Test functions are for manufacturing tests only and are not available to customers.

6.1.12 POWER FAIL DETECTOR

The power fail detector monitors the internal power supply for the digital part of the device. If the supply has temporarily been lower than the specified lower limit, the power failure register bit PFR in subaddress 0 (see Section 7.4.1), will be set to logic 1. Bit CLRPFR, slave register subaddress 1 (see Section 7.3.3), resets the Power-on reset flip-flop to logic 0. If this is detected, an initialization of the TDA9874A has to be performed to ensure reliable operation.

6.1.13 POWER-ON RESET

The reset is active LOW. In order to perform a reset at power-up, a simple RC circuit may be used which consists of an integrated passive pull-up resistor and an external capacitor connected to ground. The pull-up resistor has a nominal value of 50 kΩ, which can easily be measured between pins CRESET and V_{DDD3}. Before the supply voltage has reached a certain minimum level, the state of the circuit is completely undefined and remains in this undefined state until a reset is applied.

The reset is guaranteed to be active when:

- The power supply is within the specified limits (4.5 to 5.5 V)
- The crystal oscillator (DCXO) is functioning
- The voltage at pin CRESET is below $0.3V_{DDD}$ (1.5 V if V_{DDD} = 5.0 V, typically below 1.8 V).

The required capacitor value depends on the gradient of the rising power supply voltage. The time constant of the RC circuit should be clearly larger than the rise time of the power supply [to make sure that the reset condition is always satisfied (see Fig.4)], even when considering tolerance spreading. To avoid problems with a too slow discharging of the capacitor at power-down, it may be helpful to add a diode from pin CRESET to V_{DDD}.

It should be noted that the internal ESD protection diode does not help here as it only conducts at higher voltages. Under difficult power supply conditions (e.g. very slow or non-monotonic ramp-up), it is recommended to drive the reset line from a microcontroller port or the like.

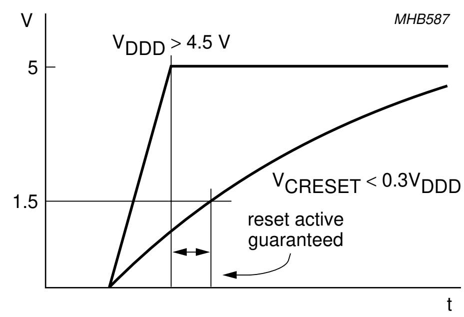


Fig.4 Reset at Power-on.

6.2 Description of the DSP

6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch are equipped with a level adjustment facility to change the signal level in a range of ±15 dB. Adjusting the signal level is intended to compensate for the different modulation parameters of the various TV standards. Under nominal conditions it is recommended to scale all input channels to be 15 dB below full-scale. This will create sufficient headroom to cope with overmodulation and avoids changes of the volume impression when switching from FM to NICAM or vice versa.

6.2.2 NICAM PATH

The NICAM path has a switchable J17 de-emphasis.

6.2.3 NICAM AUTO-MUTE

If NICAM is received, the auto-mute is enabled and the signal quality becomes poor. The digital crossbar switches automatically to FM, channel 1 or the analog mono input, as selected by bit AMSEL. This automatic switching depends on the NICAM bit error rate. The auto-mute function can be disabled via the I^2C-bus.

6.2.4 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator that may occur due to carrier frequency offsets, and supplies the FM monitor function with DC values, e.g. for the purpose of microprocessor controlled carrier search or fine tuning functions.

An adaptive de-emphasis is available for Wegener-Panda 1 encoded satellite programs.

The de-emphasis stage offers a choice of settings for the supported TV standards.

The 2-channel decoder performs the dematrixing of $\frac{1}{2}$(L + R), R to L and R signals of $\frac{1}{2}$(L + R) and $\frac{1}{2}$(L − R) to L and R signals or of channel 1 and channel 2 to L and R signals, as demanded by the different TV standards or user preferences.

Automatic FM dematrixing is also supported.

Using the high deviation mode, only channel 1 (mono) can be demodulated. The scaling is −6 dB compared to 2-channel decoding.

6.2.5 MONITOR

This function provides data words from the FM demodulator outputs and FM and NICAM signals for external use, such as carrier search or fine tuning. The peak level of these signals can also be observed. Source selection and data read out are performed via the I^2C-bus.

6.2.6 DIGITAL CROSSBAR SWITCH

The input channels are derived from the FM and NICAM paths, while the output channels comprise I^2S-bus and the audio DACs to the analog crossbar switch. It should be noted that there is no connection from the external analog audio inputs to the digital crossbar switch.

6.2.7 DIGITAL AUDIO OUTPUT

The digital audio output interface comprises an I^2S-bus output port and a system clock output. The I^2S-bus port is equipped with a level adjustment facility that can change the signal level in a ±15 dB range in 1 dB steps. Muting is possible, too, and outputs can be disabled to improve EMC performance.

The I^2S-bus output matrix provides the functions for forced mono, stereo, channel swap, channel 1 or channel 2.

Automatic selection for TV applications is possible. In this case the microcontroller program only has to provide a user controlled sound A or sound B selection.

6.2.8 STEREO CHANNEL TO THE ANALOG CROSSBAR PATH

A level adjustment function is provided with control positions of 0 dB, +3 dB, +6 dB and +9 dB in combination with the audio DACs. The Automatic Volume Level (AVL) function provides a constant output level of −20 dB (full-scale) for input levels between 0 dB (full-scale) and −26 dB (full-scale). There are some fixed decay time constants to choose from, i.e. 2, 4 or 8 seconds.

Automatic selection for TV applications is possible. In this case the microcontroller program only has to provide a user controlled sound A or sound B selection.

6.2.9 GENERAL

The level adjustment functions can provide signal gain at multiple locations. Great care has to be taken when using gain with large input signals, e.g., due to overmodulation, in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full-scale (−15 dB full-scale).

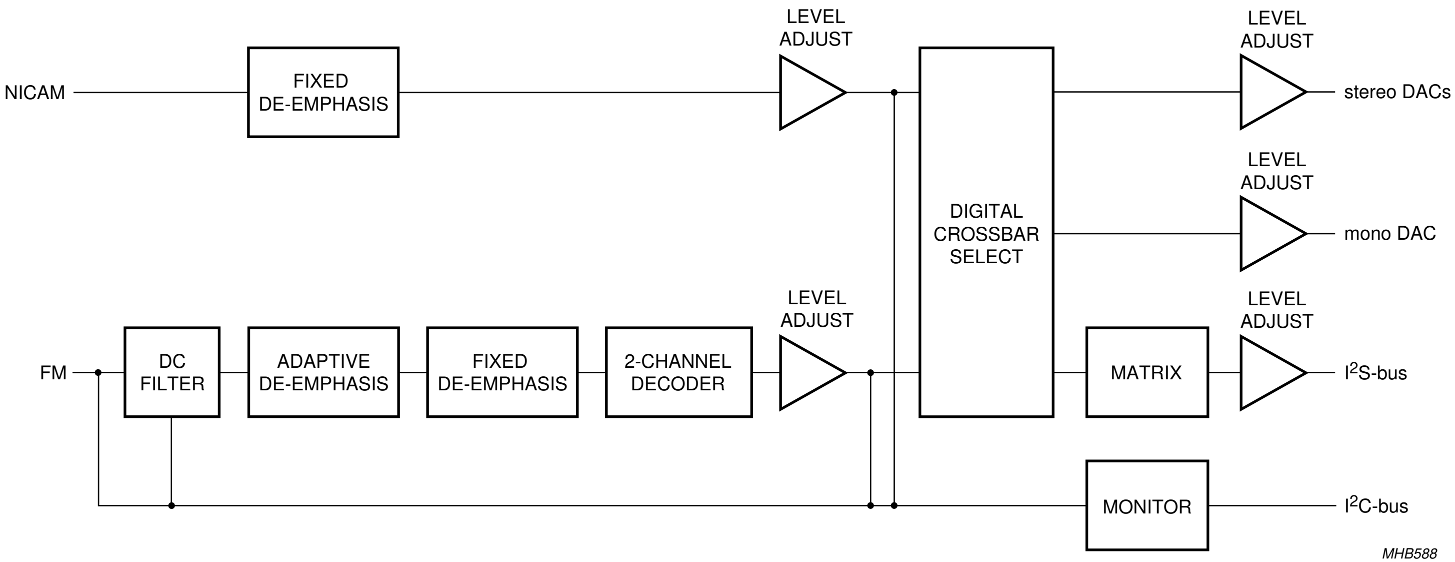


Fig.5 DSP data flow diagram.

6.3 Description of the analog audio section

6.3.1 ANALOG CROSSBAR SWITCH AND ANALOG MATRIX

The TDA9874A has one external analog stereo input, one mono input, one 2-channel and one single-channel output port. Analog source selector switches are employed to provide the desired analog signal routing capability, which is done by the analog crossbar switch section.

The basic signal routing philosophy of the TDA9874A is that each switch handles two signal channels at the same time (e.g. left and right, language A and B) directly at the source. For an overview of the signal flow see Fig.7.

Each source selector switch is followed by an analog matrix to perform further selection tasks, such as putting a signal from one input channel, say language A, to both output channels or for swapping left and right channels. The analog matrix provides the functions given in Table 5. Automatic matrixing for TV applications is also supported.

All switches and matrices are controlled via the I^{2}C-bus.

Table 5 Analog matrix functions

MODE	MATRIX OUTPUT	
	L OUTPUT	R OUTPUT
1	L input	R input
2	R input	L input
3	L input	L input
4	R input	R input

6.3.2 EXTERNAL AND MONO INPUTS

The external and mono inputs accept signal levels of up to 1.4 V (RMS). By adding external series resistors to provide suitable attenuation, the external input could be used as a SCART input. Whenever the external or mono input is selected, the output of the DAC is muted to improve the crosstalk performance.

6.3.3 AUDIO DACS

The TDA9874A comprises a 2-channel audio DAC and an additional single-channel audio DAC for feeding signals from the DSP section to the analog crossbar switch. These DACs have a resolution of 15 bits and employ four-times oversampling and noise shaping.

6.3.4 AUDIO OUTPUT BUFFERS

The output buffers provide a gain of 0 dB and offer a muting possibility. The post filter capacitors of the audio DACs are connected to the buffer outputs.

6.3.5 STANDBY MODE

The standby mode (see Section 7.3.3) disables most functions and reduces power dissipation of the TDA9874A. It provides no other function.

Internal registers may lose their information in standby mode. Therefore, the device needs to be initialized on returning to normal operation. This can be accomplished in the same way as after a Power-on reset.

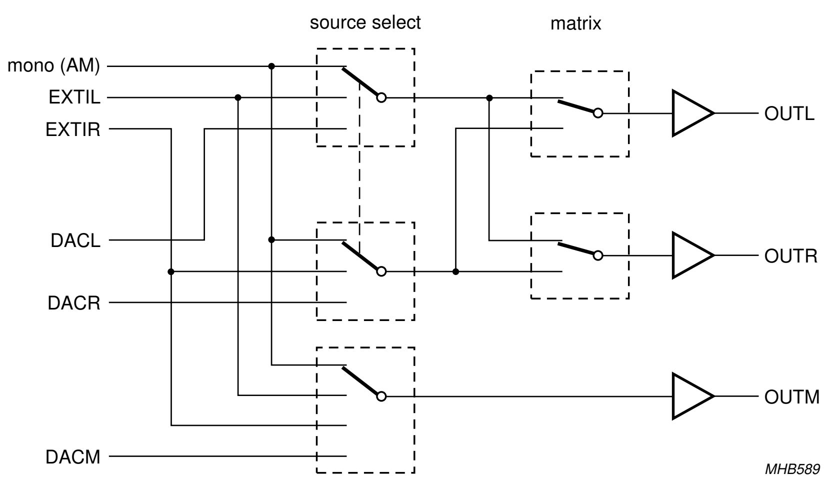


Fig.6 Switch diagram for the analog audio section.

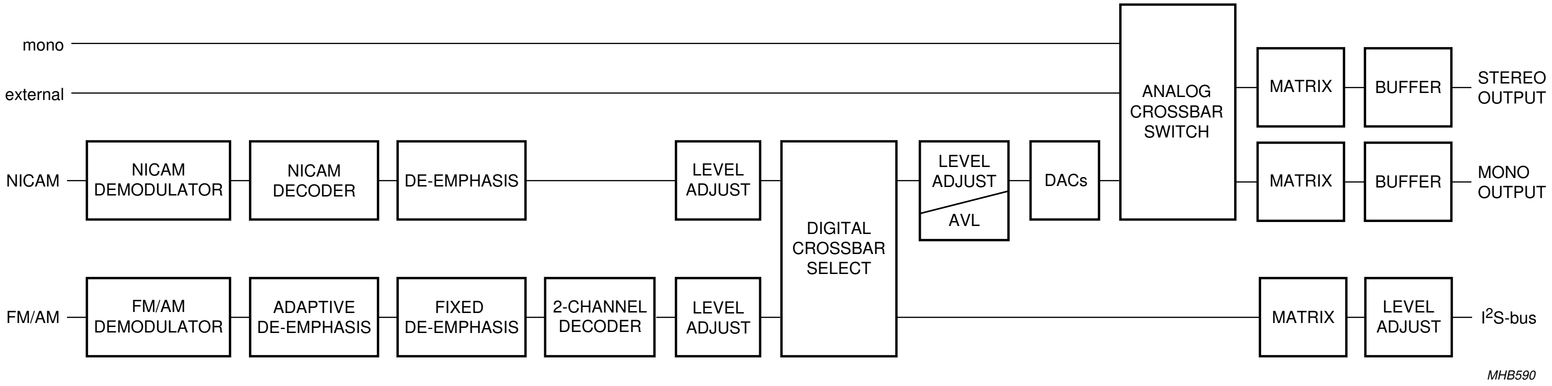


Fig.7 Audio signal flow.

7 I²C-BUS CONTROL

7.1 Introduction

The TDA9874A is controlled only via the I²C-bus. Control is exercised by writing data to one or more internal registers. Status information can be read from an array of registers to let the controlling microprocessor determine whether any action is required.

The device has an I²C-bus slave transceiver in accordance with the fast-mode specification with a maximum speed of 400 kbits/s. Information about the I²C-bus can be found in brochure *"I²C-bus and how to use it"* (order number 9398 393 40011). To avoid conflicts in a real application with other ICs providing similar or complementing functions, there are four possible slave addresses available, which can be selected by pins ADDR1 and ADDR2 (see Table 6).

Table 6 Possible slave addresses

ADDR2	ADDR1	SLAVE ADDRESS						
		A6	A5	A4	A3	A2	A1	A0
0	0	1	0	1	1	0	0	0
0	1	1	0	1	1	0	0	1
1	0	1	0	1	1	0	1	0
1	1	1	0	1	1	0	1	1

The I²C-bus interface remains operational in the standby mode of the TDA9874A to allow the device to be reactivated via the I²C-bus.

The device will not respond to a 'general call' on the I²C-bus, i.e. when a slave address of 0000 000 is sent by a master.

7.2 Power-up state

After Power-on reset respectively at power-up the device is in the following state:

- All outputs muted
- No sound carrier frequency loaded
- General purpose I/O pins ready for input (HIGH)
- Input SIF1 selected with:
  - AGC on
  - SIF 10 dB attenuator off
  - Small hysteresis.
- Demodulators for both sound carriers set to FM with:
  - Identification for B/G, D/K, identification mode 'slow'
  - Level adjustment set to 0 dB
  - De-emphasis 50 µs
  - Dematrix set to mono
  - Adaptive de-emphasis off.
- Analog outputs are muted and connected to DACs
- Digital audio interface all outputs off
- Monitor set to carrier 1 DC output.

After Power-on reset or power-up, a device initialization has to be performed via the I²C-bus to put the TDA9874A into the proper mode of operation, in accordance with the desired TV standard, etc. This can be done by writing to all registers with a single I²C-bus transmission (such as a refresh operation) or by writing selectively only to those registers, the contents of which need to be changed with regard to the power-up state. Easy Standard Programming (ESP) can also be used.

7.3 Slave receiver mode

As a slave receiver, the TDA9874A provides 26 registers for storing commands and data. Each register is accessed via a so-called subaddress. A subaddress can be thought of as a pointer to an internal memory location.

Detailed descriptions of the slave receiver registers are given in Sections 7.3.2 to 7.3.21.

It is allowed to send more than one data byte per transmission to the TDA9874A. In this event, the subaddress is automatically incremented after each data byte, resulting in storing the sequence of data bytes at successive register locations, starting at SUBADDRESS. A transmission can start at any valid subaddress. Each byte that is properly stored, is acknowledged with A (acknowledge).

If an attempt is made to write data to a non-existing subaddress, the device acknowledges with $\overline{A}$ (not acknowledge), therefore telling the I^{2}C-bus master to abort the transmission. There is no 'wrap-around' of subaddresses.

Commands and data will be processed as soon as they have been received completely. Functions requiring more than one byte will thus be executed only after all bytes for that function have been received. If the transmission is terminated (STOP condition) before all bytes have been received, the incomplete data for that function is ignored.

Data patterns sent to the various subaddresses are not checked for being illegal or not at that address, except for the level adjustment functions.

Detection of a STOP condition without a preceding acknowledge bit is regarded as a bus error. In this case, the last operation will not be executed.

Table 7 I^{2}C-bus; slave address, subaddress, data format

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA	A	P

Table 8 Explanation of Table 7

BIT	FUNCTION
S	START condition
SLAVE ADDRESS	7-bit device address
0	data direction bit (write to device)
A	acknowledge
SUBADDRESS	address of register to write to
DATA	data byte to be written into register
P	STOP condition

Table 9 Format for a transmission employing auto-increment of subaddresses

S	SLAVE ADDRESS	0	A	SUBADDRESS	A	DATA BYTE A(1)	DATA	A	P

Note

1. n data bytes with auto-increment of subaddresses.

7.3.1 PROGRAMMING VIA THE I^{2}C-BUS

The TDA9874A can be programmed in the same way as its predecessor (TDA9874H) using the subaddresses 0 to 24 or by using ESP.

7.3.1.1 Programming via subaddresses 0 to 24

While programming the TDA9874A, by writing to subaddresses 0 to 24, it is not allowed to access subaddress 255. Writing data to subaddress 255 will overwrite the data previously written to subaddresses 3 to 10. This may cause unwanted effects.

7.3.1.2 Using Easy Standard Programming (ESP)

This facility simplifies programming by reducing the amount of data to be set-up and transferred via the I^2C-bus.

Subaddress 255 gives control of most standard dependent settings of the IC; see ESP register in Section 7.3.23.

When using ESP it is recommended not to write data to subaddresses 3 to 10.

A possible programming flow for using ESP and automatic FM dematrixing (bit TVSM = 1 and bit IDSWFM = 1) is shown in Table 10. It should be noted that the NICAM configuration register and the level adjustment registers for FM and NICAM are not affected by ESP.

Table 10 Programming the TDA9874A by using ESP and automatic FM dematrixing

REGISTER		CONTENT OF REGISTER
NUMBER	NAME	
0	AGCGR	Set AGCGR = 20H for using the –10 dB attenuator at the SIF input, otherwise write a 00H to this register.
1	GCONR	Select the chosen SIF input pin by writing data to bit SIFSEL (bit 0) and choose the AGC decay time corresponding to your application by writing the appropriate data to bit AGCSLOW (bit 2).
2	MSR	set this register according to your sound mode detection algorithm
3 to 10	–	do NOT write data to these registers while using ESP
11	FMMR	set FMMR = 80H to choose automatic FM dematrixing
12	C1OLAR	see Table 36
13	C2OLAR	see Table 37
14	NCONR	set NCONR = 04H to select FM source automatically if NICAM is not available
15	NOLAR	see Table 40
16	NLELR	set NLELR = 14H (default setting after Power-on reset) if no other value is chosen
17	NUELR	set NUELR = 50H (default setting after Power-on reset) if no other value is chosen
18	AMCONR	set AMCONR = F9H to enable all analog outputs
19	SDACOSR	set SDACOSR = 81H to select +6 dB gain (see Table 46) and NICAM or FM output
20	AOSR	To select an internal source set AOSR = 80H to select dual A or set AOSR = C0H to select dual B (if dual mode is transmitted) to all analog outputs. For selecting an external source see Section 7.3.18.
21	DAICONR	use only for I^2S-bus output, see detailed description in Section 7.3.19
22	I^2SOSR	use only for I^2S-bus output, see detailed description in Section 7.3.20
23	I^2SOLAR	use only for I^2S-bus output, see detailed description in Section 7.3.21
24	MDACOSR	Set MDACOSR = 82H to select dual A or set MDACOSR = 83H to select dual B (if dual mode is transmitted) to all analog outputs. For selecting an external source see Section 7.3.22.
255	ESP	see detailed description in Section 7.3.23

Table 11 Overview of the slave receiver registers

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	6	5	4	3	2	1	0	
0	0	0	AGCLEV	B4	B3	B2	B1	B0	AGC gain selection (ignored if AGC on)
1	P2OUT	P1OUT	STDBY	INIT	CLRPFR	AGCSLOW	AGCOFF	SIFSEL	general configuration
2	PEAK	0	0	MCSM1	MCSM0	0	MSS1	MSS0	monitor select
3	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; MS part
4	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency
5	B7	B6	B5	B4	B3	B2	B1	B0	carrier 1 frequency; LS part
6	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency; MS part
7	B7	B6	B5	B4	B3	B2	B1	B0	carrier 2 frequency
8	B7	B5	B5	B4	B3	B2	B1	B0	carrier 2 frequency; LS part
9	IDMOD1	IDMOD0	IDAREA	FILTBW1	CH2MOD1	CH2MOD0	FILTBW0	CH1MODE	demodulator configuration
10	ADEEM2	FMDSC23	FMDSC22	FMDSC21	ADEEM1	FMDSC13	FMDSC12	FMDSC11	FM de-emphasis
11	IDSWFM	0	0	0	0	FDMS2	FDMS1	FDMS0	FM dematrix
12	0	0	0	B4	B3	B2	B1	B0	channel 1 output level adjustment
13	0	0	0	B4	B3	B2	B1	B0	channel 2 output level adjustment
14	DCXOPULL	DCXOTEST	0	DOUTEN	0	AMSEL	NDEEM	AMUTE	NICAM configuration
15	0	0	0	B4	B3	B2	B1	B0	NICAM output level adjustment
16	B7	B6	B5	B4	B3	B2	B1	B0	NICAM lower error limit
17	B7	B6	B5	B4	B3	B2	B1	B0	NICAM upper error limit
18	1	MUTI2S	1	1	1	MUTSOUT	MUTMOUT	1	audio mute control
19	SDGS1	0	AVL1	AVL0	SDGS0	0	SDOS1	SDOS0	stereo DAC output select
20	TVSM	CSM2	CSM1	CSM0	MOS1	MOS0	SSS1	SSS0	analog output select

SUBADDRESS (DECIMAL)	DATA								FUNCTION
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
21	0	0	0	SYSCL1	SYSCL0	SYSOUT	I2SFORM	IS2OUT	digital audio interface configuration
22	TVSMIIS	ICSM2	ICSM1	ICSM0	0	0	ISS1	ISS0	I^2S-bus output select
23	0	0	0	B3	B2	B1	B0	B0	I^2S-bus output level adjustment
24	MDGS1	0	0	0	MDGS0	0	MDOS1	MDOS0	mono DAC output select
25	0	0	0	0	0	0	0	0	reserved
255	FILTBW1	FILTBW0	IDMOD1	IDMOD0	EPB3	EPB2	EPB1	EPB0	ESP

7.3.2 AGC GAIN REGISTER (AGCGR)

If the AGC function is switched off in the general configuration register (see Section 7.3.3), the contents of this register defines a fixed gain of the SIF input stage. The input voltages given are meant to generate a nearly full-scale output from the SIF ADC. If the AGC is on, the AGC gain setting is ignored. After switching off the AGC function, the latest gain control setting is copied to the AGC gain register.

If the AGC input level shift bit AGCLEV is set to logic 1 the input signal is scaled with −10 dB. The bit AGCLEV is also active if the AGC function is enabled.

The default setting after Power-on reset is 0000 0000.

In Table 14 the stated step number corresponds with the SIF level read from subaddress 7 (see Section 7.4.6); the input voltages should be considered as approximate target values.

Table 12 AGC gain register (subaddress 0)

7	6	5	4	3	2	1	0
0	0	AGCLEV	AGCB4	AGCB3	AGCB2	AGCB1	AGCB0

Table 13 Description of the AGC gain register bits

BIT	NAME	DESCRIPTION
7	–	this bit is not used and should be set to a logic 0
6	–	this bit is not used and should be set to a logic 0
5	AGCLEV	If the AGC input level shift bit AGCLEV = 1 the input signal is scaled with −10 dB. Bit AGCLEV is also active if the automatic gain function is enabled.
4	AGCB4	If the automatic gain control function is switched off in the general configuration register, the contents of this register will define a fixed gain of the AGC stage.
3	AGCB3	
2	AGCB2	
1	AGCB1	
0	AGCB0	

Table 14 AGC gain register

7	6	5	4	3	2	1	0	AGC GAIN (dB)	MAX. SIF INPUT VOLTAGE [mV (RMS)]
–	–	AGCLEV	AGCB4	AGCB3	AGCB2	AGCB1	AGCB0		
0	0	0/1	1	1	1	1	1	0.0	333/1 052
0	0	0/1	1	1	1	1	0	0.8	304/963
0	0	0/1	1	1	1	0	1	1.5	278/881
0	0	0/1	1	1	1	0	0	2.3	255/806
0	0	0/1	1	1	0	1	1	3.1	233/737
0	0	0/1	1	1	0	1	0	3.9	213/674
0	0	0/1	1	1	0	0	1	4.6	195/617
0	0	0/1	1	1	0	0	0	5.4	178/564
0	0	0/1	1	0	1	1	1	6.2	163/516
0	0	0/1	1	0	1	1	0	7.0	149/472
0	0	0/1	1	0	1	0	1	7.7	136/432
0	0	0/1	1	0	1	0	0	8.5	125/395
0	0	0/1	1	0	0	1	1	9.3	114/361
0	0	0/1	1	0	0	1	0	10.1	104/330
0	0	0/1	1	0	0	0	1	10.8	96/302
0	0	0/1	1	0	0	0	0	11.6	87/276
0	0	0/1	0	1	1	1	1	12.4	80/253
0	0	0/1	0	1	1	1	0	13.2	73/231
0	0	0/1	0	1	1	0	1	13.9	67/212
0	0	0/1	0	1	1	0	0	14.7	61/194
0	0	0/1	0	1	0	1	1	15.5	56/177
0	0	0/1	0	1	0	1	0	16.3	51/162
0	0	0/1	0	1	0	0	1	17.0	47/148
0	0	0/1	0	1	0	0	0	17.8	43/135
0	0	0/1	0	0	1	1	1	18.6	39/124
0	0	0/1	0	0	1	1	0	19.4	36/113
0	0	0/1	0	0	1	0	1	20.1	33/104
0	0	0/1	0	0	1	0	0	20.9	30/95
0	0	0/1	0	0	0	1	1	21.7	27/87
0	0	0/1	0	0	0	1	0	22.5	25/79
0	0	0/1	0	0	0	0	1	23.2	23/73
0	0	0/1	0	0	0	0	0	24.0	21/66

7.3.3 GENERAL CONFIGURATION REGISTER (GCONR)

The default setting after Power-on reset is 1100 0000.

Table 15 General configuration register (subaddress 1)

7	6	5	4	3	2	1	0
P2OUT	P1OUT	STDBY	INIT	CLRPFR	AGCSLOW	AGCOFF	SIFSEL

Table 16 Description of the general configuration register bits

BIT	SYMBOL	DESCRIPTION
7	P2OUT	General purpose I/O pins 1 and 2: these bits control the general purpose input/output pins. The contents of these bits is written directly to the corresponding pins. If an input is desired, the bits must be set to 1 to allow the pins to be pulled to LOW levels externally. Input from the pins is reflected in the device status register (see Section 7.4.1). Bit P1OUT is recommended to be used for switching an SIF trap for the adjacent picture carrier in designs that employ such a trap.
6	P1OUT	
5	STDBY	Standby mode on/off: if bit STDBY = 1 the TDA9874A is set to the standby mode. Most functions are disabled and power dissipation is somewhat reduced. If bit STDBY = 0 the TDA9874A is in its normal mode of operation. On return from standby mode, the device is in its Power-on reset mode and needs to be re-initialized with data defined by the user.
4	INIT	Initialize to default settings: if bit INIT = 1 it causes initialization of the TDA9874A to its default settings. This has the same effect as a Power-on reset. In the event of a conflict between the default settings and any bit set to logic 1 in this register, the bits actually written to this register will overwrite the default settings. This bit is automatically reset to 0 after initialization has been completed. When set to logic 0, the TDA9874A is in its normal mode of operation.
3	CLRPFR	Clear power failure register: if bit CLRPFR = 1 it resets the clear power failure register. This bit is automatically reset to logic 0 after bit PFR in the device status register has been read.
2	AGCSLOW	AGC decay time: if bit AGCSLOW = 1 a longer decay time and larger hysteresis are selected for input signals with strong video modulation (conventional intercarrier). This bit has only an effect, If bit AGCOFF = 0. If bit AGCSLOW = 0 it selects normal attack and decay times for the AGC and a small hysteresis.
1	AGCOFF	AGC on/off: if bit AGCOFF = 1 it forces the AGC block to a fixed gain as defined in the AGC gain register (see Section 7.3.2). If bit AGCOFF = 0 the AGC function is enabled and the contents of the AGC gain register are ignored.
0	SIFSEL	SIF input select: if bit SIFSEL = 1 it selects pin SIF2 for input (recommended for satellite tuner). If bit SIFSEL = 0 it selects pin SIF1 (recommended for terrestrial TV).

7.3.4 MONITOR SELECT REGISTER (MSR)

This register is used to define the signal source (the level of which is to be monitored) and the signal channel. Data can be monitored e.g. before or after the DC filter at the FM/AM demodulator outputs. The peak level of signals can also be observed. The last available data sample can be read out in the I^2C-bus slave transmitter mode (see Section 7.4.5).

Phase means the differentiated phase output of the FM demodulator and is provided when the demodulator operates in FM mode. The magnitude is supplied in AM mode.

The default setting after Power-on reset is 0000 0000.

Table 17 Monitor select register (subaddress 2)

7	6	5	4	3	2	1	0
PEAK	0	0	MCSM1	MCSM0	0	MSS1	MSS0

Table 18 Description of the monitor select register bits

BIT	SYMBOL	DESCRIPTION
7	PEAK	Peak level select: if bit PEAK = 1 it selects the rectified peak level of a source to be monitored. Peak level value is reset to logic 0 after read-out (see read registers 5 and 6). After changing the monitor signal source for peak calculation it is advisable to ignore the first read-out value due to stored data from previous calculations.
6	–	these bits are not used and should be set to logic 0
5	–	
4	MCSM1	Signal channel select: the state of these bits determine which signal channel is selected; see Table 19.
3	MCSM0	
2	–	this bit is not used and should be set to logic 0
1	MSS1	Signal source select: the state of these bits determine which signal source is selected; see Table 20.
0	MSS0	

Table 19 Signal channel selection

MCSM1	MCSM0	SIGNAL CHANNEL
0	0	$\frac{CH1 + CH2}{2}$
0	1	CH1
1	0	CH2

Table 20 Signal source selection

MSS1	MSS0	SIGNAL SOURCE
0	0	DC output of FM/AM demodulator
0	1	magnitude/phase output of FM/AM demodulator
1	0	FM/AM path output
1	1	NICAM path output

7.3.5 CARRIER 1 FREQUENCY REGISTER

This register should not be used when applying ESP. Three bytes are required to define a 24-bit frequency control word to represent the sound carrier (i.e. mixer) frequency. These three bytes are stored at subaddresses 3 to 5; subaddress 3 being the high byte. Execution of the command starts only after all bytes have been received. If an error occurs, e.g. a premature STOP condition, partial data for this function is ignored. The relation of the sound carrier frequency and the control word is given in the following formula:

$$\text{data} = \frac{f_{mix}}{f_{clk}} \times 2^{24}$$

where:

data = 24-bit frequency control word

f_{mix} = desired sound carrier frequency

f_{clk} = 12288 MHz (clock frequency of mixer)

2^{24} = 16777216 (number of steps in a 24-bit word size).

Example: A 5.5 MHz sound carrier frequency will be generated by sending the following sequence of data bytes to the TDA9874A (data = 7509333 in decimal notation or 729555 in hexadecimal notation): 0111 0010 1001 0101 0101 0101.

The default setting after Power-on reset is 0000 0000 for all three bytes.

Table 21 Carrier 1 frequency register high byte (subaddress 3)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 22 Carrier 1 frequency register middle byte (subaddress 4)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Table 23 Carrier 1 frequency register low byte (subaddress 5)

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

7.3.6 CARRIER 2 FREQUENCY REGISTER

This register should not be used when applying ESP. The format is the same as for sound carrier 1, except subaddresses 6 to 8 are used. Subaddress 6 holds the high byte.

If this register is used, it will be for either the second FM sound carrier of a terrestrial or satellite FM program or for the NICAM sound carrier.