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TDA9885; TDA9886

I2C-bus controlled single and multistandard alignment-free IF-PLL demodulators

Rev. 03 — 16 December 2008 **Product data sheet**

1. General description

The TDA9885 is an alignment-free multistandard (PAL and NTSC) vision and sound IF signal Phase-Locked Loop (PLL) demodulator for negative modulation only and FM processing.

The TDA9886 is an alignment-free multistandard (PAL, SECAM and NTSC) vision and sound IF signal PLL demodulator for positive and negative modulation, including sound AM and FM processing.

2. Features

- 5 V supply voltage
- Gain controlled wideband Vision Intermediate Frequency (VIF) amplifier, AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics, and excellent pulse response
- Gated phase detector for L and L-accent standard
- Fully integrated VIF Voltage-Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I2C-bus
- Digital acquisition help, VIF frequencies of 33.4 MHz, 33.9 MHz, 38.0 MHz, 38.9 MHz, 45.75 MHz and 58.75 MHz
- 4 MHz reference frequency input: signal from PLL tuning system or operating as crystal oscillator
- VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit digital-to-analog converter, AFC bits readable via I2C-bus
- TakeOver Point (TOP) adjustable via I2C-bus or alternatively with potentiometer
- Fully integrated sound carrier trap for 4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz, controlled by FM-PLL oscillator
- Sound IF (SIF) input for single reference Quasi Split Sound (QSS) mode, PLL controlled
- SIF AGC for gain controlled SIF amplifier, single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode, switchable via I2C-bus
- AM demodulator without extra reference circuit
- Alignment-free selective FM-PLL demodulator with high linearity and low noise

- Four selectable I²C-bus addresses
- I²C-bus control for all functions
- I²C-bus transceiver with pin programmable Module ADdress (MAD)

3. Applications

- TV, VTR, PC, and STB applications

4. Quick reference data

Table 1.   Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
τ_P	time constant (R × C) for network at pin V_P	for applications without I²C-bus		1.2	-	-	μs
Video part							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	−1 dB video at output		-	60	100	μV
$G_{VIF(cr)}$	control range VIF gain	see Figure 9		60	66	-	dB
f_{VIF}	vision carrier operating frequencies	see Table 13		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f_{VIF}; see Figure 12		-	±2.3	-	MHz
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7					
		normal mode (sound carrier trap active) and sound carrier on		1.7	2.0	2.3	V
		trap bypass mode and sound carrier off	[2]	0.95	1.10	1.25	V
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[3]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*		-	2	4	deg
$B_{v(-1dB)}$	−1 dB video bandwidth	trap bypass mode and sound carrier off; AC load: C_L < 20 pF, R_L > 1 kΩ	[2]	5	6	-	MHz
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[4]	3.95	4.05	-	MHz
		f_{trap} = 5.5 MHz	[4]	4.90	5.00	-	MHz
		f_{trap} = 6.0 MHz	[4]	5.40	5.50	-	MHz
		f_{trap} = 6.5 MHz	[4]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz		30	36	-	dB
		f = 5.5 MHz		30	36	-	dB

Table 1. **Quick reference data** …continued

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
S/N$_W$	weighted signal-to-noise ratio	unified weighting filter (*"ITU-T J.61"*); see Figure 13	[5]	56	59	-	dB
PSRR$_{CVBS}$	power supply ripple rejection on pin CVBS	f$_{ripple}$ = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB
AFC$_{stps}$	AFC control steepness	definition: ΔI$_{AFC}$ / Δf$_{VIF}$		0.85	1.05	1.25	µA/kHz
Audio part							
V$_{o(AF)(rms)}$	AF output voltage (RMS value)	27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
THD	total harmonic distortion	25 kHz FM deviation; 50 µs de-emphasis		-	0.15	0.50	%
		54 % AM modulation		-	0.5	1.0	%
B$_{AF(-3dB)}$	−3 dB AF bandwidth	without de-emphasis; measured with FM-PLL filter of Figure 26		80	100	-	kHz
S/N$_{W(AF)}$	weighted signal-to-noise ratio of audio signal	black picture; see Figure 21		50	56	-	dB
		in accordance with *"ITU-R BS.468-4"*		45	50	-	dB
α$_{AM(sup)}$	AM suppression of FM demodulator	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		40	46	-	dB
PSRR$_{AM}$	power supply ripple rejection	see Figure 8		20	26	-	dB
PSRR$_{FM}$	power supply ripple rejection	f$_{ripple}$ = 70 Hz; see Figure 8		14	20	-	dB
V$_{o(intc)(rms)}$	IF intercarrier output level (RMS value)	QSS mode; SC$_1$; SC$_2$ off		90	140	180	mV
		L standard; without modulation		90	140	180	mV
		intercarrier mode; PC / SC$_1$ = 20 dB; SC$_2$ off	[6]	-	75	-	mV
Reference frequency input; pin REF							
f$_{ref}$	reference signal frequency		[7]	-	4	-	MHz
V$_{ref(rms)}$	reference signal voltage (RMS value)	operation as input terminal		80	-	400	mV

[1] Values of video and sound parameters can be decreased at V$_P$ = 4.5 V.

[2] The sound carrier trap can be bypassed by switching the I²C-bus. In this way the full composite video spectrum appears at pin CVBS. The amplitude is 1.1 V (p-p).

[3] Condition: luminance range (5 steps) from 0 % to 100 %.

[4] AC load; C$_L$ < 20 pF and R$_L$ > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps (see Figure 15 to Figure 20; |H (s)| is the absolute value of transfer function).

[5] S/N is the ratio of black-to-white amplitude to the noise voltage (RMS value measured on pin CVBS and tested at video black level, 'quiet line'). Noise analyzer settings: B = 5 MHz, 200 kHz high-pass and sound carrier trap on. In case of S/N$_W$ weighted in accordance with *"ITU-T J.61"*. Measurements taken for B/G standard.

[6] The intercarrier output signal at pin SIOMAD can be calculated by the following formula taking into account the internal video signal with

1.1 V (p-p) as a reference: $V_{o(intc)(rms)} = 1.1 \times \frac{1}{2\sqrt{2}} \times 10^r \ V$ and $r = \frac{1}{20} \times \left(\frac{V_{i(SC)}}{V_{i(PC)}} (dB) + 6 \ dB \pm 3 \ dB \right)$, where: $\frac{1}{2\sqrt{2}}$ is the

correction term for RMS value, $\frac{V_{i(SC)}}{V_{i(PC)}}$ (dB) is the sound-to-picture carrier ratio at pins VIF1 and VIF2 in dB, 6 dB is the correction term

of internal circuitry and ±3 dB is the tolerance of video output and intercarrier output V$_{o(intc)(rms)}$.
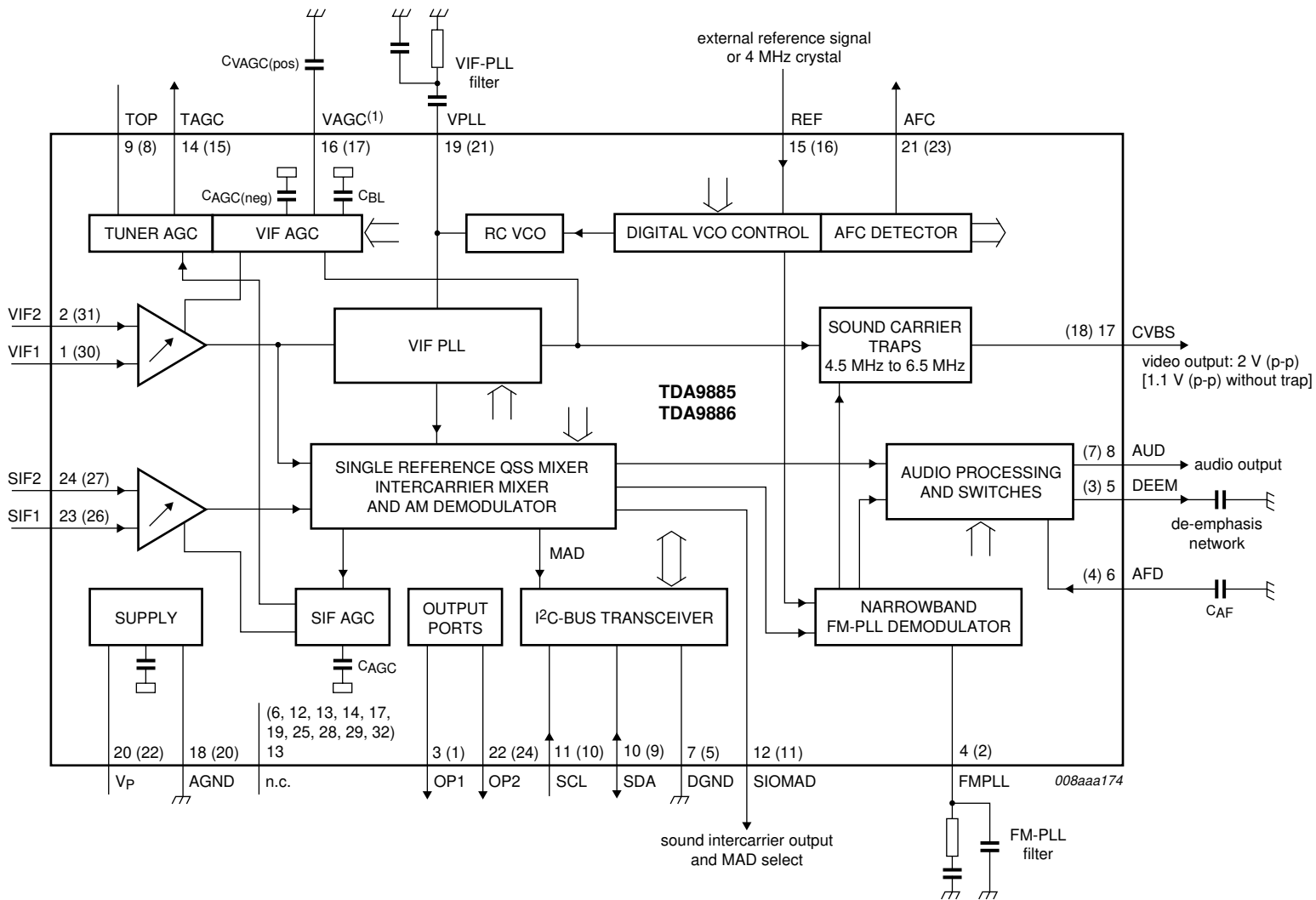
[7]   Pin REF is able to operate as a 1-pin crystal oscillator input as well as an external reference signal input, e.g. from the tuning system.

5. Ordering information

Table 2.   Ordering information

Type number	Package			Version
	Name	**Description**		
TDA9885T/V3	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
TDA9885TS/V3	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1
TDA9885HN/V3	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm		SOT617-3
TDA9886T/V4	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
TDA9886TS/V4	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1
TDA9886HN/V4	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm		SOT617-3
TDA9885T/V5	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
TDA9885TS/V5	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1
TDA9885HN/V5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm		SOT617-3
TDA9886T/V5	SO24	plastic small outline package; 24 leads; body width 7.5 mm		SOT137-1
TDA9886TS/V5	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm		SOT340-1
TDA9886HN/V5	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body $5 \times 5 \times 0.85$ mm		SOT617-3

6. Block diagram

external reference signal
or 4 MHz crystal

| TOP | TAGC | | VAGC(1) | VPLL | | REF | AFC |
| 9 (8) | 14 (15) | | 16 (17) | 19 (21) | | 15 (16) | 21 (23) |

C_VAGC(pos)

VIF-PLL filter

C_AGC(neg)   C_BL

TUNER AGC   VIF AGC   RC VCO   DIGITAL VCO CONTROL   AFC DETECTOR

VIF2 2 (31)
VIF1 1 (30)

VIF PLL

**TDA9885
TDA9886**

SOUND CARRIER TRAPS
4.5 MHz to 6.5 MHz

(18) 17   CVBS
video output: 2 V (p-p)
[1.1 V (p-p) without trap]

SIF2 24 (27)
SIF1 23 (26)

SINGLE REFERENCE QSS MIXER
INTERCARRIER MIXER
AND AM DEMODULATOR

AUDIO PROCESSING
AND SWITCHES

(7) 8   AUD   audio output
(3) 5   DEEM

de-emphasis network

MAD

(4) 6   AFD

C_AF

SUPPLY   SIF AGC   OUTPUT PORTS   I²C-BUS TRANSCEIVER   NARROWBAND
FM-PLL DEMODULATOR

C_AGC

(6, 12, 13, 14, 17,
19, 25, 28, 29, 32)
13

| 20 (22) | 18 (20) | | 3 (1) | 22 (24) | 11 (10) | 10 (9) | 7 (5) | 12 (11) | | 4 (2) |
| V_P | AGND | n.c. | OP1 | OP2 | SCL | SDA | DGND | SIOMAD | | FMPLL |

sound intercarrier output
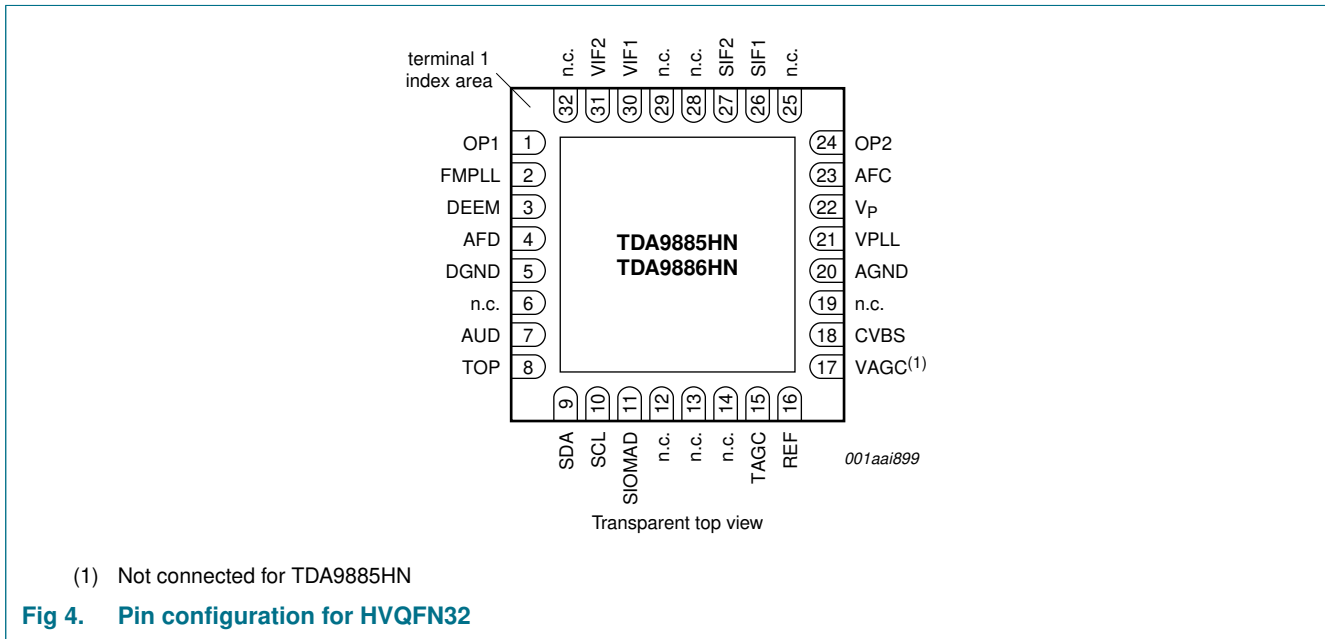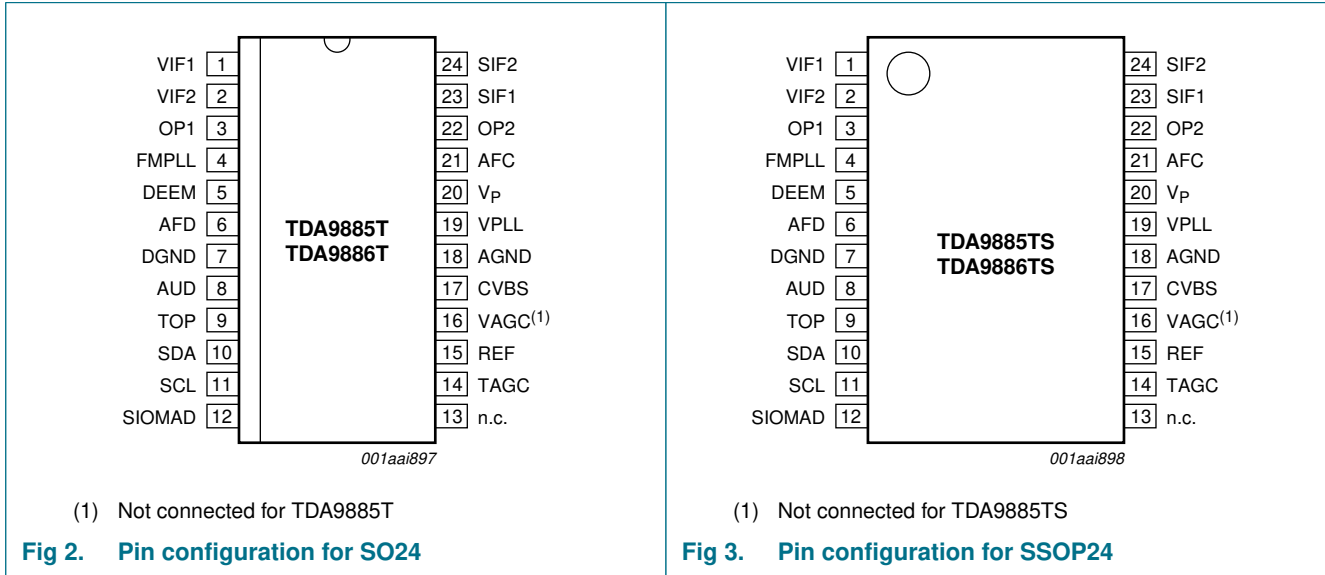and MAD select

FM-PLL filter

008aaa174

Pin numbers for TDA9885HN and TDA9886HN in parentheses.

(1) Not connected for TDA9885

Fig 1.   Block diagram of TDA9885; TDA9886

7. Pinning information

7.1 Pinning

(1) Not connected for TDA9885T

Fig 2. **Pin configuration for SO24**

(1) Not connected for TDA9885TS

Fig 3. **Pin configuration for SSOP24**

(1) Not connected for TDA9885HN

Fig 4. **Pin configuration for HVQFN32**

7.2 Pin description

Table 3.   Pin description

Symbol	Pin				Description
	TDA9885T TDA9885TS	**TDA9886T TDA9886TS**	**TDA9885HN**	**TDA9886HN**	
VIF1	1	1	30	30	VIF differential input 1
VIF2	2	2	31	31	VIF differential input 2
n.c.	-	-	32	32	not connected
OP1	3	3	1	1	output port 1; open-collector
FMPLL	4	4	2	2	FM PLL for loop filter
DEEM	5	5	3	3	de-emphasis output for capacitor
AFD	6	6	4	4	AF DC-decoupling capacitor
DGND	7	7	5	5	digital ground
n.c.	-	-	6	6	not connected
AUD	8	8	7	7	audio output
TOP	9	9	8	8	tuner AGC TOP for resistor adjustment
SDA	10	10	9	9	I2C-bus data input and output
SCL	11	11	10	10	I2C-bus clock input
SIOMAD	12	12	11	11	sound intercarrier output and MAD select with resistor
n.c.	-	-	12	12	not connected
n.c.	13	13	13	13	not connected
n.c.	-	-	14	14	not connected
TAGC	14	14	15	15	tuner AGC output
REF	15	15	16	16	4 MHz crystal or reference signal input
VAGC	-	16	-	17	VIF AGC for capacitor
n.c.	16	-	17	-	not connected
CVBS	17	17	18	18	composite video output
n.c.	-	-	19	19	not connected
AGND	18	18	20	20	analog ground
VPLL	19	19	21	21	VIF PLL for loop filter
V_P	20	20	22	22	supply voltage
AFC	21	21	23	23	AFC output
OP2	22	22	24	24	output port 2; open-collector
n.c.	-	-	25	25	not connected
SIF1	23	23	26	26	SIF differential input 1 and MAD select with resistor
SIF2	24	24	27	27	SIF differential input 2 and MAD select with resistor
n.c.	-	-	28	28	not connected
n.c.	-	-	29	29	not connected

TDA9885_TDA9886_3

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8. Functional description

Figure 1 shows the simplified block diagram of the device which comprises the following functional blocks:

- VIF amplifier
- Tuner AGC and VIF AGC
- VIF-AGC detector
- Frequency Phase-Locked Loop (FPLL) detector
- VCO and divider
- AFC and digital acquisition help
- Video demodulator and amplifier
- Sound carrier trap
- SIF amplifier
- SIF-AGC detector
- Single reference QSS mixer
- AM demodulator
- FM demodulator and acquisition help
- Audio amplifier and mute time constant
- Internal voltage stabilizer
- I²C-bus transceiver and MAD

8.1 VIF amplifier

The VIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration and collector resistor variation. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

8.2 Tuner AGC and VIF AGC

This block adapts the voltage, generated at the VIF-AGC detector, to the internal signal processing at the VIF amplifier and performs the tuner AGC control current generation. The onset of the tuner AGC control current generation can be set either via the I²C-bus (see Table 12) or optionally by a potentiometer at pin TOP (in case that the I²C-bus information cannot be stored, related to the device). The presence of a potentiometer is automatically detected and the I²C-bus setting is disabled.

Furthermore, derived from the AGC detector voltage, a comparator is used to detect if the corresponding VIF input voltage is higher than 200 µV. This information can be read out via the I²C-bus (bit VIFLEV = 1).

8.3 VIF-AGC detector

Gain control is performed by sync level detection (negative modulation) or peak white detection (positive modulation).

For negative modulation, the sync level voltage is stored at an integrated capacitor by means of a fast peak detector. This voltage is compared with a reference voltage (nominal sync level) by a comparator which charges or discharges the integrated AGC capacitor for providing of the required VIF gain. The time constants for decreasing or increasing the gain are nearly equal and the total AGC reaction time is fast to cope with 'aeroplane fluttering'.

For positive modulation, the white peak level voltage is compared with a reference voltage (nominal white level) by a comparator which charges (fast) or discharges (slow) the external AGC capacitor directly for providing the required VIF gain. The need of a very long time constant for VIF gain increase is due to peak white level may appear only once in a field. In order to reduce this time constant, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step controlled by the detected actual black level voltage. The threshold level for fast mode AGC is typically −6 dB video amplitude. The fast mode state is also transferred to the SIF-AGC detector for speed-up. In case of missing peak white pulses, the VIF gain increase is limited to typically +3 dB by comparing the detected actual black level voltage with a corresponding reference voltage.

8.4 FPLL detector

The VIF amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier for removing the video AM.

During acquisition the frequency detector produces a current proportional to the frequency difference between the VIF and the VCO signals. After frequency lock-in the phase detector produces a current proportional to the phase difference between the VIF and the VCO signals. The currents from the frequency and phase detectors are charged into the loop filter which controls the VIF VCO and locks it to the frequency and phase of the VIF carrier.

For a positive modulated VIF signal, the charging currents are optional gated by the composite sync in order to avoid signal distortion in case of overmodulation. The gating depth is switchable via the I²C-bus.

8.5 VCO and divider

The VCO of the VIF FPLL operates as an integrated low radiation relaxation oscillator at double the picture carrier frequency. The control voltage, required to tune the VCO to double the picture carrier frequency, is generated at the loop filter by the frequency phase detector. The possible frequency range is 50 MHz to 140 MHz (typical value).

The oscillator frequency is divided-by-two to provide two differential square wave signals with exactly 90 degrees phase difference, independent of the frequency, for use in the FPLL detectors, the video demodulator and the intercarrier mixer.

8.6 AFC and digital acquisition help

Each relaxation oscillator of the VIF-PLL and FM-PLL demodulator has a wide frequency range. To prevent false locking of the PLLs and with respect to the catching range, the digital acquisition help provides an individual control, until the frequency of the VCO is within the preselected standard dependent lock-in window of the PLL.

The in-window and out-window control at the FM PLL is additionally used to mute the audio stage (if auto mute is selected via the I²C-bus).

The working principle of the digital acquisition help is as follows. The PLL VCO output is connected to a down counter which has a predefined start value (standard dependent). The VCO frequency clocks the down counter for a fixed gate time. Thereafter, the down counter stop value is analyzed. In case the stop value is higher (lower) than the expected value range, the VCO frequency is lower (higher) than the wanted lock-in window frequency range. A positive (negative) control current is injected into the PLL loop filter and consequently the VCO frequency is increased (decreased) and a new counting cycle starts.

The gate time as well as the control logic of the acquisition help circuit is dependent on the precision of the reference signal at pin REF. Operation as a crystal oscillator is possible as well as connecting this input via a serial capacitor to an external reference frequency, e.g. the tuning system oscillator.

The AFC signal is derived from the corresponding down counter stop value after a counting cycle. The last four bits are latched and can be read out via the I²C-bus (see Table 8). Also the digital-to-analog converted value is given as current at pin AFC.

8.7 Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The VIF signal is multiplied with the 'in phase' signal of the VIF-PLL VCO.

The demodulator output signal is fed into the video preamplifier via a level shift stage with integrated low-pass filter to achieve carrier harmonics attenuation.

The output signal of the preamplifier is fed to the VIF-AGC detector (see Section 8.3) and in the sound trap mode also fed internally to the integrated sound carrier trap (see Section 8.8). The differential trap output signal is converted to a single-ended signal and amplified by the following post-amplifier. The video output level at pin CVBS is 2 V (p-p).

In the trap bypass mode the output signal of the preamplifier is fed directly through the post-amplifier to pin CVBS. The output video level is 1.1 V (p-p) for using an external sound trap with 10 % overall loss.

Noise clipping is provided in both cases.

8.8 Sound carrier trap

The sound trap is constructed of three separate traps to realize sufficient suppression of the first and second sound carriers.

For frequency control of the sound trap additionally a reference low-pass filter and a phase detector are built in.

A sound carrier reference signal is fed into the reference low-pass filter and is shifted by nominal 90 degrees. The phase detector compares the original reference signal with the signal shifted by the reference filter and produces a DC voltage by charging or discharging an integrated capacitor with a current proportional to the phase difference between both signals, respectively to the frequency error of the integrated filters. The DC voltage controls the frequency position of the reference filter and the sound trap. So the accurate frequency position for the different standards is set by the sound carrier reference signal.

8.9 SIF amplifier

The SIF amplifier consists of three AC-coupled differential stages. Gain control is performed by emitter degeneration and collector resistor variation. The total gain control range is typically 66 dB. The differential input impedance is typically 2 kΩ in parallel with 3 pF.

8.10 SIF-AGC detector

SIF gain control is performed by detection and controlling to a reference value of the DC component of the AM demodulator output signal. This DC signal corresponds directly to the SIF voltage at the output of the SIF amplifier so that a constant SIF signal is supplied to the AM demodulator and to the single reference QSS mixer.

By switching the gain of the input amplifier of the SIF-AGC detector via the I²C-bus, the internal SIF level for FM sound is 5.5 dB lower than for AM sound. This is to adapt the SIF-AGC characteristic to the VIF-AGC characteristic. The adaption is ideal for a picture-to-sound FM carrier ratio of 13 dB.

Via a comparator, the integrated AGC capacitor is charged or discharged for providing the required SIF gain. Due to AM sound, the AGC reaction time is slow (f_c < 20 Hz for the closed AGC loop). For reducing this AM sound time constant in the event of a decreasing IF amplitude step, the charge/discharge current of the AGC capacitor is increased (fast mode) when the VIF-AGC detector (at positive modulation mode) operates in the fast mode too. An additional circuit (threshold approximately 7 dB) ensures a very fast gain reduction for a large increasing IF amplitude step.

8.11 Single reference QSS mixer

With the present system a high performance Hi-Fi stereo sound processing can be achieved. For a simplified application without a SIF SAW filter, the single reference QSS mixer can be switched to the intercarrier mode via the I²C-bus.

The single reference QSS mixer generates the 2nd FM TV sound intercarrier signal. It is realized by a linear multiplier which multiplies the SIF amplifier output signal and the VIF-PLL VCO signal (90 degrees output) which is locked to the picture carrier. In this way the QSS mixer operates as a quadrature mixer in the intercarrier mode and provides suppression of the low frequency video signals.

The QSS mixer output signal is fed internally via a high-pass and low-pass combination to the FM demodulator as well as via an operational amplifier to the intercarrier output pin SIOMAD.

8.12 AM demodulator

The amplitude modulated SIF amplifier output signal is fed both to a two-stage limiting amplifier that removes the AM and to a linear multiplier. The result of the multiplication of the SIF signal with the limiter output signal is AM demodulation (passive synchronous demodulator). The demodulator output signal is fed via a low-pass filter that attenuates the carrier harmonics and through the input amplifier of the SIF-AGC detector to the audio amplifier.

8.13 FM demodulator and acquisition help

The narrowband FM-PLL detector consists of:

- Gain controlled FM amplifier and AGC detector
- Narrowband PLL

The 2nd SIF signal from the intercarrier mixer is fed to the input of an AC-coupled gain controlled amplifier with two stages. The gain controlled output signal is fed to the phase detector of the narrowband FM PLL (FM demodulator). For good selectivity and robustness against disturbance caused by the video signal, a high linearity of the gain controlled FM amplifier and of the phase detector as well as a constant signal level are required. The gain control is done by means of an 'in phase' demodulator for the 2nd SIF signal (from the output of the FM amplifier). The demodulation output is fed into a comparator for charging or discharging the integrated AGC capacitor. This leads to a mean value AGC loop to control the gain of the FM amplifier.

The FM demodulator is realized as a narrowband PLL with an external loop filter, which provides the necessary selectivity (bandwidth approximately 100 kHz). To achieve good selectivity, a linear phase detector and a constant input level are required. The gain controlled intercarrier signal from the FM amplifier is fed to the phase detector. The phase detector controls via the loop filter the integrated low radiation relaxation oscillator. The designed frequency range is from 4 MHz to 7 MHz.

The VCO within the FM PLL is phase-locked to the incoming 2nd SIF signal, which is frequency modulated. As well as this, the VCO control voltage is superimposed by the AF voltage. Therefore, the VCO tracks with the FM of the 2nd SIF signal. So, the AF voltage is present at the loop filter and is typically 5 mV (RMS) for 27 kHz FM deviation. This AF signal is fed via a buffer to the audio amplifier.

The correct locking of the PLL is supported by the digital acquisition help circuit (see Section 8.6).

8.14 Audio amplifier and mute time constant

The audio amplifier consists of two parts:

- AF preamplifier
- AF output amplifier

The AF preamplifier used for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator is 5 mV (RMS) for a frequency deviation of 27 kHz and is amplified by 30 dB. By the use of a DC operating point control circuit (with external capacitor CAF), the AF preamplifier is decoupled from the PLL DC voltage. The low-pass characteristic of the amplifier reduces the harmonics of the 2nd SIF signal at the AF output terminal.

For FM sound a switchable de-emphasis network (with external capacitor) is implemented between the preamplifier and the output amplifier.

The AF output amplifier provides the required AF output level by a rail-to-rail output stage. A preceding stage makes use of an input selector for switching between FM sound, AM sound and mute state. The gain can be switched between 10 dB (normal) and 4 dB (reduced).

Switching to the mute state is controlled automatically, dependent on the digital acquisition help in case the VCO of the FM PLL is not in the required frequency window. This is done by a time constant: fast for switching to the mute state and slow (typically 40 ms) for switching to the no-mute state.

All switching functions are controlled via the I²C-bus:

- AM sound, FM sound and forced mute
- Auto mute enable or disable
- De-emphasis off or on with 50 µs or 75 µs
- Audio gain normal or reduced

8.15 Internal voltage stabilizer

The band gap circuit internally generates a voltage of approximately 2.4 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.55 V which is used as an internal reference voltage.

8.16 I²C-bus transceiver and MAD

The device can be controlled via the 2-wire I²C-bus by a microcontroller. Two wires carry serial data (SDA) and serial clock (SCL) information between the devices connected to the I²C-bus.

The device has an I²C-bus slave transceiver with auto-increment. The circuit operates up to clock frequencies of 400 kHz.

A slave address is sent from the master to the slave receiver. To avoid conflicts in a real application with other devices providing similar or complementing functions, there are four possible slave addresses available. These MADs can be selected by connecting resistors on pin SIOMAD and/or pins SIF1 and SIF2 (see Figure 26). Pin SIOMAD relates with bit A0 and pins SIF1 and SIF2 relate with bit A3. The slave addresses of this device are given in Table 4.

The power-on preset value is dependent on the use of pin SIOMAD and can be chosen for 45.75 MHz NTSC as default (pin SIOMAD left open-circuit) or 58.75 MHz NTSC (resistor on pin SIOMAD). In this way the device can be used without the I²C-bus as an NTSC only device.

Remark: In case of using the device without the I²C-bus, then the rise time of the supply voltage after switching on power must be longer than 1.2 µs.

Table 4. **Slave address detection**

Slave address	Selectable address bit		Resistor on pin	
	A3	**A0**	**SIF1 and SIF2**	**SIOMAD**
MAD1	0	1	no	no
MAD2	0	0	no	yes
MAD3	1	1	yes	no
MAD4	1	0	yes	yes

9. I²C-bus control

9.1 Read format

S	BYTE 1		A	BYTE 2	NA	P
	A6 to A0	R/$\overline{\text{W}}$		D7 to D0		
	slave address	1		data		

from master to slave

from slave to master

S = START condition
A = acknowledge
NA = not acknowledge
P = STOP condition

008aaa115
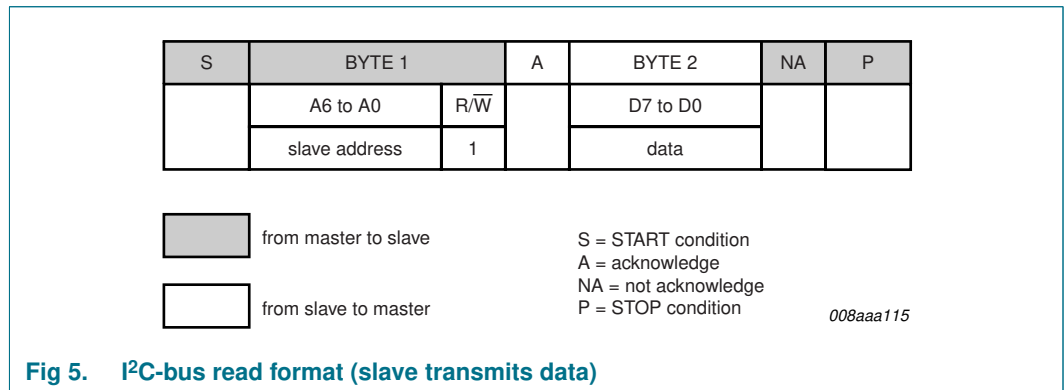
Fig 5. **I²C-bus read format (slave transmits data)**

The master generates an acknowledge when it has received the data word READ. The master next generates an acknowledge, then slave begins transmitting the data word READ, and so on until the master generates an acknowledge-not bit and transmits a STOP condition.

9.1.1 Slave address

The first module address MAD1 is the standard address (see Table 4).

Table 5. **Slave addresses**
For MAD activation via external resistor: see Table 4 and Figure 26.
For applications without I²C-bus: see Table 16 and Table 17.

Slave address		Bit						
Name	**Value**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
MAD1	43h	1	0	0	0	0	1	1
MAD2	42h	1	0	0	0	0	1	0
MAD3	4Bh	1	0	0	1	0	1	1
MAD4	4Ah	1	0	0	1	0	1	0

9.1.2　Data byte

Table 6.　Data read register (status register)

MSB							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
AFCWIN	VIFLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 7.　Description of status register bits

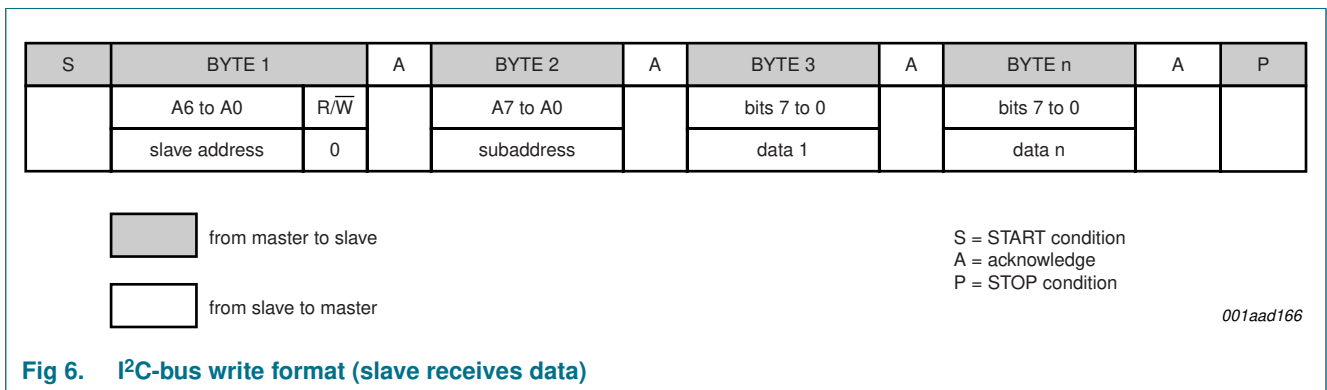| Bit	Symbol	Description
7	AFCWIN	AFC window
		1 = VCO in ±1.6 MHz AFC window[1]
		0 = VCO out of ±1.6 MHz AFC window
6	VIFLEV	VIF input level
		1 = high level; VIF input voltage ≥ 200 μV (typically)
		0 = low level
5	CARRDET	FM carrier detection
		1 = detection
		0 = no detection
4 to 1	AFC[4:1]	automatic frequency control; see Table 8
0	PONR	power-on reset
		1 = after power-on reset or after supply breakdown
		0 = after a successful reading of the status register

[1]　If no IF input is applied, then bit AFCWIN = 1 due to the fact that the VCO is forced to the AFC window border for fast lock-in behavior.

Table 8.   Automatic frequency control bits

f_0 is the nominal frequency of f_{VIF}.

Bit				f_{VIF}
AFC4	**AFC3**	**AFC2**	**AFC1**	
0	1	1	1	$\leq (f_0 - 187.5 \text{ kHz})$
0	1	1	0	$f_0 - 162.5 \text{ kHz}$
0	1	0	1	$f_0 - 137.5 \text{ kHz}$
0	1	0	0	$f_0 - 112.5 \text{ kHz}$
0	0	1	1	$f_0 - 87.5 \text{ kHz}$
0	0	1	0	$f_0 - 62.5 \text{ kHz}$
0	0	0	1	$f_0 - 37.5 \text{ kHz}$
0	0	0	0	$f_0 - 12.5 \text{ kHz}$
1	1	1	1	$f_0 + 12.5 \text{ kHz}$
1	1	1	0	$f_0 + 37.5 \text{ kHz}$
1	1	0	1	$f_0 + 62.5 \text{ kHz}$
1	1	0	0	$f_0 + 87.5 \text{ kHz}$
1	0	1	1	$f_0 + 112.5 \text{ kHz}$
1	0	1	0	$f_0 + 137.5 \text{ kHz}$
1	0	0	1	$f_0 + 162.5 \text{ kHz}$
1	0	0	0	$\geq (f_0 + 187.5 \text{ kHz})$

9.2 Write format

S	BYTE 1		A	BYTE 2	A	BYTE 3	A	BYTE n	A	P
	A6 to A0	R/$\overline{W}$		A7 to A0		bits 7 to 0		bits 7 to 0		
	slave address	0		subaddress		data 1		data n		

from master to slave

from slave to master

S = START condition
A = acknowledge
P = STOP condition

001aad166

Fig 6.   I²C-bus write format (slave receives data)

9.2.1 Subaddress (A data)

If more than one data byte is transmitted, then auto-increment is performed: starting from the transmitted subaddress and auto-increment of subaddress in accordance with the order of Table 9.

Table 9.   Definition of the subaddress (second byte after slave address)
X = don't care.

Register	MSB							LSB
	A7[1]	A6[2]	A5[2]	A4[2]	A3[2]	A2[2]	A1	A0
SAD for switching mode	0	X	X	X	X	X	0	0
SAD for adjust mode	0	X	X	X	X	X	0	1
SAD for data mode	0	X	X	X	X	X	1	0

[1]   Bit A7 = 1 is not allowed.

[2]   Bits A6 to A2 will be ignored by the internal hardware.

9.2.2 Data byte for switching mode (B data)

Table 10.   Bit description of SAD register for switching mode (SAD = 00)

Bit	Symbol	Description
7	B7	output port 2 for SAW switching or monitoring
		1 = high-impedance, disabled or HIGH
		0 = low-impedance, active or LOW
6	B6	output port 1 for SAW switching or external input
		1 = high-impedance, disabled or HIGH
		0 = low-impedance, active or LOW
5	B5	forced audio mute
		1 = on
		0 = off
4 and 3	B[4:3]	TV standard modulation
		00 = positive AM TV[1]
		01 = not used
		10 = negative FM TV
		11 = not used
2	B2	carrier mode
		1 = QSS mode
		0 = intercarrier mode
1	B1	auto mute of FM AF output
		1 = active
		0 = inactive
0	B0	video mode (sound trap)
		1 = sound trap bypass
		0 = sound trap active

[1]   For positive AM TV choose 6.5 MHz for the second SIF.

9.2.3 Data byte for adjust mode (C data)

Table 11. Bit description of SAD register for adjust mode (SAD = 01)

Bit	Symbol	Description
7	C7	audio gain
		1 = −6 dB
		0 = 0 dB
6	C6	de-emphasis time constant
		1 = 50 µs
		0 = 75 µs
5	C5	de-emphasis
		1 = on
		0 = off
4 to 0	C[4:0]	tuner TOP adjustment; see Table 12

Table 12. Tuner takeover point adjustment bits

Bit					TOP adjustment (dB)
C4	C3	C2	C1	C0	
1	1	1	1	1	+15
1	1	1	1	0	+14
1	1	1	0	1	+13
1	1	1	0	0	+12
1	1	0	1	1	+11
1	1	0	1	0	+10
1	1	0	0	1	+9
1	1	0	0	0	+8
1	0	1	1	1	+7
1	0	1	1	0	+6
1	0	1	0	1	+5
1	0	1	0	0	+4
1	0	0	1	1	+3
1	0	0	1	0	+2
1	0	0	0	1	+1
1	0	0	0	0	0[1]
0	1	1	1	1	−1
0	1	1	1	0	−2
0	1	1	0	1	−3
0	1	1	0	0	−4
0	1	0	1	1	−5
0	1	0	1	0	−6
0	1	0	0	1	−7
0	1	0	0	0	−8
0	0	1	1	1	−9
0	0	1	1	0	−10

Table 12.   Tuner takeover point adjustment bits *…continued*

Bit					TOP adjustment (dB)
C4	C3	C2	C1	C0	
0	0	1	0	1	−11
0	0	1	0	0	−12
0	0	0	1	1	−13
0	0	0	1	0	−14
0	0	0	0	1	−15
0	0	0	0	0	−16

[1]   For 0 dB refer to Section 12 symbol QV_{TOP}.

9.2.4   Data byte for data mode (E data)

Table 13.   Bit description of SAD register for data mode (SAD = 10)

Bit	Symbol	Description
7	E7	VIF AGC and port features; dependent on bit E5; see Table 14
6	E6	L standard PLL gating
		1 = gating in case of 36 % positive modulation
		0 = gating in case of 0 % positive modulation
5	E5	VIF, SIF and tuner minimum gain; dependent on bit E7; see Table 14
4 to 2	E[4:2]	vision intermediate frequency selection; see Table 15
1 and 0	E[1:0]	sound intercarrier frequency selection (sound 2nd IF)
		00 = f_{FM} = 4.5 MHz
		01 = f_{FM} = 5.5 MHz
		10 = f_{FM} = 6.0 MHz
		11 = f_{FM} = 6.5 MHz[1]

[1]   For positive modulation choose 6.5 MHz.

Table 14.   Options in extended TV mode; bit B3 = 0 of SAD 00 register

Function	Bit E7 = 0		Bit E7 = 1	
	Bit E5 = 0	Bit E5 = 1	Bit E5 = 0	Bit E5 = 1
Pin OP1	port function	port function	port function	VIF-AGC external input[1]
Pin OP2	port function	port function	VIF-AGC output[1]	port function
Gain	normal gain	minimum gain	normal gain	external gain

[1]   The corresponding port function has to be disabled (set to 'high-impedance'); see Table 10 and Table note 12 of Table 20.

Table 15. TV standard selection for VIF

Video IF select bits			f_{VIF} (MHz)
E4	**E3**	**E2**	
0	0	0	58.75[1]
0	0	1	45.75[1]
0	1	0	38.9
0	1	1	38.0
1	0	0	33.9
1	0	1	33.4
1	1	0	not applicable
1	1	1	not applicable

[1] Pin SIOMAD can be used for the selection of the different NTSC standards without I²C-bus. With a resistor on pin SIOMAD, f_{VIF} = 58.75 MHz; without a resistor on pin SIOMAD, f_{VIF} = 45.75 MHz (NTSC-M).

Table 16. Data setting after power-on reset (default setting with a resistor on pin SIOMAD)

Register	Byte							
	MSB							**LSB**
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Switching mode (B data)	1	1	0	1	0	1	1	0
Adjust mode (C data)	0	0	1	1	0	0	0	0
Data mode (E data)	0	0	0	0	0	0	0	0

Table 17. Data setting after power-on reset (default setting without a resistor on pin SIOMAD)

Register	Byte							
	MSB							**LSB**
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Switching mode (B data)	1	1	0	1	0	1	1	0
Adjust mode (C data)	0	0	1	1	0	0	0	0
Data mode (E data)	0	0	0	0	0	1	0	0

10. Limiting values

Table 18. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_P	supply voltage		-	5.5	V
V_n	voltage on				
	pins VIF1, VIF2, SIF1, SIF2, OP1, OP2, V_P and FMPLL		0	V_P	V
	pin TAGC		0	8.8	V
t_{sc}	short-circuit time	to ground or V_P	-	10	s
T_{stg}	storage temperature		−25	+150	°C
T_{amb}	ambient temperature	TDA9885T (SO24), TDA9885TS (SSOP24), TDA9886T (SO24) and TDA9886TS (SSOP24)	−20	+70	°C
		TDA9885HN (HVQFN32) and TDA9886HN (HVQFN32)	−20	+85	°C
V_{esd}	electrostatic discharge voltage	machine model [1]	−400	+400	V
		human body model [2]	−4000	+3500	V

[1]   Class C according to EIA/JESD22-A115.

[2]   Class 2 according to JESD22-A114.

11. Thermal characteristics

Table 19. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TDA9885T (SO24)		76	K/W
	TDA9885TS (SSOP24)		118	K/W
	TDA9885HN (HVQFN32)		40	K/W
	TDA9886T (SO24)		76	K/W
	TDA9886TS (SSOP24)		118	K/W
	TDA9886HN (HVQFN32)		40	K/W

12. Characteristics

Table 20.   Characteristics

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply; pin V$_P$							
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current			52	63	70	mA
P_{tot}	total power dissipation			-	305	385	mW
Power-on reset							
$V_{P(start)}$	supply voltage for start of reset	decreasing supply voltage		2.5	3.0	3.5	V
$V_{P(stop)}$	supply voltage for end of reset	increasing supply voltage; I²C-bus transmission enable		-	-	4.4	V
τ_P	time constant (R × C) for network at pin V$_P$	for applications without I²C-bus		1.2	-	-	µs
VIF amplifier; pins VIF1 and VIF2							
$V_{i(VIF)(rms)}$	VIF input voltage sensitivity (RMS value)	−1 dB video at output		-	60	100	µV
$V_{i(max)(rms)}$	maximum input voltage (RMS value)	+1 dB video at output		150	190	-	mV
$V_{i(ovl)(rms)}$	overload input voltage (RMS value)		[2]	-	-	440	mV
$\Delta V_{IF(int)}$	internal IF amplitude difference between picture and sound carrier	within AGC range; Δf = 5.5 MHz		-	0.7	-	dB
$G_{VIF(cr)}$	control range VIF gain	see Figure 9		60	66	-	dB
$B_{VIF(−3dB)(ll)}$	lower limit −3 dB VIF bandwidth			-	15	-	MHz
$B_{VIF(−3dB)(ul)}$	upper limit −3 dB VIF bandwidth			-	80	-	MHz
$R_{i(dif)}$	differential input resistance		[3]	-	2	-	kΩ
$C_{i(dif)}$	differential input capacitance		[3]	-	3	-	pF
V_I	DC input voltage			-	1.93	-	V
FPLL and true synchronous video demodulator[4]							
$f_{VCO(max)}$	maximum oscillator frequency for carrier regeneration	f = 2f$_{PC}$		120	140	-	MHz
f_{VIF}	vision carrier operating frequencies	see Table 13		-	33.4	-	MHz
				-	33.9	-	MHz
				-	38.0	-	MHz
				-	38.9	-	MHz
				-	45.75	-	MHz
				-	58.75	-	MHz
Δf_{VIF}	VIF frequency window of digital acquisition help	related to f$_{VIF}$; see Figure 12		-	±2.3	-	MHz

Table 20. Characteristics …continued

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{acq}	acquisition time	BL = 70 kHz	[5]	-	-	30	ms
$V_{i(lock)(rms)}$	input voltage sensitivity for PLL to be locked (RMS value)	measured on pins VIF1 and VIF2; maximum IF gain		-	30	70	μV
$T_{cy(dah)}$	digital acquisition help cycle time			-	64	-	μs
$K_{O(VIF)}$	VIF VCO steepness	definition: Δf_{VIF} / ΔV_{VPLL}		-	20	-	MHz/V
$K_{D(VIF)}$	VIF phase detector steepness	definition: ΔI_{VPLL} / $\Delta \varphi_{VIF}$		-	23	-	μA/rad
Video output 2 V; pin CVBS							
Normal mode (sound carrier trap active) and sound carrier on							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7		1.7	2.0	2.3	V
ΔV_o	video output voltage difference	difference between L and B/G standard		−12	-	+12	%
V/S	ratio between video (black-to-white) and sync level			1.90	2.33	3.00	
V_{sync}	sync voltage level			1.0	1.2	1.4	V
$V_{clip(u)}$	upper video clipping voltage level			V_P − 1.1	V_P − 1	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.7	0.9	V
R_o	output resistance		[3]	-	-	30	Ω
$I_{bias(int)}$	internal bias current (DC)	for emitter-follower		1.5	2.0	-	mA
$I_{sink(o)(max)}$	maximum output sink current	AC and DC		1	-	-	mA
$I_{source(o)(max)}$	maximum output source current	AC and DC		3.9	-	-	mA
$\Delta V_{o(CVBS)}$	deviation of CVBS output voltage	50 dB gain control		-	-	0.5	dB
		30 dB gain control		-	-	0.1	dB
$\Delta V_{o(bl)}$	black level tilt	negative modulation		-	-	1	%
$\Delta V_{o(bl)(v)}$	vertical black level tilt for worst case in L standard	vision carrier modulated by test line (VITS) only		-	-	3	%
G_{dif}	differential gain	"ITU-T J.63 line 330"	[6]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	"ITU-T J.63 line 330"		-	2	4	deg
S/N_W	weighted signal-to-noise ratio	unified weighting filter ("ITU-T J.61"); see Figure 13	[7]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[7]	47	51	-	dB
$\alpha_{IM(blue)}$	intermodulation attenuation at 'blue'	see Figure 14	[8]				
		f = 1.1 MHz		58	64	-	dB
		f = 3.3 MHz		58	64	-	dB

Table 20.   Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\alpha_{IM(yellow)}$	intermodulation attenuation at 'yellow'	see Figure 14	[8]				
		f = 1.1 MHz		60	66	-	dB
		f = 3.3 MHz		59	65	-	dB
$\Delta V_{r(PC)(rms)}$	residual picture carrier (RMS value)	fundamental wave and harmonics		-	2	5	mV
$\Delta f_{unw(p-p)}$	robustness for unwanted frequency deviation of picture carrier (peak-to-peak value)	3 % residual carrier; 50 % serration pulses; L standard	[3]	-	-	12	kHz
$\Delta \varphi$	robustness for modulator imbalance	0 % residual carrier; 50 % serration pulses; L standard; L-gating = 0 %	[3]	-	-	3	%
α_H	suppression of video signal harmonics	AC load: C_L < 20 pF, R_L > 1 kΩ	[9]	35	40	-	dB
α_{spur}	suppression of spurious elements		[10]	40	-	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 8		20	25	-	dB
M/N standard including Korea; see Figure 15							
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	f_{trap} = 4.5 MHz	[11]	3.95	4.05	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 4.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 4.5 MHz		21	27	-	dB
α_{SC2}	attenuation at second sound carrier	f = 4.724 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 4.724 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 3.58 MHz; see Figure 16		110	180	250	ns
B/G standard; see Figure 17							
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	f_{trap} = 5.5 MHz	[11]	4.90	5.00	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 5.5 MHz		30	36	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 5.5 MHz		24	30	-	dB
α_{SC2}	attenuation at second sound carrier	f = 5.742 MHz		21	27	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 5.742 MHz		15	21	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz; see Figure 18		110	180	250	ns

Table 20.   Characteristics *…continued*

V_P = 5 V; T_{amb} = 25 °C; see Table 22 for input frequencies; B/G standard is used for the specification (f_{PC} = 38.9 MHz; f_{SC} = 33.4 MHz; PC / SC = 13 dB; f_{mod} = 400 Hz); input level $V_{i(VIF)}$ = 10 mV (RMS) (sync level for B/G; peak white level for L); IF input from 50 Ω via broadband transformer 1 : 1; video modulation DSB; residual carrier for B/G is 10 % and for L is 3 %; video signal in accordance with "ITU-T J.63 line 17 and line 330" or "NTC-7 Composite"; measurements taken in test circuit of Figure 26; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I standard; see Figure 19							
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	f_{trap} = 6.0 MHz	[11]	5.40	5.50	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.0 MHz		26	32	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.0 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.55 MHz		12	18	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.55 MHz		10	15	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.43 MHz		-	90	160	ns
D/K standard; see Figure 20							
$B_{v(-3dB)(trap)}$	−3 dB video bandwidth including sound carrier trap	f_{trap} = 6.5 MHz	[11]	5.50	5.95	-	MHz
α_{SC1}	attenuation at first sound carrier	f = 6.5 MHz		26	32	-	dB
$\alpha_{SC1(60kHz)}$	attenuation at first sound carrier f_{SC1} ± 60 kHz	f = 6.5 MHz		20	26	-	dB
α_{SC2}	attenuation at second sound carrier	f = 6.742 MHz		18	24	-	dB
$\alpha_{SC2(60kHz)}$	attenuation at second sound carrier f_{SC2} ± 60 kHz	f = 6.742 MHz		13	18	-	dB
$t_{d(g)(cc)}$	group delay at color carrier frequency	f = 4.28 MHz		-	60	130	ns
Video output 1.1 V; pin CVBS							
Trap bypass mode and sound carrier off[12]							
$V_{o(v)(p-p)}$	video output voltage (peak-to-peak value)	see Figure 7		0.95	1.10	1.25	V
V_{sync}	sync voltage level			1.35	1.5	1.6	V
$V_{clip(u)}$	upper video clipping voltage level			3.5	3.6	-	V
$V_{clip(l)}$	lower video clipping voltage level			-	0.9	1.0	V
$B_{v(-1dB)}$	−1 dB video bandwidth	AC load: C_L < 20 pF, R_L > 1 kΩ		5	6	-	MHz
$B_{v(-3dB)}$	−3 dB video bandwidth	AC load: C_L < 20 pF, R_L > 1 kΩ		7	8	-	MHz
S/N_W	weighted signal-to-noise ratio	unified weighting filter ("ITU-T J.61"); see Figure 13	[7]	56	59	-	dB
S/N_{UW}	unweighted signal-to-noise ratio		[7]	48	52	-	dB