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TDA9897; TDA9898

Multistandard hybrid IF processing

Rev. 04 — 25 May 2009 | Product data sheet

1. General description

The Integrated Circuit (IC) is suitable for Intermediate Frequency (IF) processing including global multistandard Analog TV (ATV), Digital Video Broadcast (DVB) and mono FM radio using only 1 IC and 1 to 3 fixed Surface Acoustic Waves (SAWs) (application dependent). TDA9898 includes, TDA9897 excludes L and L-accent standard.

2. Features

2.1 General

- 5 V supply voltage
- I^2C-bus control over all functions
- Four I^2C-bus addresses provided; selection by programmable Module Address (MAD)
- Three I^2C-bus voltage level supported; selection via pin BVS
- Separate gain controlled amplifiers with input selector and conversion for incoming IF [analog Vision IF (VIF) or Sound IF (SIF) or Digital TV (DTV)] allows the use of different filter shapes and bandwidths
- All conventional ATV standards applicable by using DTV bandwidth window (SAW) filter
- Two 4 MHz reference frequency stages; the first one operates as crystal oscillator, the second one as external signal input
- Stabilizer circuit for ripple rejection and to achieve constant output signals
- Smallest size, simplest application
- ElectroStatic Discharge (ESD) protection for all pins

2.2 Analog TV processing

- Gain controlled wideband VIF amplifier; AC-coupled
- Multistandard true synchronous demodulation with active carrier regeneration: very linear demodulation, good intermodulation figures, reduced harmonics and excellent pulse response
- Integrated Nyquist processing, providing additionally image suppression for high adjacent channel selectivity
- Optional use of conventional Nyquist filter to support a wide range of applications
- Gated phase detector for L and L-accent standards
- Fully integrated VIF Voltage-Controlled Oscillator (VCO), alignment-free, frequencies switchable for all negative and positive modulated standards via I^2C-bus
- VIF Automatic Gain Control (AGC) detector for gain control; operating as a peak sync detector for negative modulated signals and as a peak white detector for positive modulated signals

- Optimized AGC modes for negative modulation; e.g. very fast reaction time for VIF and SIF
- Precise fully digital Automatic Frequency Control (AFC) detector with 4-bit Digital-to-Analog Converter (DAC); AFC bits can be read-out via I^2C-bus
- High precise Tuner AGC (TAGC) TakeOver Point (TOP) for negative modulated standards; TOP adjust via I^2C-bus
- TAGC TOP for positive standards and Received Signal Strength Indication (RSSI); adjustable via I^2C-bus or alternatively by potentiometer
- Fully integrated Sound Carrier (SC) trap for any ATV standard (SC at 4.5 MHz, 5.5 MHz, 6.0 MHz and 6.5 MHz)
- SIF AGC for gain controlled SIF amplifier and high-performance single-reference Quasi Split Sound (QSS) mixer
- Fully integrated sound BP filter supporting any ATV standard
- Optional use of external FM or AM sound BP filter
- AM sound demodulation for L and L-accent standard
- Alignment-free selective FM Phase-Locked Loop (PLL) demodulator with high linearity and low noise; external FM input
- Port function
- VIF AGC voltage monitor output or port function
- TAGC voltage monitor output or port function
- VIF AFC current or tuner, VIF, SIF or FM AGC voltage monitor output
- 2nd SIF output, gain controlled by internal SIF AGC or by internal FM carrier AGC for Digital Signal Processor (DSP)
- Fully integrated BP filter for 2nd SIF at 4.5 MHz, 5.5 MHz, 6.0 MHz or 6.5 MHz

2.3 Digital TV processing

- Applicable for terrestrial and cable TV reception
- 70 dB variable gain wideband IF amplifier (AC-coupled)
- Gain control via external control voltage (0 V to 3 V)
- 2 V (p-p) differential low IF (downconverted) output or 1 V (p-p) 1st IF output for direct Analog-to-Digital Converter (ADC) interfacing
- DVB downconversion with integrated selectivity for Low IF (LIF)
- Integrated anti-aliasing tracking low-pass filter
- Fully integrated synthesizer controlled oscillator with excellent phase noise performance
- Synthesizer frequencies for a wide range of world wide DVB standards (for IF center frequencies of e.g. 34.5 MHz, 36 MHz, 44 MHz and 57 MHz)
- TAGC detector for independent tuner gain control loop applications
- TAGC operating as peak detector, fast reaction time due to additional speed-up detector
- Port function
- TAGC voltage monitor output

2.4 FM radio mode

- Gain controlled wideband Radio IF (RIF) amplifier; AC-coupled
- Buffered RIF amplifier wideband output, gain controlled by internal RIF AGC
- Use of external FM sound BP filter
- 2nd RIF output, gain controlled by internal RIF AGC or by internal FM carrier AGC for DSP
- Alignment-free selective FM PLL demodulator with high linearity and low noise
- Precise fully digital AFC detector with 4-bit DAC; AFC bits read-out via I^{2}C-bus
- Port function
- Radio AFC or tuner, RIF or FM AGC voltage monitor output

3. Applications

- Analog and digital TV front-end applications for TV sets, recording applications and personal computer cards

4. Quick reference data

Table 1. Quick reference data
V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_P	supply voltage		[1]	4.5	5.0	5.5	V
I_P	supply current	ATV QSS; B/G standard; sound carrier trap on; sound BP on		-	-	175	mA
Analog TV signal processing							
Video part							
$V_{i(IF)(RMS)}$	RMS IF input voltage	lower limit at −1 dB video output signal		-	60	100	µV
$G_{VIF(cr)}$	control range VIF gain			60	66	-	dB
f_{VIF}	VIF frequency	see Table 24		-	-	-	MHz
$\Delta f_{VIF(dah)}$	digital acquisition help VIF frequency window	related to f_{VIF}					
		all standards except M/N		-	±2.3	-	MHz
		M/N standard		-	±1.8	-	MHz
$V_{o(video)(p-p)}$	peak-to-peak video output voltage	positive or negative modulation; normal mode and sound carrier on; W6[1] = 0; W4[7] = 0; W7[4] = 0; see Figure 10		1.7	2.0	2.3	V
G_{dif}	differential gain	*"ITU-T J.63 line 330"*	[2][3]				
		B/G standard		-	-	5	%
		L standard		-	-	7	%
φ_{dif}	differential phase	*"ITU-T J.63 line 330"*	[2][3]				
		B/G standard		-	2	4	deg
		L standard		-	2	4	deg

Table 1. Quick reference data *…continued*

V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$B_{video(-3dB)}$	−3 dB video bandwidth	trap bypass mode and sound carrier off; AC load: C_L < 20 pF, R_L > 1 kΩ	[4]	6	8	-	MHz
α_{SC1}	first sound carrier attenuation	M/N standard; f = f_{SC1} = 4.5 MHz; see Figure 21	[4]	38	-	-	dB
		B/G standard; f = f_{SC1} = 5.5 MHz; see Figure 23	[4]	35	-	-	dB
$(S/N)_w$	weighted signal-to-noise ratio	normal mode and sound carrier on; B/G standard; 50 % grey video signal; unified weighting filter (*"ITU-T J.61"*); see Figure 20	[2][5]	53	57	-	dB
$PSRR_{CVBS}$	power supply ripple rejection on pin CVBS	normal mode and sound carrier on; f_{ripple} = 70 Hz; video signal; grey level; positive and negative modulation; see Figure 11	[2]	14	20	-	dB
$\Delta I_{AFC}/\Delta f_{VIF}$	change of AFC current with VIF frequency	AFC TV mode	[6]	0.85	1.05	1.25	µA/kHz
Audio part							
$V_{o(AF)(RMS)}$	RMS AF output voltage	FM: QSS mode; 27 kHz FM deviation; 50 µs de-emphasis		430	540	650	mV
		AM: 54 % modulation		400	500	600	mV
THD	total harmonic distortion	FM: 50 µs de-emphasis; FM deviation: for TV mode 27 kHz and for radio mode 22.5 kHz		-	0.15	0.50	%
		AM: 54 % modulation; BP on; see Figure 33		-	0.5	1.0	%
$f_{-3dB(AF)}$	AF cut-off frequency	W3[2] = 0; W3[4] = 0; without de-emphasis; FM window width = 237.5 kHz		80	100	-	kHz
$(S/N)_{w(AF)}$	AF weighted signal-to-noise ratio	*"ITU-R BS.468-4"*					
		FM: 27 kHz FM deviation; 50 µs de-emphasis; vision carrier unmodulated; FM PLL only		48	56	-	dB
		AM: BP off		44	50	-	dB
PSRR	power supply ripple rejection	f_{ripple} = 70 Hz; see Figure 11		14	20	-	dB

Table 1. Quick reference data *...continued*

V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{o(RMS)}$	RMS output voltage	IF intercarrier single-ended to GND; see Figure 9 and Table 21					
		B/G standard; SC1 on; SC2 off; internal BP via FM AGC		90	140	180	mV
		L standard; without modulation; W7[5] = 0; internal BP + 6 dB		90	140	180	mV
FM sound part							
$V_{i(FM)(RMS)}$	RMS FM input voltage	gain controlled operation; W1[1:0] = 10 or W1[1:0] = 11 or W1[1:0] = 01; see Figure 9		2	-	300	mV
$\Delta I_{AFC}/\Delta f_{RIF}$	change of AFC current with RIF frequency	AFC radio mode	[6]	0.85	1.05	1.25	µA/kHz
α_{AM}	AM suppression	referenced to 27 kHz FM deviation; 50 µs de-emphasis; AM: f = 1 kHz; m = 54 %		35	46	-	dB
Digital TV signal processing							
Digital direct IF							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT2A and pin OUT2B	[7]				
		W4[7] = 0		-	1.0	1.1	V
		W4[7] = 1		-	0.50	0.55	V
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[8]	-	83	-	dB
$G_{IF(cr)}$	control range IF gain		[8]	60	66	-	dB
PSRR	power supply ripple rejection	residual spurious at nominal differential output voltage dependent on power supply ripple	[8]				
		f_{ripple} = 70 Hz		-	60	-	dB
		f_{ripple} = 20 kHz		-	60	-	dB
Digital low IF							
$V_{o(dif)(p-p)}$	peak-to-peak differential output voltage	between pin OUT1A and pin OUT1B; W4[7] = 0	[7]	-	2	-	V
$G_{IF(max)}$	maximum IF gain	output peak-to-peak level to input RMS level ratio	[8]	-	89	-	dB
$G_{IF(cr)}$	control range IF gain		[8]	60	66	-	dB
f_{synth}	synthesizer frequency	see Table 34 and Table 35		-	-	-	MHz

Table 1. Quick reference data *...continued*

V_P = 5 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\varphi_{n(synth)}$	synthesizer phase noise	with 4 MHz crystal oscillator reference; f_{synth} = 31 MHz; f_{IF} = 36 MHz					
		at 1 kHz	[8]	89	99	-	dBc/Hz
		at 10 kHz	[8]	89	99	-	dBc/Hz
		at 100 kHz	[8]	98	102	-	dBc/Hz
		at 1.4 MHz	[8]	115	119	-	dBc/Hz
$\alpha_{ripple(pb)LIF}$	low IF pass-band ripple	6 MHz bandwidth		-	-	2.7	dB
		7 MHz bandwidth		-	-	2.7	dB
		8 MHz bandwidth		-	-	2.7	dB
α_{stpb}	stop-band attenuation	8 MHz band; f = 15.75 MHz		30	40	-	dB
α_{image}	image rejection	−10 MHz to 0 MHz; BP on		30	34	-	dB
C/N	carrier-to-noise ratio	at f_o = 4.9 MHz; $V_{i(IF)}$ = 10 mV (RMS); see Figure 37	[8][9][10]	112	118	-	dBc/Hz
Reference frequency input from external source							
f_{ref}	reference frequency	W7[7] = 0	[11]	-	4	-	MHz
$V_{ref(RMS)}$	RMS reference voltage	W7[7] = 0; see Figure 34 and Figure 46		15	150	500	mV

[1] Values of video and sound parameters can be decreased at V_P = 4.5 V.

[2] AC load; C_L < 20 pF and R_L > 1 kΩ. The sound carrier frequencies (depending on TV standard) are attenuated by the integrated sound carrier traps.

[3] Condition: luminance range (5 steps) from 0 % to 100 %. Measurement value is based on 4 of 5 steps.

[4] The sound carrier trap can be bypassed by setting the I²C-bus bit W2[0] to logic 0; see Table 23. In this way the full composite video spectrum appears at pin CVBS. The video amplitude is reduced to 1.1 V (p-p).

[5] Measurement using 200 kHz high-pass filter, 5 MHz low-pass filter and subcarrier notch filter (*“ITU-T J.64”*).

[6] To match the AFC output signal to different tuning systems a current output is provided. The test circuit is given in Figure 19. The AFC steepness can be changed by resistors R1 and R2.

[7] With single-ended load for f_{IF} < 45 MHz $R_L \geq$ 1 kΩ and $C_L \leq$ 5 pF to ground and for f_{IF} = 45 MHz to 60 MHz R_L = 1 kΩ and $C_L \leq$ 3 pF to ground.

[8] This parameter is not tested during production and is only given as application information.

[9] Noise level is measured without input signal but AGC adjusted corresponding to the given input level.

[10] Set with AGC nominal output voltage as reference. For C/N measurement switch input signal off.

[11] The tolerance of the reference frequency determines the accuracy of VIF AFC, RIF AFC, FM demodulator center frequency, maximum FM deviation, sound trap frequency, LIF band-pass cut-off frequency, as well as the accuracy of the synthesizer.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA9897HL/V3	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA9897HN/V3	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1
TDA9898HL/V3	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA9898HN/V3	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-1

6. Block diagram

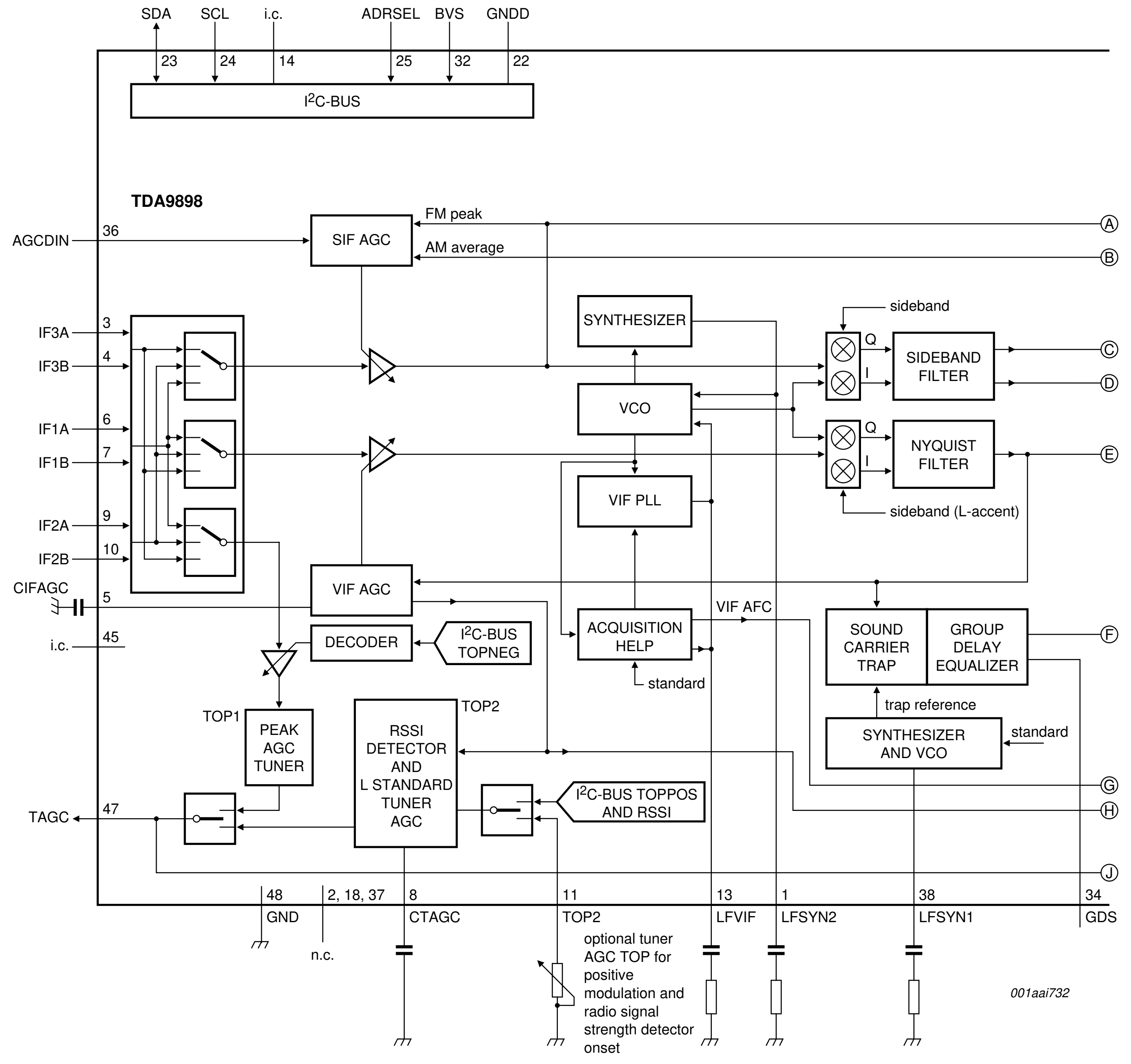
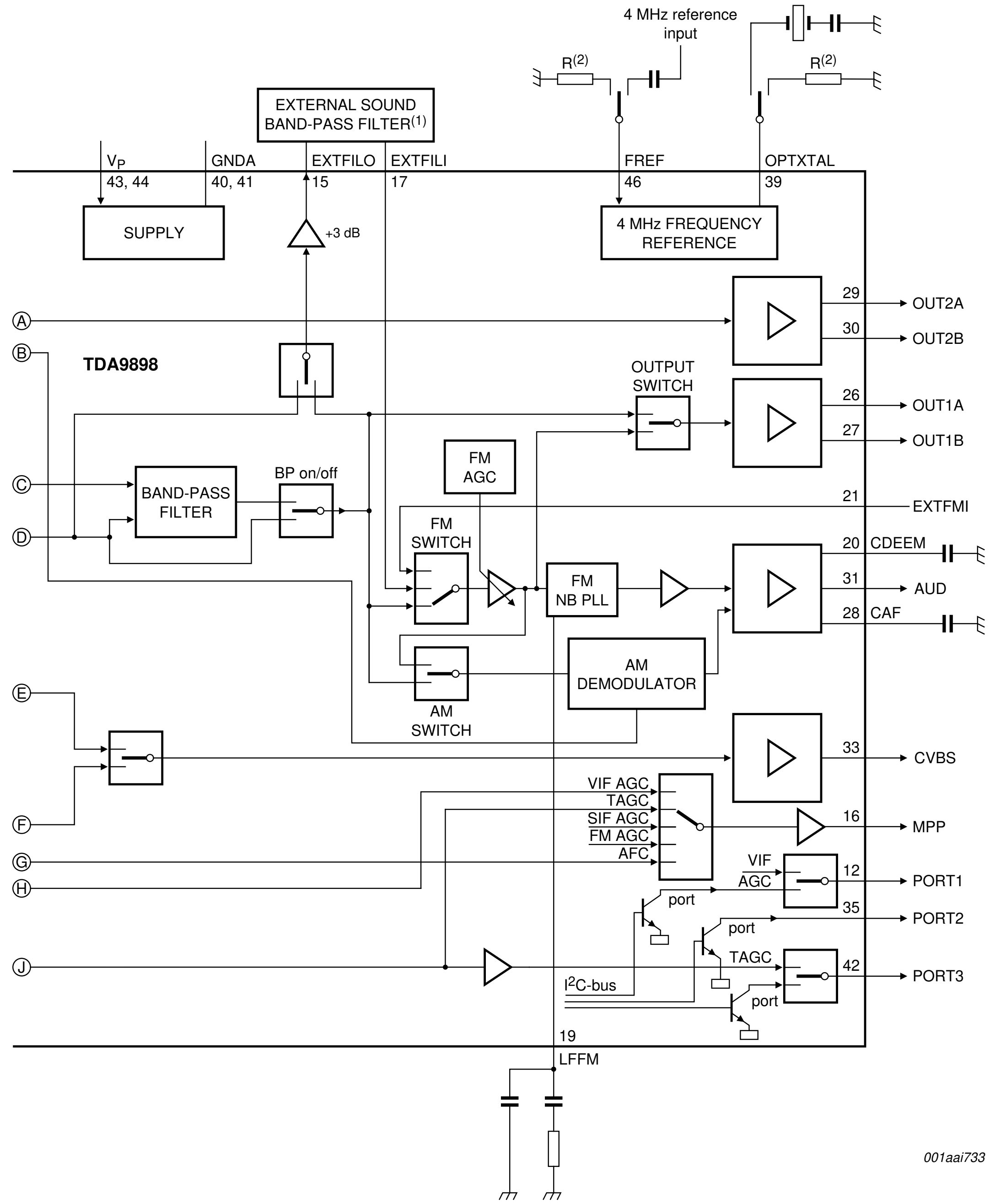


Fig 1. Block diagram of TDA9898 (continued in Figure 2)



(1) Optional.

(2) Connect resistor if input or crystal is not used.

Fig 2. Block diagram of TDA9898 (continued from Figure 1)

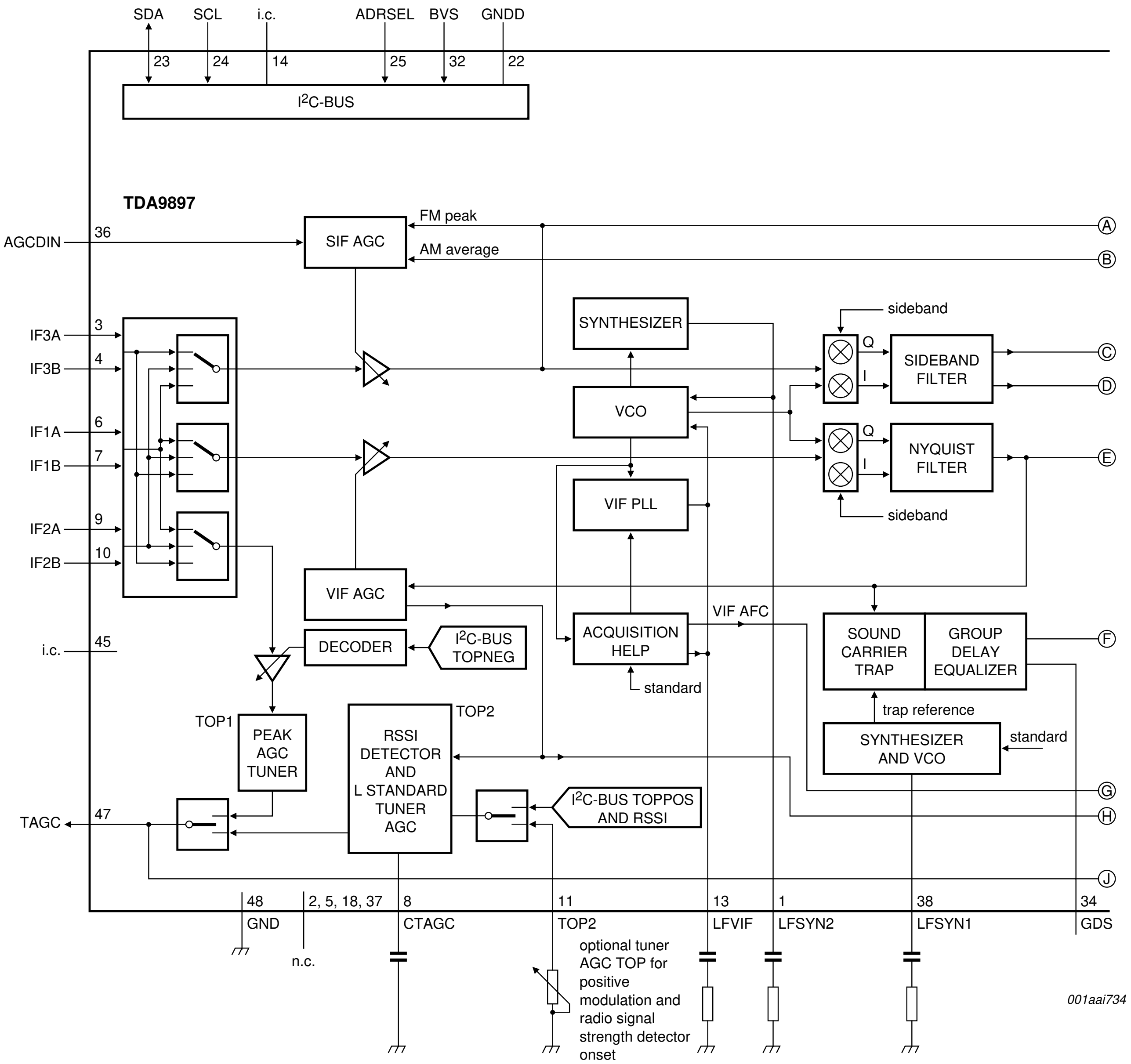
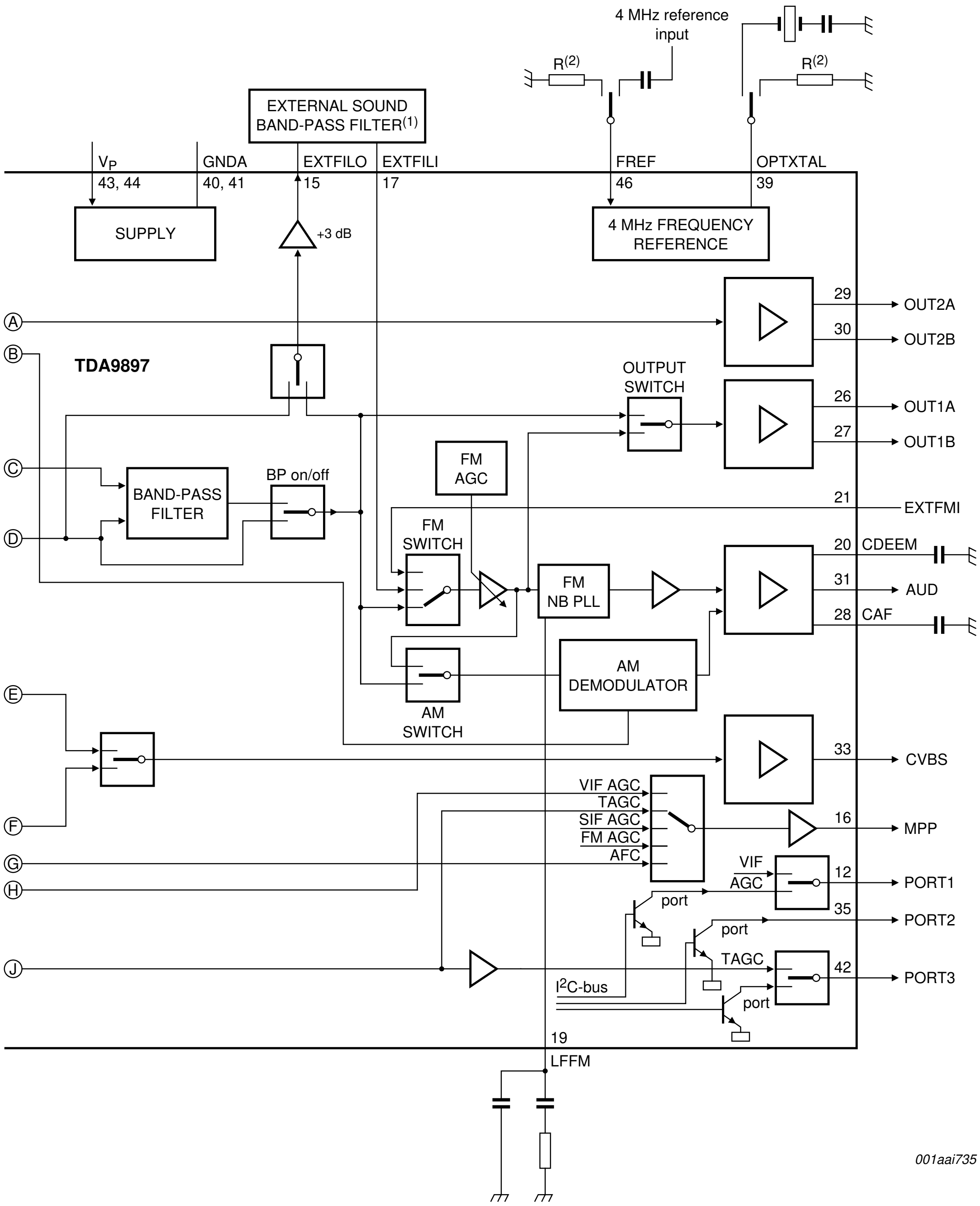


Fig 3. Block diagram of TDA9897 (continued in Figure 4)



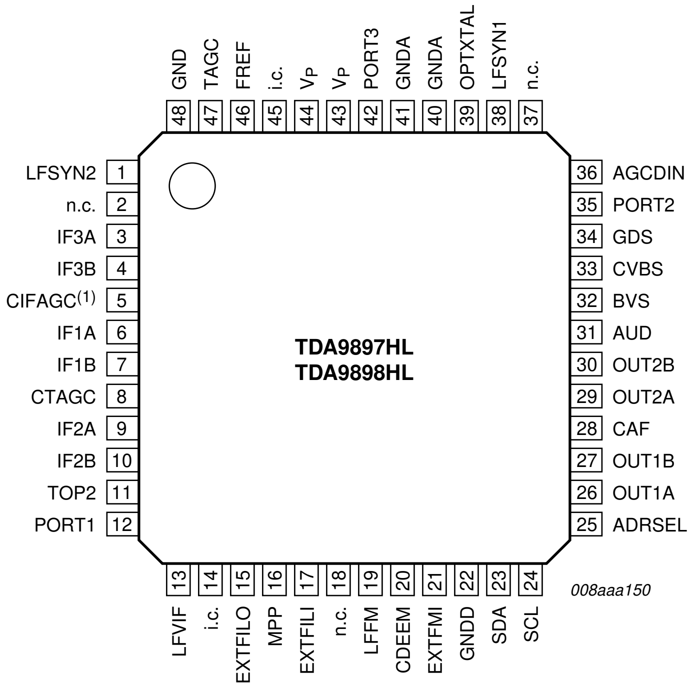
(1) Optional.

(2) Connect resistor if input or crystal is not used.

Fig 4. Block diagram of TDA9897 (continued from Figure 3)

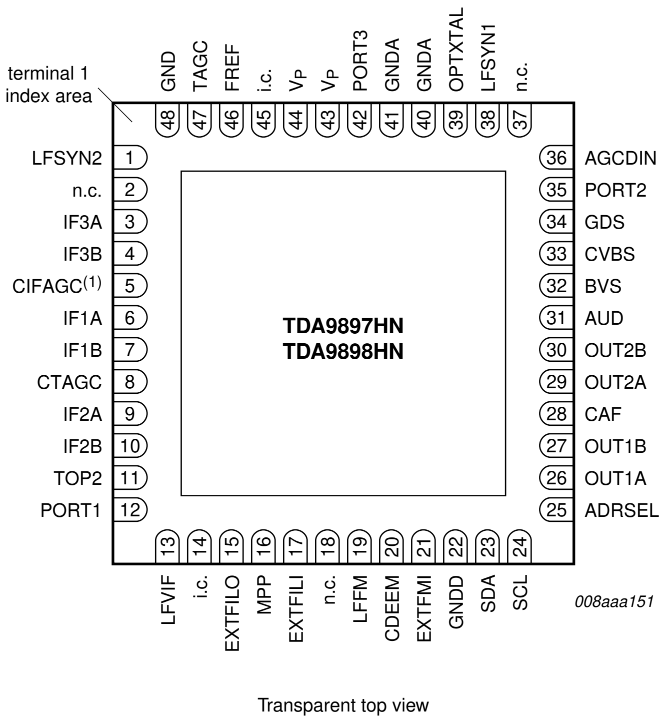
7. Pinning information

7.1 Pinning



(1) Not connected for TDA9897HL.

Fig 5. Pin configuration for LQFP48



(1) Not connected for TDA9897HN.

Fig 6. Pin configuration for HVQFN48

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
LFSYN2	1	loop filter synthesizer 2 (conversion synthesizer)
n.c.	2	not connected
IF3A	3	IF symmetrical input 3 for sound
IF3B	4	
CIFAGC	5	TDA9898: IF AGC capacitor; L standard
		TDA9897: not connected
IF1A	6	IF symmetrical input 1 for vision or digital
IF1B	7	
CTAGC	8	TAGC capacitor
IF2A	9	IF symmetrical input 2 for vision or digital
IF2B	10	
TOP2	11	TOP potentiometer for positive modulated standards and RSSI reference
PORT1	12	digital port function 1 or VIF AGC monitor output
LFVIF	13	loop filter VIF PLL
i.c.	14	internally connected; connect to ground
EXTFILO	15	output to external filter

Table 3. Pin description *…continued*

Symbol	Pin	Description
MPP	16	multipurpose pin: VIF AGC or SIF AGC or FM AGC or TAGC or VIF AFC or FM AFC monitor output
EXTFILI	17	input from external filter
n.c.	18	not connected
LFFM	19	loop filter FM PLL
CDEEM	20	de-emphasis capacitor
EXTFMI	21	external FM input
GNDD	22	digital ground
SDA	23	I^2C-bus data input and output
SCL	24	I^2C-bus clock input
ADRSEL	25	address select
OUT1A	26	low IF or 2nd sound intercarrier symmetrical output
OUT1B	27	
CAF	28	Direct Current (DC) decoupling capacitor
OUT2A	29	1st Digital IF (DIF) symmetrical output
OUT2B	30	
AUD	31	audio signal output
BVS	32	I^2C-bus voltage select
CVBS	33	composite video signal output
GDS	34	additional video group delay select; leave open for default operation[1]
PORT2	35	digital port function 2
AGCDIN	36	AGC input for DIF amplifier for e.g. input from channel decoder AGC
n.c.	37	not connected
LFSYN1	38	loop filter synthesizer 1 (filter control synthesizer)
OPTXTAL	39	optional quartz input
GNDA	40	analog ground
GNDA	41	analog ground
PORT3	42	digital port function 3 or TAGC monitor output
V_P	43	supply voltage
V_P	44	supply voltage
i.c.	45	internally connected; connect to ground
FREF	46	4 MHz reference input
TAGC	47	TAGC output
GND	48	ground; plateau connection

[1] Recommendation: Leave this pin open or use a capacitor to GND, as shown in the application diagrams in Figure 47, Figure 48 and Figure 49.

8. Functional description

8.1 IF input switch

Different signal bandwidth can be handled by using two signal processing chains with individual gain control.

Switch configuration allows independent selection of filter for analog VIF and for analog SIF (used at same time) or DIF.

The switch takes into account correct signal selection for TAGC in the event of VIF and DIF signal processing.

8.2 VIF demodulator

ATV demodulation using 6 MHz DVB window (band-pass) filter (for 6 MHz, 7 MHz or 8 MHz channel width).

IF frequencies adapted to enable the use of different filter configurations. The Nyquist processing is integrated. The integrated Nyquist processing provides also adjacent channel suppression. Sideband switch supplies selection of lower or upper sideband (e.g. for L-accent).

For optional use of standard Nyquist filter the integrated Nyquist processing can be switched off.

Equalizer provides optimum pulse response at different standards [e.g. to cope with higher demands for Liquid Crystal Display (LCD) TV].

Integrated sound traps.

Sound trap reference independent from received 2nd sound IF (reference taken from integrated reference synthesizer).

IF level selection provides an optimum adaptation of the demodulator to high linearity or low noise.

8.3 VIF AGC and tuner AGC

8.3.1 Mode selection of VIF AGC

Peak white AGC for positive modulation mode with adaptation for speed up and black level AGC (using proven system from TDA9886).

For negative modulation mode equal response times for increasing or decreasing input level (optimum for amplitude fading) **or** normal peak AGC **or** ultra fast peak AGC.

8.3.2 VIF AGC monitor

VIF AGC DC voltage monitor output (with expanded internal characteristic).

VIF AGC read out via I^2C-bus (for IF level indication) with zero-calibration via TOP setting (TOP setting either via I^2C-bus or via TOP potentiometer).

8.3.3 Tuner AGC

Independent integral tuner gain control loop (not nested with VIF AGC). Integral characteristic provides high control accuracy.

Accurate setting of tuner control onset (TOP) for integral tuner gain control loop via I^2C-bus.

For L standard, TAGC remains VIF AGC nested, as from field experience in the past this narrowband TAGC gives best performance.

Thus two switchable TAGC systems for negative/DIF and positive modulation implemented.

L standard tuner time constant switching integrated (= speed up function in the event of step into high input levels), to speed up settling time.

For TOP setting at L standard, additional adjustment via optional potentiometer or I^2C-bus is provided.

Tuner AGC status bit provided.

8.4 DIF/SIF FM and AM sound AGC

External AGC control input for DIF. DIF includes direct IF and low IF.

Integrated gain control loop for SIF.

AGC control for FM SIF related to used SAW bandwidth.

Peak AGC control in the event of FM SIF.

Ultra fast SIF AGC time constant when VIF AGC set to ultra fast mode.

Slow average AGC control in the event of AM sound.

AM sound AGC related to AM sound carrier level.

Fast AM sound AGC in the event of fast VIF AGC (speed up).

SIF/FM AGC DC voltage monitor output with expanded internal characteristic.

8.5 Frequency phase-locked loop for VIF

Basic function as previous TDA9887 design.

PLL gating mode for positive and negative modulation, optional.

PLL optimized for either overmodulation or strong multipath.

8.6 DIF/SIF converter stage

Frequency conversion with sideband suppression.

Selection mode of upper or lower sideband for pass or suppression.

Suppression around zero for frequency conversion.

Conversion mode selection via synthesizer for DIF and radio mode or via VIF Frequency Phase-Locked Loop (FPLL) for TV QSS sound (FM/AM).

External BP filter (e.g. for 4.5 MHz) for additional filtering, optional.

Bypass mode selection for use of external filter.

Integrated SIF BP tracking filter for chroma suppression.

Integrated tracking filters for LIF.

Symmetrical output stages for direct IF, LIF and 2nd SIF (intercarrier signal).

Second narrowband gain control loop for 2nd SIF via FM PLL.

8.7 Mono sound demodulator

8.7.1 FM PLL narrowband demodulation

Additional external input for either TV or radio intercarrier signal.

FM carrier selection independent from VIF trap, because VIF trap uses reference via synthesizer.

FM wide and ultra wide mode with adapted loop bandwidth and different selectable FM acquisition window widths to cope with FM overmodulation conditions.

8.7.2 AM sound demodulation

AM sound envelope detector.

L and L-accent standard without SAW switching (done by sideband selection of SIF converter).

8.8 Audio amplifier

Different gain settings for FM sound to adapt to different FM deviation.

Switchable de-emphasis for FM sound.

Automatic mute function when FM PLL is unlocked.

Forced mute function.

Output amplifier for AM sound.

8.9 Synthesizer

The synthesizer supports SIF/DIF frequency conversion. A large set of synthesizer frequencies in steps of 0.5 MHz enables flexible combination of SAW filter and required conversion frequency.

Synthesizer loop internally adapted to divider ratio range for optimum phase noise requirement (loop bandwidth).

Synthesizer reference either via 4 MHz crystal or via an external source. Individual pins for crystal and external reference allows optimum interface definition and supports use of custom reference frequency offset.

8.10 I^{2}C-bus transceiver and slave address

Four different I^{2}C-bus device addresses to enable application with multi-IC use.

I^{2}C-bus transceiver input ports can handle three different I^{2}C-bus voltages.

Read-out functions as TDA9887 plus additional read out of VIF AGC and VIFLOCK, BLCKLEV and TAGC status.

Table 4. Slave address detection

Slave address	Selectable address bit		Pin ADRSEL
	A3	A0	
MAD1	0	1	GND
MAD2	0	0	V_P
MAD3	1	1	resistor to GND
MAD4	1	0	resistor to V_P

9. I^{2}C-bus control

Table 5. Slave addresses

For MAD activation via pin ADRSEL: see Table 4.

Slave address		Bit						
Name	Value	A6	A5	A4	A3	A2	A1	A0
MAD1	43h	1	0	0	0	0	1	1
MAD2	42h	1	0	0	0	0	1	0
MAD3	4Bh	1	0	0	1	0	1	1
MAD4	4Ah	1	0	0	1	0	1	0

9.1 Read format

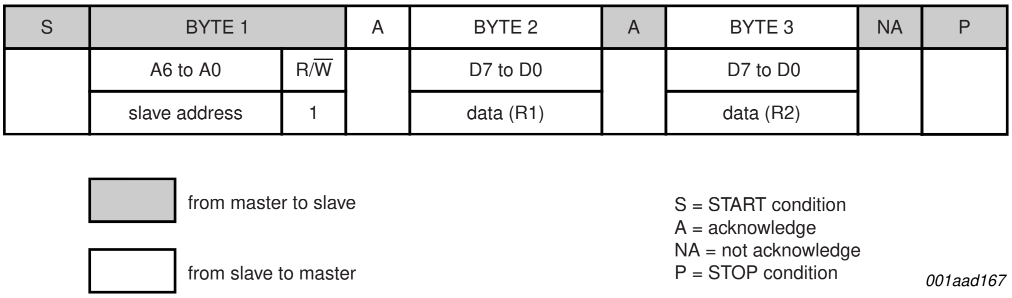


Fig 7. I^{2}C-bus read format (slave transmits data)

Table 6. R1 - data read register 1 bit allocation

7	6	5	4	3	2	1	0
AFCWIN	BLCKLEV	CARRDET	AFC4	AFC3	AFC2	AFC1	PONR

Table 7. R1 - data read register 1 bit description

Bit	Symbol	Description
7	AFCWIN	AFC window[1]
		1 = VCO in ±1.6 MHz AFC window[2]
		1 = VCO in ±0.8 MHz AFC window[3]
		0 = VCO out of ±1.6 MHz AFC window[2]
		0 = VCO out of ±0.8 MHz AFC window[3]
6	BLCKLEV	black level detection
		1 = black level detected
		0 = no black level detected
5	CARRDET	FM carrier detection[4]
		1 = detection (FM PLL is locked and level is less than 6 dB below gain controlled range of FM AGC)
		0 = no detection
4 to 1	AFC[4:1]	automatic frequency control; see Table 8
0	PONR	power-on reset
		1 = after power-on reset or after supply breakdown
		0 = after a successful reading of the status register

[1] If no IF input is applied, then bit AFCWIN can be logic 1 due to the fact that the VCO is forced to the AFC window border for fast lock-in behavior.

[2] All standards except M/N standard.

[3] M/N standard.

[4] Typical time constant of FM carrier detection is 50 ms. The minimal recommended wait time for read out is 80 ms.

Table 8. Automatic frequency control bits

f_{nom} is the nominal frequency.

Bit				f[1]
AFC4	AFC3	AFC2	AFC1	
R1[4]	R1[3]	R1[2]	R1[1]	
0	1	1	1	≤ (f_{nom} − 187.5 kHz)
0	1	1	0	f_{nom} − 162.5 kHz
0	1	0	1	f_{nom} − 137.5 kHz
0	1	0	0	f_{nom} − 112.5 kHz
0	0	1	1	f_{nom} − 87.5 kHz
0	0	1	0	f_{nom} − 62.5 kHz
0	0	0	1	f_{nom} − 37.5 kHz
0	0	0	0	f_{nom} − 12.5 kHz
1	1	1	1	f_{nom} + 12.5 kHz
1	1	1	0	f_{nom} + 37.5 kHz
1	1	0	1	f_{nom} + 62.5 kHz
1	1	0	0	f_{nom} + 87.5 kHz
1	0	1	1	f_{nom} + 112.5 kHz
1	0	1	0	f_{nom} + 137.5 kHz
1	0	0	1	f_{nom} + 162.5 kHz
1	0	0	0	≥ (f_{nom} + 187.5 kHz)

[1] In ATV mode f means vision intermediate frequency; in radio mode f means radio intermediate frequency.

Table 9. R2 - data read register 2 bit allocation

7	6	5	4	3	2	1	0
VIFLOCK	TAGC	VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0

Table 10. R2 - data read register 2 bit description

Bit	Symbol	Description
7	VIFLOCK	VIF PLL lock-in detection
		1 = VIF PLL is locked
		0 = VIF PLL is not locked
6	TAGC	tuner AGC
		1 = active
		0 = inactive
5 to 0	VAGC[5:0]	AGC level detector; VIF AGC in ATV mode, SIF AGC in radio mode and DIF AGC in DTV mode; see Table 11

Table 11. AGC bits

Bit						Typical $\Delta V_{AGC(VIF)}$ (V)
VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0	
R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	
1	1	1	1	1	1	0 (TOP)[1]
1	1	1	1	1	0	−0.04
1	1	1	1	0	1	−0.08
1	1	1	1	0	0	−0.12
1	1	1	0	1	1	−0.16
1	1	1	0	1	0	−0.20
1	1	1	0	0	1	−0.24
1	1	1	0	0	0	−0.28
1	1	0	1	1	1	−0.32
1	1	0	1	1	0	−0.36
1	1	0	1	0	1	−0.40
1	1	0	1	0	0	−0.44
1	1	0	0	1	1	−0.48
1	1	0	0	1	0	−0.52
1	1	0	0	0	1	−0.56
1	1	0	0	0	0	−0.60
1	0	1	1	1	1	−0.64
1	0	1	1	1	0	−0.68
1	0	1	1	0	1	−0.72
1	0	1	1	0	0	−0.76
1	0	1	0	1	1	−0.80
1	0	1	0	1	0	−0.84
1	0	1	0	0	1	−0.88
1	0	1	0	0	0	−0.92
1	0	0	1	1	1	−0.96
1	0	0	1	1	0	−1.00
1	0	0	1	0	1	−1.04
1	0	0	1	0	0	−1.08
1	0	0	0	1	1	−1.12
1	0	0	0	1	0	−1.16
1	0	0	0	0	1	−1.20
1	0	0	0	0	0	−1.24
0	1	1	1	1	1	−1.28
0	1	1	1	1	0	−1.32
0	1	1	1	0	1	−1.36
0	1	1	1	0	0	−1.40
0	1	1	0	1	1	−1.44
0	1	1	0	1	0	−1.48
0	1	1	0	0	1	−1.52

Table 11. AGC bits *…continued*

Bit						Typical $\Delta V_{AGC(VIF)}$ (V)
VAGC5	VAGC4	VAGC3	VAGC2	VAGC1	VAGC0	
R2[5]	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]	
0	1	1	0	0	0	−1.56
0	1	0	1	1	1	−1.60
0	1	0	1	1	0	−1.64
0	1	0	1	0	1	−1.68
0	1	0	1	0	0	−1.72
0	1	0	0	1	1	−1.76
0	1	0	0	1	0	−1.80
0	1	0	0	0	1	−1.84
0	1	0	0	0	0	−1.88
0	0	1	1	1	1	−1.92
0	0	1	1	1	0	−1.96
0	0	1	1	0	1	−2.00
0	0	1	1	0	0	−2.04
0	0	1	0	1	1	−2.08
0	0	1	0	1	0	−2.12
0	0	1	0	0	1	−2.16
0	0	1	0	0	0	−2.20
0	0	0	1	1	1	−2.24
0	0	0	1	1	0	−2.28
0	0	0	1	0	1	−2.32
0	0	0	1	0	0	−2.36
0	0	0	0	1	1	−2.40
0	0	0	0	1	0	−2.44
0	0	0	0	0	1	−2.48
0	0	0	0	0	0	−2.52

[1] The reference of 0 (TOP) can be adjusted via TOPPOS[4:0] (register W10; see Table 47 and Table 45) or via potentiometer at pin TOP2.

9.2 Write format

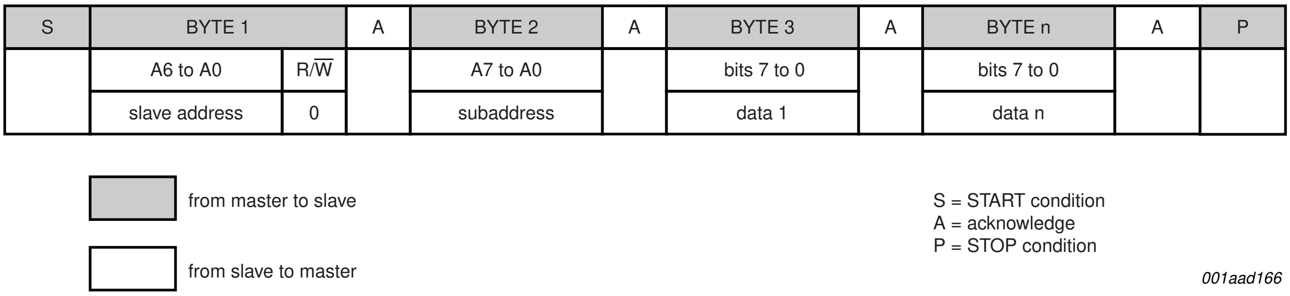


Fig 8. I²C-bus write format (slave receives data)

9.2.1 Subaddress

Table 12. W0 - subaddress register bit allocation

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Table 13. W0 - subaddress register bit description

Bit	Symbol	Description
7 to 4	A[7:4]	has to be set to logic 0
3 to 0	A[3:0]	subaddress; see Table 14

Table 14. Subaddress control bits

Bit				Mode
A3	A2	A1	A0	
0	0	0	0	subaddress for register W1
0	0	0	1	subaddress for register W2
0	0	1	0	subaddress for register W3
0	0	1	1	subaddress for register W4
0	1	0	0	subaddress for register W5
0	1	0	1	subaddress for register W6
0	1	1	0	subaddress for register W7
0	1	1	1	subaddress for register W8
1	0	0	0	subaddress for register W9
1	0	0	1	subaddress for register W10
1	0	1	0	subaddress for register W11

Table 15. I²C-bus write register overview

The register setting after power-on is not specified.

Register	7	6	5	4	3	2	1	0
W1[1]	RADIO	STD1	STD0	TV	0	0	FM	EXTFIL
W2[2]	MOD	STD4	STD3	STD2	SB	PLL	GATE	TRAP
W3[3]	RESCAR	AMUTE	FMUTE	FMWIDE0	DEEMT	DEEM	AGAIN1	AGAIN0
W4[4]	VIFLEVEL	BP	MPPS1	MPPS0	AMMODE	IFIN1	IFIN0	VIFIN
W5[5]	FSFREQ1	FSFREQ0	SFREQ5	SFREQ4	SFREQ3	SFREQ2	SFREQ1	SFREQ0
W6[6]	TAGC1	TAGC0	AGC2	AGC1	FMWIDE1	TWOFLO	VIDEO1V7	DIRECT
W7[7]	EXTFILO	VAGC	SIFLEVEL	VIDLEVEL	PORT1	MODEP1	FILOUTBP	NYQOFF
W8[8]	FEATURE	AVIDRED	MODEP3	TAGCIN3	FORCESP	PORT3	PORT2	0
W9[9]	DAGCSLOPE	TAGCIS	TAGCTC	TOPNEG4	TOPNEG3	TOPNEG2	TOPNEG1	TOPNEG0
W10[10]	0	READTAGC	XPOTPOS	TOPPOS4	TOPPOS3	TOPPOS2	TOPPOS1	TOPPOS0
W11[11]	0	0	OFFSETN	OFFSETP	BLACKAGC	GDEQ	VIFIN3	VIF31875

[1] See Table 17 for detailed description of W1.
[2] See Table 23 for detailed description of W2.
[3] See Table 27 for detailed description of W3.
[4] See Table 29 for detailed description of W4.
[5] See Table 33 for detailed description of W5.
[6] See Table 37 for detailed description of W6.
[7] See Table 40 for detailed description of W7.
[8] See Table 42 for detailed description of W8.
[9] See Table 44 for detailed description of W9.
[10] See Table 47 for detailed description of W10.
[11] See Table 50 for detailed description of W11.

9.2.2 Description of data bytes

Table 16. W1 - data write register bit allocation

7	6	5	4	3	2	1	0
RADIO	STD1	STD0	TV	0	0	FM	EXTFIL

Table 17. W1 - data write register bit description

Bit	Symbol	Description
7	RADIO	FM mode
		1 = radio
		0 = ATV/DTV
6 and 5	STD[1:0]	2nd sound IF; see Table 18 and Table 19
4	TV	TV mode
		1 = ATV QSS
		0 = DTV; direct IF or LIF; depends on setting of TV mode (W6[0])
3 and 2	-	0 = fixed value
1 and 0	FM and EXTFIL	FM and output switching; see Table 21

Table 18. Intercarrier sound BP and FM PLL frequency select for ATV, QSS mode

For description of bit MOD refer to Table 23 and bits FSFREQ[1:0] are described in Table 33.

Bit						f_{FMPLL} (MHz)	Sound BP
RADIO	MOD	STD1	STD0	FSFREQ1	FSFREQ0		
W1[7]	W2[7]	W1[6]	W1[5]	W5[7]	W5[6]		
0	1	0	0	X	X	4.5	M/N standard
0	1	0	1	X	X	5.5	B/G standard
0	1	1	0	X	X	6.0	I standard
0	1	1	1	X	X	6.5	D/K standard
0	0	1	1	X	X	off	L/L-accent standard

Table 19. Intercarrier sound BP and FM PLL frequency select for radio

For description of bit MOD refer to Table 23 and bits FSFREQ[1:0] are described in Table 33.

Bit						f_{FMPLL} (MHz)	Sound BP
RADIO	MOD	STD1	STD0	FSFREQ1	FSFREQ0		
W1[7]	W2[7]	W1[6]	W1[5]	W5[7]	W5[6]		
1	1	X	X	0	0	4.5	M/N standard
1	1	X	X	0	1	5.5	B/G standard
1	1	X	X	1	0	6.0	I standard
1	1	X	X	1	1	6.5	D/K standard

Table 20. Intercarrier sound FM PLL frequency select for radio 10.7 MHz

For description of bit MOD refer to Table 23 and for BP refer to Table 29.

Bit			f_{FMPLL} (MHz)
BP	MOD	RADIO	
W4[6]	W2[7]	W1[7]	
0	0	1	10.7