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TDA9955HL

Triple 8-bit analog-to-digital video converter for HDTV

Rev. 01 — 17 March 2008 Product data sheet

1. General description

The TDA9955HL is a triple 8-bit video converter interface.

The TDA9955HL converts an RGB analog signal into a RGB or YUV (YC_BC_R) digital signal or converts a YUV (YP_BP_R) analog signal into a YUV (YC_BC_R) or RGB digital signal with a sampling rate up to 170 MHz.

The TDA9955HL supports analog TV resolutions from 480i (720 × 480i at 60 Hz) to High-Definition TV (HDTV) (up to 1 920 × 1 080p at 60 Hz) and analog PC resolutions from VGA (640 × 480p at 60 Hz) to UXGA (1600 × 1200p at 60 Hz).

The YUV digital output signal can be 4 : 4 : 4 or 4 : 2 : 2 ITU-R BT.656 standard or semi-planar format following the ITU-R BT.601 standard.

All settings are controlled via the I^2C-bus.

2. Features

- Triple 8-bit Analog-to-Digital Converter (ADC)
- Three independent analog video sources, up to 170 MHz selectable via the I^2C-bus
- Analog composite sync slicer and recognition integrated
- Frame and field detection for interlaced video signal
- Video analog voltage input from 0.45 V to 0.9 V (p-p) to produce a full-scale ADC input of 1.0 V (p-p)
- Three clamps for programming a 8-bit clamping code from 0 to +191 in steps of 1 LSB for RGB and YUV signals
- Three video amplifiers controlled via I^2C-bus to reach the full-scale resolution
- Amplifier bandwidth of 100 MHz
- Low gain variation with temperature
- I^2C-bus controlled Phase-Locked Loop (PLL) to generate the ADCs, formatter and output clocks which can be locked into a line frequency from 15 kHz to 95 kHz
- Integrated PLL divider
- Programmable clock phase adjustment cells
- Matrix and offsets available for conversion of RGB or YUV signal coming from analog video sources into YUV or RGB
- Output format RGB 4 : 4 : 4, YUV 4 : 4 : 4, YUV 4 : 2 : 2 ITU-R BT.656 or YUV 4 : 2 : 2 semi-planar standard on output bus
- Integrated downsampling-by-two with selectable filters on C_B and C_R channels in the 4 : 2 : 2 mode
- IC controlled via the I^2C-bus, 5 V tolerant and bit rate up to 400 kbit/s

- TTL inputs 5 V tolerant
- LV-TTL outputs
- Power-down mode
- 1.8 V and 3.3 V power supplies

3. Applications

- Set Top Box (STB)
- YUV or RGB high-speed video digitizer
- Projector, plasma and LCD TV
- Rear projection TV
- High-end TV

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TDA9955HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5. Block diagram

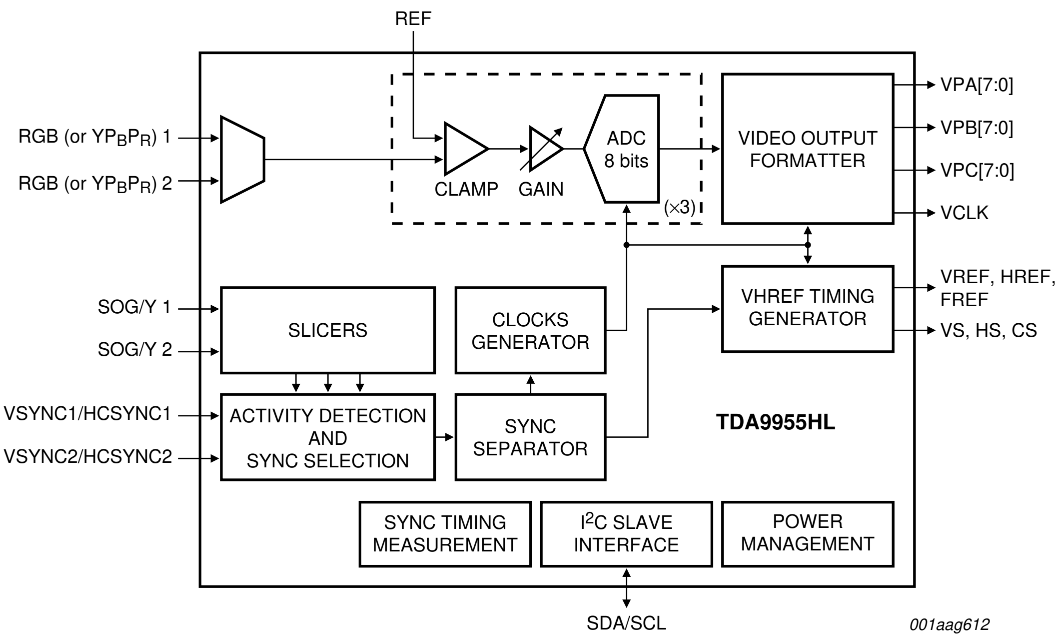

Fig 1. Block diagram

6. Functional diagram

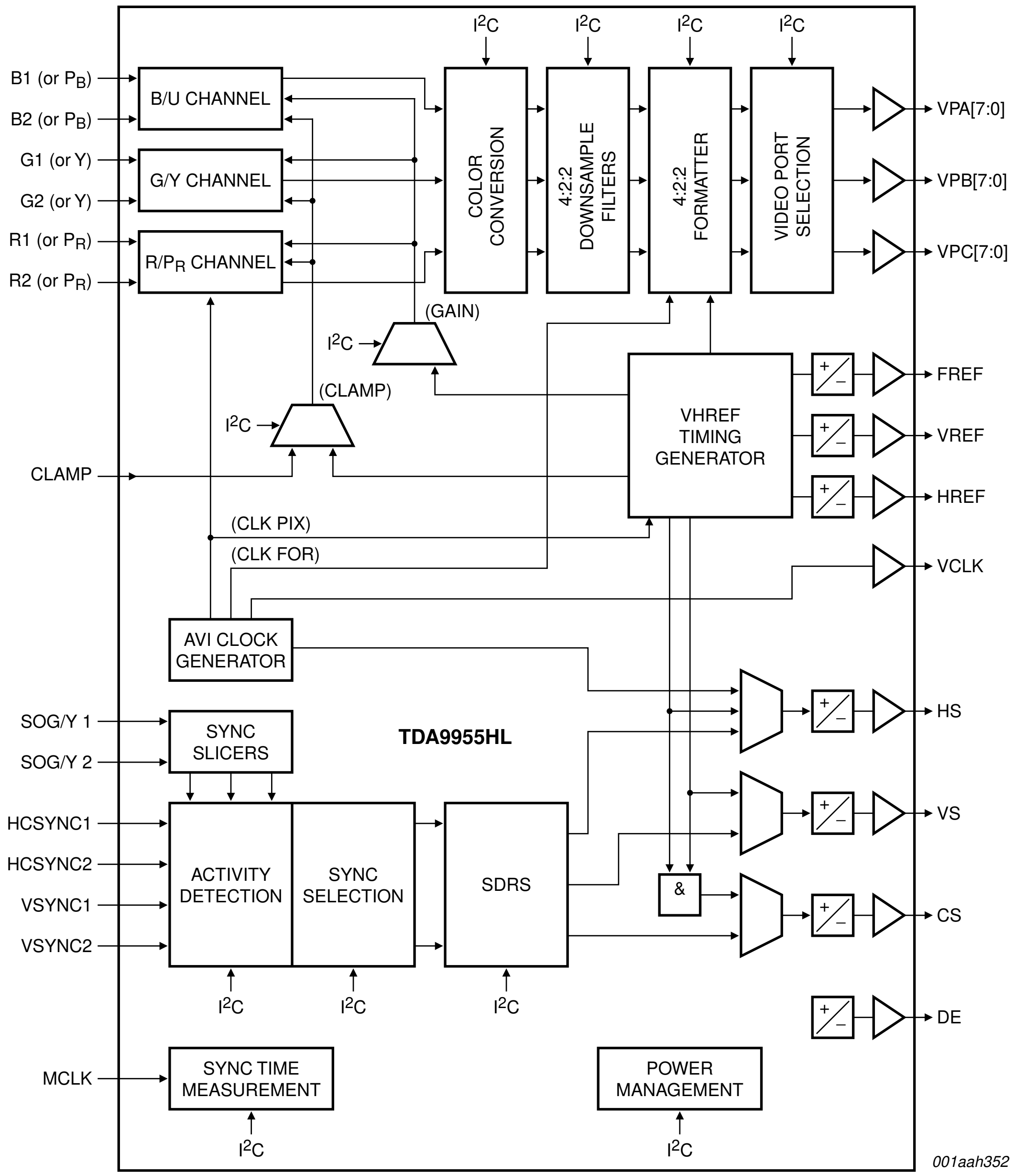

Fig 2. Functional diagram

7. Pinning information

7.1 Pinning

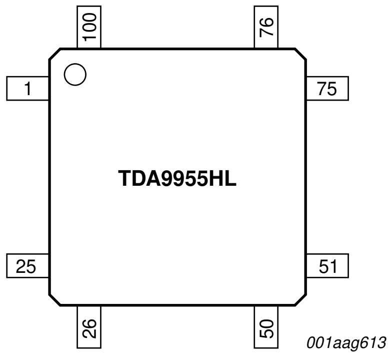

Fig 3. Pin configuration

7.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
VPC1	1	O	video port C output bit 1
VPC2	2	O	video port C output bit 2
VPC3	3	O	video port C output bit 3
$V_{DDC(1V8)}$	4	P	supply voltage for the digital core (1.8 V)
V_{SSC}	5	G	ground for the digital core
$V_{DDO(3V3)}$	6	P	supply voltage for the video port output (3.3 V)
V_{SSO}	7	G	ground for the video port output
VPC4	8	O	video port C output bit 4
VPC5	9	O	video port C output bit 5
VPC6	10	O	video port C output bit 6
VPC7	11	O	video port C output bit 7
$V_{DDO(3V3)}$	12	P	supply voltage for the video port output (3.3 V)
V_{SSO}	13	G	ground for the video port output
VCLK	14	O	pixel clock output
FREF/CS	15	O	filed reference output or composite synchronization
VREF/VS	16	O	vertical reference output or vertical synchronization
HREF/HS	17	O	horizontal reference output or horizontal synchronization
DE	18	O	data enable signal output
VAI_N	19	O	video activity indication output (active LOW)
$V_{DDA(OSC)(3V3)}$	20	P	analog supply for the free running oscillator (3.3 V)
$V_{SSA(OSC)}$	21	G	analog ground for the free running oscillator
$V_{DDA(BIAS)(3V3)}$	22	P	bias analog supply voltage (3.3 V)
$V_{SSA(BIAS)}$	23	G	bias analog ground

Table 2. Pin description *...continued*

Symbol	Pin	Type[1]	Description
BIAS	24	I	bias input
V_{SSA}	25	G	PCB ground
$V_{SSA(B)}$	26	G	analog ground for the blue (or blue chrominance) channel
$V_{DDA(B)(3V3)}$	27	P	analog supply voltage for blue (or blue chrominance) channel (3.3 V)
B2	28	I	blue channel input 2
REF_B	29	I	blue channel reference input
B1	30	I	blue channel input 1
$V_{DDA(B)(1V8)}$	31	P	analog supply voltage for blue (or blue chrominance) channel ADC (1.8 V)
$V_{SSA(B)}$	32	G	analog ground for blue (or blue chrominance) channel ADC
$V_{SSA(G)}$	33	G	analog ground for green (or green luminance) channel
$V_{DDA(G)(3V3)}$	34	P	analog supply voltage for green (or green luminance) channel (3.3 V)
G2	35	I	green channel input 2
REF_G	36	I	green channel reference input
G1	37	I	green channel input 1
$V_{DDA(G)(1V8)}$	38	P	analog supply voltage for green (or green luminance) channel ADC (1.8 V)
$V_{SSA(G)}$	39	G	analog ground for green (or green luminance) channel ADC
$V_{SSA(R)}$	40	G	analog ground for red (or red chrominance) channel
$V_{DDA(R)(3V3)}$	41	P	analog supply voltage for red (or red chrominance) channel (3.3 V)
R2	42	I	red channel input 2
REF_R	43	I	red channel reference input
R1	44	I	red channel input 1
$V_{DDA(R)(1V8)}$	45	P	analog supply voltage for red (or red chrominance) channel ADC (1.8 V)
$V_{SSA(R)}$	46	G	analog ground for red (or red chrominance) channel ADC
SOG2	47	I	Sync-On-Green (SOG) input 2
SOG1	48	I	sync-on-green input 1
$V_{DDA(SOG)(3V3)}$	49	P	analog supply voltage for SOG (3.3 V)
$V_{SSA(SOG)}$	50	G	analog ground for SOG
$V_{DDA(SOG)(3V3)}$	51	P	analog supply voltage for SOG (3.3 V)
$V_{SSA(SOG)}$	52	G	analog ground for SOG
$V_{SSA(PLL)}$	53	G	analog ground for PLL
$V_{SSA(PLL)}$	54	G	analog ground for PLL
$V_{DDA(PLL)(3V3)}$	55	P	analog supply voltage for PLL (3.3 V)
$V_{DDA(PLL)(1V8)}$	56	P	analog supply voltage for PLL (1.8 V)
TEST0	57	I	reserved for test (connected to the digital ground of the core)
TEST1	58	I	reserved for test (connected to the digital ground of the core)
HCSYNC1	59	I	horizontal (composite) SYNC input 1
HCSYNC2	60	I	horizontal (composite) SYNC input 2

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
VSYNC1	61	I	vertical SYNC input 1
VSYNC2	62	I	vertical SYNC input 2
MCLK	63	I	synchronization timing measurement clock
CLAMP	64	I	clamp input (external mode)
COAST	65	I	coast (PLL) input (external mode)
CKEXT	66	I	external clock input (external mode)
A0	67	I	I^2C-bus address select bit 0
$V_{DDI(3V3)}$	68	P	digital supply for the input (3.3 V)
SCL	69	I	I^2C-bus clock
SDA	70	I	I^2C-bus data
V_{SSA}	71	G	analog ground
$V_{DDC(1V8)}$	72	P	digital supply for core (1.8 V)
V_{SSC}	73	G	digital ground of the core (1.8 V)
$V_{DDO(3V3)}$	74	P	supply voltage for the video port output (3.3 V)
V_{SSO}	75	G	ground for video port output
VPA0	76	O	video port A output bit 0
VPA1	77	O	video port A output bit 1
VPA2	78	O	video port A output bit 2
VPA3	79	O	video port A output bit 3
$V_{DDO(3V3)}$	80	P	supply voltage for the video port output (3.3 V)
V_{SSO}	81	G	ground for video port output
VPA4	82	O	video port A output bit 4
VPA5	83	O	video port A output bit 5
VPA6	84	O	video port A output bit 6
VPA7	85	O	video port A output bit 7
$V_{DDO(3V3)}$	86	P	supply voltage for the video port output (3.3 V)
V_{SSO}	87	G	ground for video port output
VPB0	88	O	video port output bit 0
VPB1	89	O	video port output bit 1
VPB2	90	O	video port output bit 2
VPB3	91	O	video port output bit 3
$V_{DDO(3V3)}$	92	P	supply voltage for the video port output (3.3 V)
V_{SSO}	93	G	ground for video port output
VPB4	94	O	video port output bit 4
VPB5	95	O	video port output bit 5
VPB6	96	O	video port output bit 6
VPB7	97	O	video port output bit 7
$V_{DDO(3V3)}$	98	P	supply voltage for the video port output (3.3 V)
V_{SSO}	99	G	ground for video port output
VPC0	100	O	video port C output bit 0

[1] P = power supply; G = ground; I = input and O = output.

8. Functional description

This high-rate front end is designed to convert analog signals coming from an analog source (RGB or YUV) into parallel digital data used by media processor ICs such as the NXP Semiconductors Nexperia devices for HDTV or by other video signal ICs. The high-rate front end is able to output RGB 4 : 4 : 4, YUV 4 : 4 : 4, YUV 4 : 2 : 2 semi-planar and YUV 4 : 2 : 2 ITU-R BT.656 formats and accepts progressive and interlaced input formats. The high-rate front end also contains a RGB-to-YUV and YUV-to-RGB conversion matrix, downsampling filters and range control function.

8.1 Analog multiplexers

The choice between the two analog video inputs is either automatic (activity detection) or controlled by the I^2C-bus. An analog video input is defined by pins SOGx, Rx, Bx, Gx, HCSYNCx and VSYNCx (where x equals 1 or 2).

8.2 R/P_R, B/P_B and G/Y channels

8.2.1 Clamps

Three independent parallel clamping circuits are used to clamp the video input signals on programmable black/blanking levels. The clamp level of each channel can be changed from 0 to 191 in steps of 1 LSB. The clamp signal comes from the VHREF timing generator or from the CLAMP pin.

The clamping circuits can be inhibited during the vertical sync pulse and also during false black/blanking level in the end of active video signal in a frame/field.

8.2.2 ADCs

Three ADCs convert analog signals into three series of 8-bit codes, with a maximum sampling frequency of 170 MHz. The ADCs input range is 1 V (p-p).

During the gain calibration pulse period, the ADCs are used to calibrate the video amplifiers and during the clamp active period the ADCs are used to set the clamp level to the desired values.

8.2.3 Automatic Gain Control (AGC)

Gain registers, one per channel, control directly the gain of each video amplifier. The programming of these registers is done by I^2C-bus and their content is validated only on the next horizontal synchronization pulse. These contrast registers are programmable from 0 dB to 5 dB (gain registers on 11 bits).

The gain calibration control signal comes from the VHREF timing generator.

8.3 Sync slicing

Two sync slicers extract the composite sync from the green, luminance or CVBS signal through SOGx pins. This synchronization signal can be bi-level or tri-level.

8.4 Activity detection

The device detects the presence of signals on each sync input VSYNCx, HCSYNCx and SOGx after slicing to indicate which kind of synchronization is present (where x equals 1 or 2):

- Digital separated syncs on VSYNCx and HCSYNCx
- Analog composite sync on SOGx

A change of activity is notified by a HIGH-to-LOW transition on the VAI_N output pin.

8.5 Sync detection and selection

The management of the synchronization is done by using vertical sync, horizontal sync and analog composite sync on the green/luminance signal.

The device scans if a signal is present on the VSYNCx pin. If a signal is detected on this pin, it means that there is a digital separated sync signal.

If no signal is detected on the HCSYNCx pin, the device scans if a signal is present on the SOGx pin. If a signal is detected on this pin (and not on the HCSYNCx pin), it means that there is an analog composite sync signal and the signal is sent into the sync recognition function after slicing.

If the analog composite sync signal is on the green or on the luminance of the video signal, the SOGx pin must be connected to this signal.

8.6 Sync Detection Recognition and Separation

The Sync Detection Recognition and Separation (SDRS) allows to retrieve the horizontal and the vertical synchronizations from composite sync. This composite sync comes from the sync slicing function when the sync is on the green, luminance or CVBS signal or from the digital composite sync on the HCSYNCx pin.

This function is able to eliminate any additional synchronization pulses which may be added in the vertical blanking.

8.7 Clock generator

An internal PLL locked to the reference HSYNC signal from sync recognition provides three different clocks, one pixel-clock for R/P_R, B/P_B and G/Y channels sampling and for the VHREF timing generator, one formatter-clock at double frequency for the 4 : 2 : 2 formatter and one output-clock for the VCLK output pin.

The COAST signal, coming from SDRS and/or VHREF timing generator or coming from the COAST input pin, allows to freeze the PLL phase frequency detector during the vertical blanking.

A phase-locked flag indicates if the PLL is locked.

8.8 Sync multiplexers

The sync multiplexer allow to select via the I^2C-bus the origin of the synchronization pulses signals HS, VS, CS and DE.

The origin of those pulses can be the VHREF timing generator or the SDRS block.

8.9 Color conversion

The color conversion allows an RGB signal coming from the analog video interface to convert into YUV format or to convert a YUV signal coming from the analog video interface into an RGB format. The color matrix formula is:

$$\begin{bmatrix} YG \\ VR \\ UB \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} GY \\ RV \\ BU \end{bmatrix} - \begin{bmatrix} Oin_1 \\ Oin_2 \\ Oin_3 \end{bmatrix} \right) + \begin{bmatrix} Oout_1 \\ Oout_2 \\ Oout_3 \end{bmatrix}$$

Activation of the matrix function and programming of all coefficients is made by I^2C-bus.

8.10 4 : 2 : 2 downsample filters

These filters downsample the U and V signals with a factor 2.

A delay is added on the G/Y channel corresponding to the pipeline delay of the filters to put the Y channel in phase with the UV channel.

Four filters are selectable by I^2C-bus, from the simple cut to the ITU-R BT.656 compliant digital filter.

8.11 Range control

The range control function truncates the range of data at specified ceiling and floor values to remove super-white and super-black pixels.

8.12 4 : 2 : 2 formatter

The 4 : 2 : 2 formatter contains the YUV 4 : 2 : 2 semi-planar and the YUV 4 : 2 : 2 ITU-R BT.656 formatting functions. The choice between these functions is done using the I^2C-bus. A delay is added on the G/Y channel corresponding to the pipeline delay of the YUV 4 : 2 : 2 semi-planar formatting function to put the Y channel in phase with the UV channel.

In the case of the YUV 4 : 2 : 2, the data frequency corresponding to the Y signal is at pixel clock frequency and the data frequency corresponding to the U and V signals is at half the pixel clock frequency. For semi-planar, the output clock should be at the same frequency as the pixel clock and for ITU-R BT.656 at the same frequency as the formatter clock (double of the pixel-clock).

The Start Active Video (SAV) and End Active Video (EAV) timing reference codes can be included in the data stream according the HREF, VREF and FREF signal positions from the VHREF timing generator.

Specific codes programmed via the I^2C-bus can replace the data stream during the blanking period to mask gain and clamp calibration.

8.13 Video port selection

Each channel (R or G or B in RGB 4 : 4 : 4 mode, Y or C_B or C_R in YUV 4 : 4 : 4 mode, Y or C_BC_R in 4 : 2 : 2 semi-planar mode, C_BYC_RY in 4 : 2 : 2 ITU-R BT.656 mode) can be affected to a specified video port VPA, VPB or VPC via the I^2C-bus.

8.14 Output buffers

The levels of the output buffers are LV-TTL compatible. The switch of the outputs between active and high-impedance is set by the I^2C-bus.

8.15 VHREF timing generator

The VHREF timing generator outputs all the timing signals used by the device: gain and clamp pulses for calibration, coast signal to manage the PLL, VREF, HREF and FREF signals for SAV/EAV and other, VS and HS signals to change width and position compared with the synchronization inputs.

8.16 I^2C-bus serial interface

The I^2C-bus serial interface allows to program the internal registers of the device. The slave address of the device is selected by pin A0. The programmed values in the registers remain valid.

8.17 Power management

Only the serial interface (and the I^2C-bus registers) and the activity detection are powered up in all cases even in the case when the device is set to power-down with the PD-registers.

8.18 Sync timing measurement

To assist the recognition of the input format, the vertical and horizontal periods are measured based on the externally provided MCLK frequency (13.5 MHz). The width of the horizontal pulse is also measured.

9. I^2C-bus interface

9.1 I^2C-bus protocol

The TDA9955HL is a slave I^2C-bus device and the SCL pin is only an input pin. The timing and protocol for I^2C-bus are standard.

Bit A0 of the I^2C-bus device address is externally selected by the A0 pin. The main device I^2C-bus address is given in Table 3.

Table 3. I^2C-bus slave address

Device address							$R/\overline{W}$
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**-**
1	0	0	1	1	1	A0	0/1

9.2 Registers definitions

The configuration of the registers is given in Table 4.

Table 4. I²C-bus registers; (R): reading register[1]

Register	Sub addr	R/W	Bit definition 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Default value
VERSION	00h	R	0	0	0	1	0	1	0	0	0001 0100
INPUT_SEL	01h	W	x	x	x	x	x	x	VINS[1:0]		0000 0100
Reserved for test	02h	W	-	-	x	x	x	-	x	x	0000 0000
Reserved for test	03h	W	x	x	x	x	x	x	x	x	0110 0000
SDRS_CTRL1	04h	W	x	ASD_DIS	SOGF	DCSF	x	x	x	x	0000 0000
Reserved for test	05h	W	x	x	x	x	x	x	x	x	0000 0010
Reserved for test	06h	W	x	x	x	x	x	x	x	x	0001 0100
Reserved for test	07h	W	x	x	x	x	x	x	x	x	0001 0000
Reserved for test	08h	W	x	x	x	x	x	x	x	x	0000 0000
Reserved for test	09h	W	x	x	x	x	x	x	x	x	0111 1111
Reserved for test	0Ah	W	x	x	x	x	x	x	x	x	0010 0101
Reserved for test	0Bh	R	-	-	-	x	x	x	x	x	0000 0000
Reserved for test	0Ch	R	x	x	x	x	x	x	x	x	0000 0000
SDRS_FLAGS	0Dh	R	ASD	SOGD2	-	DSSD2	-	SOGD1	-	DSSD1	0000 0000
PLL_CTRL	10h	W	x	-	-	-	EDG	x	x	x	0000 0000
PLL_MNDIV_MSB	11h	W	MDIV[1:0]		-	-	NDIV[11:8]				1100 0011
PLL_NDIV_LSB	12h	W	NDIV[7:0]								0110 0000
LOCK_FLAG	13h	R	-	-	-	-	-	-	x	PLL_LOCK	0000 0000
DLL_PHASE	14h	W	-	-	-	PHASE[4:0]					0001 0000
PIXCLKGEN_PRST	15h	W	CLKOUT_PRST[2:0]			CLKFOR_PRST[1:0]		CLKPIX_PRST[2:0]			1101 0111
PIXCLKGEN_CTRL0	16h	W	CLKOUT_DIV[1:0]		CLKFOR_DIV[1:0]		CLKPIX_DIV[1:0]		PR_DEL	PH_CORR	0011 1011
PIXCLKGEN_CTRL1	17h	W	CLKOUT_TOG	CLKOUT_SEL[2:0]			CLKFOR_SEL[1:0]		x	x	0100 0110
BRIGHT_GY	1Ah	W	BRIGHT_GY[7:0]								0001 0000
BRIGHT_BU	1Bh	W	BRIGHT_BU[7:0]								1000 0000
BRIGHT_RV	1Ch	W	BRIGHT_RV[7:0]								1000 0000
Reserved for test	1Dh	W	x	x	x	x	x	x	x	x	0000 0000
Reserved for test	1Eh	W	-	-	-	-	-	x	x	x	0000 0000

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
COARSE_GAINRV	20h	W	-	-	-	-	COARSE_RV[3:0]				0000 0100
FINE_GAINRV	21h	W	-	FINE_RV[6:0]							0101 1100
AGC_HIGHRV	22h	W	HIGH_RV[7:0]								1111 0000
AGC_LOWRV	23h	W	x	LOW_RV[6:0]							1001 0000
COARSE_GAINBU	2Ah	W	-	-	-	-	COARSE_BU[3:0]				0000 0100
FINE_GAINBU	2Bh	W	-	FINE_BU[6:0]							0101 1100
AGC_HIGHBU	2Ch	W	HIGH_BU[7:0]								1111 0000
AGC_LOWBU	2Dh	W	x	LOW_BU[6:0]							1001 0000
AGC_CONTGY	34h	W	-	-	-	-	COARSE_GY[3:0]				0000 0100
AGC_OFFSETGY	35h	W	-	FINE_GY[6:0]							0101 1100
AGC_HIGHGY	36h	W	HIGH_GY[7:0]								1110 1011
AGC_LOWGY	37h	W	x	LOW_GY[6:0]							1001 0000
V_PER_MSB	40h	R	V_PER[19:12]								0000 0000
V_PER_ISB	41h	R	V_PER[11:4]								0000 0000
H_PER_MSB	42h	R	H_PER[9:2]								0000 0000
HS_WIDTH_MSB	43h	R	HS_WIDTH[9:2]								0000 0000
STM_LSB	44h	R	V_PER[3:0]				H_PER[1:0]		HS_WIDTH[1:0]		0000 0000
MAT_CTRL	80h	W	-	-	-	-	-	-	MAT_SC[1:0]		0000 0010
MAT_OI1_MSB	81h	W	-	-	-	-	-	MAT_OI1[8:6]			0000 0000
MAT_OI1_LSB	82h	W	OFFSET_IN1[5:0]						-	-	0000 0000
MAT_OI2_MSB	83h	W	-	-	-	-	-	MAT_OI2[8:6]			0000 0000
MAT_OI2_LSB	84h	W	OFFSET_IN2[5:0]						-	-	0000 0000
MAT_OI3_MSB	85h	W	-	-	-	-	-	MAT_OI3[8:6]			0000 0000
MAT_OI3_LSB	86h	W	OFFSET_IN3[5:0]						-	-	0000 0000
MAT_P11_MSB	87h	W	-	-	-	-	-	P11[10:8]			0000 0000
MAT_P11_LSB	88h	W	P11[7:0]								0000 0010
MAT_P12_MSB	89h	W	-	-	-	-	-	P12[10:8]			0000 0001
MAT_P12_LSB	8Ah	W	P12[7:0]								0000 0110
MAT_P13_MSB	8Bh	W	-	-	-	-	-	P13[10:8]			0000 0000
MAT_P13_LSB	8Ch	W	P13[7:0]								0110 0100

Table 4. I²C-bus registers; (R): reading register[1] …continued

Register	Sub addr	R/W	Bit definition 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Default value
MAT_P21_MSB	8Dh	W	-	-	-	-	-	P21[10:8]			0000 0110
MAT_P21_LSB	8Eh	W	P21[7:0]								1000 1001
MAT_P22_MSB	8Fh	W	-	-	-	-	-	P22[10:8]			0000 0001
MAT_P22_LSB	90h	W	P22[7:0]								1100 0000
MAT_P23_MSB	91h	W	-	-	-	-	-	P23[10:8]			0000 0111
MAT_P23_LSB	92h	W	P23[7:0]								1011 0111
MAT_P31_MSB	93h	W	-	-	-	-	-	P31[10:8]			0000 0110
MAT_P31_LSB	94h	W	P31[7:0]						-	-	1101 0111
MAT_P32_MSB	95h	W	-	-	-	-	-	P32[10:8]			0000 0111
MAT_P32_LSB	96h	W	P32[7:0]						-	-	0110 1001
MAT_P33_MSB	97h	W	-	-	-	-	-	P33[10:8]			0000 0001
MAT_P33_LSB	98h	W	P33[7:0]						-	-	1100 0000
MAT_OO1_MSB	99h	W	-	-	-	-	-	OFFSET_OUT1[8:6]			0000 0000
MAT_OO1_LSB	9Ah	W	OFFSET_OUT1[5:0]						-	-	0100 0000
MAT_OO2_MSB	9Bh	W	-	-	-	-	-	OFFSET_OUT2[8:6]			0000 0010
MAT_OO2_LSB	9Ch	W	OFFSET_OUT2[5:0]						-	-	0000 0000
MAT_OO3_MSB	9Dh	W	-	-	-	-	-	OFFSET_OUT3[8:6]			0000 0010
MAT_OO3_LSB	9Eh	W	OFFSET_OUT3[5:0]						-	-	0000 0000
MAT_BYPASS	9Fh	W	-	-	-	-	-	-	-	MAT_BP	0000 0001
Reserved for test	A0h	W	x	x	x	x	x	x	x	x	0001 0000
PXCNT_PR_LSB	A1h	W	PXCNT_PR[7:0]								0000 0011
PXCNT_MSB	A2h	W	PXCNT_PR[11:8]				PXCNT_NPIX[11:8]				0000 0011
PXCNT_NPIX_LSB	A3h	W	PXCNT_NPIX[7:0]								0110 0000
LCNT_PR_LSB	A4h	W	LCNT_PR[7:0]								0000 0001
LCNT_MSB	A5h	W	LCNT_PR[11:8]				LCNT_NLIN[11:8]				0000 0000
LCNT_NLIN_LSB	A6h	W	PXCNT_NLIN[7:0]								0000 0000
HREF_S_LSB	A7h	W	HREF_START[7:0]								0000 0000
HREF_MSB	A8h	W	HREF_START[11:8]				HREF_END[11:8]				0000 0000
HREF_E_LSB	A9h	W	HREF_END[7:0]								0000 0000
HS_S_LSB	AAh	W	HS_START[7:0]								0000 0000

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Default value
HS_MSB	ABh	W	HS_START[11:8]				HS_END[11:8]				0000 0000
HS_E_LSB	ACh	W	HS_END[7:0]								0000 0000
VREF_F1_S_MSB	ADh	W	-	-	-	-	-	VREF_F1_START[10:8]			0000 0000
VREF_F1_S_LSB	AEh	W	VREF_F1_START[7:0]								0000 0000
VREF_F1_WIDTH	AFh	W	VREF_F1_WIDTH[7:0]								0000 0000
VREF_F2_S_MSB	B0h	W	-	-	-	-	-	VREF_F2_START[10:8]			0000 0000
VREF_F2_S_LSB	B1h	W	VREF_F2_START[7:0]								0000 0000
VREF_F2_WIDTH	B2h	W	VREF_F2_WIDTH[7:0]								0000 0000
VS_F1_LINE_S_MSB	B3h	W	-	-	-	-	-	VS_F1_LINE_START[10:8]			0000 0000
VS_F1_LINE_S_LSB	B4h	W	VS_F1_LINE_START[7:0]								0000 0000
VS_F1_LINE_WIDTH	B5h	W	VS_F1_LINE_WIDTH[7:0]								0000 0000
VS_F2_LINE_S_MSB	B6h	W	-	-	-	-	-	VS_F2_LINE_START[10:8]			0000 0000
VS_F2_LINE_S_LSB	B7h	W	VS_F2_LINE_START[7:0]								0000 0000
VS_F2_LINE_WIDTH	B8h	W	VS_F2_LINE_WIDTH[7:0]								0000 0000
VS_F1_PIX_S_LSB	B9h	W	VS_F1_PIX_START[7:0]								0000 0001
VS_F1_PIX_MSB	BAh	W	VS_F1_PIX_START[11:8]				VS_F1_PIX_END[11:8]				0000 0000
VS_F1_PIX_E_LSB	BBh	W	VS_F1_PIX_END[7:0]								0000 0001
VS_F2_PIX_S_LSB	BCh	W	VS_F2_PIX_START[7:0]								0000 0001
VS_F2_PIX_MSB	BDh	W	VS_F2_PIX_START[11:8]				VS_F2_PIX_END[11:8]				0000 0000
VS_F2_PIX_E_LSB	BEh	W	VS_F2_PIX_END[7:0]								0000 0001
FREF_F1_S_LSB	BFh	W	FREF_F1_START[7:0]								0000 0000
FREF_POL_MSB	C0h	W	FPOL	FREF_F1_START[10:8]			-	FREF_F2_START[10:8]			0000 0000
FREF_F2_S_LSB	C1h	W	FREF_F2_START[7:0]								0000 0000
CLAMP_PIX_S_LSB	C8h	W	CLAMP_PIX_START[7:0]								0000 0000
CLAMP_PIX_MSB	C9h	W	CLAMP_PIX_START[11:8]				CLAMP_PIX_END[11:8]				0000 0000
CLAMP_PIX_E_LSB	CAh	W	CLAMP_PIX_END[7:0]								0000 0000
CLP_F1_LINE_S_MSB	CBh	W	-	-	-	-	-	CLAMP_F1_LINE_START[10:8]			0000 0000
CLP_F1_LINE_S_LSB	CCh	W	CLAMP_F1_LINE_START[7:0]								0000 0000
CLP_F1_LINE_WIDTH	CDh	W	CLAMP_F1_LINE_WIDTH[7:0]								0000 0000
CLP_F2_LINE_S_MSB	CEh	W	-	-	-	-	-	CLAMP_F2_LINE_START[10:8]			0000 0000

Table 4. I2C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition 7 (MSB)	6	5	4	3	2	1	0 (LSB)	Default value
CLP_F2_LINE_S_LSB	CFh	W	CLAMP_F2_LINE_START[7:0]								0000 0000
CLP_F2_LINE_WIDTH	D0h	W	CLAMP_F2_LINE_WIDTH[7:0]								0000 0000
GAIN_S_LSB	D1h	W	GAIN_START[7:0]								0000 0001
GAIN_MSB	D2h	W	GAIN_START[11:8]				GAIN_END[11:8]				0000 0000
GAIN_E_LSB	D3h	W	GAIN_END[7:0]								0101 0001
FDW_S_LSB	D4h	W	FDW_START[7:0]								0000 0000
FDW_MSB	D5h	W	FDW_START[11:8]				FDW_END[11:8]				0000 0000
FDW_E_LSB	D6h	W	FDW_END[7:0]								0000 0000
ASD_MEASLIN_MSB	D7h	R	x	x	x	x	x	MEAS_LINES[10:8]			0000 0000
MEASLIN_LSB	D8h	R	MEAS_LINES[7:0]								0000 0000
MEASPIX_MSB	D9h	R	-	-	-	-	MEAS_PIX[11:8]				0000 0000
MEASPIX_LSB	DAh	R	MEAS_PIX[7:0]								0000 0000
Reserved for test	DBh	W	x	x	x	x	x	x	x	x	0000 0000
BLK_GY_LSB	DCh	W	BLK_GY[5:0]						-	-	0100 0000
BLK_BU_LSB	DDh	W	BLK_BU[5:0]						-	-	0000 0000
BLK_RV_LSB	DEh	W	BLK_RV[5:0]						-	-	0000 0000
BLK_MSB	DFh	W	BLK_GY[7:6]		-	BLK_BU[7:6]		-	BLK_RV[7:6]		0001 0010
PRE_FILTERS	E0h	W	-	-	FILTERBU[1:0]		-	-	FILTERRV[1:0]		0010 0010
OF_CCEIL	E1h	W	-	-	C_CEIL[5:0]						1100 0000
OF_CFLOOR	E2h	W	-	-	C_FLOOR[5:0]						0100 0000
OF_YCEIL	E3h	W	-	-	Y_CEIL[5:0]						1010 1100
OF_YFLOOR	E4h	W	-	-	Y_FLOOR[5:0]						0100 0000
OF_CTRL	E5h	W	OUT	VPL	-	BLC	TRC	-	FOR_SEL[1:0]		0100 0010
Reserved for test	E6h	W	x	x	x	x	x	x	x	x	0000 0001
Reserved for test	E7h	W	-	-	-	-	x	x	x	x	0000 0000
CSVSHS_SEL	E8h	W	CS_SEL[2:0]			VS_SEL[1:0]		HS_SEL[2:0]			0000 0000
POL_CTRL	E9h	W	-	-	CS_POL	HS_POL	VS_POL	FREF_POL	HREF_POL	VREF_POL	0000 0000
OUTPUT_CTRL	EAh	W	-	-	VPC_SEL[1:0]		VPB_SEL[1:0]		VPA_SEL[1:0]		1010 0100
DE_CNTRL	EBh	W	HR_PXQ	HR_SEL	DE_PXQ	DE_POL	-	-	-	-	0000 1000
RESET_CNTRL	F1h	W	-	-	-	RST_MAN	RST_AVI	-	-	-	0000 0101

Table 4. I²C-bus registers; (R): reading register[1] *…continued*

Register	Sub addr	R/W	Bit definition								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
PD_AVI_CNTRL0	F4h	W	-	-	-	PD_SOG2	PD_SOG1	PD_DLL	PD_PLL	PD_AVI	0000 0000
PD_AVI_CNTRL1	F5h	W	-	-	-	-	-	PD_ADC_B	PD_ADC_G	PD_ADC_R	0010 0000
FVH_SEL	F6h	W	-	-	-	-	-	-	-	FVH_SEL	0000 0001
LSB_OUT_SEL	F7h	W	LSB_SEL[7:0]								0000 0000
OR_SEL	F9h	W	x	x	x	x	x	x	x	x	0000 0000

[1] The symbol ‘x’ indicates a bit reserved for test and the symbol ‘-’ indicates that the bit is not used.

9.2.1 Version register

Table 5. VERSION register (address 00h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 0	-	R	14h*	the version register gives the version of the device, version is 0001 0100

9.2.2 Input selection register

Table 6. INPUT_SEL register (address 01h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	x	W	00 0001*	for test: must be set to default value for proper operation
1 to 0	VINS[1:0]	W		**video input selection:** enables analog video input 1, analog video input 2
			00*	video input 1
			01	video input 2

9.2.3 Sync detection recognition and separation registers

Table 7. SDRS_CTRL1 register (address 04h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	x	R/W	0*	for test: must be set to default value for proper operation
6	ASD_DIS	W		**automatic sync detection disable:** Digital Separated Syncs > Digital Composite Sync > Sync On Green
			0*	enable
			1	disable
5	SOGF	W		**sync on green forced:** when set, forces the use of SOGx (where x corresponds to the selected analog video input) input when the automatic sync detection is disabled
			0*	enable
			1	disable
4	DCSF	W		**digital composite sync forced:** when set, forces the use of HCSYNCx (where x corresponds to the selected analog video input) input when the automatic sync detection is disabled
			0*	enable
			1	disable
3 to 0	x	W	0000*	for test: must be set to default value for proper operation

Table 8. SDRS_FLAGS register (address 0Dh) bit description[1]

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	ASD	R		**additional sync pulses detected:** additional sync pulses on the selected analog input
			0*	are not detected
			1	are detected

Table 8. SDRS_FLAGS register (address 0Dh) bit description[1] *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
6	SOGD2	R		**sync on green detected:** on pin SOG2
			0*	pulses are not detected
			1	pulses are detected
5	-			not used
4	DSSD2	R		**digital separated syncs detected:** on pins VSYNC2 and HCSYNC2
			0*	pulses are not detected
			1	pulses are detected
3	-			not used
2	SOGD1	R		**sync on green detected:** on pin SOG1
			0*	pulses are not detected
			1	pulses are detected
1	-			not used
0	DSSD1	R		**digital separated syncs detected:** on pins VSYNC1 and HCSYNC1
			0*	pulses are not detected
			1	pulses are detected

[1] When one of these bits changes, the VAI_N pin is pulled down until SDRS_FLAGS0 is read.

9.2.4 PLL registers

Table 9. PLL_CTRL register (address 10h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7		R		reserved for test
6 to 4	-	R	-	not used
3	EDG	R		**edge:** synchronizes the PLL on the internal HSYNC pulses
			0*	on the rising edge
			1	on the falling edge
2 to 0		R		reserved for test

[1] By default, the SDRS toggles automatically the HSYNC to have an internal positive HSYNC signal

Table 10. PLL_MNDIV registers (address 11h and 12h) bit description
*Legend: * = default value*

Address	Register	Bit	Symbol	Access	Value	Description
11h	PLL_MNDIV_MSB	7 to 6	MDIV[1:0]	W		**master divider:** selects the master divider to adjust the sampling frequency range with the PLL frequency range from 110 MHz to 200 MHz
					00	divided by 1; > 110 Msample/s
					01	divided by 2; 50 Msample/s to 110 Msample/s
					10	divided by 4; 25 Msample/s to < 50 Msample/s
					11*	divided by 8; 12.5 Msample/s to < 25 Msample/s
		5 to 4	-	W	00*	not used
		3 to 0	NDIV[11:8]	W	3h*	**pixel divider:** pixel division value
12h	PLL_NDIV_LSB	7 to 0	NDIV[7:0]	W	60h*	

Table 11. LOCKFLAG register (address 13h) bit description
*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	-	W	00 0000*	not used
1	x	W	0*	for test; must be set to default value for proper operation
0	PLL_LOCK	R		**PLL_lock:** indicates when the PLL is locked
			0*	not locked
			1	locked

9.2.5 Pixel clocks generation registers

Table 12. DLL_PHASE register (address 14h) bit description
*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	-	W	000*	not used
4 to 0	PHASE[4:0]	W	1 0000*	**phase:** these bits set the phase shift for the three clock signals CLKPIX, CLKFOR and CLKOUT; it is the fine adjustment of the phase, see Table 15

Table 13. PIXCLKGEN_PRST register (address 15h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 5	CLKOUT_PRST[2:0]	W	110*	**output clock preset:** these bits set the phase shift for the output clock CLKOUT; it is the rough adjustment of the phase and there is the same number of steps as the division factor selected for CLKOUT
4 to 3	CLKFOR_PRST[1:0]	W	10*	**formatter clock preset** used to program the phase shift for the 4 : 2 : 2 formatter clock CLKFOR It Is the rough adjustment of the phase and there is the same number of steps than the division factor selected for CLKFOR
2 to 0	CLKPIX_PRST[2:0]	W	111*	**pixel clock preset:** these bits set the phase shift for the ADC and VHREF pixel clock CLKPIX; it is the rough adjustment of the phase and there is the same number of steps as the division factor selected for CLKPIX

Table 14. PIXCLKGEN_CTRL0 register (address 16h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 6	CLKOUT_DIV[1:0]	W		**output clock division factor:** selects the PLL frequency division factor for the output clock CLKOUT. For 4 : 2 : 2 semi-planar or 4 : 4 : 4 output formats, the division factor must be the same as the master division factor. In case of the 4 : 2 : 2 ITU-R BT.656 formats, it must be half of the master division factor
			00*	divide by 2
			01	divide by 4
			10	divide by 8
			11	not defined
5 to 4	CLKFOR_DIV[1:0]	W		**formatter clock division factor:** selects the PLL frequency division factor for the ITU-R BT.656 formatter clock CLKFOR The division factor must be the half of the master division factor
			00	divide by 2
			01	divide by 4
			10	not defined
			11*	not defined
3 to 2	CLKPIX_DIV[1:0]	W		**pixel clock division factor:** selects the PLL frequency division factor for the pixel clock CLKPIX. The division factor must be the same as the master division factor
			00	divide by 2
			01	divide by 4
			10*	divide by 8
			11	not defined

Table 14. PIXCLKGEN_CTRL0 register (address 16h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
1	PR_DEL	W		**phase delay:** delays the rough adjustment of the three clock signals, see Table 15
			0	no delay
			1*	delay of one PLL period
0	PH_CORR	W		**phase correction:** selects the falling or rising edge of the horizontal reference signal from the PLL to synchronize the three clock divisions, see Table 15
			0	falling edge selected
			1*	rising edge selected

Table 15. Relationship between bits PR_DEL, PH_CORR and phase value

PHASE[4:0]	PR_DEL	PH_CORR
0 to 7	0	0
8 to 15	1	1
16 to 31	1	0

Table 16. Relation between master division and clock division

MDIV[1:0]	Master division	4 : 4 : 4 or semi-planar		4 : 2 : 2 ITU-R BT.656		formatter clock		pixel clock	
		CLKOUT_DIV	CLKOUT_PRST	CLKOUT_DIV	CLKOUT_PRST	CLKFOR_DIV	CLKFOR_PRST	CLKPIX_DIV	CLKPIX_PRST
11	8	10	0 to 7	01	0, 1, 2, 3	01	0, 1, 2, 3	10	0 to 7
10	4	01	0 to 3	00	0 or 1	00	0 or 1	01	0 to 3
01	2	00	0 or 1	11	0	11	0	00	0 or 1
00	1	11	0	not available		not available		00	0

9.2.6 Pixel clocks generation registers

Table 17. PIXCLKGEN_CTRL1 register (address 17h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7	CLKOUT_TOG	W		**output clock toggle**
			0*	does not toggle the signal CLKOUT
			1	toggles the signal CLKOUT
6 to 4	CLKOUT_SEL[2:0]	W		**output clock selection:** select the clock available on pin VCLK
			000	reserved for test
			001	reserved for test
			010	not defined
			011	not defined
			100*	CLKOUT
			101	CLKFOR
			110	CLKPIX
			111	not defined

Table 17. PIXCLKGEN_CTRL1 register (address 17h) bit description *…continued*

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
3 to 2	CLKFOR_SEL[1:0]	W		**formatter clock selection:** select the clock for the ITU-R656 formatter
			00	reserved for test
			01*	CLKFOR
			10	not defined
			11	0
1 to 0	x	W	10*	for test: must be set to default value for proper operation

9.2.7 Clamp levels registers

Table 18. Bright levels registers (address 1Ah to 1Ch) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
1Ah	BRIGHT_GY	7 to 0	BRIGHT_ GY[7:0]	W	10h*	**G/Y brightness:** these bits control the clamp level of the G/Y channel
1Bh	BRIGHT_BU	7 to 0	BRIGHT_ BU[7:0]	W	80h*	**B/P_B brightness:** these bits control the clamp level of the B/P_B channel
1Ch	BRIGHT_RV	7 to 0	BRIGHT_ RV[7:0]	W	80h*	**R/P_R brightness:** these bits control the clamp level of the R/P_R channel

Table 19. Relationship between the brightness code and the clamp level

Programmed code (8-bits)		Clamp code (decimal)
Decimal	Binary MSB/LSB	
0	0000 0000	0
:	:	:
247	1111 0111	247

9.2.8 Video gain registers (GAIN_RV, GAIN_BU, GAIN_GY)

Table 20. R/V video gain registers (addresses 20h to 23h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
20h	COARSE_GAINRV	7 to 4	-	W		not used
		3 to 0	COARSE_RV[3:0]	W	04h*	**coarse_rv:** coarse gain value for channel R/V
21h	FINE_GAINRV	7	-	W		not used
		6 to 0	FINE_RV[6:0]	W	5Ch*	**fine_rv:** fine gain value for channel R/V
22h	AGC_HIGHRV	7 to 0	HIGH_RV[7:0]	W	F0h*	**high_rv:** AGC high value for channel R/V
23h	AGC_LOWRV	7	-	W		not used
		6 to 0	LOW_RV[6:0]	W	90h*	**low_rv:** AGC low value for channel R/V

Table 21. B/U video gain registers (addresses 2Ah to 2Dh) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
2Ah	COARSE_GAINBU	7 to 4	-	W		not used
		3 to 0	COARSE_GY[3:0]	W	04h*	**coarse_bu:** coarse gain value for channel B/U
2Bh	FINE_GAINBU	7	-	W		not used
		6 to 0	FINE_BU[6:0]	W	5Ch*	**fine_bu:** fine gain value for channel B/U
2Ch	AGC_HIGHBU	7 to 0	HIGH_BU[7:0]	W	F0h*	**high_bu:** AGC high value for channel B/U
2Dh	AGC_LOWBU	7	-	W		not used
		6 to 0	LOW_BU[6:0]	W	90h*	**low_bu:** AGC low value for channel B/U

Table 22. G/Y video gain registers (addresses 34h to 37h) bit description

*Legend: * = default value*

Addr	Register	Bit	Symbol	Access	Value	Description
34h	COARSE_GAINGY	7 to 4	-	W		not used
		3 to 0	COARSE_GY[3:0]	W	04h*	**coarse_gy:** coarse gain value for the channel G/Y
35h	FINE_GAINGY	7	-	W		not used
		6 to 0	FINE_GY[6:0]	W	5Ch*	**fine_gy:** fine gain value for the channel G/Y
36h	AGC_HIGHGY	7 to 0	HIGH_GY[7:0]	W	F0h*	**high_gy:** AGC high value for the channel G/Y
37h	AGC_LOWGY	7	-	W		not used
		6 to 0	LOW_GY[6:0]	W	90h*	**low_gy:** AGC low value for the channel G/Y

9.2.9 Sync timing measurement registers

Table 23. Sync timing measurement registers (address 40h to 44h) bit description

Addr	Register	Bit	Symbol	Access	Value	Description
40h	V_PER_MSB	7 to 0	V_PER[19:12]	R	00h*	**vertical period:** indicates the period of two fields (interlaced) or frames (progressive), counted in MCLK clock periods[1]
41h	V_PER_ISB	7 to 0	V_PER[11:4]	R	00h*	
44h	STM_LSB	7 to 4	V_PER[3:0]	R	0000*	
42h	H_PER_MSB	7 to 0	H_PER[9:2]	R	00h*	**horizontal period:** indicates the period of the line, counted in MCLK clock periods[1]
44h	STM_LSB	3 to 2	H_PER[1:0]	R	00*	
43h	HS_WIDTH_MSB	7 to 0	HS_WIDTH[9:2]	R	00h*	**horizontal sync width:** indicates the width of the horizontal sync pulse, counted in MCLK clock periods[1]
44h	STM_LSB	1 to 0	HS_WIDTH[1:0]	R	00*	

[1] The recommended frequency for MCLK signal is 13.5 MHz.

9.2.10 Color space conversion registers

Table 24. MAT_CTRL register (address 80h) bit description

*Legend: * = default value*

Bit	Symbol	Access	Value	Description
7 to 2	-	W	00 0000*	not used
1 and 0	MAT_SC[1:0]	W		**scale factor selection:** fix the scale factor to convert the floating matrix [C_{xy}] into an integer matrix [P_{xy}]: $\begin{bmatrix} P_{11} & P_{12} & P_{13} \\ P_{21} & P_{22} & P_{23} \\ P_{31} & P_{32} & P_{33} \end{bmatrix} = INT\left(S \times \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix}\right)$. The choice depends on the biggest coefficient in absolute value $\|C_{xy}\|$:
			00	when $2 \leq \|C_{xy}\| < 4$; S = 256
			01	when $1 \leq \|C_{xy}\| < 2$; S = 512
			10*	when $\|C_{xy}\| < 1$; S = 1024
			11	undefined

Table 25. Offset input registers (address 81h to 86h) bit description

*Legend: * = default value*[1]

Addr	Register	Bit	Symbol	Access	Value	Description
81h	MAT_OI1_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI1[8:6]	W	000*	**offset in 1** compensate the brightness value for the channel G/Y, e.g. with YC_BC_R input, –16 for Y so OFFSET_IN1 = 1111 0000b = F0h[2]
82h	MAT_OI1_LSB	7 to 2	OFFSET_IN1[5:0]	W	00h*	
		1 to 0	-	W	00*	not used
83h	MAT_OI2_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI2[8:6]	W	000*	**offset in 2** compensate the brightness value for the channel R/V, e.g. with YC_BC_R input, –128 for C_R so OFFSET_IN2 = 1000 0000b = 80h[2]
84h	MAT_OI2_LSB	7 to 2	OFFSET_IN2[5:0]	W	00h*	
		1 to 0	-	W	00*	not used

Table 25. Offset input registers (address 81h to 86h) bit description *…continued*
*Legend: * = default value[1]*

Addr	Register	Bit	Symbol	Access	Value	Description
85h	MAT_OI3_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	MAT_OI3[8:6]	W	000*	**offset_in3** compensate the brightness value for the channel B/U, e.g. with YC_BC_R input, –128 for C_B so OFFSET_IN3 = 1000 0000b = 80h[2]
86h	MAT_OI3_LSB-	7 to 0	OFFSET_IN3[5:0]	W	00h*	
		1 to 0	-	W	00*	not used

[1] The default values correspond with the RGB full-scale to YC_BC_R ITU-R BT.601 reduced-scale conversion.

[2] The value is signed 11-bit two's complement integer.

Table 26. Coefficient registers (address 87h to 98h) bit description
*Legend: * = default value[1]*

Addr	Register	Bit	Symbol	Access	Value	Description
87h	MAT_P11_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P11[10:8]	W	010*	**coefficient (1,1):** coefficient from the G/Y channel to the G/Y channel[2]
88h	MAT_P11_LSB	7 to 0	P11[7:0]	W	02h*	
89h	MAT_P12_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P12[10:8]	W	001*	**coefficient (1,2):** coefficient from the R/C_R channel to the G/Y channel[2]
8Ah	MAT_P12_LSB	7 to 0	P12[7:0]	W	06h*	
8Bh	MAT_P13_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P13[10:8]	W	000*	**coefficient (1,3):** coefficient from the B/C_B channel to the G/Y channel[2]
8Ch	MAT_P13_LSB	7 to 0	P13[7:0]	W	64h*	
8Dh	MAT_P21_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P21[10:8]	W	110*	**coefficient (2,1):** coefficient from the G/Y channel to the R/C_R channel[2]
8Eh	MAT_P21_LSB	7 to 0	P21[7:0]	W	89h*	
8Fh	MAT_P22_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P22[10:8]	W	001*	**coefficient (2,2):** coefficient from the R/C_R channel to the R/C_R channel[2]
90h	MAT_P22_LSB	7 to 0	P22[7:0]	W	C0h*	
91h	MAT_P23_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P23[10:8]	W	111*	**coefficient (2,3):** coefficient from the B/C_B channel to the R/C_R channel[2]
92h	MAT_P23_LSB	7 to 0	P23[7:0]	W	B7h*	
93h	MAT_P31_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P31[10:8]	W	110	**coefficient (3,1):** coefficient from the G/Y channel to the B/C_B channel[2]
94h	MAT_P31_LSB	7 to 0	P31[7:0]	W	D7h*	
95h	MAT_P32_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P32[10:8]	W	111*	**coefficient (3,2):** coefficient from the R/C_R channel to the B/C_B channel[2]
96h	MAT_P32_LSB	7 to 0	P32[7:0]	W	69h*	
97h	MAT_P33_MSB	7 to 3	-	W	0 0000*	not used
		2 to 0	P33[10:8]	W	001*	**coefficient (3,3):** coefficient from the B/C_B channel to the B/C_B channel[2]
98h	MAT_P33_LSB	7 to 0	P33[7:0]	W	C0h*	

[1] The default values of the coefficients correspond with the RGB full-scale to YC_BC_R ITU-R BT601 reduced scale conversion.

[2] The value is signed 11-bit two's complement integer.