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TDA9983B

HDMI transmitter up to 150 MHz pixel rate with 3 × 8-bit video inputs and 4 × I²S-bus with S/PDIF

Rev. 01 — 20 May 2008 Product data sheet

1. General description

The TDA9983B is an HDMI transmitter (which also supports DVI) that enables a 3 × 8-bit RGB or YC_BC_R video stream (with a pixel rate up to 150 MHz for the TDA9983BHW/15 version), up to 4 I²S-bus audio streams (with an audio sampling rate up to 192 kHz) and the additional information required by all the HDMI 1.2a standards.

A programmable upscaling block enables a 720p/1080i output from a standard definition input. An intrafield deinterlacer is included in the scaler.

In order to be compatible with most applications, the TDA9983B integrates a full programmable input formatter and color space conversion block. The video input formats accepted are YC_BC_R 4 : 4 : 4 (up to 3 × 8-bit), YC_BC_R 4 : 2 : 2 semi-planar (up to 2 × 12-bit), YC_BC_R 4 : 2 : 2 compliant with ITU656 and ITU656-like (up to 1 × 12-bit).

For ITU656-like formats, double edges are supported so that data can be sampled on rising and falling edges.

The device can be controlled via an I²C-bus interface.

2. Features

- 3 × 8-bit video data input bus, CMOS and LV-TTL compatible
- Horizontal synchronization, vertical synchronization and Data Enable (DE) inputs or VREF, HREF and FREF could be used for input data synchronization
- Pixel rate clock input can be made active on one or both edges (selectable by I²C-bus)
- The TDA9983B has 4 I²S-bus audio input channels and 1 S/PDIF channel; audio sampling rate up to 192 kHz
- 250 MHz to 1.50 GHz HDMI transmitter operation
- Programmable input formatter and upsampler/interpolator allows input of any of the 4 : 4 : 4, 4 : 2 : 2 semi-planar, 4 : 2 : 2 ITU656 and ITU656-like formats
- Programmable color space converter:
  - RGB to YC_BC_R
  - YC_BC_R to RGB
- The upscaler enables a 720p/1080i output from a standard definition input using intelligent edge interpolation
- Controllable via I²C-bus
- Low power dissipation
- 1.8 V and 3.3 V power supplies
- Power-down mode

- Hard reset

3. Applications

- DVD players and recorders
- Set-Top Box (STB)
- AV receivers and amplifiers (repeater)
- Camcorders
- Digital still cameras
- Media players
- PVRs
- Media centers PCs, graphics add-in boards, notebook PCs
- Switches

4. Quick reference data

Table 1. Quick reference data

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TDA9983BHW/8 and TDA9983BHW/15							
$V_{DDA(FRO\_3V3)}$	free running oscillator 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDA(PLL\_3V3)}$	PLL 3.3 V analog supply voltage			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)		[1]	3.0	3.3	3.6	V
$V_{DDH(3V3)}$	HDMI supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDC(1V8)}$	core supply voltage (1.8 V)		[1]	1.65	1.8	1.95	V
T_{amb}	ambient temperature			0	-	70	°C
TDA9983BHW/8; up to 81 MHz							
$f_{clk(max)}$	maximum clock frequency		[2]	81	-	-	MHz
P_{cons}	power consumption		[2]	-	322	-	mW
		worst case	[3]	-	338	503	mW
P_{tot}	total power dissipation		[2]	-	458	-	mW
		worst case	[3]	-	472	651	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW

Table 1. Quick reference data *...continued*

$V_{DDA(FRO\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDA(PLL\_3V3)}$ = 3.0 V to 3.6 V; $V_{DDH(3V3)}$ = 3.0 V to 3.6 V; $V_{DDD(3V3)}$ = 3.0 V to 3.6 V; $V_{DDC(1V8)}$ = 1.65 V to 1.95 V; V_{PP} = 0 V; T_{amb} = 0 °C to 70 °C. Typical values are measured at $V_{DDA(FRO\_3V3)}$ = $V_{DDA(PLL\_3V3)}$ = $V_{DDH(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V; $V_{DDC(1V8)}$ = 1.8 V; V_{PP} = 0 V and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TDA9983BHW/15; up to 150 MHz							
$f_{clk(max)}$	maximum clock frequency		[4]	150	-	-	MHz
P_{cons}	power consumption		[4]	-	361	583	mW
P_{tot}	total power dissipation		[4]	-	495	732	mW
P_{pd}	power dissipation in power-down mode			-	13.5	38.4	mW

[1] The $V_{DDD(3V3)}$ and $V_{DDC(1V8)}$ power supplies must always follow the sequence shown in Figure 14 to ensure proper power-up conditions.

[2] Video format:
- a) Input 480p (ITU656 embedded sync, rising edge)
- b) Output 1080i (YC_BC_R 4 : 2 : 2)

[3] Worst case video format:
- a) Input 480p (YC_BC_R 4 : 2 : 2 semi-planar)
- b) Output 720p (YC_BC_R 4 : 2 : 2)

[4] Video format:
- a) Input 1080p (RGB 4 : 4 : 4 external sync, rising edge)
- b) Output 1080p (RGB 4 : 4 : 4)

5. Ordering information

Table 2. Ordering information

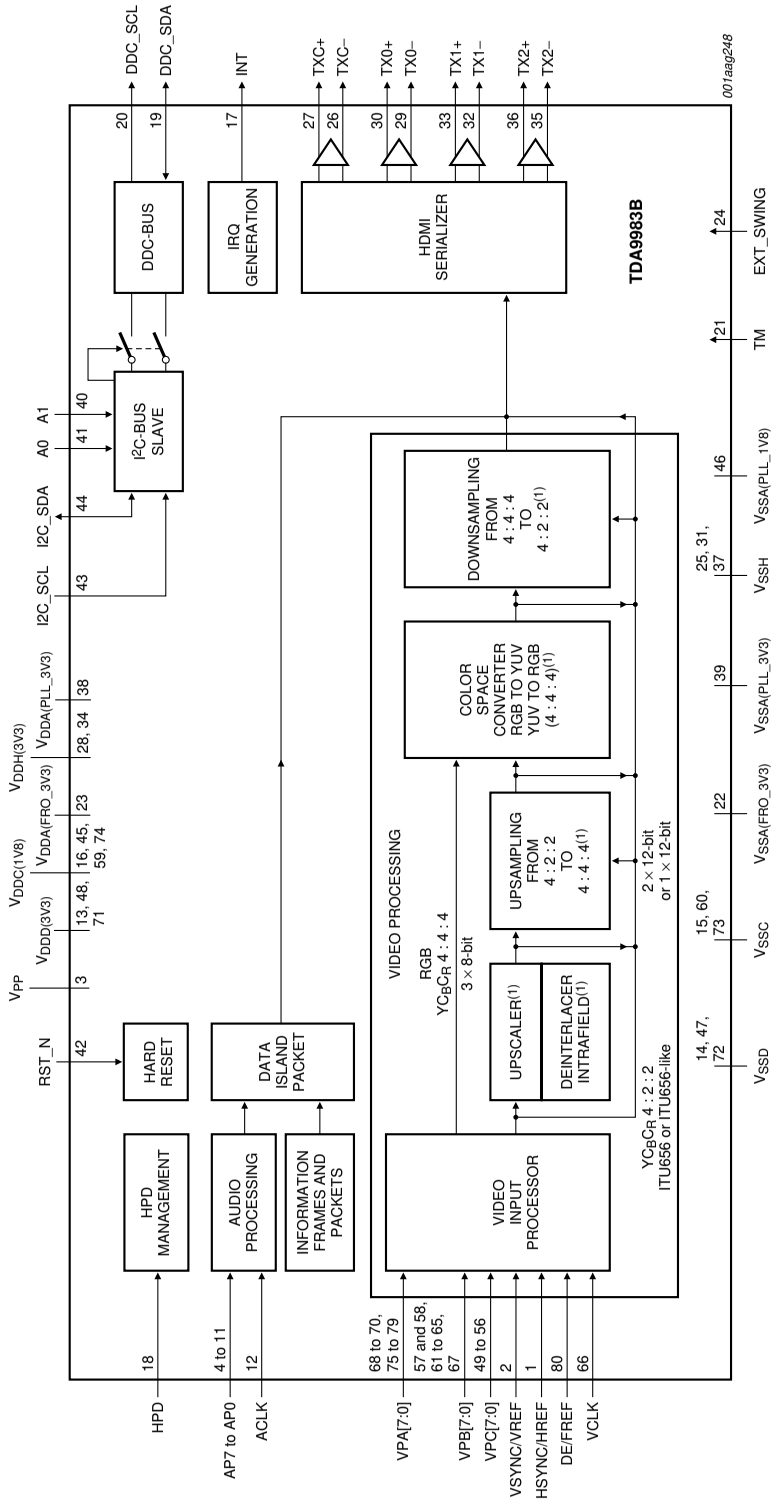
Type number	Package		
	Name	Description	Version
TDA9983BHW	HTQFP80	plastic thermal enhanced thin quad flat package; 80 leads; body 12 × 12 × 1 mm; exposed die pad	SOT841-4

5.1 Ordering options

Table 3. Survey of type numbers

Extended type number	Sampling frequency (Msample/s)	Application
TDA9983BHW/8/C1	81	customer specific version
TDA9983BHW/15/C1	150	customer specific version

6. Block diagram



(1) Block can be bypassed.

Fig 1. Block diagram

7. Pinning information

7.1 Pinning

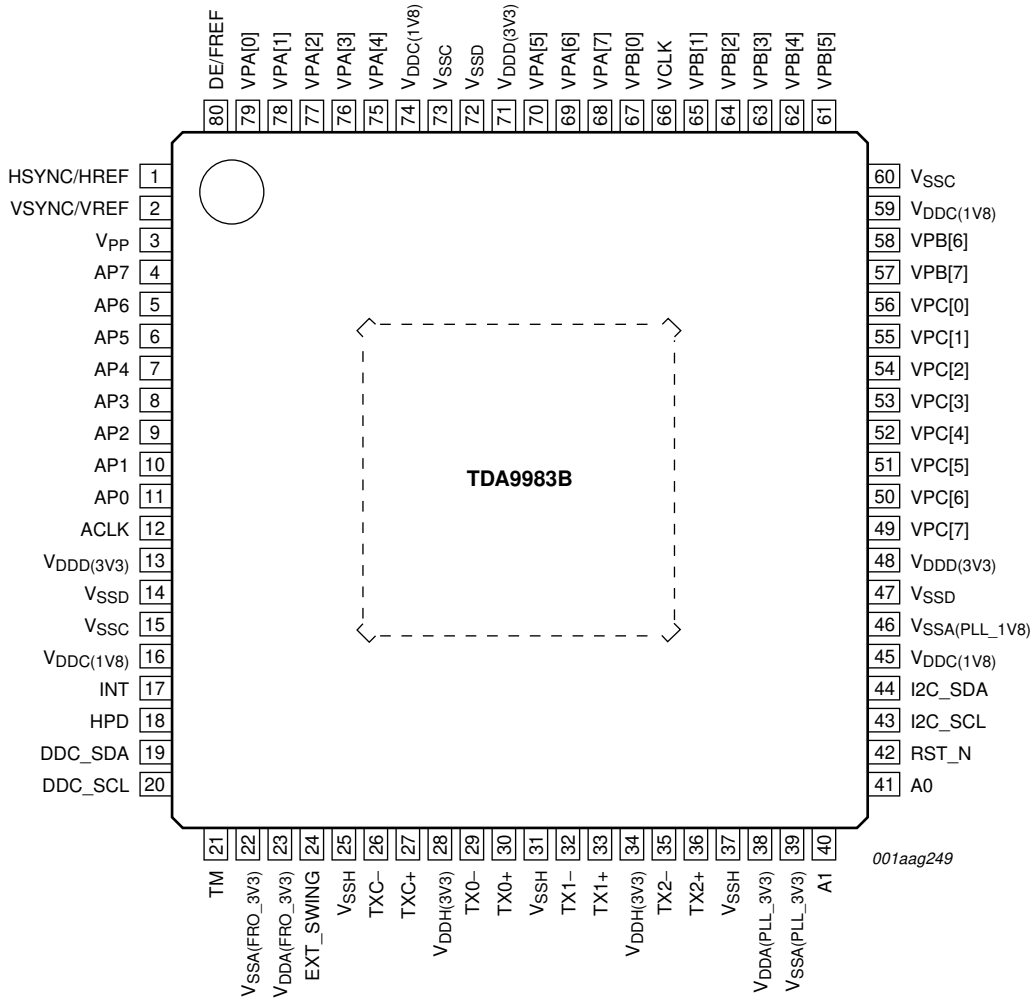


Fig 2. Pin configuration

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
HSYNC/HREF	1	I	horizontal synchronization or reference input
VSYNC/VREF	2	I	vertical synchronization or reference input
V_{PP}	3	P	programming voltage (must be connected to the ground of the digital core in normal operation)
AP7	4	I	audio port 7 input; auxiliary (AUX)
AP6	5	I	audio port 6 input; S/PDIF stream
AP5	6	I	audio port 5 input; optional master clock MCLK for S/PDIF

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
AP4	7	I	audio port 4 input; I^2S-bus 3
AP3	8	I	audio port 3 input; I^2S-bus 2
AP2	9	I	audio port 2 input; I^2S-bus 1
AP1	10	I	audio port 1 input; I^2S-bus 0
AP0	11	I	audio port 0 input; word select WS for I^2S-bus
ACLK	12	I	audio clock input; clock SCK for I^2S-bus
$V_{DDD(3V3)}$	13	P	supply voltage for input ports (3.3 V)
V_{SSD}	14	G	ground for input ports
V_{SSC}	15	G	ground for digital core
$V_{DDC(1V8)}$	16	P	supply voltage for digital core (1.8 V)
INT	17	O	interrupt output (open drain); warns the external microprocessor that a special event has occurred; must be connected to a pull-up resistor; 5 V tolerant
HPD	18	I	hot plug detect input; 5 V tolerant
DDC_SDA	19	I/O	DDC-bus data input/output (open drain); must be connected to a pull-up resistor; 5 V tolerant
DDC_SCL	20	O	DDC-bus clock output (open drain); must be connected to a pull-up resistor; 5 V tolerant
TM	21	I	internal test mode input (must be connected to the ground of the digital core in normal operation)
$V_{SSA(FRO\_3V3)}$	22	G	analog ground for free running oscillator
$V_{DDA(FRO\_3V3)}$	23	P	analog supply voltage for free running oscillator (3.3 V)
EXT_SWING	24	I	external swing adjust input; a fixed resistor must be connected between this pin and $V_{DDH(3V3)}$ to set the HDMI output swing (see Section 8.14.1)
V_{SSH}	25	G	ground for HDMI transmitter
TXC–	26	O	negative clock channel for HDMI output
TXC+	27	O	positive clock channel for HDMI output
$V_{DDH(3V3)}$	28	P	supply voltage for HDMI transmitter (3.3 V)
TX0–	29	O	negative data channel 0 for HDMI output
TX0+	30	O	positive data channel 0 for HDMI output
V_{SSH}	31	G	ground for HDMI transmitter
TX1–	32	O	negative data channel 1 for HDMI output
TX1+	33	O	positive data channel 1 for HDMI output
$V_{DDH(3V3)}$	34	P	supply voltage for HDMI transmitter (3.3 V)
TX2–	35	O	negative data channel 2 for HDMI output
TX2+	36	O	positive data channel 2 for HDMI output
V_{SSH}	37	G	ground for HDMI transmitter
$V_{DDA(PLL\_3V3)}$	38	P	analog supply voltage for PLL (3.3 V)
$V_{SSA(PLL\_3V3)}$	39	G	analog ground reference for PLL
A1	40	I	I^2C-bus slave address input 1; bit 1
A0	41	I	I^2C-bus slave address input 0; bit 0
RST_N	42	I	hard reset input; active LOW

Table 4. Pin description *...continued*

Symbol	Pin	Type[1]	Description
I2C_SCL	43	I	I^2C-bus clock input of device (open drain); must be connected to a pull-up resistor; 5 V tolerant
I2C_SDA	44	I/O	I^2C-bus data input/output of device; open drain; must be connected to a pull-up resistor; 5 V tolerant
$V_{DDC(1V8)}$	45	P	supply voltage for digital core (1.8 V)
$V_{SSA(PLL\_1V8)}$	46	G	analog ground reference for PLL
V_{SSD}	47	G	ground for input ports
$V_{DDD(3V3)}$	48	P	supply voltage for input ports (3.3 V)
VPC[7]	49	I	video port C input bit 7
VPC[6]	50	I	video port C input bit 6
VPC[5]	51	I	video port C input bit 5
VPC[4]	52	I	video port C input bit 4
VPC[3]	53	I	video port C input bit 3
VPC[2]	54	I	video port C input bit 2
VPC[1]	55	I	video port C input bit 1
VPC[0]	56	I	video port C input bit 0
VPB[7]	57	I	video port B input bit 7
VPB[6]	58	I	video port B input bit 6
$V_{DDC(1V8)}$	59	P	supply voltage for digital core (1.8 V)
V_{SSC}	60	G	ground for digital core
VPB[5]	61	I	video port B input bit 5
VPB[4]	62	I	video port B input bit 4
VPB[3]	63	I	video port B input bit 3
VPB[2]	64	I	video port B input bit 2
VPB[1]	65	I	video port B input bit 1
VCLK	66	I	video pixel clock input
VPB[0]	67	I	video port B input bit 0
VPA[7]	68	I	video port A input bit 7
VPA[6]	69	I	video port A input bit 6
VPA[5]	70	I	video port A input bit 5
$V_{DDD(3V3)}$	71	P	supply voltage for input ports (3.3 V)
V_{SSD}	72	G	ground for input ports
V_{SSC}	73	G	ground for digital core
$V_{DDC(1V8)}$	74	P	supply voltage for digital core (1.8 V)
VPA[4]	75	I	video port A input bit 4
VPA[3]	76	I	video port A input bit 3
VPA[2]	77	I	video port A input bit 2
VPA[1]	78	I	video port A input bit 1
VPA[0]	79	I	video port A input bit 0
DE/FREF	80	I	video data enable input or field reference input
Exposed die pad	central	G	exposed die pad; must be connected to the ground of the HDMI transmitter (V_{SSH})

[1] P = power supply; G = ground; I = input; O = output.

8. Functional description

The TDA9983B is designed to convert digital data (video and audio) into an HDMI or a DVI stream. This HDMI stream can handle RGB, YC_BC_R 4 : 4 : 4 and YC_BC_R 4 : 2 : 2. The TDA9983B can accept at its inputs any of the following video modes:

- RGB
- YC_BC_R 4 : 4 : 4
- YC_BC_R 4 : 2 : 2 semi-planar
- YC_BC_R 4 : 2 : 2 ITU656 and ITU656-like

It can also handle audio. The TDA9983B can accept at its inputs any of the following audio buses:

- I^2S-bus (4 lines): up to 8 audio channels
- S/PDIF (1 channel): L-PCM (IEC 60958) or compressed audio (IEC 61937)

8.1 System clock

The clock management is based on a set of 3 PLLs that generate the different clocks required inside the chip. This includes:

- PLL double edge can generate a clock at twice the VCLK input frequency to capture the data at the video input formatter
- PLL scaling can create a new video processing scaled clock taking into account the scaling ratio programmed in the scaler
- PLL serializer is a system clock generator, which enables the stream produced by the encoder to be transmitted on the HDMI data channel at ten times the sampling rate or more; see Section 8.14.2

8.2 Video input processor

The TDA9983B has three video input ports VPA[7:0], VPB[7:0] and VPC[7:0]. The TDA9983B can reallocate and swap each of the 3 ports input channels by inverting the bus and swapping each port.

The TDA9983B can be set to latch data at either the rising or falling edge or both.

The video input formats accept (see Table 5):

- RGB
- YC_BC_R 4 : 4 : 4 (up to 3 $\times$ 8-bit)
- YC_BC_R 4 : 2 : 2 semi-planar (up to 2 $\times$ 12-bit)
- YC_BC_R 4 : 2 : 2 compliant with ITU656 and ITU656-like (up to 1 $\times$ 12-bit)

Table 5. Inputs of video input formatter

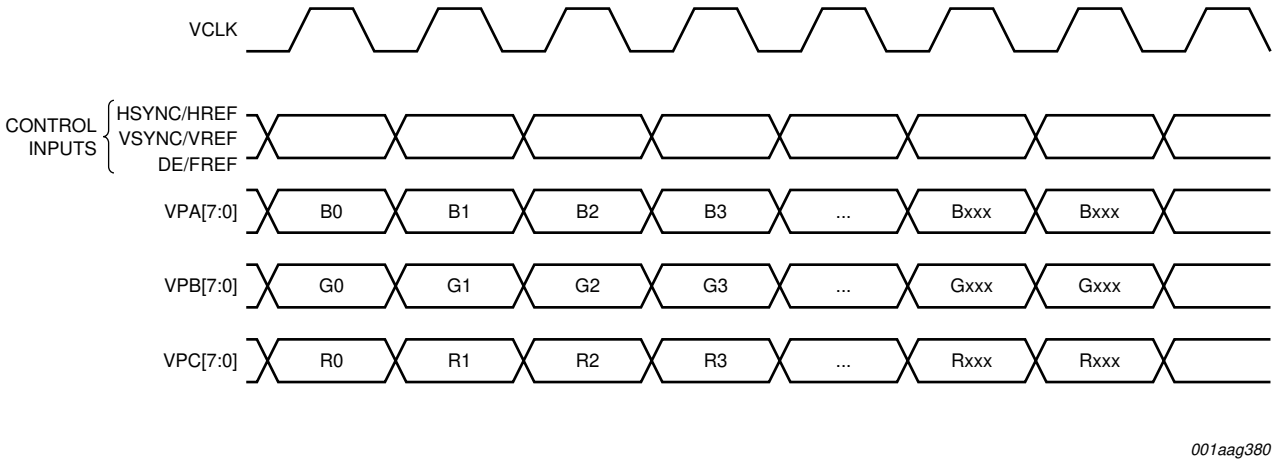
Color space	Format	Channels	Sync	Rising edge	Falling edge	Double edge[1]	Transmission input format	Max. pixel clock on pin VCLK (MHz)	Max. input format	Reference
RGB	4 : 4 : 4	3 × 8-bit	external	X				150		Table 6
			external		X			150		
			embedded	X				150		
			embedded		X			150		
YC_BC_R	4 : 4 : 4	3 × 8-bit	external	X				150		Table 7
			external		X			150		
			embedded	X				150		
			embedded		X			150		
YC_BC_R	4 : 2 : 2	up to 1 × 12-bit ITU656-like	external	X			ITU656-like	54.054	480p/576p	Table 8
			external		X		ITU656-like	54.054	480p/576p	
			external			X	ITU656-like	27.027	480p/576p	Table 9
			embedded	X			ITU656-like	54.054	480p/576p	Table 10
			embedded		X		ITU656-like	54.054	480p/576p	
			embedded			X	ITU656-like	27.027	480p/576p	Table 11
		up to 2 × 12-bit semi-planar	external	X				148.5	1080p	Table 12
			external		X			148.5	1080p	
			embedded	X			SMPTE293M	148.5	1080p	Table 13
			embedded		X		SMPTE293M	148.5	1080p	

[1] Double edge means both rising and falling edges.

Table 6. RGB 4 : 4 : 4 mappings

RGB 4 : 4 : 4 (3× 8-bit) external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**	**Pin**	**RGB 4 : 4 : 4**
VPA[0]	B[0]	VPB[0]	G[0]	VPC[0]	R[0]	HSYNC/HREF	used
VPA[1]	B[1]	VPB[1]	G[1]	VPC[1]	R[1]	VSYNC/VREF	used
VPA[2]	B[2]	VPB[2]	G[2]	VPC[2]	R[2]	DE/FREF	used
VPA[3]	B[3]	VPB[3]	G[3]	VPC[3]	R[3]		
VPA[4]	B[4]	VPB[4]	G[4]	VPC[4]	R[4]		
VPA[5]	B[5]	VPB[5]	G[5]	VPC[5]	R[5]		
VPA[6]	B[6]	VPB[6]	G[6]	VPC[6]	R[6]		
VPA[7]	B[7]	VPB[7]	G[7]	VPC[7]	R[7]		



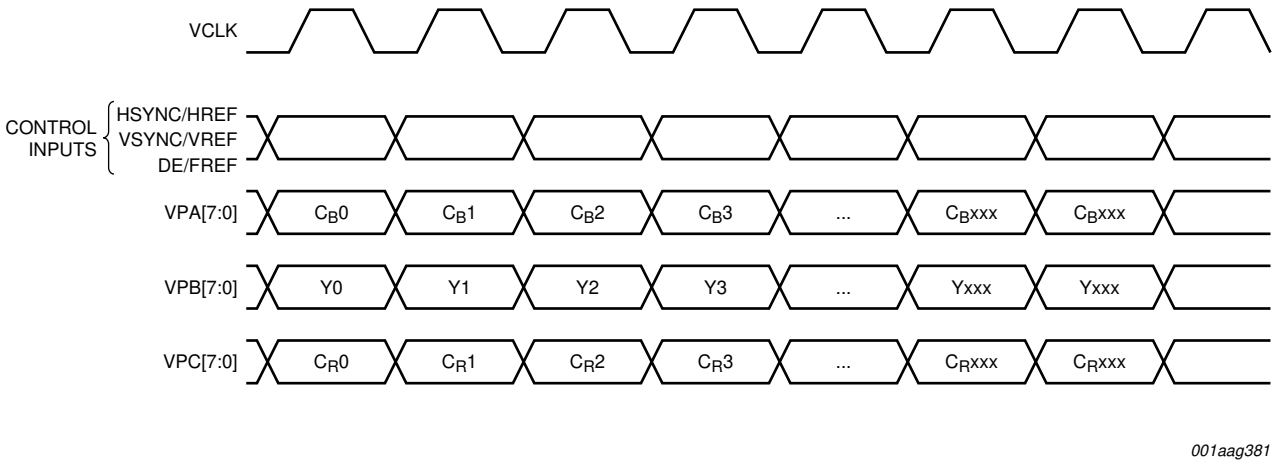
DE could also be generated from HSYNC/HREF and VSYNC/VREF

Fig 3. Pixel encoding in RGB 4 : 4 : 4 (rising edge) input

Table 7. YC_BC_R 4 : 4 : 4 mappings

YC_BC_R 4 : 4 : 4 (3× 8-bit) external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 45h; VIP_CNTRL_2 = 01h.

Video port A		Video port B		Video port C		Control	
Pin	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**	**Pin**	**YC_BC_R 4 : 4 : 4**
VPA[0]	C_B[0]	VPB[0]	Y[0]	VPC[0]	C_R[0]	HSYNC/HREF	used
VPA[1]	C_B[1]	VPB[1]	Y[1]	VPC[1]	C_R[1]	VSYNC/VREF	used
VPA[2]	C_B[2]	VPB[2]	Y[2]	VPC[2]	C_R[2]	DE/FREF	used
VPA[3]	C_B[3]	VPB[3]	Y[3]	VPC[3]	C_R[3]		
VPA[4]	C_B[4]	VPB[4]	Y[4]	VPC[4]	C_R[4]		
VPA[5]	C_B[5]	VPB[5]	Y[5]	VPC[5]	C_R[5]		
VPA[6]	C_B[6]	VPB[6]	Y[6]	VPC[6]	C_R[6]		
VPA[7]	C_B[7]	VPB[7]	Y[7]	VPC[7]	C_R[7]		



DE could also be generated from HSYNC/HREF and VSYNC/VREF

Fig 4. Pixel encoding in YC_BC_R 4 : 4 : 4 (rising edge) input

Table 8. YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]	VPB[0]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]	VPB[1]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]	VPB[2]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]	DE/FREF	used
VPA[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]	VPB[3]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]		

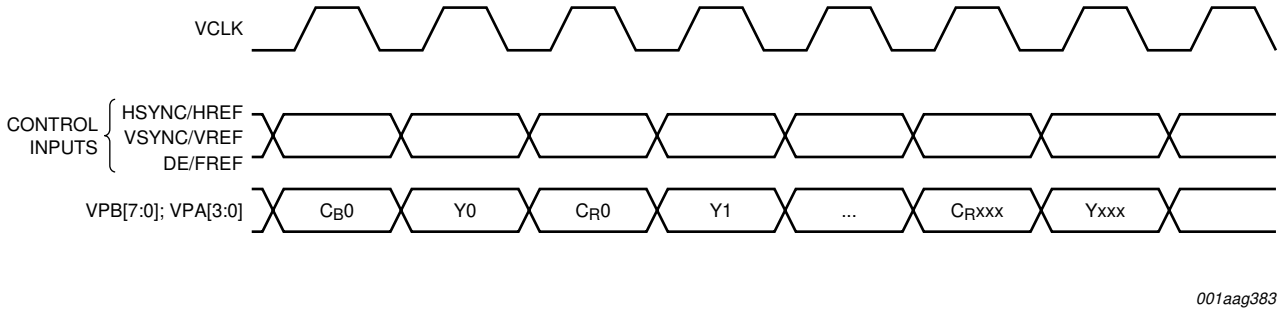


Fig 5. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like external synchronization single edge (rising edge) input

Table 9. YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]	VPB[0]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]	HSYNC/HREF	used
VPA[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]	VPB[1]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]	VSYNC/VREF	used
VPA[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]	VPB[2]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]	DE/FREF	used
VPA[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]	VPB[3]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]		

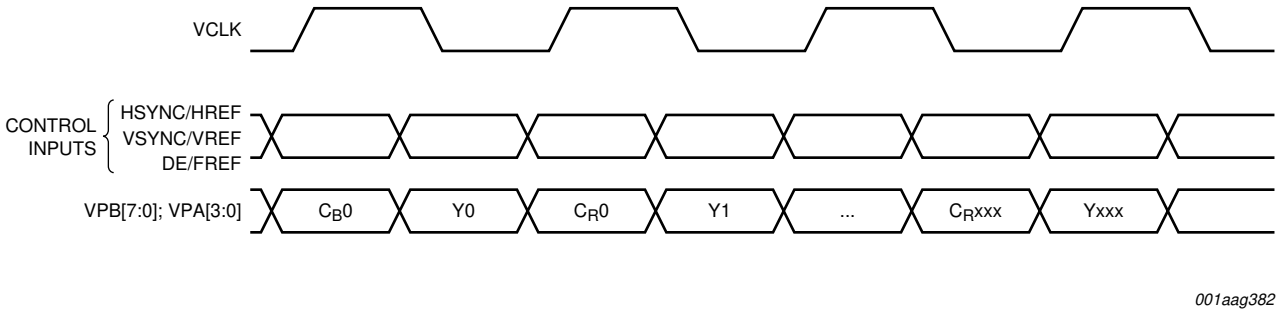


Fig 6. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like external synchronization double edge (rising and falling) input

Table 10. YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]	VPB[0]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]	VPB[1]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]	VPB[2]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]	DE/FREF	not used
VPA[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]	VPB[3]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]		

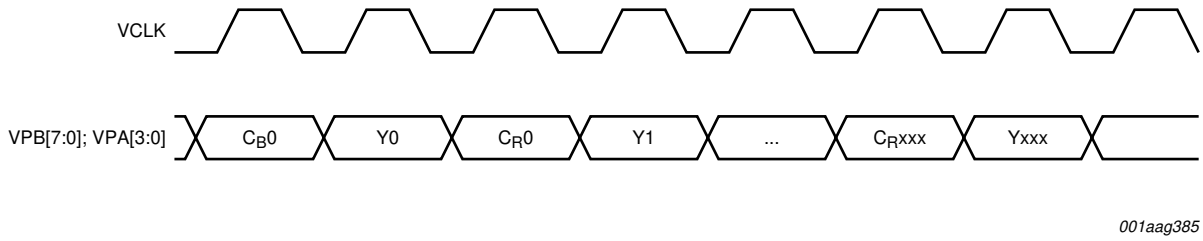


Fig 7. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization single edge (rising edge) input

Table 11. YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge mappings

YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 00h.

Video port A					Video port B					Control	
Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2 (ITU656-like)				Pin	YC_BC_R 4 : 2 : 2
VPA[0]	C_B[0]	Y_0[0]	C_R[0]	Y_1[0]	VPB[0]	C_B[4]	Y_0[4]	C_R[4]	Y_1[4]	HSYNC/HREF	not used
VPA[1]	C_B[1]	Y_0[1]	C_R[1]	Y_1[1]	VPB[1]	C_B[5]	Y_0[5]	C_R[5]	Y_1[5]	VSYNC/VREF	not used
VPA[2]	C_B[2]	Y_0[2]	C_R[2]	Y_1[2]	VPB[2]	C_B[6]	Y_0[6]	C_R[6]	Y_1[6]	DE/FREF	not used
VPA[3]	C_B[3]	Y_0[3]	C_R[3]	Y_1[3]	VPB[3]	C_B[7]	Y_0[7]	C_R[7]	Y_1[7]		
VPA[4]	-	-	-	-	VPB[4]	C_B[8]	Y_0[8]	C_R[8]	Y_1[8]		
VPA[5]	-	-	-	-	VPB[5]	C_B[9]	Y_0[9]	C_R[9]	Y_1[9]		
VPA[6]	-	-	-	-	VPB[6]	C_B[10]	Y_0[10]	C_R[10]	Y_1[10]		
VPA[7]	-	-	-	-	VPB[7]	C_B[11]	Y_0[11]	C_R[11]	Y_1[11]		

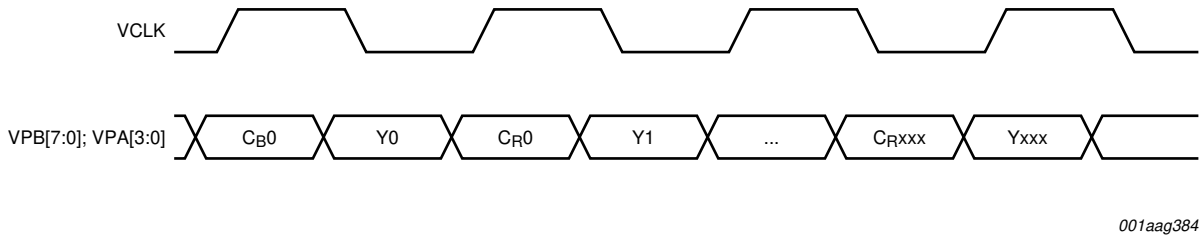


Fig 8. Pixel encoding YC_BC_R 4 : 2 : 2 ITU656-like embedded synchronization double edge (rising and falling) input

Table 12. YC_BC_R 4 : 2 : 2 semi-planar external synchronization mappings

YC_BC_R 4 : 2 : 2 semi-planar external synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	C_B[4]	C_R[4]	HSYNC/HREF	used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	C_B[5]	C_R[5]	VSYNC/VREF	used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	C_B[6]	C_R[6]	DE/FREF	used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	C_B[7]	C_R[7]		
VPA[4]	C_B[0]	C_R[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	C_B[8]	C_R[8]		
VPA[5]	C_B[1]	C_R[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	C_B[9]	C_R[9]		
VPA[6]	C_B[2]	C_R[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	C_B[10]	C_R[10]		
VPA[7]	C_B[3]	C_R[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	C_B[11]	C_R[11]		

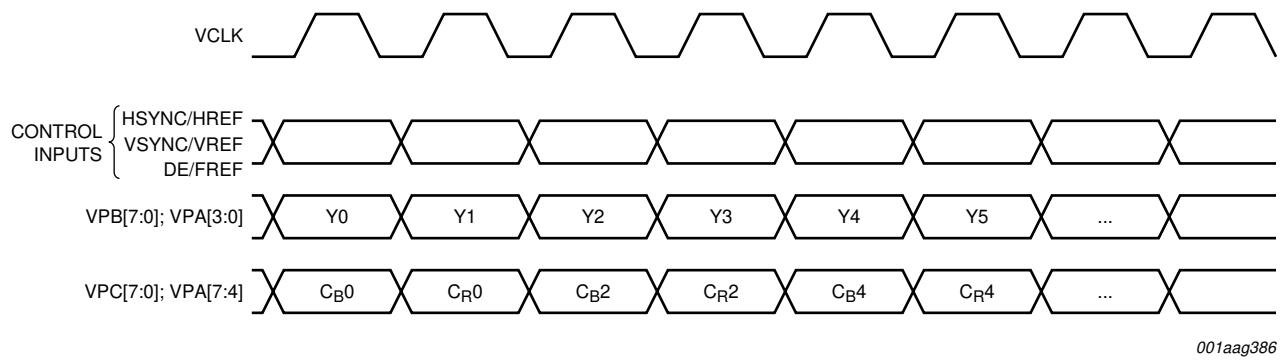


Fig 9. Pixel encoding YC_BC_R 4 : 2 : 2 semi-planar external synchronization (rising edge) input

Table 13. YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization mappings

YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization single edge.
Register VIP_CNTRL_0 = 23h; VIP_CNTRL_1 = 50h; VIP_CNTRL_2 = 14h.

Video port A			Video port B			Video port C			Control	
Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2 semi-planar		Pin	YC_BC_R 4 : 2 : 2
VPA[0]	Y_0[0]	Y_1[0]	VPB[0]	Y_0[4]	Y_1[4]	VPC[0]	C_B[4]	C_R[4]	HSYNC/HREF	not used
VPA[1]	Y_0[1]	Y_1[1]	VPB[1]	Y_0[5]	Y_1[5]	VPC[1]	C_B[5]	C_R[5]	VSYNC/VREF	not used
VPA[2]	Y_0[2]	Y_1[2]	VPB[2]	Y_0[6]	Y_1[6]	VPC[2]	C_B[6]	C_R[6]	DE/FREF	not used
VPA[3]	Y_0[3]	Y_1[3]	VPB[3]	Y_0[7]	Y_1[7]	VPC[3]	C_B[7]	C_R[7]		
VPA[4]	C_B[0]	C_R[0]	VPB[4]	Y_0[8]	Y_1[8]	VPC[4]	C_B[8]	C_R[8]		
VPA[5]	C_B[1]	C_R[1]	VPB[5]	Y_0[9]	Y_1[9]	VPC[5]	C_B[9]	C_R[9]		
VPA[6]	C_B[2]	C_R[2]	VPB[6]	Y_0[10]	Y_1[10]	VPC[6]	C_B[10]	C_R[10]		
VPA[7]	C_B[3]	C_R[3]	VPB[7]	Y_0[11]	Y_1[11]	VPC[7]	C_B[11]	C_R[11]		

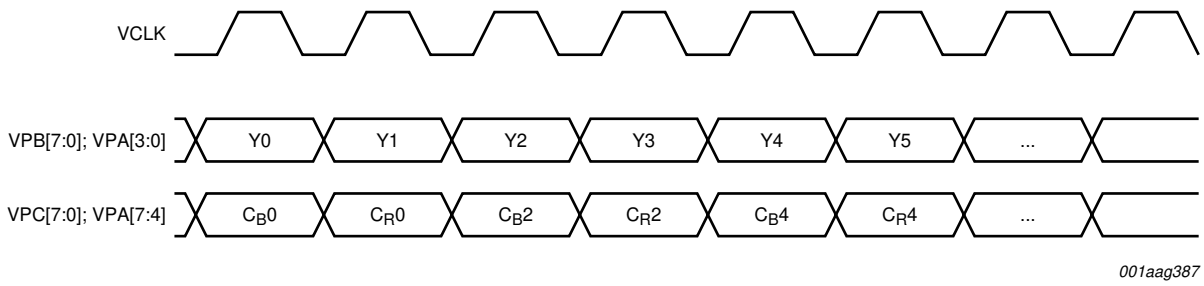


Fig 10. Pixel encoding YC_BC_R 4 : 2 : 2 semi-planar embedded synchronization (rising edge) input

8.3 Synchronization

The TDA9983B can be synchronized with Hsync/Vsync external inputs or with extraction of the sync information from embedded sync (SAV/EAV) codes inside the video stream.

8.3.1 Timing extraction generator

This block can extract the synchronization signals Href, Vref and Fref from Start Active Video (SAV) and End Active Video (EAV) in case of embedded synchronization in the data stream. Synchronization signals can be embedded in RGB, YC_BC_R 4 : 4 : 4, YC_BC_R 4 : 2 : 2 semi-planar (up to 2 × 12-bit), YC_BC_R 4 : 2 : 2 ITU656 and ITU656-like (up to 1 × 12-bit).

8.3.2 Data enable generator

The TDA9983B contains a Data Enable (DE) generator; this can generate an internal DE signal for a system which does not provide one.

8.4 Input and output video format

Due to the flexible video input formatter, the TDA9983B can accept a large range of input formats. This flexibility allows the TDA9983B to be compatible with the maximum possible number of MPEG decoders. Moreover, these input formats may be changed in many ways (color space converter, upsampler, downsampler and scaler) to be transmitted across the HDMI link. Table 14 gives the possible inputs and outputs.

Table 14. Use of color space converter, upsampler, downsampler and scaler

Input			Scaler	Output		
Color space	Format	Channels		Color space	Format	Channels
RGB	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
			no scaling	YC_BC_R	4 : 2 : 2	2 × 12-bit
			no scaling	YC_BC_R	4 : 4 : 4	3 × 8-bit
YC_BC_R	4 : 4 : 4	3 × 8-bit	no scaling	RGB	4 : 4 : 4	3 × 8-bit
			no scaling	YC_BC_R	4 : 2 : 2	2 × 12-bit
			no scaling	YC_BC_R	4 : 4 : 4	3 × 8-bit
YC_BC_R	4 : 2 : 2	up to 1 × 12-bit	scalable	YC_BC_R	4 : 2 : 2	2 × 12-bit
			scalable	YC_BC_R	4 : 4 : 4	3 × 8-bit
			scalable	RGB	4 : 4 : 4	3 × 8-bit
		up to 2 × 12-bit	scalable	YC_BC_R	4 : 2 : 2	2 × 12-bit
			scalable	YC_BC_R	4 : 4 : 4	3 × 8-bit
			scalable	RGB	4 : 4 : 4	3 × 8-bit

8.5 Upsampler

The incoming YC_BC_R 4 : 2 : 2 (2 × 12-bit) data stream format could be upsampled into a 12-bit YC_BC_R 4 : 4 : 4 (3 × 12-bit) data stream by repeating or linearly interpolating the chrominance pixels.

8.6 Color space converter

The color space converter is used to convert input video data from one type to another color space (RGB to YC_BC_R and YC_BC_R to RGB). This block can be bypassed and each coefficient is programmable via the I²C-bus register.

$$\begin{bmatrix} Y\backslash G \\ C_B\backslash R \\ C_R\backslash B \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{bmatrix} \times \left(\begin{bmatrix} G\backslash Y \\ R\backslash C_B \\ B\backslash C_R \end{bmatrix} + \begin{bmatrix} Oin_{G\backslash Y} \\ Oin_{R\backslash C_B} \\ Oin_{B\backslash C_R} \end{bmatrix} \right) + \begin{bmatrix} Oout_{Y\backslash G} \\ Oout_{C_B\backslash R} \\ Oout_{C_R\backslash B} \end{bmatrix}$$

8.7 Downsampler

This block works only with YC_BC_R input format; these filters downsample the C_B and C_R signals by a factor 2. A delay is added on the G/Y channel, which corresponds to the pipeline delay of the filters, to put the Y channel in phase with the C_B-C_R channels.

8.8 Audio input format

The TDA9983B is compatible with HDMI 1.2a (DVD support). The TDA9983B can carry audio in I²S-bus format (one stereo up to four stereo channels) or in S/PDIF format. S/PDIF or I²S-bus format can be selected via the I²C-bus. Only one audio format can be used at a time: either S/PDIF or I²S-bus. Table 15 shows the audio port allocation.

Table 15. Audio port configuration

All audio ports are LV-TTL compatible.

Audio port	I²S-bus and S/PDIF input configuration
AP0	WS (word select)
AP1	I²S-bus audio port 0
AP2	I²S-bus audio port 1
AP3	I²S-bus audio port 2
AP4	I²S-bus audio port 3
AP5	MCLK (master clock for S/PDIF)
AP6	S/PDIF input
AP7	AUX (internal test)
ACLK	SCK (I²S-bus clock)

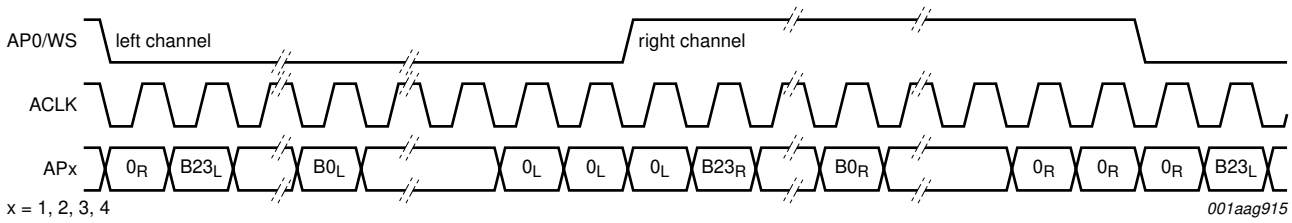
8.9 S/PDIF

The audio port AP6 is used for the S/PDIF feature. In this format the TDA9983B supports 2-channel uncompressed PCM data (IEC 60958) layout 0 or compressed bit stream up to 8 multichannels (Dolby Digital, DTS, AC-3, etc.) layout 1. The TDA9983B is able to recover the original clock from the S/PDIF signal (no need for an external clock). In addition it can also use an external clock (MCLK) to decode the S/PDIF signal.

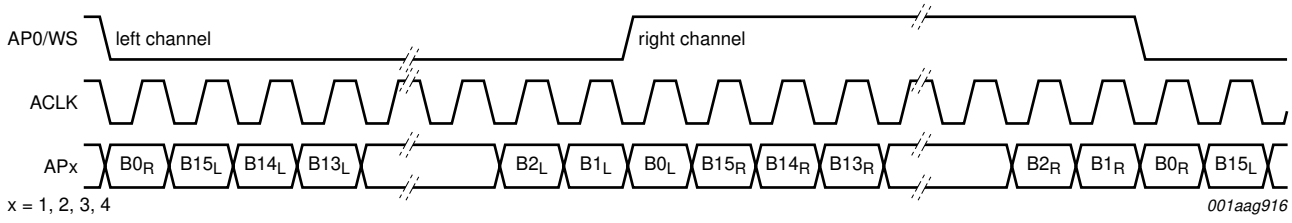
8.10 I²S-bus

The TDA9983B supports the NXP I²S-bus format. There are four I²S-bus stereo input channels (AP1 to AP4), which enable 8 uncompressed audio channels to be carried. The I²S-bus input interface receives an I²S-bus signal including serial data, word select and

serial clock. Various I²S-bus formats are supported and can be selected by setting the appropriate bits of the register. The I²S-bus input interface can receive up to 24-bit wide audio samples via the serial data input with a clock frequency of at least 32 times the input sample frequency f_s. Since the I²S-bus format is MSB aligned, audio data with an arbitrary precision can be received automatically. Audio samples with a precision better than 24 bits are truncated to 24 bits. If the input clock has a frequency of $32 \times f_s$, only 16-bit audio samples can be received. In this case, the 8 LSBs will be set to logic 0. The serial data signal carries the serial baseband audio data, sample by sample left/right interleaved. The word select signal WS indicates whether left or right channel information is transferred over the serial data line. The formats for 16-bit and 32-bit modes are shown in Figure 11.



a. 32-bit mode



b. 16-bit mode

Fig 11. NXP I²S-bus formats

8.11 Power management

The TDA9983B can be powered down via the I²C-bus register.

8.12 Interrupt controller

Pin INT is used to alert the microcontroller that a critical event concerning the HDMI has occurred (hot plug detect). This interrupt is maskable.

Hot plug or unplug detect: pin HPD is the hot plug detection pin; it is 5 V input tolerant.

8.13 Initialization

Hard reset: after power-up, the TDA9983B is activated by a hard reset via pin RST_N. However, the TDA9983B has a power-on reset.

8.14 HDMI

8.14.1 Output HDMI buffers

An external resistor must be used to set the HDMI output amplitude. It has to be connected between pin EXT_SWING and $V_{DDH(3V3)}$.

8.14.2 Pixel repetition

To transmit video formats with pixel rates below 25 Msample/s or to increase the number of audio sample packets in each frame, the TDA9983B uses pixel repetition to increase the transmitted pixel clock.

Table 16. Pixel repetition

SRL_PR[3]	SRL_PR[2]	SRL_PR[1]	SRL_PR[0]	Pixel repeated
0	0	0	0	no repetition
0	0	0	1	once
0	0	1	0	twice
0	0	1	1	3 times
0	1	0	0	4 times
0	1	0	1	5 times
0	1	1	0	6 times
0	1	1	1	7 times
1	0	0	0	8 times
1	0	0	1	9 times
1	0	1	x	undefined
1	1	x	x	undefined

8.14.3 HDMI and DVI receiver discrimination

This information is located in the E-EDID receiver part, in the ‘Vendor-Specific Data block’ within the first CEA EDID timing extension. If the 24-bit IEEE registration identifier contains the value 00 0C03h, then the receiver will support HDMI, otherwise the device will be treated as a DVI device. However, the TDA9983B does not have direct access to that information since E-EDID is read by an external microprocessor through the TDA9983B I^2C-bus gate.

8.14.4 DDC channel

The DDC-bus pins DDC_SDA and DDC_SCL are 5 V tolerant and can work at standard mode (100 kHz).

8.14.4.1 E-EDID reading

In order to get receiver capabilities, the TDA9983B must read the E-EDID of the receiver. This is made possible by temporarily connecting the I^2C-bus to the DDC lines, so that the microprocessor is able to read full EDID.

8.15 Scaler unit

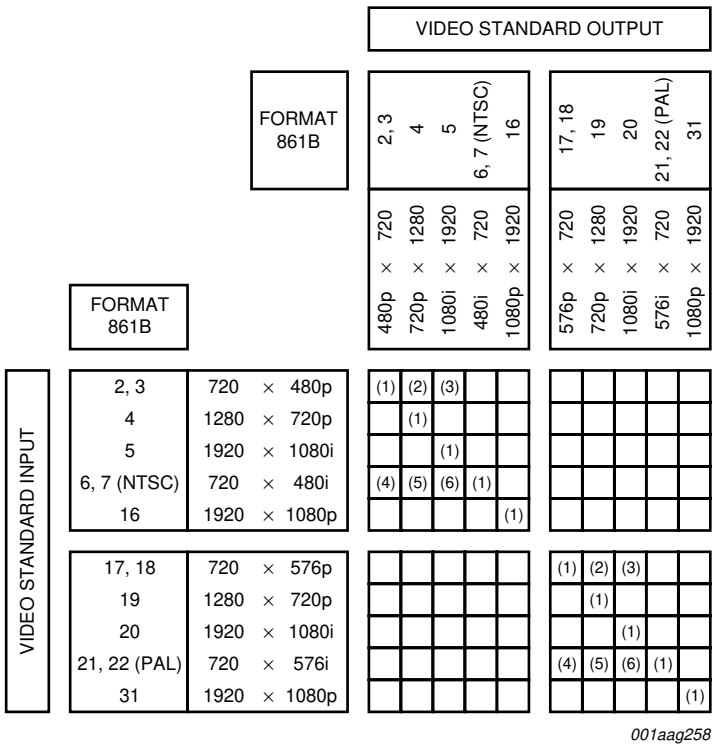
The scaler unit has the following features:

- Upscaling only: to expand input image horizontally and vertically

- Embedded deinterlacer (no need for output memory)
- Maximum output operating frequency: 74.5 MHz (HDTV supported 1080i, 720p)
- Input video standards (YC_BC_R 4 : 2 : 2 semi-planar, ITU656 and ITU656-like YC_BC_R, no RGB and no YC_BC_R 4 : 4 : 4)

8.16 Input and output video scaler

The scaler converts the standard definition video signals (480i/576i, 480p/576p) into 720p, 1080i as illustrated in Figure 12.



All upscaling modes are available only for YC_BC_R 4 : 2 : 2 input format.

(1) Pass through
(2) Upscaling
(3) Upscaling and interlacing
(4) Deinterlacing
(5) Deinterlacing and upscaling
(6) Deinterlacing, upscaling and interlacing

Fig 12. Input and output video scaler

8.17 I²C-bus interface

The I²C-bus pins I2C_SDA and I2C_SCL are 5 V tolerant and can work at fast mode (400 kHz).

9. I²C-bus register definitions

9.1 I²C-bus protocol

The registers of the TDA9983B can be accessed via the I²C-bus. The TDA9983B is used as a slave device and both the fast mode 400 kHz and the standard mode 100 kHz are supported.

Bits A0 and A1 of the I²C-bus device address are externally selected by pins A0 and A1. The I²C-bus device address is given in Table 17.

Table 17. Device address

Device address							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	-
1	1	1	0	0	A1	A0	1/0

The I²C-bus access format is shown in Figure 13.

For read access, the master writes the address of the TDA9983B, the subaddress to access the specific register and then the data.

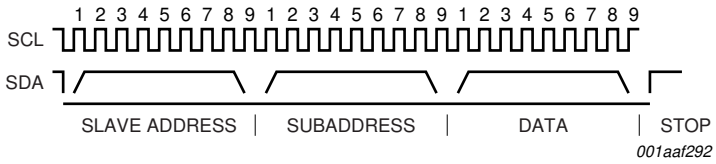


Fig 13. I²C-bus access

9.2 Memory page management

The I²C-bus memory is split into several pages and the selection between pages is made with common register CURPAGE_ADR. It is only necessary to write in this register once to change the current page. So multiple read or write operations in the same page need a write register CURPAGE_ADR once at the beginning.

Table 18. Memory pages

Page address	Memory page description	Reference
00h	General control	see Section 9.3 on page 23
01h	Scaler	see Section 9.4 on page 43
02h	PLL settings	see Section 9.5 on page 55
10h	Information frames and packets	see Section 9.6 on page 63
11h	Audio settings and content info packets	see Section 9.7 on page 81
12h	HDMI and DVI	see Section 9.8 on page 98

9.3 General control page register definitions

The current page address for the general control page is 00h.

The configuration of the registers for this page is given in Table 19.

Table 19. I²C-bus registers of memory page 00h[1]

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
VERSION	00h	R	0	1	1	0	0	0	1	0	0110 0010
MAIN_CNTRL0	01h	W	SCALER	x	x	CEHS	CECS	DEHS	DECS	SR	0000 0000
Not used	02h	-	-								0000 0000
:	:	:	:								:
Not used	0Eh	-	-								0000 0000
INT_FLAGS_0	0Fh	R/W	x	x	x	x	x	x	HPD	x	0000 0000
INT_FLAGS_1	10h	R/W	HPD_IN	x	SC_DEIL	SC_VID	SC_OUT	SC_IN	x	VS_RPT	0000 0000
Not used	11h	-	-								0000 0000
:	:	:	:								:
Not used	1Fh	-	-								0000 0000
VIP_CNTRL_0	20h	W	MIRR_A	SWAP_A[2:0]			MIRR_B	SWAP_B[2:0]			0000 0001
VIP_CNTRL_1	21h	W	MIRR_C	SWAP_C[2:0]			MIRR_D	SWAP_D[2:0]			0010 0100
VIP_CNTRL_2	22h	W	MIRR_E	SWAP_E[2:0]			MIRR_F	SWAP_F[2:0]			0101 0110
VIP_CNTRL_3	23h	W	EDGE	x	SP_SYNC[1:0]		EMB	V_TGL	H_TGL	X_TGL	0001 0110
VIP_CNTRL_4	24h	W	TST_PAT	TST_656	x	CCIR656	BLANKIT[1:0]		BLC[1:0]		0000 0001
VIP_CNTRL_5	25h	W	x	x	x	x	x	SP_CNT[1:0]		CKCASE	0000 0000
Not used	26h	-	-								0000 0000
:	:	:	:								:
Not used	7Fh	-	-								0000 0000
MAT_CONTRL	80h	W	x	x	x	x	x	MAT_BP	MAT_SC[1:0]		0000 0101
MAT_OI1_MSB	81h	W	x	x	x	x	x	OFFSET_IN1[10:8]			0000 0000
MAT_OI1_LSB	82h	W	OFFSET_IN1[7:0]								0000 0000
MAT_OI2_MSB	83h	W	x	x	x	x	x	OFFSET_IN2[10:8]			0000 0110
MAT_OI2_LSB	84h	W	OFFSET_IN2[7:0]								0000 0000
MAT_OI3_MSB	85h	W	x	x	x	x	x	OFFSET_IN3[10:8]			0000 0110
MAT_OI3_LSB	86h	W	OFFSET_IN3[7:0]								0000 0000
MAT_P11_MSB	87h	W	x	x	x	x	x	P11[10:8]			0000 0010
MAT_P11_LSB	88h	W	P11[7:0]								0000 0000
MAT_P12_MSB	89h	W	x	x	x	x	x	P12[10:8]			0000 0110
MAT_P12_LSB	8Ah	W	P12[7:0]								1001 0010
MAT_P13_MSB	8Bh	W	x	x	x	x	x	P13[10:8]			0000 0111
MAT_P13_LSB	8Ch	W	P13[7:0]								0101 0000

Table 19. I²C-bus registers of memory page 00h[1] …continued

Register	Sub addr	R/W	Bit								Default value
			7 (MSB)	6	5	4	3	2	1	0 (LSB)	
MAT_P21_MSB	8Dh	W	x	x	x	x	x	P21[10:8]			0000 0010
MAT_P21_LSB	8Eh	W	P21[7:0]								0000 0000
MAT_P22_MSB	8Fh	W	x	x	x	x	x	P22[10:8]			0000 0010
MAT_P22_LSB	90h	W	P22[7:0]								1100 1110
MAT_P23_MSB	91h	W	x	x	x	x	x	P23[10:8]			0000 0000
MAT_P23_LSB	92h	W	P23[7:0]								0000 0000
MAT_P31_MSB	93h	W	x	x	x	x	x	P31[10:8]			0000 0010
MAT_P31_LSB	94h	W	P31[7:0]								0000 0000
MAT_P32_MSB	95h	W	x	x	x	x	x	P32[10:8]			0000 0000
MAT_P32_LSB	96h	W	P32[7:0]								0000 0000
MAT_P33_MSB	97h	W	x	x	x	x	x	P33[10:8]			0000 0011
MAT_P33_LSB	98h	W	P33[7:0]								1000 1100
MAT_OO1_MSB	99h	W	x	x	x	x	x	OFFSET_OUT1[10:8]			0000 0000
MAT_OO1_LSB	9Ah	W	OFFSET_OUT1[7:0]								0000 0000
MAT_OO2_MSB	9Bh	W	x	x	x	x	x	OFFSET_OUT2[10:8]			0000 0000
MAT_OO2_LSB	9Ch	W	OFFSET_OUT2[7:0]								0000 0000
MAT_OO3_MSB	9Dh	W	x	x	x	x	x	OFFSET_OUT3[10:8]			0000 0000
MAT_OO3_LSB	9Eh	W	OFFSET_OUT3[7:0]								0000 0000
Not used	9Fh	-	-	-	-	-	-	-	-	-	0000 0000
VIDFORMAT	A0h	W	x	x	x	VIDFORMAT[4:0]					0000 0000
REFPIX_MSB	A1h	W	x	x	x	PRESET_PIX[12:8]					0000 0000
REFPIX_LSB	A2h	W	PRESET_PIX[7:0]								0000 0001
REFLINE_MSB	A3h	W	x	x	x	x	x	PRESET_LINE[10:8]			0000 0000
REFLINE_LSB	A4h	W	PRESET_LINE[7:0]								0000 0001
NPIX_MSB	A5h	W	x	x	x	NPIX[12:8]					0000 0000
NPIX_LSB	A6h	W	NPIX[7:0]								0000 0000
NLINE_MSB	A7h	W	x	x	x	x	x	NLINE[10:8]			0000 0000
NLINE_LSB	A8h	W	NLINE[7:0]								0000 0000
VS_LINE_STRT_1_MSB	A9h	W	x	x	x	x	x	VS_LINE_START_1[10:8]			0000 0000
VS_LINE_STRT_1_LSB	AAh	W	VS_LINE_START_1[7:0]								0000 0000
VS_PIX_STRT_1_MSB	ABh	W	x	x	x	VS_PIX_START_1[12:8]					0000 0000
VS_PIX_STRT_1_LSB	ACh	W	VS_PIX_START_1[7:0]								0000 0000