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TDC-GPX

Ultra-high Performance 8 Channel
Time-to-Digital Converter

Datasheet

JAN 18TH , 2007

acam - solutions in time

Precision Time Interval Measurement

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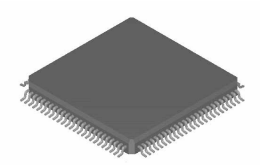
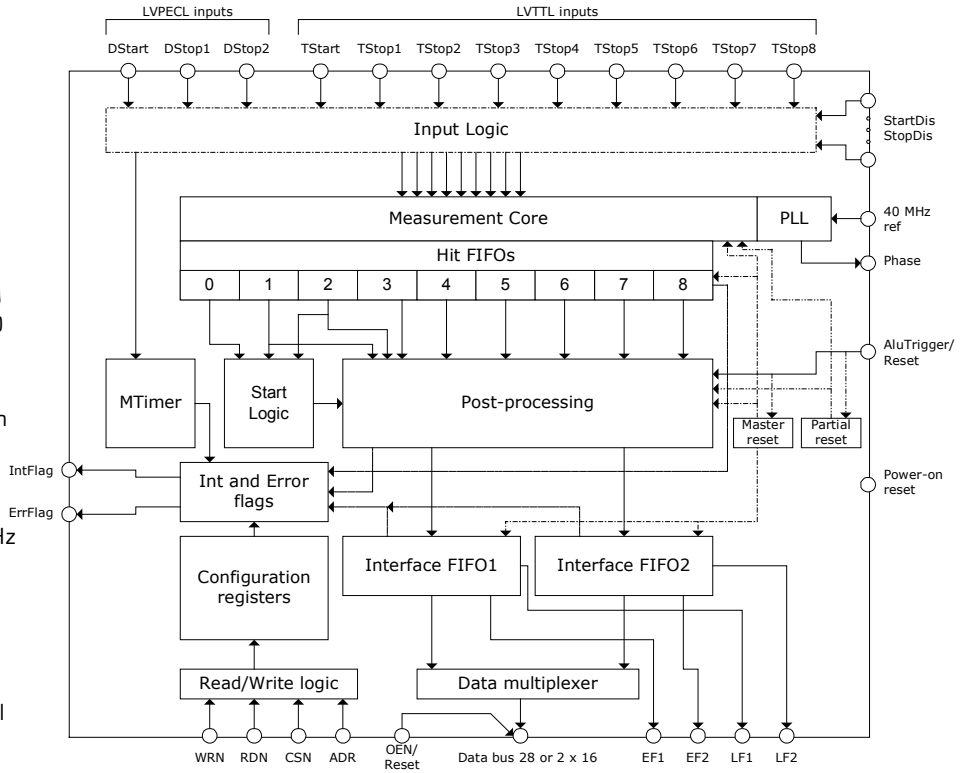
1. Introduction

1.1 System overview



TQFP100

TFBGA120



I-Mode

- 8 channels with typ. 81 ps resolution
- 9 LVTTL inputs, optional 3 LVPECL inputs
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Measurement range 9,8 µs, endless measurement range by internal retrigger of START
- 10 MHz continuous rate per channel
- 40 MHz continuous rate per chip

G-Mode

- 2 channels with 40 ps resolution
- Differential LVPECL inputs, optional LVTTL
- Measurement range 0 ns to 65 µs
- 5.5 ns pulse-pair resolution between edges of equal slope with 32-fold multi-hit = 182 MHz peak rate
- Minimum pulse width 1.5 ns
- Trigger to rising **and** falling edge
- Optional Quiet Mode (no ALU operation and Data-output during measurements)
- 20 MHz continuous rate per channel
- 40 MHz continuous rate per chip

R-Mode

- 2 channels with 27 ps resolution
- Differential LVPECL inputs, optional LVTTL
- Measurement range 0 µs up to 40 µs
- 5.5 ns pulse-pair resolution with 32-fold multi-hit capability = 182 MHz peak rate
- Trigger to rising or falling edge
- Optional Quiet Mode (no ALU operation and Data-output during measurements)
- 40 MHz continuous rate per channel
- 40 MHz continuous rate per chip

M-Mode

- 2 channels with 10 ps resolution (70 ps peak-peak)
- Differential LVPECL inputs
- Measurement range 0 ns up to 10 µs
- Single hit per Start and channel
- Trigger to rising or falling edge
- Quiet Mode (no ALU operation and Data-output during measurements)
- Max. 500 kHz continuous rate per channel
- Max. 1 MHz continuous rate per chip

General

- Start retrigger option (besides M-Mode)
- Packages: TQFP100, TFBGA120
- IO voltage 3.0 V – 3.6 V
- Core voltage 2.3 V – 3.6 V regulated by resolution adjust unit
- Data bus: 28 Bit or 2 x 16 Bit asynchronous with Chipselect, Readstrobe, Writestrobe
- 40 MHz continuous rate per chip
- Address range: 4 Bit

1.2 Index

1.3 Electrical Characteristics

Absolute Maximum Ratings (Vss = 0V, Tj = 25°C)

Parameter		Symbol	Condition	Rated Value	Unit
Supply voltage	I/O	Vddo		-0.3 to +3.6	V
	Core	Vddc	Vdcc < Vddo + 0.6V	-0.3 to +3.6	
	Hardmacro	Vddc-h	Vdcc < Vddo + 0.6V	-0.3 to +3.6	
	Oscillator	Vddc-o	Vdcc < Vddo + 0.6V	-0.3 to +3.6	
	Diff. inputs	Vdde		-0.3 to +3.6	
Input voltage	5V Tolerant Buffers	Vi	Vddo = +0.3~3.6V	-0.3 to 6.0	V
Output current	1 mA Buffer	Io	-	-5 to +5	mA
	4 mA Buffer			-9 to +9	
Storage temperature		Tstg		-65 to 150	°C
Junction temperature		Tj		-40 to 125	°C
Thermal resistance	junction-ambient	R_{thj-a}	TQFP100	96	K/W
			TFBGA120	105	

Terminal Capacitance

Terminal	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
Input	Ci	measured @Vdd = Vi = Vo = Vss, f = 1 MHz, Ta = 25°C	-	6	-	pF
Output	Co		-	9	-	
Bidirectional	Cio		-	10	-	

DC Characteristics (Vddo = 3.3 V ± 0.3 V, Vss = 0 V, Tj = -40 to +85°C)

Parameter	Symbol	Condition	Rated Value			Unit
			Min	Typ	Max	
High-level input voltage	Vih	TTL 5V tolerant input	2.0	-	5.5	V
Low-level input voltage	Vil	TTL 5V tolerant input	0.0	-	0.8	
High-level output voltage	Voh		2.4			
Low-level output voltage	Vol				0.4	
Supply current			Typ			mA
	Vddo	I/O	1.4 + Bus			
	Vddc	Core	20			
	Vddc-h	Hardmacro	7			
	Vddc-o	Oscillator	4			
	Vdde	Diff. inputs	19			

LVPECL inputs:

DC Parameters (VDD = 3.3 V±5 %, Tj = 0°C to 125°C)

Parameter	Val	Condition
VinOS	Vdde-1.53V < VinOS < Vdde-0.89V	-
VinDF	0.2V < VinDF < 2.1V	-

VinOS = Input offset voltage, (Via+Vian)/2
VinDF = Input differential voltage,
Via = Input voltage of A
Vian = Input voltage of AN

1.3.1 Bus Timings

(Vddo = Vddc = 3.3 V, Ta = +25°C)

Write operations

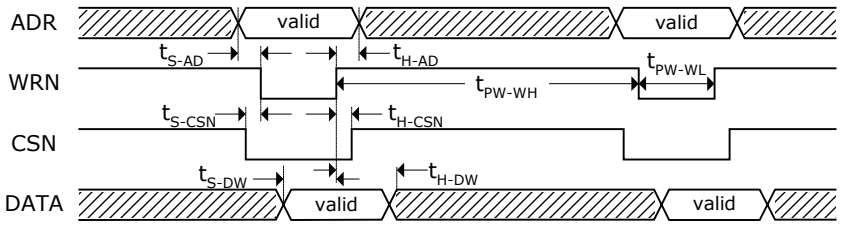


Figure 1

Spec	Description	Min (ns)	Max (ns)
t_{S-AD}	Address Setup Time	2	-
t_{H-AD}	Address Hold Time	0	-
t_{PW-WL}	Write LOW Time	6	-
t_{PW-WH}	Write HIGH Time	6	-
t_{S-DW}	Write Data Setup Time	5	-
t_{H-DW}	Write Data Hold Time	4	-
t_{S-CSN}	Chip Select Setup Time	0	-
t_{H-CSN}	Chip Select Hold Time	0	-

Read Operations

It is not allowed to read from an empty FIFO !

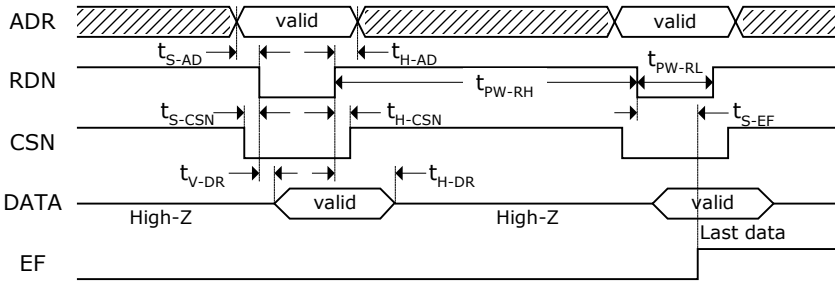


Figure 2

Spec	Description	Min (ns)	Max (ns)	
t_{S-AD}	Address Setup Time	2	-	* @ 87ps res. & 40pF load. This value depends on the capacitive load and has to be confirmed by evaluation. This value also depends on the adjusted resolution (e.g)
t_{H-AD}	Address Hold Time	0	-	
t_{PW-RL}	Read LOW Time	6	-	
t_{PW-RH}	Read HIGH Time	6	-	
t_{V-DR}	Read Data Valid Time	5	11.8*	
t_{H-DR}	Read Data Hold Time	4	8.5**	** Can be prolonged infinitely with OEN = 0 (driving the bus permanently) and stable address.
t_{S-CSN}	Chip Select Setup Time	0	-	
t_{H-CSN}	Chip Select Hold Time	0	-	
t_{S-EF}	Empty Flag Set Time	-	11.8*	

OEN operations – Driving the bus permanently

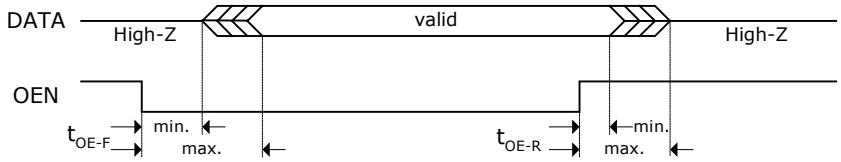


Figure 3

Spec	Description	Min (ns)	Max (ns)
t_{OE-F}	OEN Rise to Data Valid	1.5	9
t_{OE-R}	OEN Fall to Data Valid	1	8.5

Note: With OEN = Low the output buffers are driving allthe time, with OEN = High they are driving only during a read strobe. While writing to the TDC-GPX OEN has to be High.

Fake Reads for speeding up data readout

The maximum data readout rate is limited by the empty flag set time as it is not allowed to read from an empty FIFO. This can be overcome by a second fake read strobe which is delayed to the read strobe at the TDC-GPX.

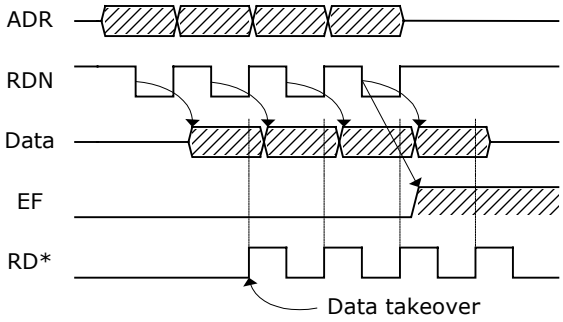


Figure 4

1.3.2 16 Bit Mode

The TDC-GPX data bus can be switched from 28 Bit to 16 Bit. This is done writing a 0x0000010 to address 14. After that all read / write commands have to be done in pairs. When reading the last data from an interface FIFO the empty flag disappears already with the first read command. Nonetheless it is mandatory to read a second time.

The first read/write command always refers to the LSW, the second one to the MSW. The highest 4 Bit of the MSW are not relevant (write) or shall be ignored (read).

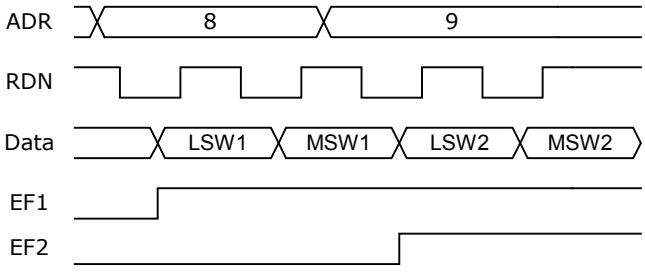


Figure 5

Note: See Bug-Report 01 at the end of the datasheet

1.3.3 Disable Timings

Disable inputs (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)	Max (ns)
t_{S1-DH}	Disable Setup Time	-	6
t_{S2-DH}	Disable Setup Time	-	1
t_{S1-DL}	Disable Hold Time	-	0
t_{S2-DL}	Disable Hold Time	-	2

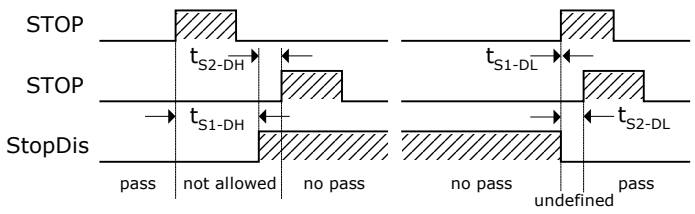


Figure 6

StopDisStart (Bit 21, register 5) @ 87 ps resolution

Spec	Description	Min (ns)	Max (ns)
t_{S1-DH}	Dead Time Rising(Start) to Rising(Stop)	-	6.3
t_{S2-DH}	Dead Time Falling(Start) to Rising(Stop)	-	6.1
t_{S1-DL}	Dead Time Rising(Start) to Falling(Stop)	-	5.2
t_{S2-DL}	Dead Time Falling (Start) to Falling (Stop)	-	7.4

1.3.4 Reset Timings

Power-up Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)	Max (ns)
t_{ph}	Reset pulse width	200	-

Master Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)
t_{ph}	Reset pulse width	10
t_{rfs}	Time after rising edge of reset pulse before hits are accepted	27
t_{rrs}	Time after falling edge of reset pulse before hits are accepted	13

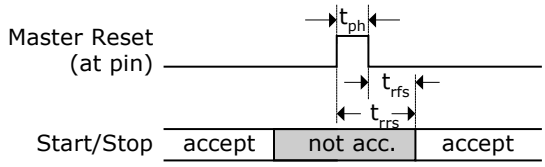


Figure 7

Partial Reset: (Vddo = Vddc = 3.3 V, Ta = +25°C)

Spec	Description	Min (ns)
t_{ph}	Reset pulse width	10
t_{rfs}	Time after rising edge of reset pulse before hits are accepted	60
t_{rrs}	Time after falling edge of reset pulse before hits are accepted	13
t_{rs}	Time berfore rising edge of reset pulse where hits will be lost	-

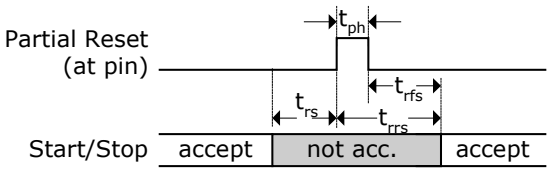


Figure 8

1.3.5 General Timings & Resolution

The TDC-GPX time measurement is based on internal propagation delays. Those delays depend on temperature and voltage. They also vary over the production lots. The resolution adjust mode (see) uses the voltage dependency to compensate for temperature and production variations and sets the circuits to a fixed and programmable resolution.

Figure 9 shows the dependency of all timings from the core voltage, referred to the 3.3V timings. The resolution at 3.3V can be varied by factors 0.93 at 3.6V to 1.4 at 2.3V.

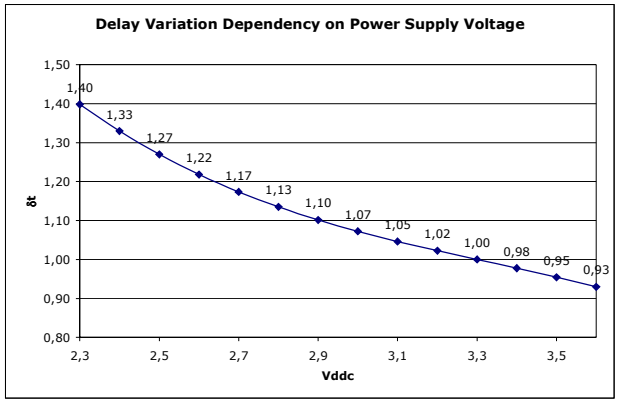


Figure 9

Figure 10 shows the dependency of all timings on the temperature, referred to 25°C junction temperature. If the temperature increases from 25°C to 70°C, the intrinsic resolution goes down by a factor 1.077. In resolution adjust mode this is compensated by increasing the core voltage from 3.3V to 3.6V.

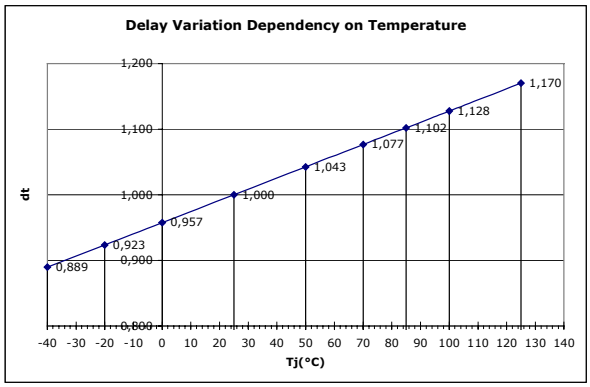


Figure 10

Without resolution adjust, the intrinsic resolution varies slightly from chip to chip. The distribution over the production lots is of gaussian type.

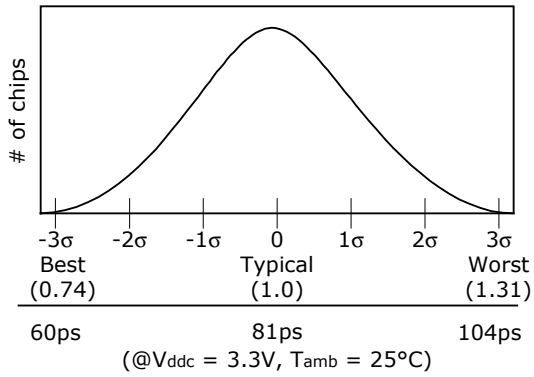


Figure 11

Within a single production lot the distribution is narrower. Figure 12 shows a typical distribution of the intrinsic resolution at 3.3 V core voltage and 25°C ambient temperature within a single production lot.

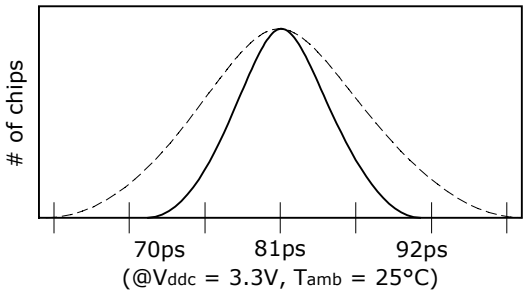


Figure 12

Example:

Taking the distribution from Figure 12 and assuming an operating temperature range of 0°C to 40°C as well as 1 Mhz data rate. The junction temperature will be about 57°C max. The slowest chips will have 92ps * 1.043 = 97ps resolution at 3.3V Vddc. Increasing the core voltage to 3.6V will speed them up to 90.2ps. Setting the resolution adjust mode to a resolution of 95ps will guarantee that the PLLs of all chips will lock at one and the same resolution over the whole operating temperature range.

1.4 Pin Description

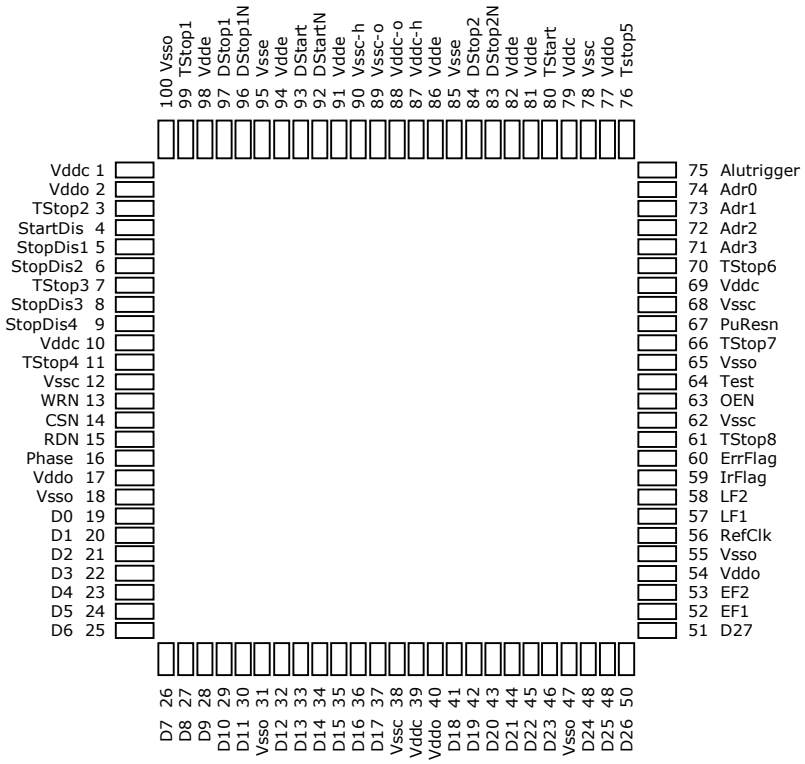


Figure 13

PIN No TQFP 100	PIN No TFBGA 120	PIN Name	Description	Type	Terminal () = if not used
001	A1	Vddc	Core supply voltage		Vddc
002	B1	Vddo	I/O supply voltage		Vddo
003	C1	Tstop2	TTL input 'Stop2'	TTL input	(10kΩ to GND)
004	C2	StartDis	Disable input 'DStart' or 'TStart'	TTL input	(GND)
005	D1	StopDis1	Disable input 'DStop1' or inputs 'TStop1 ' and 'TStop2'	TTL input	(GND)
006	C3	StopDis2	Disable input 'DStop2' or inputs 'TStop3 ' and 'TStop4'	TTL input	(GND)
007	D2	TStop3	TTL input Stop3	TTL input	(10kΩ to GND)
008	E1	StopDis3	Disable inputs 'TStop5 ' and 'TStop6'	TTL input	(GND)
009	D3	StopDis4	Disable or inputs 'TStop7 ' and 'TStop8'	TTL input	(GND)
010	F1	Vddc	Core supply voltage		Vddc
011	E3	TStop4	TTL input 'Stop4'	TTL input	(10kΩ to GND)
012	F2	Vssc	Core GND		GND
013	G1	WRN	Write (LOW active)	TTL input	
014	F3	CSN	Chip select (LOW active)	TTL input	(GND)
015	G2	RDN	Read (LOW active)	TTL input	
016	H1	Phase	Phase output PLL		

017	G3	Vddo	I/O supply voltage		Vddo
018	H2	Vsso	I/O GND		GND
019	J1	D0	Data 0	Bidirectional 4mA	10kΩ to GND
020	J2	D1	`	Bidirectional 4mA	10kΩ to GND
021	K1	D2	`	Bidirectional 4mA	10kΩ to GND
022	K2	D3	`	Bidirectional 4mA	10kΩ to GND
023	L1	D4	`	Bidirectional 4mA	10kΩ to GND
024	L2	D5	`	Bidirectional 4mA	10kΩ to GND
025	M1	D6	`	Bidirectional 4mA	10kΩ to GND
026	N2	D7	`	Bidirectional 4mA	10kΩ to GND
027	M2	D8	`	Bidirectional 4mA	10kΩ to GND
028	N3	D9	`	Bidirectional 4mA	10kΩ to GND
029	M3	D10	`	Bidirectional 4mA	10kΩ to GND
030	N4	D11	Data 11	Bidirectional 4mA	10kΩ to GND
031	M4	Vsso	I/O GND		GND
032	N5	D12	Data 12	Bidirectional 4mA	10kΩ to GND
033	L3	D13	`	Bidirectional 4mA	10kΩ to GND
034	M5	D14	`	Bidirectional 4mA	10kΩ to GND
035	N6	D15	`	Bidirectional 4mA	10kΩ to GND
036	M6	D16	`	Bidirectional 4mA	10kΩ to GND
037	N7	D17	Data 17	Bidirectional 4mA	10kΩ to GND
038	L5	Vssc	Core GND		GND
039	M7	Vddc	Core supply voltage		Vddc
040	L6	Vddo	I/O supply voltage		Vddo
041	M8	D18	Data 18	Bidirectional 4mA	10kΩ to GND
042	N9	D19	`	Bidirectional 4mA	10kΩ to GND
043	L7	D20	`	Bidirectional 4mA	10kΩ to GND
044	M9	D21	`	Bidirectional 4mA	10kΩ to GND
045	L8	D22	`	Bidirectional 4mA	10kΩ to GND
046	M10	D23	Data 23	Bidirectional 4mA	10kΩ to GND
047	L9	Vsso	I/O GND		
048	M11	D24	Data 24	Bidirectional 4mA	10kΩ to GND
049	N12	D25	`	Bidirectional 4mA	10kΩ to GND
050	L10	D26	`	Bidirectional 4mA	10kΩ to GND
051	M13	D27	Data 27	Bidirectional 4mA	10kΩ to GND
052	N13	EF1	Interface FIFO 1 empty flag, active HIGH	Output 4mA	
053	L13	EF2	Interface FIFO 2 empty flag, active HIGH	Output 4mA	
054	L12	Vddo	I/O supply voltage		Vddo
055	L11	Vsso	I/O GND		GND
056	K13	RefClk	Input reference clock	TTL input	
057	K12	LF1	Interface FIFO 1 load flag, active HIGH *	Output 1mA	
058	K11	LF2	Interface FIFO 2 load flag, active HIGH *	Output 1mA	
059	J13	IrFlag	Interrupt flag, active HIGH	Output 1mA	
060	J12	ErrFlag	Error flag, active HIGH	Output 1mA	
061	H13	Tstop8	TTL input ‚Stop8'	TTL input	(10kΩ to GND)
062	H12	Vssc	Core GND		GND
063	H11	OEN	Output enable, active LOW	TTL input	(10kΩ to Vddo)

* Valid only whileF13 it is not read

064	G11	Test	acam test input, connect it to GND !	TTL input	GND
065	F13	Vsso	I/O GND		GND
066	F12	Tstop7	TTL input ‚Stop7'	TTL input	(10kΩ to GND)
067	F11	PuResN	Power-up reset, low active	TTL input	
068	E13	Vssc	Core GND		GND
069	E12	Vddc	Core supply voltage		Vddc
070	D12	Tstop6	TTL input 'Stop6'	TTL input	(10kΩ to GND)
071	D13	Adr3	Address 3	TTL input	
072	E11	Adr2	Address 2	TTL input	
073	C13	Adr1	Address 1	TTL input	
074	C12	Adr0	Address 0	TTL input	
075	D11	AluTrigger	External ALU trigger	TTL input	(10kΩ to GND)
076	C11	Tstop5	TTL input 'Stop5'	TTL input	(10kΩ to GND)
077	A11	Vddo	I/O supply voltage		Vddo
078	C10	Vssc	Core GND		GND
079	B10	Vddc	Core supply voltage		Vddc
080	C9	Tstart	TTL input 'Start'	TTL input	(10kΩ to GND)
081	B9	Vdde	LVPECL supply voltage		Vdde
082	A9	Vdde	LVPECL supply voltage		Vdde
083	B8	DStop2N	Differential input 'Stop2' , neg	Differential input	(10kΩ to GND)
084	A8	DStop2	Differential input 'Stop2' , pos	Differential input	(10kΩ to GND)
085	C7	Vsse	LVPECL GND		GND
086	B7	Vdde	LVPECL supply voltage		Vdde
087	A7	Vddc-h	Hardmacro supply voltage		Vddc-h
088	C6	Vddc-o	Hardmacro supply voltage		Vddc-o
089	B6	Vssc-o	Hardmacro GND		GND
090	A6	Vssc-h	Hardmacro GND		GND
091	C5	Vdde	LVPECL supply voltage		Vdde
092	B5	DStartN	Differential input 'Start' , neg	Differential input	(10kΩ to GND)
093	A5	DStart	Differential input 'Start' , pos	Differential input	(10kΩ to GND)
094	C4	Vdde	LVPECL supply voltage		Vdde
095	B4	Vsse	LVPECL GND		GND
096	A4	Dstop1N	Differential input 'Stop1' , neg	Differential input	(10kΩ to GND)
097	B3	Dstop1	Differential input 'Stop1' , pos	Differential input	(10kΩ to GND)
098	A3	Vdde	LVPECL supply voltage		Vdde
099	B2	TStop1	TTL input 'Stop1'	TTL input	(10kΩ to GND)
100	A2	Vsso	I/O GND		GND

1.5 Package Drawings

TQFP100:

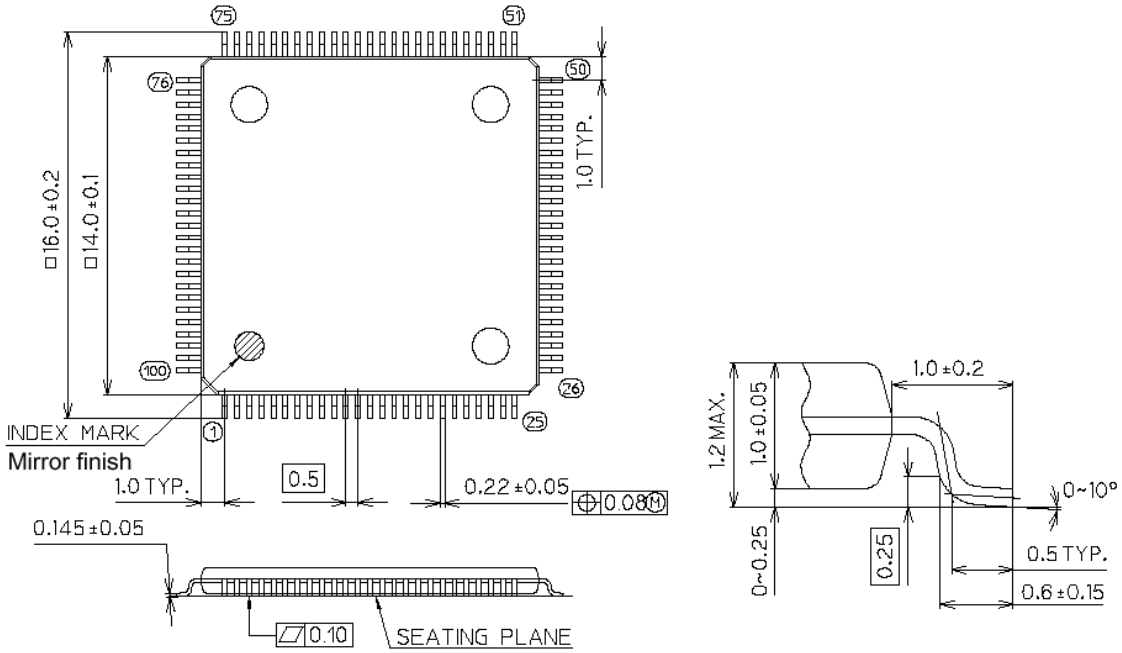
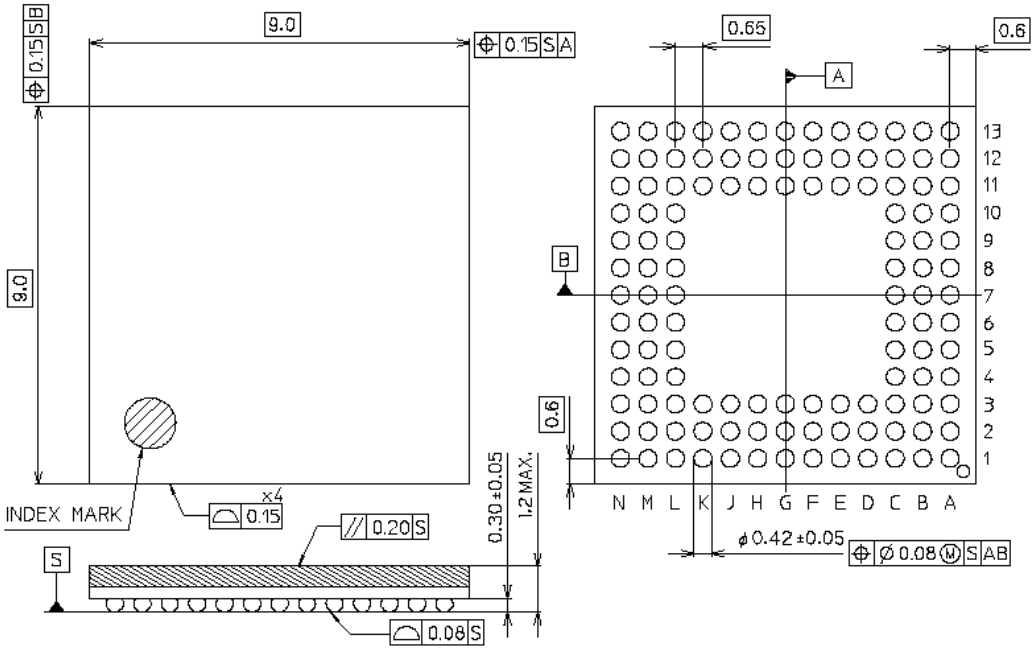


Figure 14

Sockets: E.g. Yamaichi IC149-100-025

TFBGA:



1.6 Power supply

1.6.1 Resolution adjust

In principle the high resolution of the TDC-GPX is derived from the internal gate propagation times. The gate propagation time depends upon voltage, temperature and the manufacturing process. Due to this dependency the resolution normally is not known and must be calculated via calibration measurements. In addition, the resolution is not stable, it sways with voltage and temperature. This does not apply using the resolution adjust mode for the TDC-GPX. In this mode the resolution of the TDC-GPX is adjusted quartz-accurately and absolutely temperature stable via Phase Locked Loop The phase locked loop (PLL) regulates the core voltage of the TDC-GPX so that the resolution is set exactly to the programmed value.

The BIN size is calculated as follows:

$$BIN_{I-Mode} = \frac{T_{ref} \times 2^{refclkdiv}}{216 \times hsdiv}$$

$$BIN_{G-Mode} = BIN_{I-Mode} \times \frac{1}{2}$$

$$BIN_{R-Mode} = BIN_{I-Mode} \times \frac{1}{3}$$

$$BIN_{M-Mode} = BIN_{R-Mode} \times \frac{1}{MSet + 1}$$

Tref = 25ns (40 MHz reference clock)
RefClkDiv, HSDiv → Register 7

The adjustment range of the resolution can reach values from –40 % up to +9 % of the normal resolution at 3.3 V and 25 °C. If environmental conditions lead to very large adjustments the locked-state can be lost. Then the PLL changes to floating resolution until the conditions allow the PLL to lock again.
Figure 15 shows the recommended external circuit for the regulation loop.

Note: See also application note AN013.

Example:
RefClkDiv = 7 and HSDiv = 183 give the following resolution:

I-Mode	*80.9553 ps BIN*
G-Mode	*40.4776 ps BIN*
R-Mode	*26.9851 ps BIN*

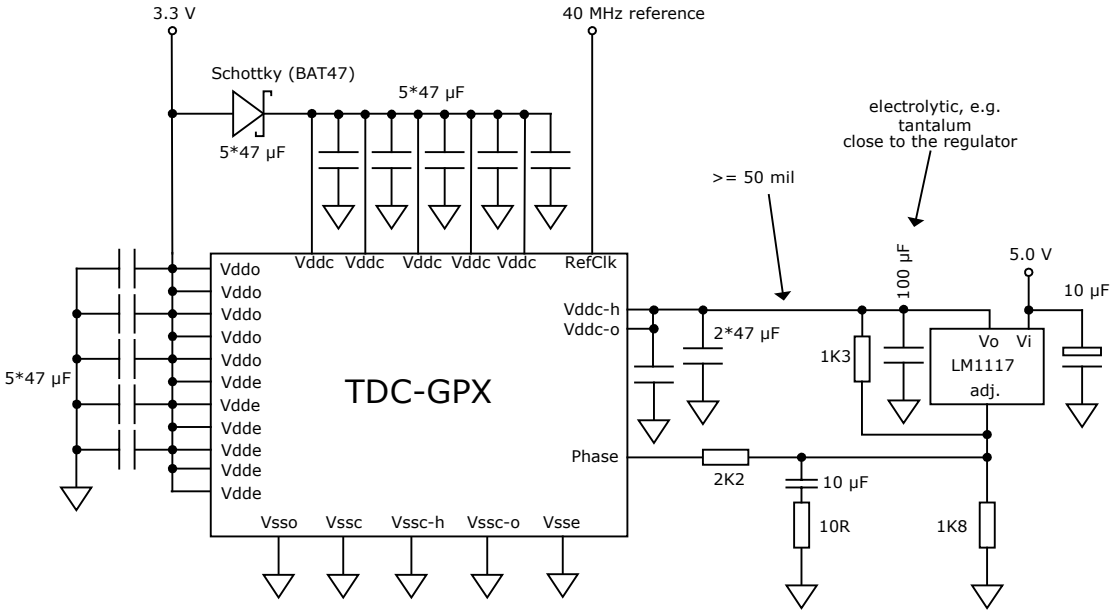


Figure 15

1.6.2 Supply voltages

Although the TDC-GPX is a fully digital circuit, some analog measures affect the circuit. The reason is that the TDC is based on the internal analog measure 'propagation delay time' which is influenced by temperature and supply voltage. A good layout of the supply voltage is essential for good measurement results. It should be high capacitive and of low inductance.

There are several connections for power supply provided at the TDC-GPX:

- Vddo - I/O supply voltage
- Vddc - Core supply voltage
- Vddc-h - Supply for the Hamac
- Vddc-o - Supply for the ring oscillator
- Vdde - Supply of LVPECL inputs
- Vsso - I/O GND
- Vssc - Core GND
- Vssc-h - Hamac GND
- Vssc-o - Ring oscillator GND

For a good stabilization we recommend the use of
5 * 47 µF, one for each Vddc pin.
1 * 47 µF for Vddc-h.
1 * 47 µF for Vddc-o.
5 * 47 µF, total for Vddo and Vdde.

Recommended capacitors:
Taiyo-Yuden LMK325BJ476MM, 47µF, 1210

The supply voltage for the core should not be higher than the supply voltage of the I/O plus 0.6 V. Otherwise the signal flow could be disturbed.
All ground pins should be connected to a ground plane on the printed circuit board.
Vddc, Vddc-h and Vddc-o are floating and are supplied from the resolution adjust voltage regulator.
Vddo should be provided by a fixed voltage regulator to avoid disturbances caused by the inputs supply.

Power consumption

The current consumption is about 45 mA in R- and G-mode and 39mA in I-mode idle plus 5 mA per million events. At 1 million continuous events per second the junction temperature will increase to 17 °C above ambient.
The thermal resistance Rth j-a is 96K/W (still air) for the TQFP package and 105K/W for the TFBGA package. With available heatsinks it can be reduced to 35k/W (still air), due to a very small Rthj-c of the package.
The maximum junction temperature is
Tj max = 125 °C.

1.6.3 Design Rules

As shown in Figure 15 the supply voltage of the measuring unit, Vddc-o/h, is provided by an adjustable linear regulator. It is strongly recommended to use only LM317 or LM1117 regulators, because only for these regulators the circuit is tested and approved. Do not use low drop regulators because these regulators' reference refers to the output voltage and the regulation might be in conflict with the PLL regulation. The input voltage of the regulator should be ≥ 5 V so that the maximum output voltage of the PLL regulation circuit is not limited by the voltage regulator's voltage drop of 1.2 V to 1.3 V.

Also for the other supply voltages, Vddc, Vddo & Vdde, linear regulators are recommended. Switched mode regulators will introduce a lot of noise to the measurement.

The width of the strip line between the regulator's output and the TDC-GPX power supply pins should be at least 50 mil.

For more detailed information concerning the PLL regulation circuit please refer to application note no. 13 at the end of this document.

1.7 Register settings

In depends on the operating mode whether bits are relevant or not. Especially the read data structure depends on the operating mode.

1.7.1 Write Registers

Service bits are for acam testing and security purposes only, Please use the recommended values.
These registers can also be read back.

Register 0: Adr = 0			I	G	R	M
0	ROsc	'1' = start ring oscillator	x	x	x	x
1	RiseEn0	'1' enable rising edge sensitivity on DStart input		x	x	x
2	FallEn0	'1' enable falling edge sensitivity on DStart input		x	x	x
3	RiseEn1	'1' enable rising edge sensitivity on DStop1 input		x	x	x
4	FallEn1	'1' enable falling edge sensitivity on DStop1 input		x	x	x
5	RiseEn2	'1' enable rising edge sensitivity on DStop2 input		x	x	x
6	FallEn2	'1' enable falling edge sensitivity on DStop2 input		x	x	x
7 – 9	HQSel	Service bits, must be set to '001'	x	x	x	x
10 – 18	TRiseEn	'1' enables rising edges for the TTL inputs Bit 10 = TStart, Bit 11 = TStop1 … Bit 18 = TStop8	x			
19 – 27	TFallEn	'1' enables falling edges for the TTL inputs Bit 19 = TStart, Bit 20 = TStop1 … Bit 27 = TStop8	x			

Register 1: Adr = 1			I	G	R	M
0 – 3	Adj0	Channel adjustment bits channel 0 (Start)		x	x	x
4 – 7	Adj1	Channel adjustment bits channel 1 (R-Mode = 2, G-Mode = 0)		x	x	x
8 – 11	Adj2	Channel adjustment bits channel 2 (R-Mode = 6, G-Mode = 5)		x	x	x
12 – 15	Adj3	Channel adjustment bits channel 3 (R-Mode = 0, G-Mode = 0)		x	x	x
16 – 19	Adj4	Channel adjustment bits channel 4 (R-Mode = 2, G-Mode = 5)		x	x	x
20 – 23	Adj5	Channel adjustment bits channel 5 (R-Mode = 6, G-Mode = 0)		x	x	x
24 – 27	Adj6	Channel adjustment bits channel 6 (R-Mode = 0, G-Mode = 5)		x	x	x

Adjustment bits recommendation:
R-Mode: Adj1 = Adj4 = Adj7 = 2, Adj 2 = Adj 8 = 6, Adj5 = 6
G-Mode: Adj2 = Adj4 = Adj6 = Adj8 = 5.

Register 2: Adr = 2			I	G	R	M
0	G-Mode	'1' = switch on G-Mode		x		
1	I-Mode	'1' = switch on I-Mode	x			
2	R-Mode	'1' = switch on R-Mode			x	x
3 – 11	Disable	'1' = disable channel Bit 3 = channel 0 (Start) … Bit 11 = channel 8	x	x	x	x
12 – 15	Adj7	Channel adjustment bits channel 7 (R-Mode = 2, G-Mode = 0)		x	x	x
16 – 19	Adj8	Channel adjustment bits channel 8 (R-Mode = 6, G-Mode = 5)		x	x	x
20 – 21	DelRise1	Service bits, set '0'		x	x	
22 – 23	DelFall1	Service bits, set '0'		x	x	
24 – 25	DelRise2	Service bits, set '0'		x	x	
26 – 27	DelFall2	Service bits, set '0'		x	x	

Register 3: Adr = 3			I	G	R	M
0 – 4	MSet	Setting resolution factors 1 to 31 in M-Mode				x
5 – 6	DelT1	Service bits, set '0'		x	x	
7 – 8	DelT2	Service bits, set '0'		x	x	
9 – 10	DelT3	Service bits, set '0'		x	x	
11 – 12	DelT4	Service bits, set '0'		x	x	
13 – 14	DelT5	Service bits, set '0'		x	x	
15 – 16	DelT6	Service bits, set '0'		x	x	
17 – 18	DelT7	Service bits, set '0'		x	x	
19 – 20	DelT8	Service bits, set '0'		x	x	
21 – 22	RaSpeed0	Service bits, set '0'		x	x	
23 – 24	RaSpeed1	Service bits, set '0'		x	x	
25 – 26	RaSpeed2	Service bits, set '0'		x	x	
27	GTest	Switches TStart to DStart, TStop1 to DStop1 and TStop2 to DStop2 (TTL to ECL, testing in G-Mode)		x	x	x

Register 4: Adr = 4			I	G	R	M
0 – 7	StartTimer	defines repetition rate of internal Start in (N + 1)*Tref recommended: 5 µs ((199 + 1) * 25ns)	x			
8	Quiet	'1' = Switch on Quiet Mode in G-, R- or M-Mode If Quiet is set to '1', the ALU doesn't start automatically, but after a rising edge at pin ALUTrigger or after writing '1' into Bit 'AluTrigSoft' (mandatory in M-Mode)		x	x	x
9	Mon	Switch on M-Mode				x
10 – 11	RaSpeed3	Pulse-pair timing adjust, typically set '0'		x	x	x
12 – 13	RaSpeed4	Pulse-pair timing adjust, typically set '0'		x	x	x
14 – 15	RaSpeed5	Pulse-pair timing adjust, typically set '0'		x	x	x
16 – 17	RaSpeed6	Pulse-pair timing adjust, typically set '0'		x	x	x
18 – 19	RaSpeed7	Pulse-pair timing adjust, typically set '0'		x	x	x
20 – 21	RaSpeed8	Pulse-pair timing adjust, typically set '0'		x	x	x
22	MasterReset	'1' = general reset excluding configuration registers	x	x	x	x
23	PartialReset	'1' = general reset excluding configuration registers and Interface FIFO content	x	x	x	x
24	AluTrigSoft	Starts ALU in Quiet Mode		x	x	x
25	EFlagHiZN	'1' = EF output pin is driving all the time	x	x	x	x
26	MTimerStart	'1' = the internal MTimer is started with a Start pulse	x	x	x	x
27	MTimerStop	'1' = the internal MTimer is started with a Stop pulse	x	x	x	x

Register 5: Adr = 5			I	G	R	M
0 – 17	StartOff1	programmable internal Start-offset	x	x	x	x
18 – 20	ServiceMAdj	Service bits, set "0"				x
21	StopDisStart	Stop disable before a Start pulse	x	x	x	x
22	StartDisStart	Start disable after a Start pulse		x	x	x
23	MasterAluTrig	Master reset by Alutrigger pin HIGH (only with no Quiet Mode)	x	x	x	
24	PartialAluTrig	Partial reset by Alutrigger pin HIGH (only with no Quiet Mode)	x	x	x	
25	MasterOenTrig	Master reset by OEN pin LOW (only with OEN not used)	x	x	x	x
26	PartialOenTrig	Partial reset by OEN pin LOW (only with OEN not used)	x	x	x	x
27	StartRetrig	Start retrigger	x	x	x	

Register 6: Adr = 6			I	G	R	M
0 – 7	Fill	Defines the level when the fill-level Flags LFx of the 2 interface FIFOs will be set.	x	x	x	
8 – 25	StartOff2	programmable internal Start-offset (in G-Mode only)		x		
26	InSelECL	select ECL inputs for I-Mode DStop1 -> TStop1, TStop3, TStop5, TStop7 DSTop2 -> TStop2, TStop4, TStop6, TStop8(single channels can be switched off using 'Disable'	x			
27	PowerOnECL	'1' = Switch-on power for ECL-inputs	x	x	x	x

When reading back register 6 the "Fill" bits 0 to 7 will be inverted.

Register 7: Adr = 7			I	G	R	M
0 – 7	HSDiv	High speed divider PLL	x	x	x	x
8 – 10	RefClkDiv	Reference clock divider PLL	x	x	x	x
11	ResAdj	Switch-on resolution adjust mode	x	x	x	x
12	NegPhase	Invert phase output of PLL	x	x	x	x
13	Track	cut regulation loop of PLL	x	x	x	x
14	Service	Service Bits, set '0'				
15 – 27	MTimer	Setting internal timer in multiples of Tref, 0 – 8191	x	x	x	x

Register 14: Adr = 14			I	G	R	
0 – 3	Service	Write "0"	x	x	x	x
4	16BitMode	'1' switches on the 16 Bit mode of the data bus	x	x	x	x
5 – 27	Service	Write "0"	x	x	x	x

After 16 Bit mode is set all further read/write commands have to be done in pairs of 16 Bit.

1.7.2 Read registers

- **I-Mode**

Register 8: Adr = 8		
0 – 16	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
17	Slope1	Slope of this hit
18 – 25	Start#1	Start number of this hit
26 – 27	ChaCode1	Channel code of this hit

Register 9: Adr = 9		
0 – 16	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
17	Slope2	Slope of this hit
18 – 25	Start#2	Start number of this hit
26 – 27	ChaCode2	Channel code of this hit

Register 10: Adr = 10		
0 – 16	Start01	Time interval between external start and first internal start
17 – 27	-	not used

- **G-Mode**

Register 8: Adr = 8		
0 – 21	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
22	Slope1	0 = falling edge, 1 = rising edge
23 – 27	-	not used

Register 9: Adr = 9		
0 – 21	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
22	Slope2	0 = falling edge, 1 = rising edge
23 – 27	-	not used

Register 10: Adr = 10		
0 – 15	-	not used
16 – 27	-	not used

- **R-Mode & M-Mode**

Register 8: Adr = 8		
0 – 22	IFIFO1	Time interval data from Interface FIFO1, Hit = Stop-Start
23 – 27	-	not used

Register 9: Adr = 9		
0 – 22	IFIFO2	Time interval data from Interface FIFO2, Hit = Stop-Start
23 – 27	-	not used

Register 10: Adr = 10		
0 – 15	-	not used
16 – 27	-	not used

1.7.3 Read/Write registers

Register 11: Adr = 11			
0 – 7	StopCounter0	# of hits on DStop1, I-Mode: not available G-Mode: counting falling edge R-Mode: counting rising edge	read only
8 – 15	StopCounter1	# of hits on DStop2, I-Mode: not available G-Mode: counting falling edge R-Mode: counting rising edge	read only
16 – 23	HFifoErrU	'1' unmasks full flags of Hit FIFOs to ErrFlag pin	read/write
24 – 25	IFifoErrU	'1' unmasks full flags of Interface FIFOs to ErrFlag pin	read/write
26	NotLockErrU	'1' unmasks 'PLL not locked' to ErrFlag pin	read/write

Register 12: Adr = 12			
0 – 7	HFifoFull	Full flags of Hit FIFOs	read only
8 – 9	IFifoFull	Full flags of Interface FIFOs	read only
10	NotLocked	'PLL not locked' flag	read only
11	HFifoE	Falg indicating that all Hit FIFOs are empty	read only
12	TimerFlag	Flag indicating end of MTimer	read only
13 – 20	HFifoIntU	'1' unmasks full flags of Hit FIFOs to IntFlag pin	read/write
21 – 22	IFifoIntU	'1' unmasks full flags of Interface FIFOs to IntFlag pin	read/write
23	NotLockIntU	'1' unmasks 'PLL not locked' to IntFlag pin	read/write
24	HFifioEU	'1' unmasks 'All Hit FIFOs empty' to IntFlag pin	read/write
25	TimerFlagU	'1' unmasks end of MTimer to IntFlag pin	read/write
26	Start#U	'1' unmasks highest bit of Start# (I-Mode) to IntFlag pin	read/write
27	Service	Set to "0"	read/write

HFifoFull and IFifoFull will be set back to "0" when reading register 12. They are re-activated by a master reset or a partial reset.

2 I-Mode

2.1 Block diagram I-Mode

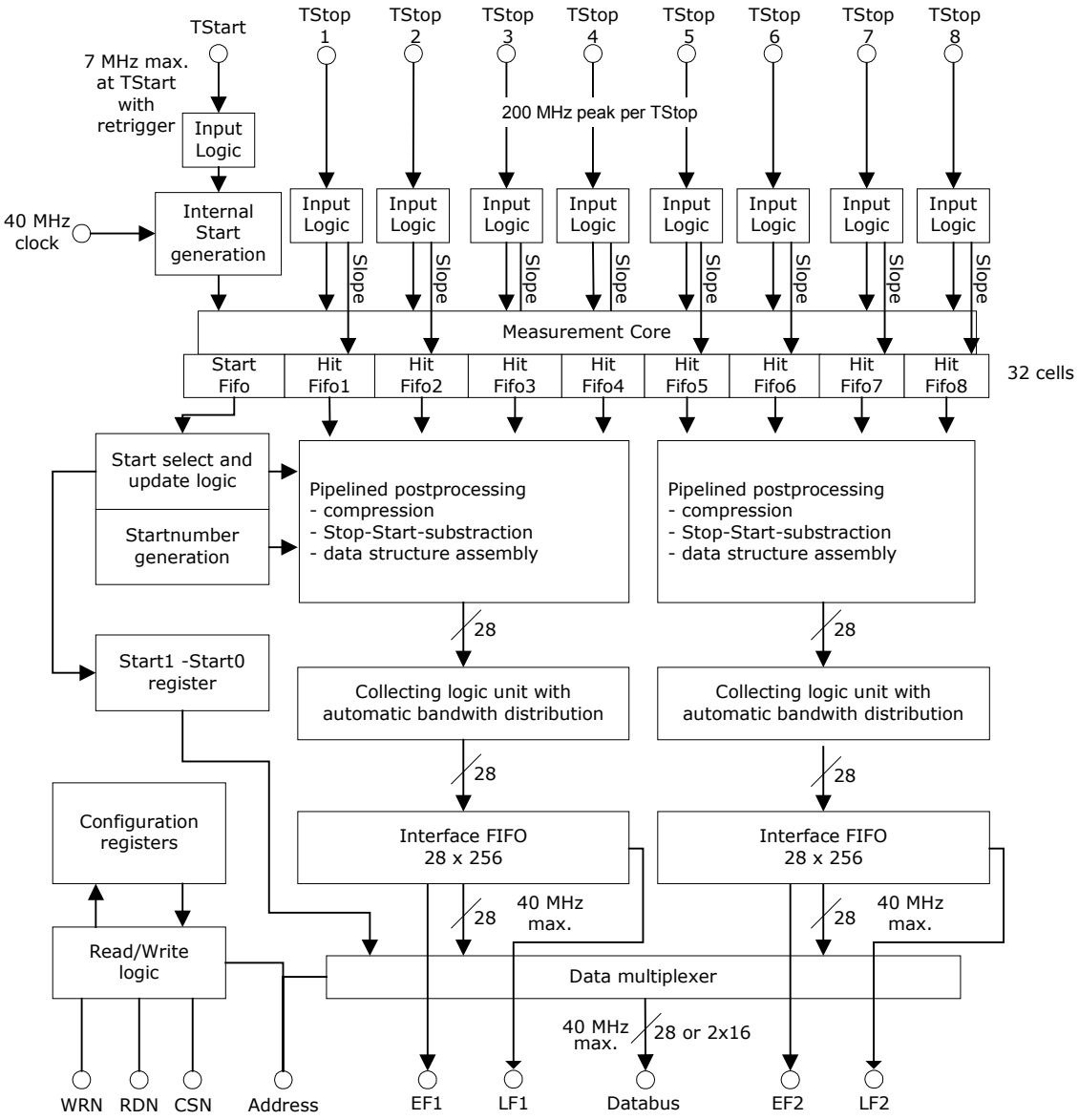


Figure 16: Block diagram

2.2 Input circuitry I-Mode

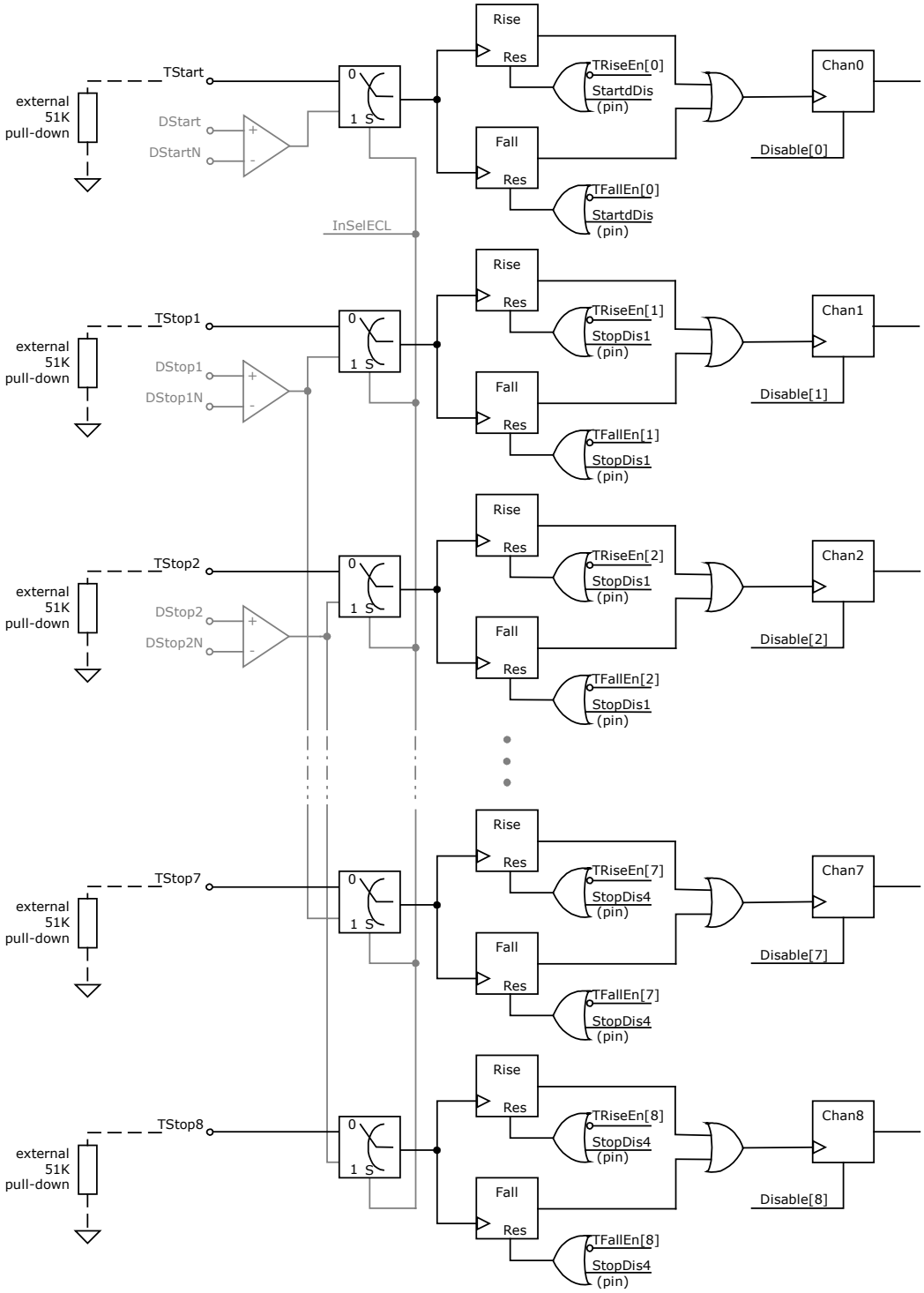


Figure 17: Input circuitry

2.3 I-Mode Basics

In this mode TDC-GPX offers

- 8 stop channels referring to 1 start channel,
- Each of typ. 81 ps resolution
- 5.5 ns pulse-pair resolution
- Start-retrigger up to 7 MHz
- Unlimited measuring range with internal start retrigger
- All inputs of LVTTL type
- Selectable rising/falling edge sensitivity for all channels
- Several disable possibilities for all channels

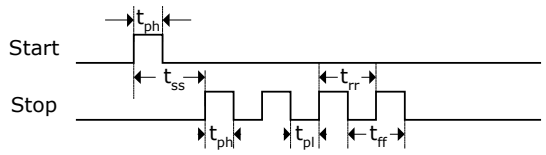


Figure 18: Measurement timings

Par.	Time (Condition) Min.	Max.	Description
t_{ph}	1.5 ns		Positive pulse width
t_{pl}	1.5 ns		Negative pulse width
t_{ss}	0 ns min **5.2 ns	9.4 µs *unlimited	Start to Stop
t_{rr}, t_{ff}	5.5 ns typ. 6.9 ns max.#		edge to edge # @ 87 ps resolution

*with int. start retrigger **with StopDisStart = 1

Input circuitry

The detailed input structure is shown in Figure 17: Input circuitry. Each input separately can be set to be sensitive to rising or falling edge. This is done in register0, TRiseEn[8...0] and TFallEn[8...0]. The LSB stands for the TStart input, the MSB TStop8 input. A zero in the channel bit for TRiseEn and TfallEn at the same time disables the channel.

All inputs can be disabled by hardware, the stop inputs in pairs (pin 'StopDis1' disables inputs TStop1 and TStop2, etc.). They also can be disabled by Software setting the 'Disable' bits in register 2. The TDC-GPX offers the possibility to disable the Stop inputs automatically until a Start is coming in. This is set by StopDisStart = '1' in register 5.

Start Retrigger

After an initial start event, the TDC-GPX can generate its own internal starts. This is controlled by the parameter "StartTimer" in register 4. The start retrigger rate may not exceed 7 MHz.

Single Start

StartTimer = 0 switches off the internal Start generation. In this mode the measuring range is limited to 2^{17} BIN ≈ 10.6 µs (@ BIN = 81 ps). Further pulses at TStart will be ignored.

Internal Start Retrigger

The period of the start repetition is programmable in multiples of the 40 MHz reference clock between (4+1) and (255+1) x 25ns (Register 4: StartTimer[7...0]).
The time interval between the initial, external start and the first internal one will vary. It is therefore measured and stored as 'Start01' in register 10. It can be read out from this register as a 17 Bit integer in multiples of BIN.
The time intervals between following starts are fixed and referred to as (N +1) x Tref. Additionally, there is an 8 Bit counter for the start number (Start#). The start number is added to the output data.
A further option is to feed the highest bit of the Start counter to the IrFlag output pin by setting register 11, Bit 26 Start#U to one. With this signal the intenal start number counter can externally be extended to any size.
The internal start retrigger allows an **unlimited measuring range** for the TDC-GPX.

External Start Retrigger

A further option is to retrigger the Start externally. This option is activated by setting StartTimer = 1 (Reg 4) and StartRetrig = 1 (Reg 5). The further behavior is the same as for the internal start retrigger. The maximum retrigger frequency is typically 7 MHz. The time interval between two Starts is measured and stored in the "Start01" register. This value is reasonable only if the delay between two Start pulses does not exceed the measuring range of 2^{17} BIN ≈ 10.6 µs.

Figure 19