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TDC-GPX2

4-Channel Time-to-Digital Converter

General Description

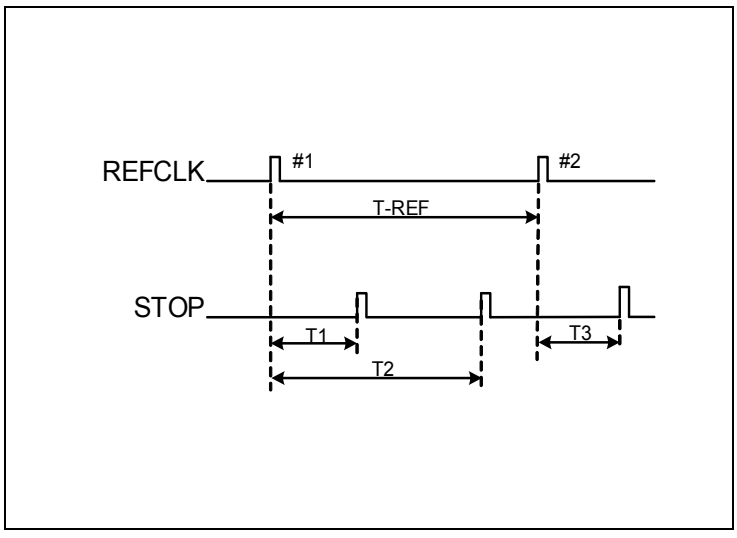
The GPX2 is a high performance time-to-digital converter (TDC) frontend device.

Highest measurement performance and highest data throughput is achieved with LVDS stop inputs and LVDS serial outputs for each channel. Current saving operation is also possible with CMOS inputs and SPI readout.

High configuration flexibility and unlimited measurement range cover many applications. They range from portable handheld laser range equipment to ambitious time-of-flight measurements of highest performance, as e.g. done in medical imaging applications.

GPX2 operates without any locked loop technologies. GPX2 calculates all stop measurements inside, proportional to the applied reference clock. Combinations of best single shot accuracy of 10ps with lowest pulse-to-pulse spacing <5ns and maximum data throughput rate of 70MSPS per stop input are possible.

Figure 1:
Time Interval Measurements



Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of this device are listed below:

Figure 2:
Added Value of Using TDC-GPX2

Benefits	Features

• Simple data post-processing thanks to calibrated results	• 4 stop channels with serial
	  • 20ns pulse-to-pulse spacing
	  • Maximum 35MSPS
	• 2 combined channels with
	  • 5ns pulse-to-pulse spacing
	  • Maximum 70MSPS
	• Single shot accuracy
	  • 20ps rms single shot resolution per channel
	  • 10ps rms with high resolution option
	• Unlimited measuring range 0s to 16s

• Event assignment thanks to reference clock index simplifies coincidence measurements • Easy pulse width measurements • High efficiency thanks high sample rate	• Differential reference clock input 2MHz to 12.5MHz, optional with quartz • Inputs optional with LVDS or CMOS level • Readout with LVDS or SPI • 16-stage FIFO per channel • Automatic calibration to reference clock (no PLL or DLL) • SPI compatible 4-wire interface for configuration
• Compact design thanks to small package and low number of external components • Reduced cooling thanks to low power consumption	• Supply voltage 3.3V • Power dissipation 60mW to 450mW • Standby current 60µA • QFN64 (9mm x 9mm) or QFP64 (12mm x 12mm)

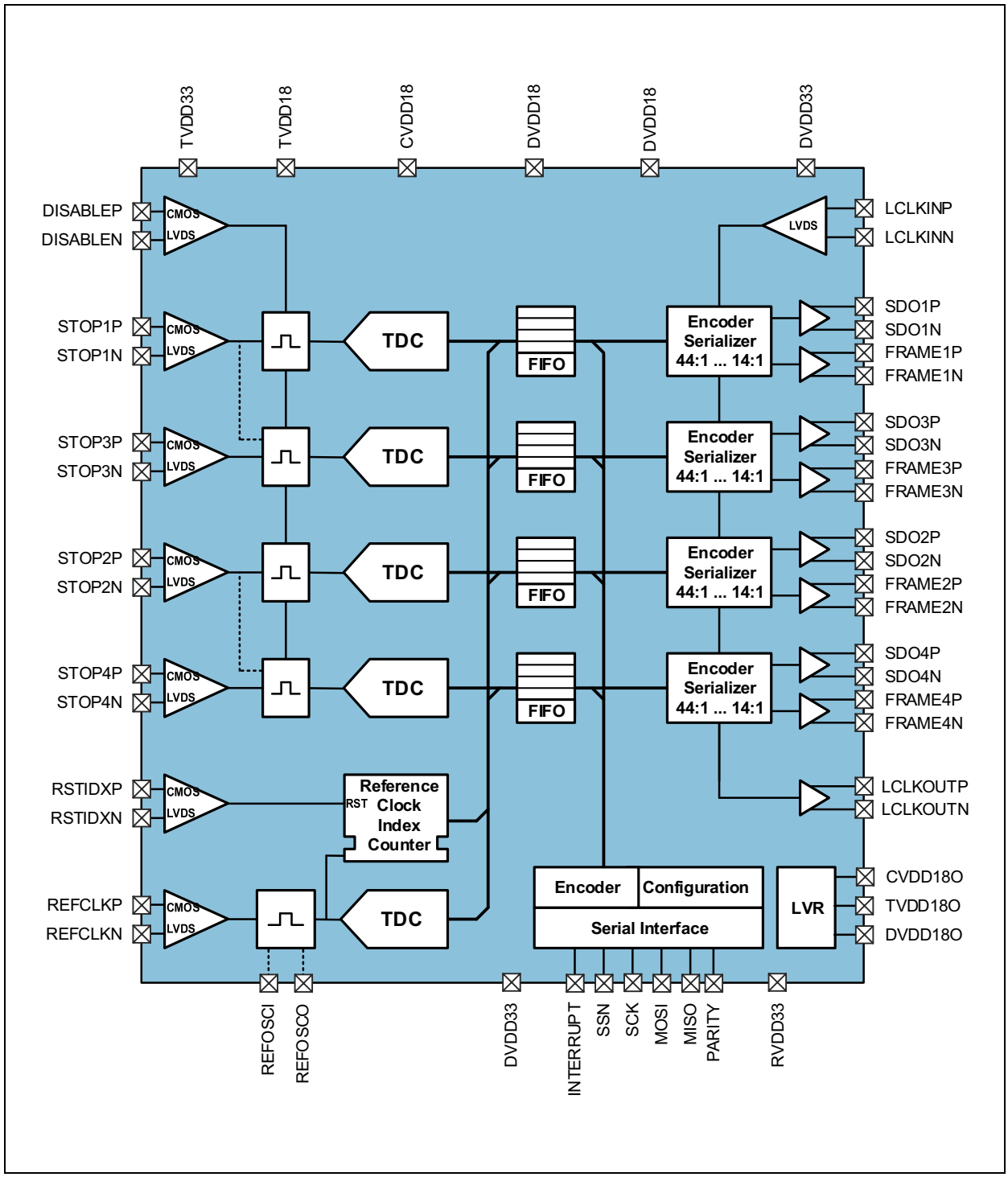
Applications

- Automated Test Equipment
- Laser Range Measurement
- Medical Imaging
- Time-of-Flight Measurement
- Particle Physics
- Lidar, Radar, Sonar

Block Diagram

The functional blocks of this device are shown below:

Figure 3:
Functional Blocks of TDC-GPX2

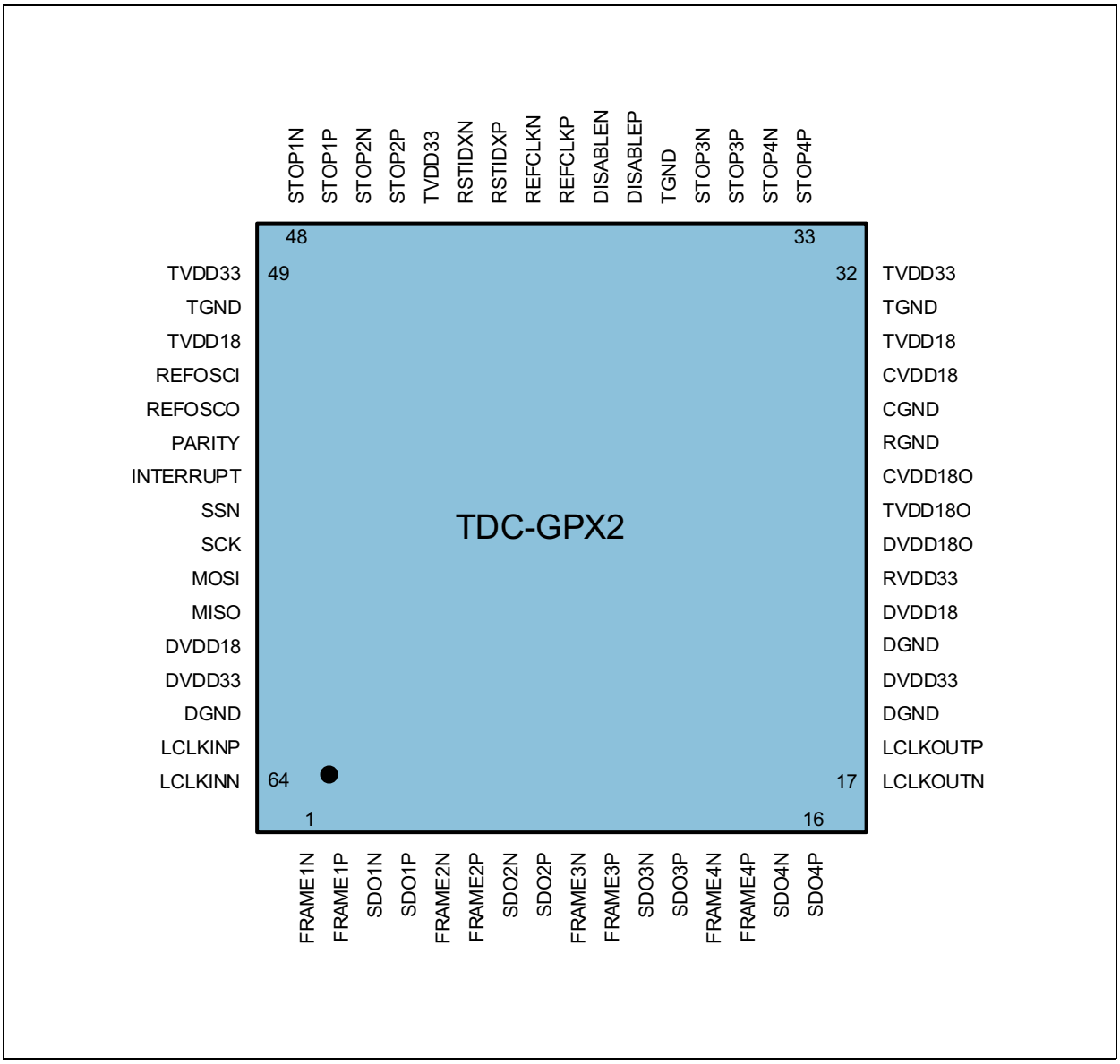


Pin Assignments

The TDC-GPX2 is shipped in QFN64 or QFP64 plastic packages with the following pin assignment.

Pin Diagram

Figure 4:
Pin Diagram of TDC-GPX2



Pin Description

Figure 5:
Pin Description of TDC-GPX2

Pin No.	Pin Name	Description	Type	Not Used
1	FRAME1N	Negative frame signal of stop channel 1	LVDS Output	Open
2	FRAME1P	Positive frame signal of stop channel 1	LVDS Output	Open
3	SDO1N	Negative serial data output of stop channel 1	LVDS Output	Open
4	SDO1P	Positive serial data output of stop channel 1	LVDS Output	Open
5	FRAME2N	Negative frame signal of stop channel 2	LVDS Output	Open
6	FRAME2P	Positive frame signal of stop channel 2	LVDS Output	Open
7	SDO2N	Negative serial data output of stop channel 2	LVDS Output	Open
8	SDO2P	Positive serial data output of stop channel 2	LVDS Output	Open
9	FRAME3N	Negative frame signal of stop channel 3	LVDS Output	Open
10	FRAME3P	Positive frame signal of stop channel 3	LVDS Output	Open
11	SDO3N	Negative serial data output of stop channel 3	LVDS Output	Open
12	SDO3P	Positive serial data output of stop channel 3	LVDS Output	Open
13	FRAME4N	Negative frame signal of stop channel 4	LVDS Output	Open
14	FRAME4P	Positive frame signal of stop channel 4	LVDS Output	Open
15	SDO4N	Negative serial data output of stop channel 4	LVDS Output	Open
16	SDO4P	Positive serial data output of stop channel 4	LVDS Output	Open
17	LCLKOUTN	Negative serial clock output	LVDS Output	Open
18	LCLKOUTP	Positive serial clock output	LVDS Output	Open
19, 21, 62	DGND	Ground for digital and IO units	Power Supply	
20, 61	DVDD33	3.3V supply for digital and IO units	Power Supply	
22, 60	DVDD18	1.8V supply for digital and IO units	Power Supply	
23	RVDD33	3.3V supply for linear voltage regulator	Power Supply	
24	DVDD18O	1.8V supply voltage for digital and IO units	Regulator Out	Open
25	TVDD18O	1.8V supply voltage for time frontend	Regulator Out	Open
26	CVDD18O	1.8V supply voltage for time digital converter	Regulator Out	Open
27	RGND	Ground for linear voltage regulator	Power Supply	
28	CGND	Ground for TDC	Power Supply	

Pin No.	Pin Name	Description	Type	Not Used
29	CVDD18	1.8V positive supply for TDC	Power Supply	
30, 51	TVDD18	1.8V positive supply for time front-end	Power Supply	
31, 37, 50	TGND	Ground for 1.8V time front-end supply	Power Supply	
32, 44, 49	TVDD33	3.3V positive supply for time front-end	Power Supply	
33	STOP4P	Positive stop input for channel 4	CMOS/LVDS Input	TVDD33
34	STOP4N	Negative stop input for channel 4	LVDS Input	TVDD33
35	STOP3P	Positive stop input for channel 3	CMOS/LVDS Input	TVDD33
36	STOP3N	Negative stop input for channel 3	LVDS Input	TVDD33
38	DISABLEP	Positive disabling pin for stop channels	CMOS/LVDS Input	TVDD33
39	DISABLEN	Negative disabling pin for stop channels	LVDS Input	TVDD33
40	REFCLKP	Positive clock signal of reference clock	CMOS/LVDS Input	TVDD33
41	REFCLKN	Negative clock signal of reference clock	LVDS Input	TVDD33
42	RSTIDXP	Positive reference index reset signal	CMOS/LVDS Input	TVDD33
43	RSTIDXN	Negative reference index reset signal	LVDS Input	TVDD33
45	STOP2P	Positive stop input for channel 2	CMOS/LVDS Input	TVDD33
46	STOP2N	Negative stop input for channel 2	LVDS Input	TVDD33
47	STOP1P	Positive stop input for channel 1	CMOS/LVDS Input	TVDD33
48	STOP1N	Negative stop input for channel 1	LVDS Input	TVDD33
52	REFOSCI	Input for quartz as reference clock	XOSC Driver In	Open
53	REFOSCO	Output for quartz as reference clock	XOSC Driver Out	Open
54	PARITY	Parity of all configuration registers	LVTTL Output	Open
55	INTERRUPT	SPI interrupt	LVTTL Output	Open
56	SSN	SPI slave select not + interface reset	LVTTL Input	
57	SCK	SPI serial clock	LVTTL Input	
58	MOSI	SPI serial data master out, slave In	LVTTL Input	
59	MISO	SPI serial data master in, slave Out	LVTTL Tristate	
63	LCLKINP	Positive serial clock in	LVDS Input	DVDD33
64	LCLKINN	Negative serial clock in	LVDS Input	DVDD33

Note(s):

1. A small dot on the package indicates the pin 1. There is no need to connect the exposed pad to GND (internally not connected). Connecting it may be helpful for heat dissipation. The package is RoHS compliant and does not contain any Pb.

Absolute Maximum Ratings

Stresses beyond the Absolute Maximum Ratings may cause permanent damages to the device. Exposure to any Absolute Maximum Rating condition for extended periods may also affect device reliability and lifetime.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
VDD33	3.3V Supply Voltage to Ground	-0.5	4.0	V	Pins DVDD33, TVDD33, RVDD33
VDD18	1.8V Supply Voltage to Ground	-0.5	2.2	V	Pins DVDD18, TVDD18, CVDD18
	Voltage between ground pins	-0.3	+0.3	V	Pins DGND, TGND, RGND, CGND
V_{iLVDS}	Voltage at differential input pins	-0.3	VDD33 + 0.3	V	Pins STOP1, STOP2, STOP3, STOP4, REFCLK, REFRES, DISABLE, LCLKIN
V_{osc}	Voltage at input of oscillator cell	-0.3	VDD18 +0.3	V	Pin REFOSCIN
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± 1000		V	JS-001-2014
Temperature Ranges and Storage Conditions					
T_J	Operating Junction Temperature	-40	125	°C	
T_{STRG}	Storage Temperature Range	-65	150	°C	
T_{BODY}	Package Body Temperature		260	°C	The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)
RH_{NC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Maximum floor life time of 168 hours

Recommended Operation Conditions

Recommended operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are expressly denoted.

Figure 7:
Recommended Operating Conditions

Symbol	Pin	Description	Min	Typ	Max	Unit
Power-Supply						
VDD33	DVDD33, TVDD33, RVDD33	Supply Voltage	2.4	3.3	3.6	V
VDD18	DVDD18, TVDD18, CVDD18	Core Supply Voltage powered by integrated regulator, pins DVDD18O, TVDD18O, CVDD18O	1.7	1.8	1.9	V
Temperature						
T_A		Operating free air temperature (1)	-40		125	°C
Reference & Stop Inputs						
$V_{ID,LVDS}$	STOP1, STOP2, STOP3, STOP4, REFCLK, RSTIDX, DISABLE,	LVDS Differential Input Voltage	200			mV
$V_{IC,LVDS}$		LVDS Common Mode Input Voltage	$V_{ID}/2$	1.25	2.2 – $V_{ID}/2$	V
$V_{IL,CMOS}$		CMOS Input Low Voltage			0.4	V
$V_{IH,CMOS}$		CMOS Input High Voltage	VDD33 - 0.4			V
SPI-Interface						
V_{IL}	SCK, MOSI, SSN	Digital Input LOW Voltage			0.8	V
V_{IH}		Digital Input HIGH Voltage	0.7 * VDD33			V
C_{LOAD}	INTERRUPT, MISO, PARITY	Load Capacitance to Ground			20	pF

Symbol	Pin	Description	Min	Typ	Max	Unit
LVDS-Interface						
$V_{ID,LVDS}$	LCLKIN	LVDS Differential Input Voltage	200			mV
$V_{IC,LVDS}$		LVDS Common Mode Input Voltage		1.25		V
R_{TERM}	SDO1, SDO2, SDO3, SDO4, FRAME1, FRAME2, FRAME3, FRAME4, LCLKOUT	Differential Termination Resistor for LVDS Outputs		100		Ω
C_{LOAD}		Load Capacitance to Ground			5	pF

Note(s):

1. Recommended Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Test conditions for guaranteed specification are explicitly denoted.

The following test levels apply to all following characteristics:

Figure 8:
Test Levels

Test Level	Description
I	100% production tested.
II	100% production tested at 25 °C and guaranteed by design and characterization testing
III	Parameter is guaranteed by design and characterization testing
IV	Sample tested
V	Parameter is a typical value only.

Converter Characteristics

General Conditions: VDD33 = 3.3V; VDD18 = 1.8V;
T_A = 0°C to 80°C.

Figure 9:
Converter Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Accuracy of Time Measurement							
RMS	Single-shot RMS resolution	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	IV		20 15 10	30 20 15	ps
INL	Integral non-linearity		IV			20	ps
DNL	Differential non-linearity		V		5		ps
	No missing code	At time quantization level	III	Assured			
	Channel to channel isolation	At same times measured	IV		20	100	ps
	Offset error	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	V		100 150 200		ps
	Offset error temperature drift	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	IV		0.5 1 1.5	3	ps/K
Switching Performance							
t_{CONV}	Converter latency	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III			20 50 100	ns
	Peak conversion rate	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III			50 20 10	MSPS
	Maximum read-out rate LVDS: 44 Bit/14 Bit SPI: Opcode + 48 Bit/16 Bit	SDR / 250MHz DDR / 250MHz SPI / 50MHz	III	5.6 11.3 0.9		17.8 35.7 2.1	MSPS

Power Supply Characteristic

General Conditions: VDD33 = 3.3V; VDD18 = 1.8V;
T_A = 0°C to 80°C

Figure 10:
Power Supply Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Supply Voltage							
t_{VDD18O}	Delay from power-up of RVDD33 to TVDD18O, CVDD18O, DVDD18O stable	C_{load} = 100µF	V			100	ms
$P_{TOT,MIN}$	Minimum total power dissipation	CMOS inputs and SPI read f_{REFCLK} = 5MHz conversion rate 1MSPS	V		60		mW
$P_{TOT,MAX}$	Maximum total power	LVDS inputs and outputs f_{REFCLK} = 10MHz $f_{STOP1..4}$ = 50MHz f_{LCLK} = 300MHz	V		450		mW
Detailed Current Consumption							
$I_{DVDD18,REFCLK}$	Core current into REFCLK	f_{REFCLK} = 5MHZ	V		2		mA
$I_{DVDD18,STOP}$	Current per stop channel		V		0.5		mA
I_{CVDD18}	Current with activated TDC core		V		14		mA
$I_{TVDD18,REFOSC}$	Quartz oscillator current if used	f_{REFOSC} = 4MHZ	III		2		mA
$I_{DVDD33,LVDS-IN}$ $I_{TVDD33,LVDS-IN}$	Current per LVDS input buffer		III		2	6	mA
$I_{DVDD33,LVDS-OUT}$	Current per LVDS output buffer	RTERM = 100Ω	III		5	10	mA
I_{DDQ}	Quiescent current mainly by I_{RVDD33}	LVDS inputs tied to VDD33	II		60	100	µA
I_{LKG}	Input leakage current	LVDS, CMOS, Digital, REFOSCI	II	-5		1	µA

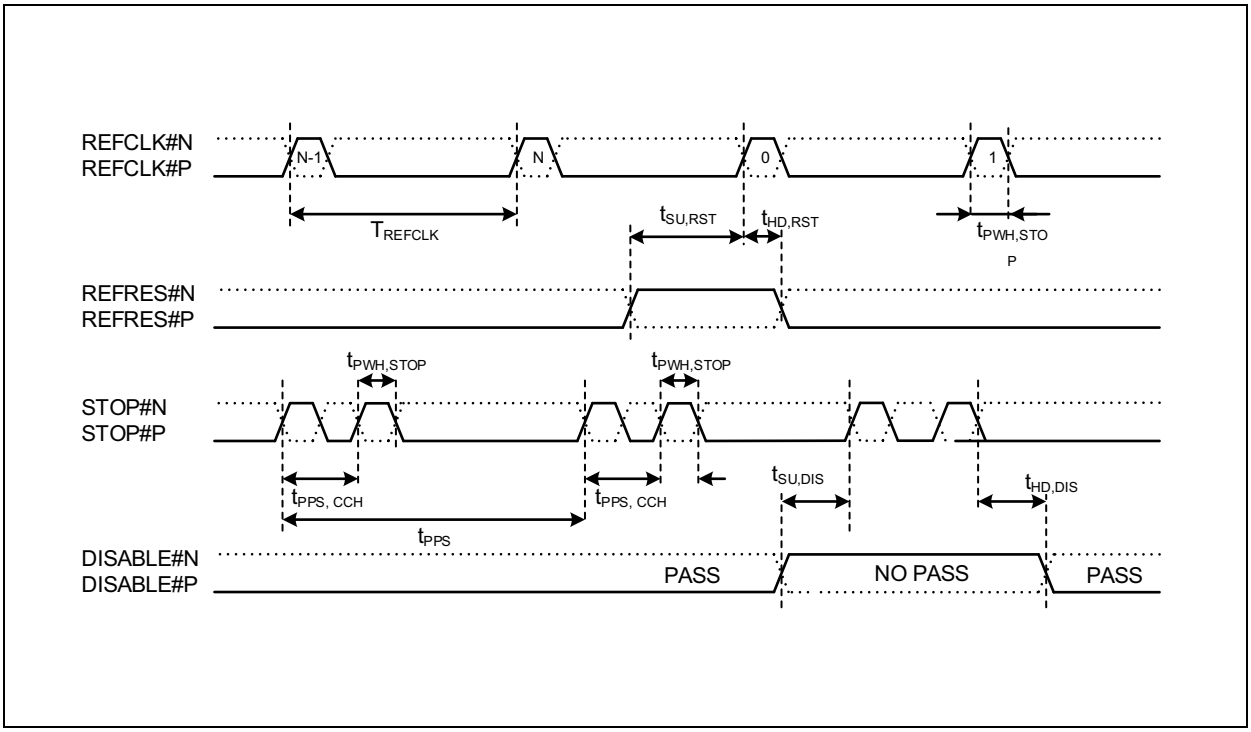
Reference Clock and Stop Input Requirements

General Conditions: VDD33 = 3.3V; VDD18 = 1.8V;
T_A = 0°C to 80°C; V_{ID} = 200mV; V_{IC} = 1.25V; V_{IL} = 0V; V_{IH} = 3.3V

Figure 11:
Clock and Input Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
f_{REFCLK}	Reference clock frequency	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III	2 2 2	5 5 5	12.5 12.5 10.0	MHz
f_{REFOSC}	Reference oscillator frequency at pin 52,53	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III	2 2 2	5 5 5	12.5 12.5 10.0	MHz
T_{REFCLK}	Reference clock period		III	83	200	500	ns
	Reference clock jitter		V			100	ps
	Reference clock stability	No requirement					
$t_{PWH,STOP}$	Minimum pulse width	LVDS CMOS	III	2 10			ns
t_{PPS}	Minimum pulse-to-pulse spacing	High_Resolution = 0 (off) High_Resolution = 1 (2x) High_Resolution = 2 (4x)	III	20 50 100			ns
$t_{PPS,CCH}$	Minimum pulse-to-pulse spacing	CHANNEL_COMBINE = 1 For a single pair of pulses.	III	5			ns
$t_{SU,RST}$	Setup time from RSTIDX to REFCLK		III	5			ns
$t_{HD,RST}$	Hold time from RSTIDX to REFCLK		III	5			ns
$t_{SU,DIS}$	Setup time from STOP to DISABLE		III	5			ns
$t_{HD,DIS}$	Hold Time from STOP to DISABLE		III	5			ns
t_{PIN_ENA}	Pin activation time from configuration of PIN_ENA… to valid data	Pins: RSTIDX, DISABLE, REFCLK, STOP1…4	III	200			µs
t_{POR}	Delay between power-on or initialization reset and next communication	Power-up, opcodes spiopc_ power & spiopc_init, pin	III	100			µs

Figure 12:
Timing Symbols and Parameters



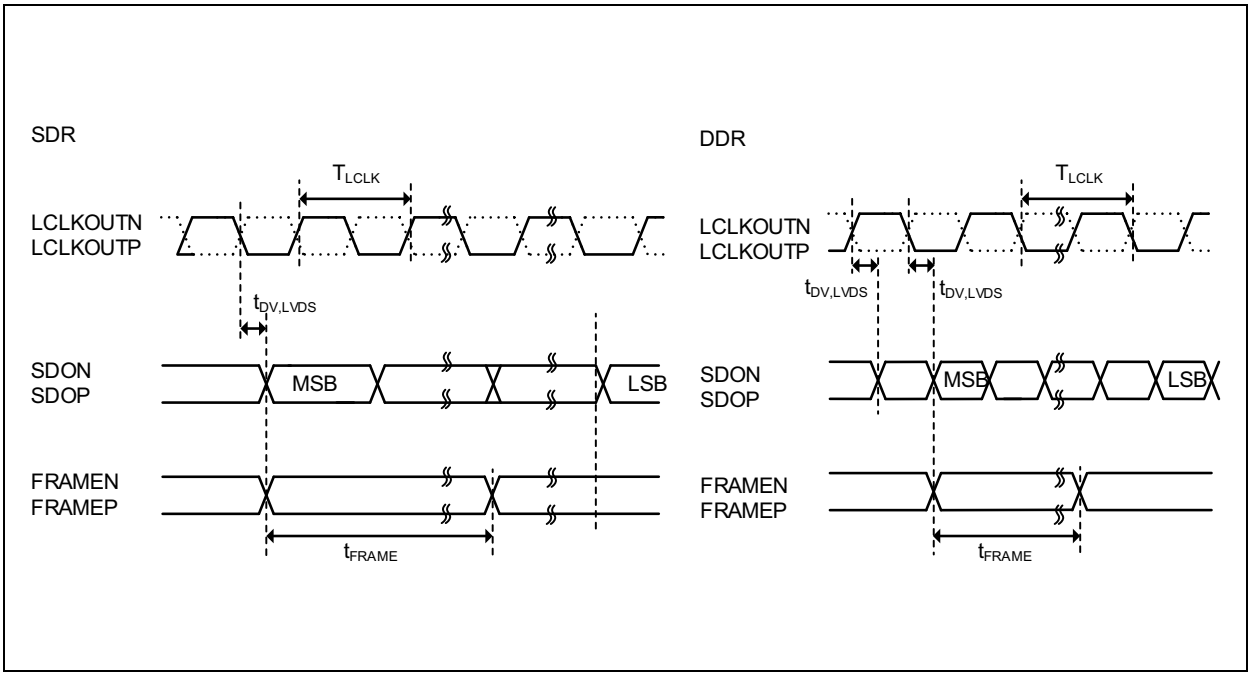
LVDS Data Interface Characteristics

General Conditions: VDD33 = 3.3V, VDD18 = 1.8V,
T_A = 0°C to 80°C, V_{ID} = 200 mV, V_{IC} = 1.25V

Figure 13:
Interface Characteristics

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Electrical Characteristics							
$V_{OD,LVDS}$	LVDS differential output voltage	R_L = 100Ω, C_L = 5pF	III	200			mV
$V_{OC,LVDS}$	LVDS common mode output voltage	R_L = 100Ω, C_L = 5pF	III	1.125	1.25	1.375	V
t_{PIN_ENA}	Pin activation time from configuration PIN_ENA_LVDS to valid data at pin	Pins: LCLKIN, LCLKOUT, SDO1…4, FRAME1…4	III			200	µs
Timing Characteristics							
t_{SYNC}	Synchronization latency	SDR DDR	III		6 3		Clock
t_{FRAME}	Frame length	SDR DDR	III		8 4		Clock
f_{LCLK}	LVDS clock frequency SDR/DDR		III	10		250	MHz
	LVDS clock duty cycle		III	45	50	55	%
	Path delay LCLKIN to LCLKOUT, SDO1…4, FRAME1…4		III		5	10	ns
$t_{DV,LVDS}$	Data valid after active clock edge	lvds_data_valid _ adjust = 1	III		0		ns

Figure 14:
LVDS Timing Symbols and Parameters



Serial Communication Interface

General Conditions: VDD33 = 3.3V; VDD18 = 1.8V;
T_A = 0°C to 80°C; V_{IL} = 0V; V_{IH} = 3.3V

Figure 15:
Serial Communication Interface

Symbol	Description	Condition	TL	Min	Typ	Max	Unit
Electrical Characteristics							
V_{OL}	Digital output LOW voltage	I_O = 2mA	III			0.3	V
V_{OH}	Digital output HIGH voltage	I_O = 2mA	III	DVDD +0.3			V
Timing Characteristics							
f_{SCK}	Serial clock frequency	C_L = 5pF	III			50	MHz
$t_{PWH,SCK}$	Serial clock pulse width HI state		III	10			ns
$t_{PWL,SCK}$	Serial clock pulse width LO state		III	10			ns
$t_{PWH,SSN}$	SSN pulse width between write cycles		III	10			ns
$t_{SU,SSN}$	SSN setup time after SCK falling		III	20			ns
$t_{HD,SSN}$	SSN hold time before SCK rising		III	20			ns
$t_{SU,MOSI}$	Data setup time prior to clock edge		III	5			ns
$t_{HD,\ MOSI}$	Data hold time after clock edge		III	5			ns
$t_{DV,MISO}$	Data valid after rising clock edge		III	8			ns
$t_{ZX,MISO}$	HighZ to output time		III	8			ns
$t_{XZ,MISO}$	Output to HighZ time		III	8			ns

Figure 16:
Write and Incremental Write

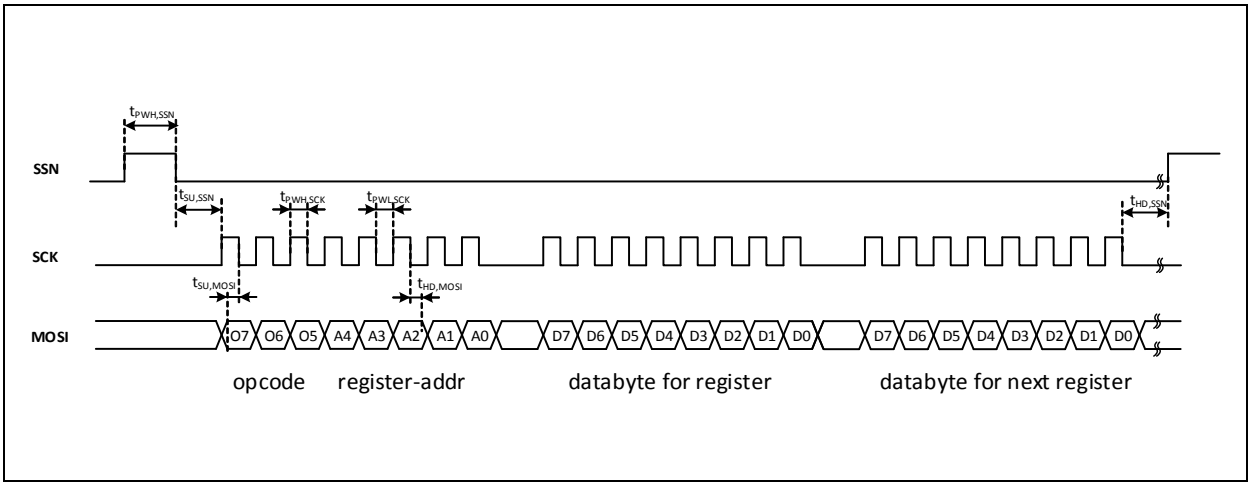
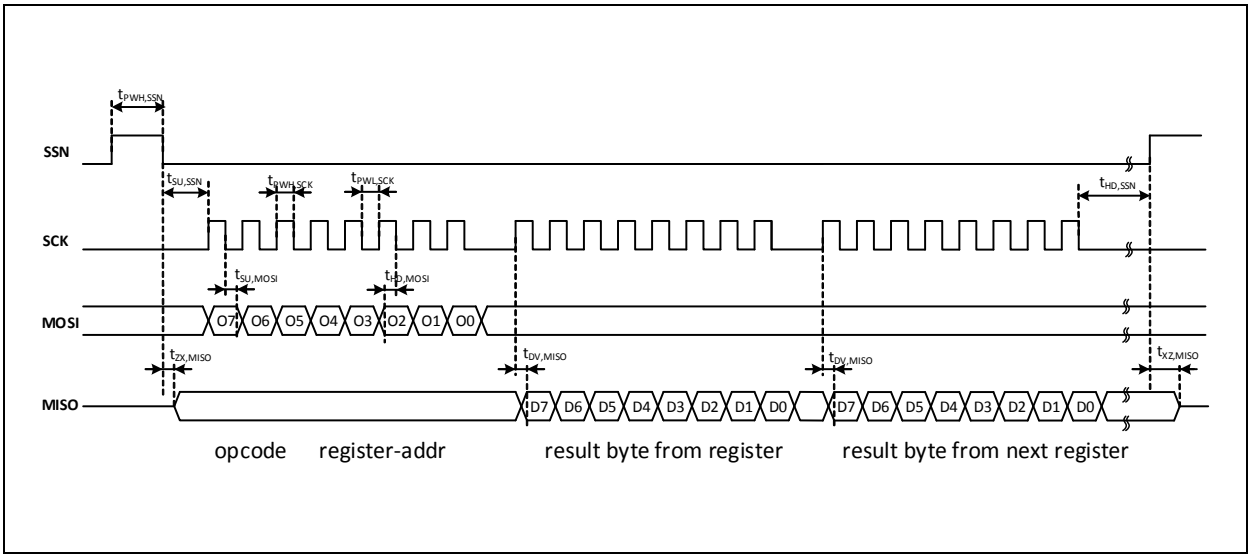


Figure 17:
Read and Incremental Read



Typical Operating Characteristics

Histograms

Figure 18:
STOP2, FWHM, Histogram 100000 Values

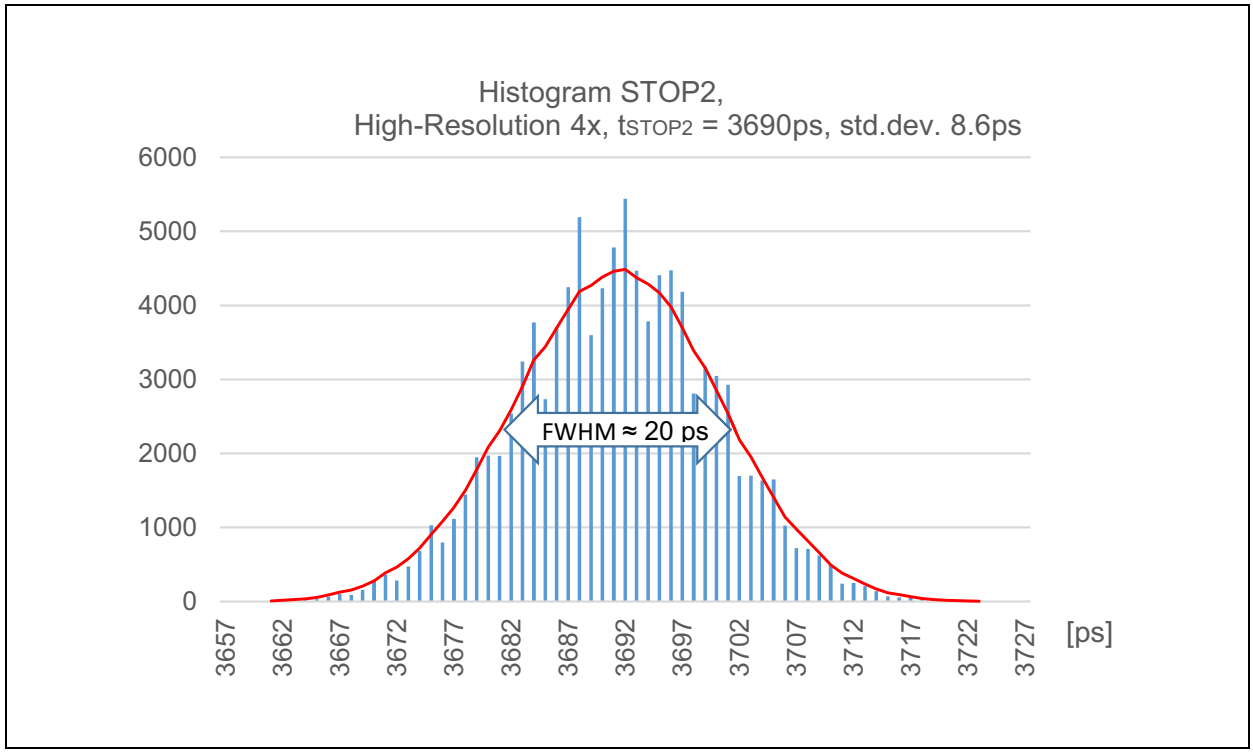


Figure 19:
STOP2 – STOP1, HIGHRES 4x, Histogram 100000 Values

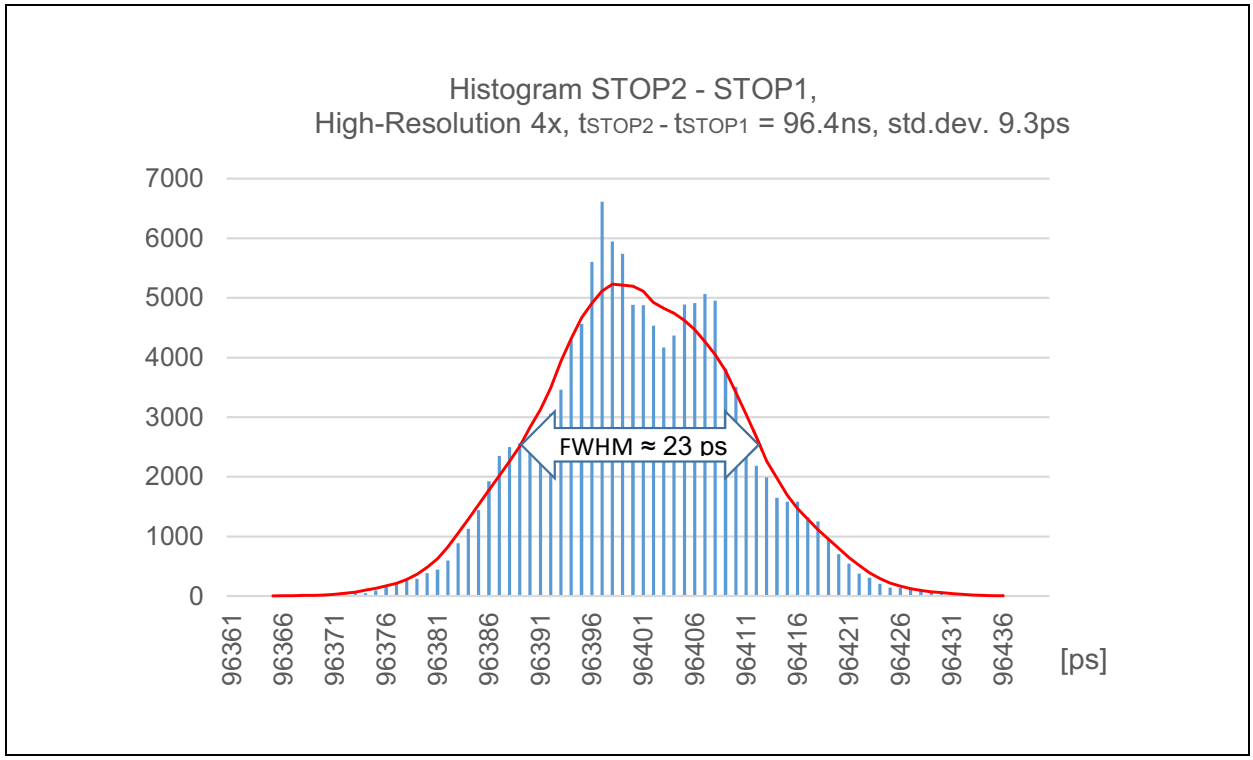


Figure 20:
STOP2 – REFCLK, HIGHRES 0, Histogram 100000 Values

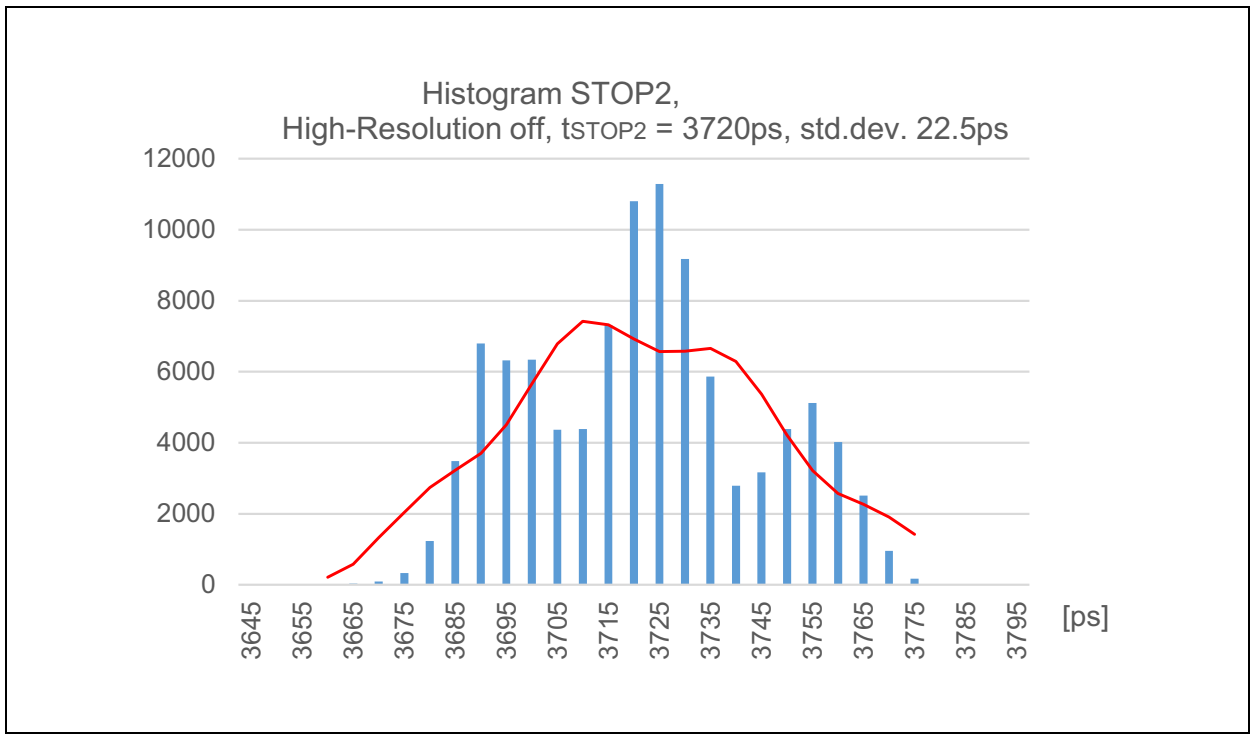
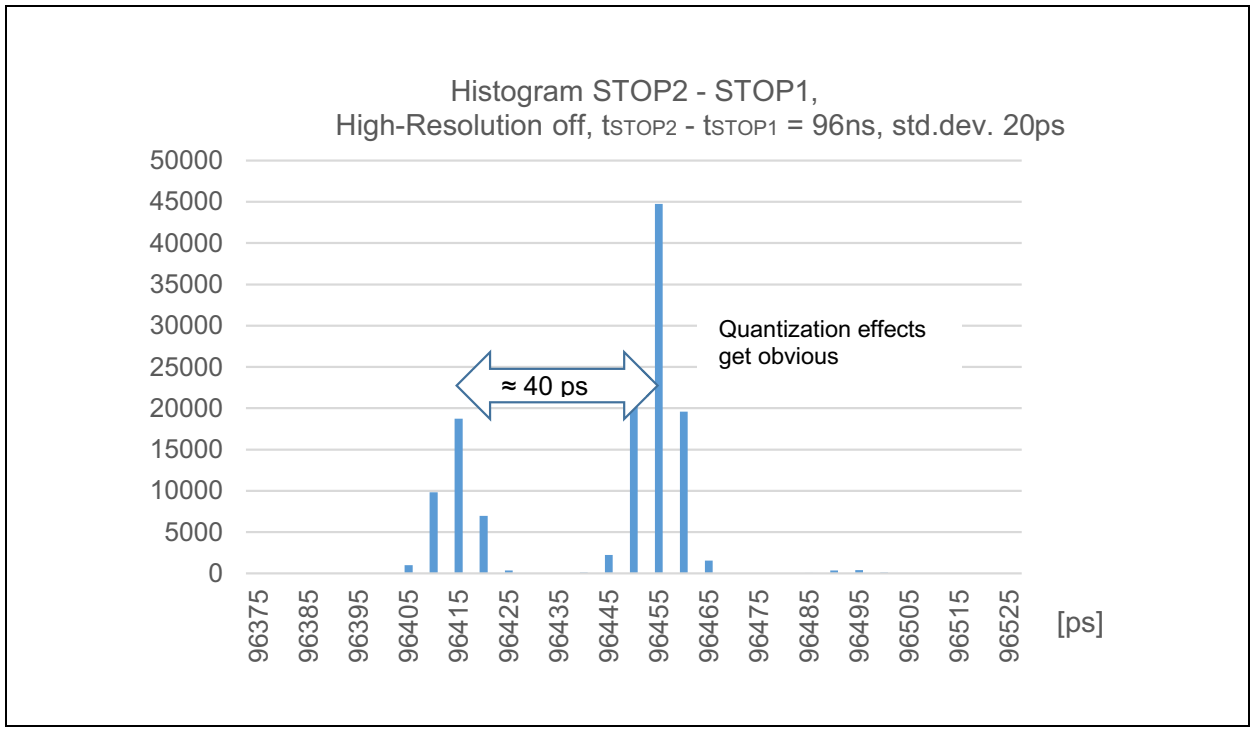
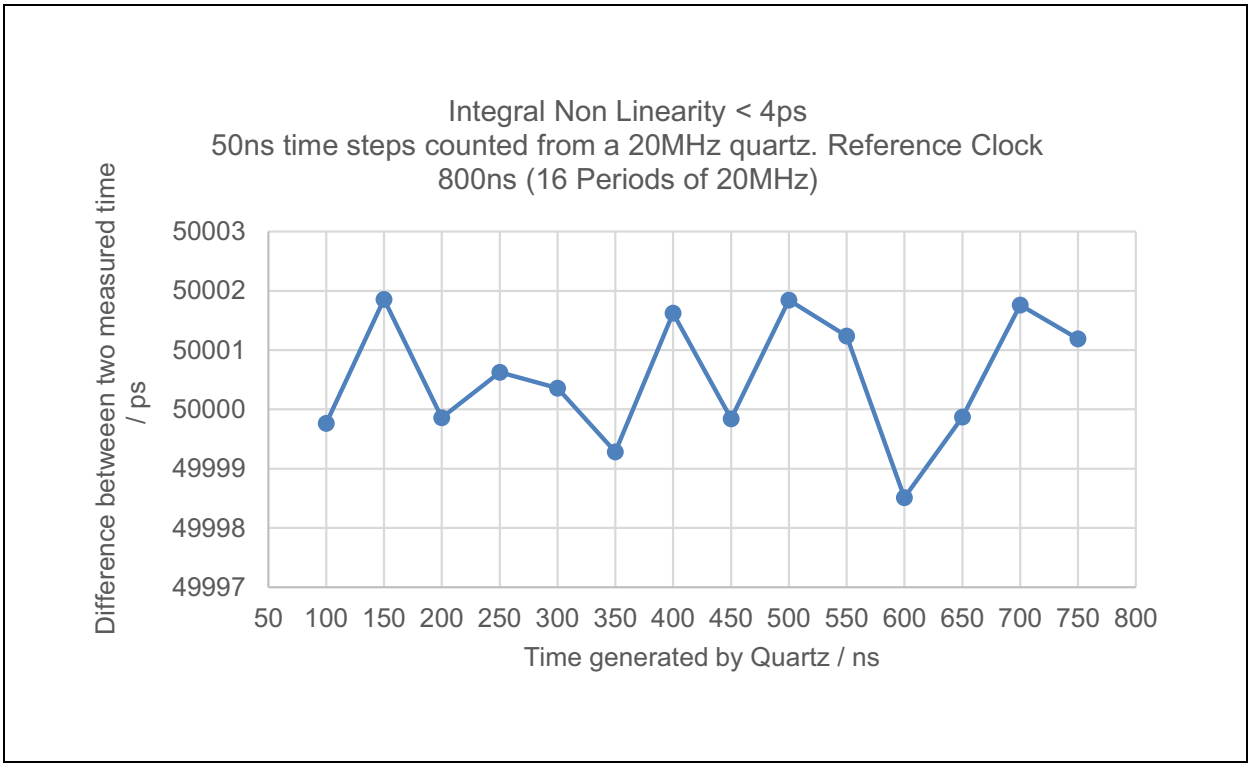


Figure 21:
STOP2 – STOP1, HIGHRES 0, Histogram 100000 Values



Integral Non-Linearity

Figure 22:
Integral Non-Linearity



Register Description

Configuration Register Overview

The configuration registers are organized in 17 addresses of one byte. All configuration registers are accessible via the SPI interface. They can be read and written individually or with an incremental access. For monitoring the chip it is possible to observe at the PARITY pin whether the sum of all set bits is even or odd.

Figure 23:
Configuration Register Overview

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
0	PIN_ENA_RSTIDX	PIN_ENA_DISABLE	PIN_ENA_LVDS_OUT	PIN_ENA_REFCLK	PIN_ENA_STOP4	PIN_ENA_STOP3	PIN_ENA_STOP2	PIN_ENA_STOP1
1	HIGH_RESOLUTION		CHANNEL_COMBINE		HIT_ENA_STOP4	HIT_ENA_STOP3	HIT_ENA_STOP2	HIT_ENA_STOP1
2	BLOCKWISE_ FIFO_READ	COMMON_FIFO_ READ	LVS_DOUBLE_DATA_ RATE	STOP_DATA_BITWIDTH		REF_INDEX_BITWIDTH		
3	REFCLK_DIVISIONS (Lower byte)							
4	REFCLK_DIVISIONS (Middle byte)							
5	Fixed value*: (0000b)				REFCLK_DIVISIONS (Upper bits)			
6	Fixed value*: (110b)			LVDS_ TEST_ PATTERN	Fixed value*: (0000b)			
7	REFCLK_BY _ XOSC	Fixed value*: (1b)	LVDS_DATA_VALID_ ADJUST		Fixed Value*: (0011b)			
8	Fixed value*: (10100001b)							
9	Fixed value*: (00010011b)							
10	Fixed value*: (00000000b)							
11	Fixed value*: (00001010b)							

Addr	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
12	Fixed value*: (11001100b)							
13	Fixed value*: (11001100b)							
14	Fixed value*: (11110001b)							
15	Fixed value*: (01111101b)							
16	Fixed value*: (00000b)					CMOS_ INPUT	Fixed value*: (00b)	

The fixed values are assigned by ams: Unless otherwise suggested, they should be set as shown in this table.

Detailed Configuration Register Description

All registers are read/write with 0 as default value, besides registers 13, 14 with 5 as default value.

Figure 24:
Configuration Register 0

Addr: 0		Pin Enable Register
Bit	**Bit Name**	**Bit Description**
The PIN_ENA registers activate the LVDS input or output drivers of the related pins. Main purpose of PIN_ENA is cutting of current consumption of differential LVDS buffers to nearly zero. But also with CMOS input levels the pins have to be activated accordingly. Unused inputs has to be tied to VDD33.		
0 to 3	PIN_ENA1 to PIN_ENA4	Activation on stop event input pins STOP1 to STOP4 0: Stop input pins not active 1: Stop input pins active
4	PIN_ENA_ REFCLK	0: REFCLK input pins not active 1: REFCLK input pins active
5	PIN_ENA_ LVDS_OUT	0: All LDVS output pins disabled 1: Activation of LCLK and LCLKOUT pins. Activation of SDO1…4 and FRAME1…4, depends further on CHANNEL_COMBINE and PIN_ENA
6	PIN_ENA_ DISABLE	0: Stop disable pin is not active. The stop measurement on all channels is always active according to configuration. 1: Stop disable pin is active. The stop measurements are disabled if the DISABLE pin on the PCB is set to HIGH
7	PIN_ENA_ RSTIDX	0: Deactivation of reference clock index counter reset pin 1: Activation of reference clock index counter reset pin

Figure 25:
Configuration Register 1

Addr: 1		Content
Bit	**Bit Name**	**Bit Description**
0 to 3	HIT_ENA1 to HIT_ENA4	0: Stop events are internally rejected. The pin enabling of STOP1…4 is not affected. 1: Stop events are internally accepted and processed. Normal working condition
4, 5	CHANNEL_ COMBINE	The four stop channels may be combined for improved pulse pair resolution or higher conversion rate. 00b: Normal operation with four independent stop channels 01b: "Pulse distance" Stop events at STOP1 are measured alternatingly by stop channels 1 & 3 Stop events at STOP2 are measured alternatingly by stop channels 2 & 4 10b: "Pulse width" The rising edges at STOP1 are measured by stop channel 1 The falling edges at STOP1 are measured by stop channel 3 The rising edges at STOP2 are measured by stop channel 2 The falling edges at STOP2 are measured by stop channel 4
6, 7	HIGH_ RESOLUTION	A stop event is internally delayed, measured several times and summed up in order to one result to increase the time resolution. = 0 (off): Off, standard resolution with minimal pulse-to-pulse spacing. = 1 (2x): A stop event is measured twice = 2 (4x): A stop event is measured four times

Figure 26:
Configuration Register 2

Addr: 2		Data Output
Bit	**Bit Name**	**Bit Description**
0 to 2	REF_INDEX_ BITWIDTH	Bit width of reference clock index in LVDS output (not applicable to SPI data readout) 000b: 0Bit, no data out 001b: 2Bits 010b: 4Bits 011b: 8Bits 100b: 16Bits 101b: 24Bits 110b: 6Bits 111b: 12Bits
3, 4	STOP_DATA_ BITWIDTH	Bit width of the stop result in LVDS output. Bit width should be sufficient to represent the REFCLK_DIVISIONS configuration value (not applicable to SPI data readout) 00b: 14Bits → max of REFCLK_DIVISIONS = 2^{14}-1 01b: 16Bits → max of REFCLK_DIVISIONS = 2^{16}-1 10b: 18Bits → max of REFCLK_DIVISIONS = 2^{18}-1 11b: 20Bits → max of REFCLK_DIVISIONS = 2^{20}-1
5	LVDS_ DOUBLE _ DATA_RATE	0: Single Data Read (SDR): The LVDS data clocked out on rising edges of LCLK-OUT 1: Double Data Read (DDR): The LVDS data are clocked on both edges of LCLK-OUT
6	COMMON_ FIFO_READ	0: LVDS: Operation with four independent stop channels SPI: INTERUPT pin is set to zero, as soon as one FIFOs does have a value. OFF, operation with four independent stop channels 1: LVDS: All active frame pins are set simultaneous as soon as all related FIFOs have values. SPI: INTERUPT pin is set to zero, as soon as all active FIFOs have value. In combination with BLOCKWISE_READ this option guaranties successive measurements in parallel on all stop channels
7	BLOCKWISE_ FIFO_READ	0: OFF, Operation with standard FIFO function 1: Data output (LVDS or SPI) is not started before a channel FIFO is full. Once FIFO is full, measurement is not restarted before FIFO is completely read-out. This option guaranties successive measurements at high stop event rate or slow read-out speeds (e.g. SPI)