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TDK5101F

315 MHz ASK/FSK Transmitter in 10-pin Package

Wireless Control Components

Never stop thinking.

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Revision History:	**2007-09-19**	V 1.3
Previous Version:	V1.2 as of August 2006	
Page	Subjects (there are only minor changes since last version)	
33, 36	Added Min.-/Max.-values of output power and supply current	
32, 34, 36	Added values of frequency range and for possible enhance of frequency range	

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Table of Contents **Page**

1 Product Description

1.1 Overview

The TDK 5101 F is a single chip ASK/FSK transmitter for operation in the frequency band 311-317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

1.2 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- frequency range 311-317 MHz
- high efficiency power amplifier (typically 5 dBm)
- low supply current
- voltage supply range 2.1 ... 4 V
- temperature range –40 ... +125°C
- power down mode
- crystal oscillator 9.84 MHz
- FSK-switch
- divided clock output for µC
- low external component count

1.3 Application

- Tire pressure monitoring systems
- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

2 Functional Description

2.1 Pin Configuration

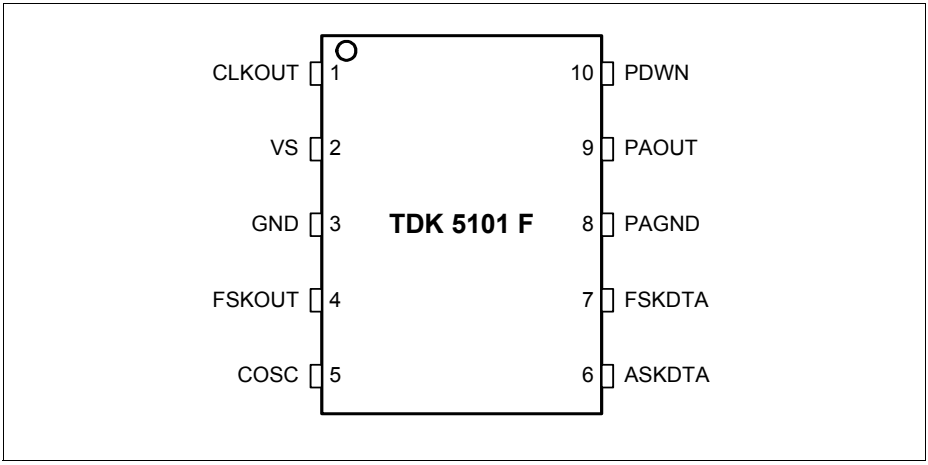


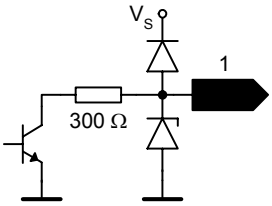
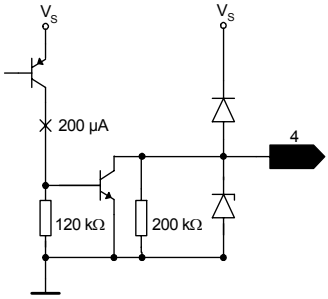
Figure 1 IC Pin Configuration

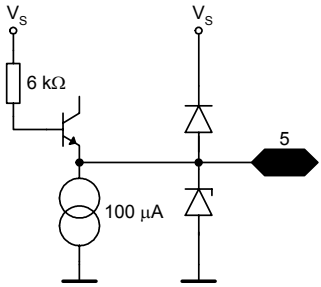
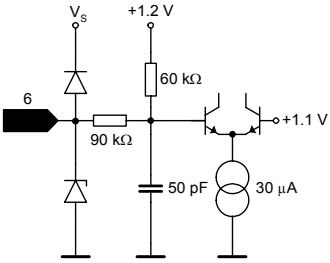
2.2 Pin Definition and Functions

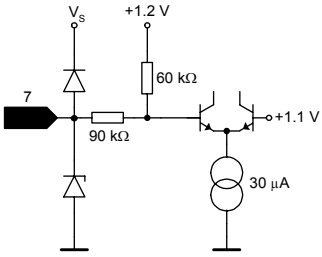
Table 1 Pin Definition and Function - Overview

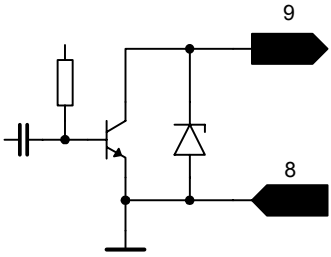
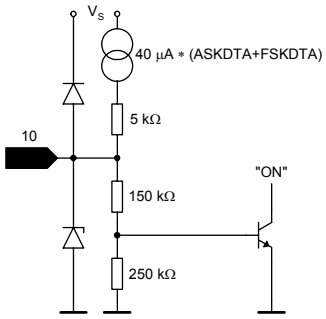
Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (615.2 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	FSKOUT	Frequency Shift Keying Switch Output
5	COSC	Crystal Oscillator Input (9.84 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (315 MHz)
10	PDWN	Power Down Mode Control

Table 2 Pin Definition and Function[1)]

Pin No.	Symbol	Interface Schematic	Function
1	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock frequency is 615.2 kHz.
2	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND		General ground connection.
4	FSKOUT		This pin is connected to a switch to GND (pin 3). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.

Pin No.	Symbol	Interface Schematic	Function
5	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.
6	ASKDTA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier

Pin No.	Symbol	Interface Schematic	Function
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 4) to GND (pin 3). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.

Pin No.	Symbol	Interface Schematic	Function
8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by either setting FSKDTA or ASKDTA to a logic high-state.

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode.
In Power Down Mode, the values are zero or high-ohmic.

2.3 Functional Block Diagram

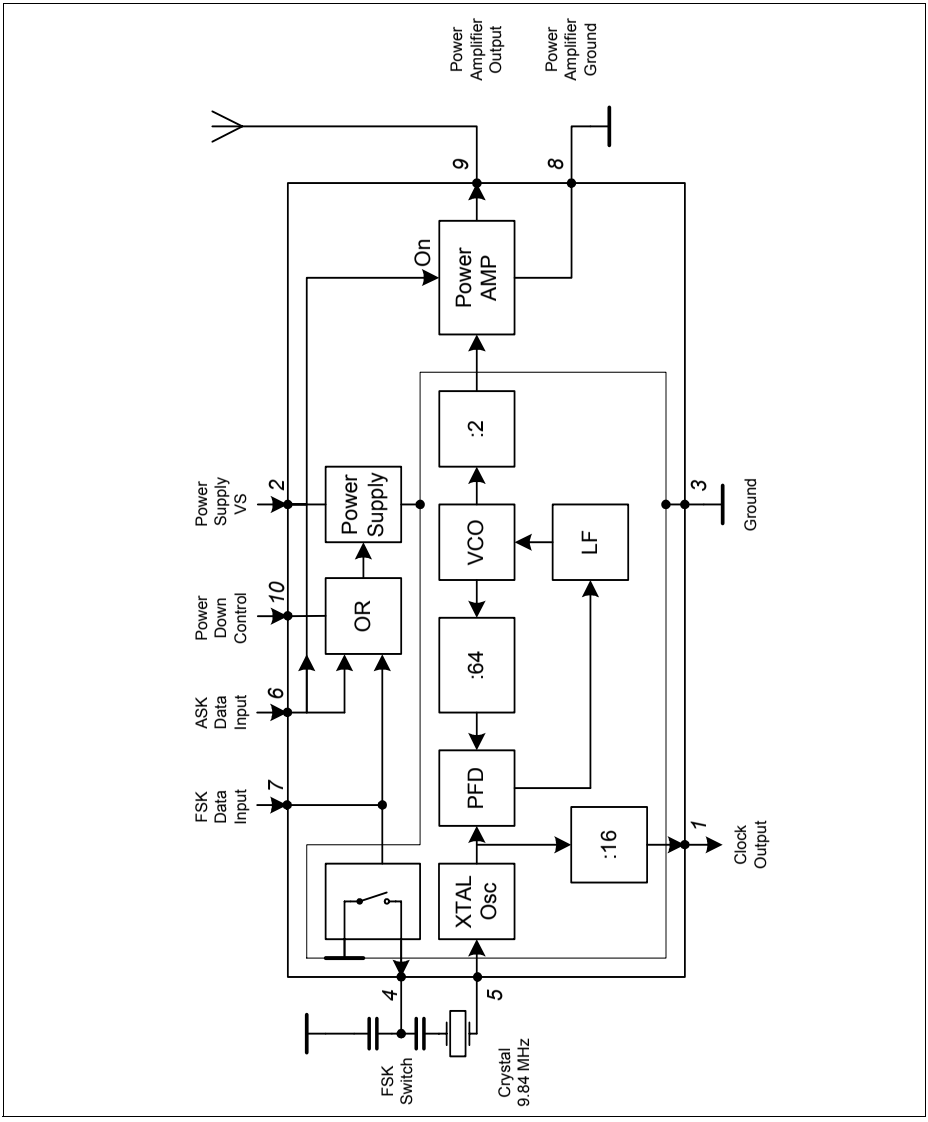


Figure 2 Functional Block diagram

2.4 Functional Block Description

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 630 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates at 9.84 MHz.

The crystal frequency is divided by 16. The resulting 615.2 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 4).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 3 FSKDTA - FSK Switch

FSKDTA (pin7)	FSK Switch
Low[1)]	CLOSED
Open[2)], High[3)]	OPEN

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off
by the signal at ASKDTA (pin 6).

Table 4 ASKDTA - Power Amplifier

ASKDTA (pin6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5V

2) Open: Pin open

3) High: Voltage at pin > 1.5V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

2.4.4 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.4.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

2.4.4.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 3.5 mA.

2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see **Figure 8**.

2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10).
When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in **Figure 3**

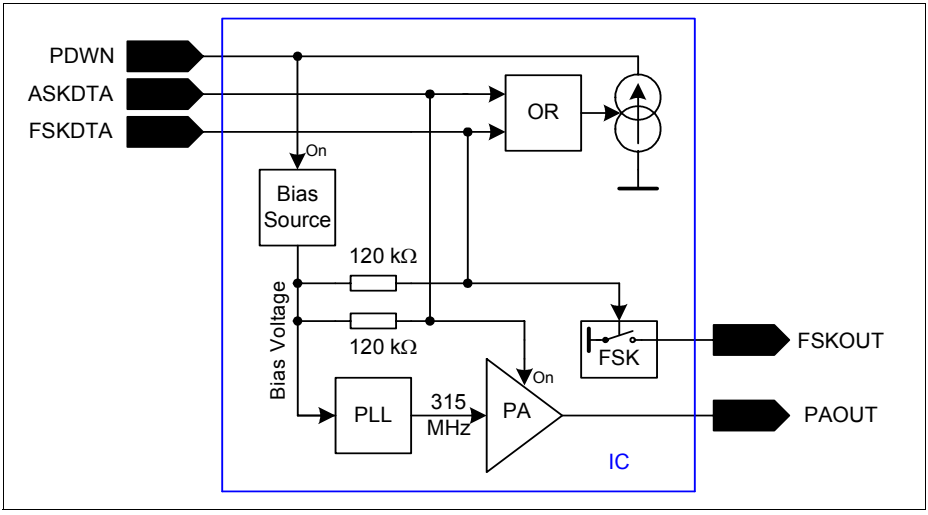


Figure 3 Power mode control circuitry

Table 5 provides a listing of how to get into the different power modes

Table 5 Power Modes

PDWN	FSKDTA	ASKDTA	MODE
Low[1)]	Low, Open	Low, Open	POWER DOWN
Open[2)]	Low	Low	
High[3)]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7V (PDWN)
Voltage at pin < 0.5V (FSKDTA, ASKDTA)

2) Open: Pin open

3) High: Voltage at pin > 1.5V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.5 Recommended Timing Diagrams for ASK- and FSK-Modulation

ASK Modulation using FSKDTA and ASKDTA, PDWN not connected

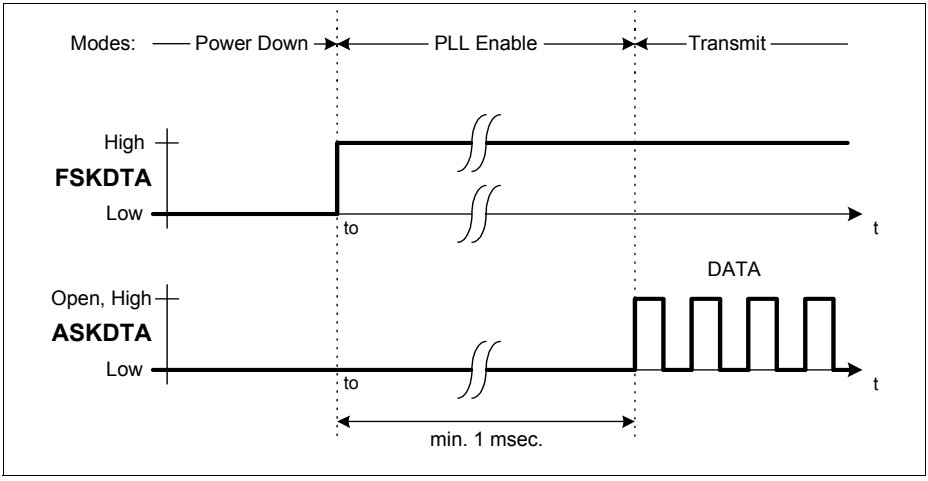


Figure 4 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected.

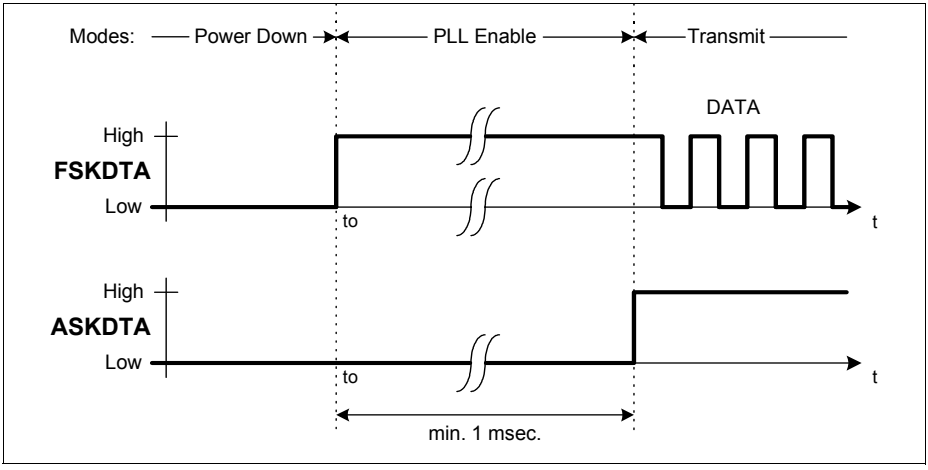


Figure 5 FSK Modulation

Alternative ASK Modulation, FSKDTA not connected.

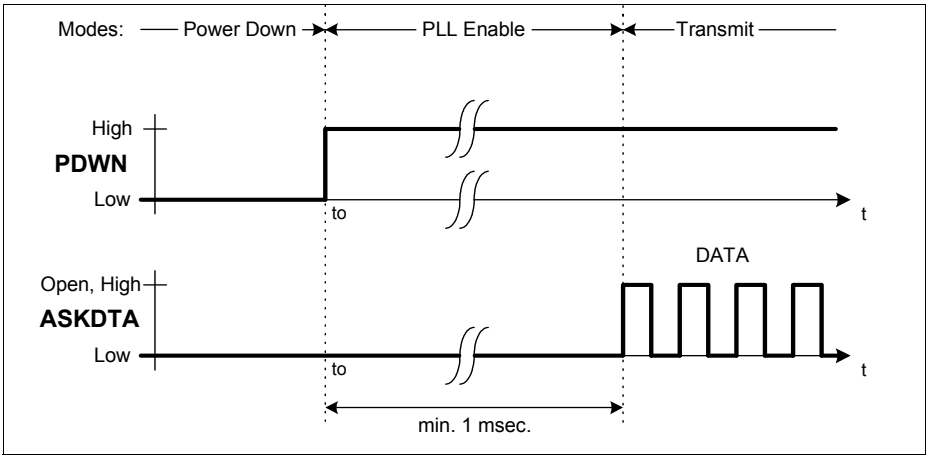


Figure 6 Alternative ASK Modulation

Alternative FSK Modulation

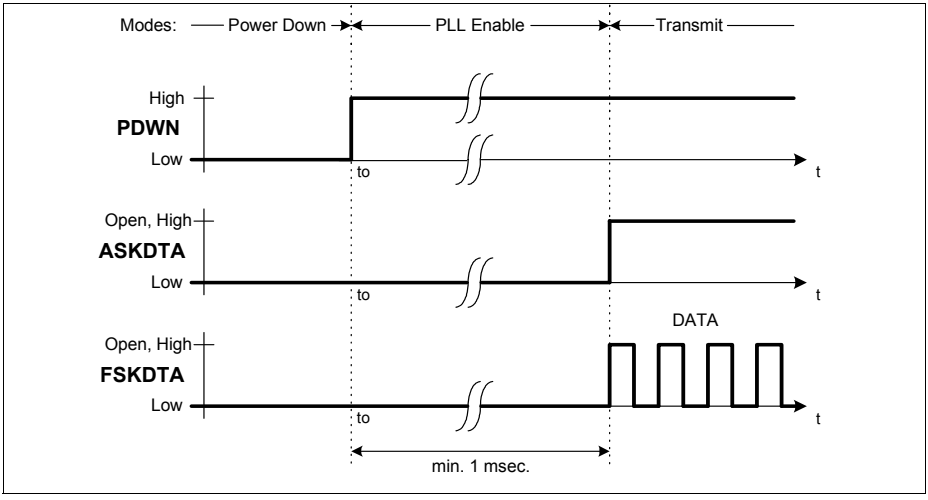


Figure 7 Alternative FSK Modulation

3 Applications

3.1 50 Ohm-Output Testboard Schematic

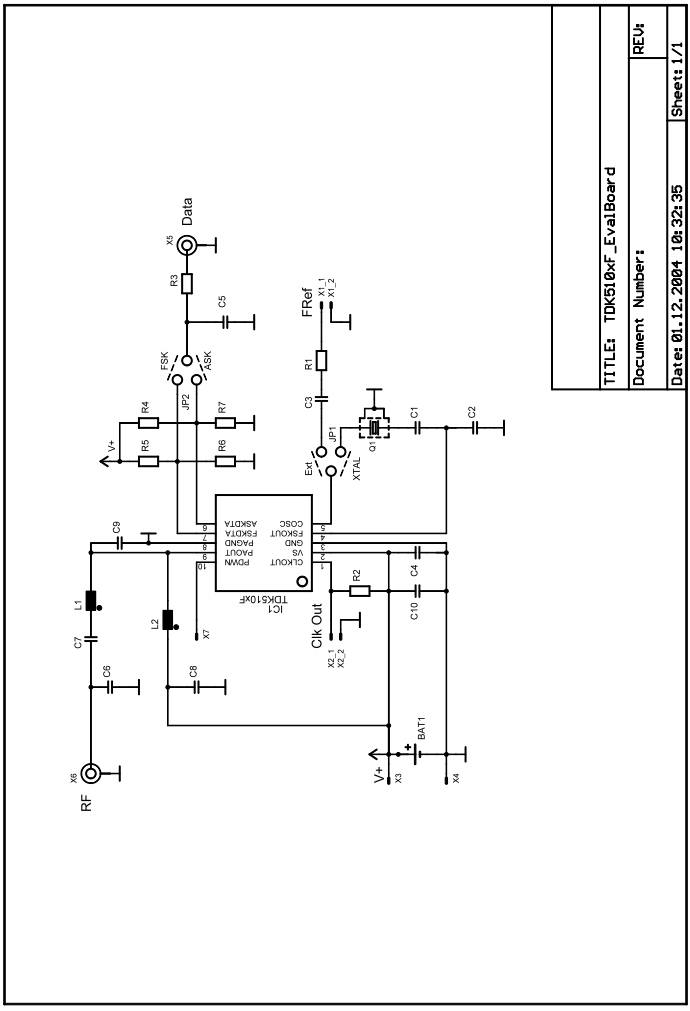


Figure 8 50 Ohm-output testboard schematic

3.2 50 Ohm-Output Testboard Layout

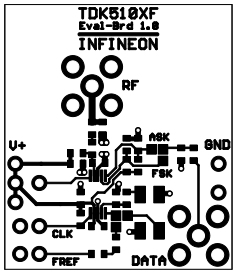


Figure 9 Top Side of TDK5101 F-Testboard with 50 Ohm-Output

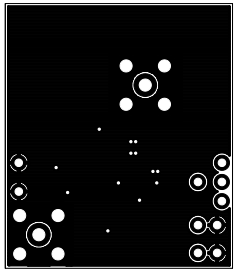


Figure 10 Bottom Side of TDK5101 F-Testboard with 50 Ohm-Output

3.3 Bill of Material (50 Ohm-Output Testboard)

Reference	Value	Specification
R1	open	
R2	open	
R3	4k7	0603, +/-5%
R4	12k	0603, +/-5%
R5	open	
R6	15k	0603, +/-5%
R7	open	
C1	15p	0603, C0G, +/-0,1p
C2	6p8	0603, C0G, +/-1%
C3	open	
C4	open	
C5	100p	0603, X7R, +/-10%
C6	15p	0603, C0G, +/-1%
C7	22p	0603, C0G, +/-1%
C8	330p	0603, C0G, +/-5%
C9	3p9	0603, C0G, +/-0,1p
C10	47n	0603, X7R, +/-10%
L1	82n	EPCOS SIMID 0603-C, +/-2%
L2	220n	EPCOS SIMID 0603-C, +/-2%
X1	n.e.	
X2	n.e.	
X3	Pin	1-polig, 2,54mm
X4	Pin	1-polig, 2,54mm
X5	SMA-Connector	
X6	SMA-Connector	
X7	n.e.	
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	9843.75 kHz, CL=12pF	Tokyo Denpa TSS-3B 9843.75 kHz Spec.No. 1053-921
IC1	TDK5101F	

3.4 Stripline-Antenna Testboard Schematic

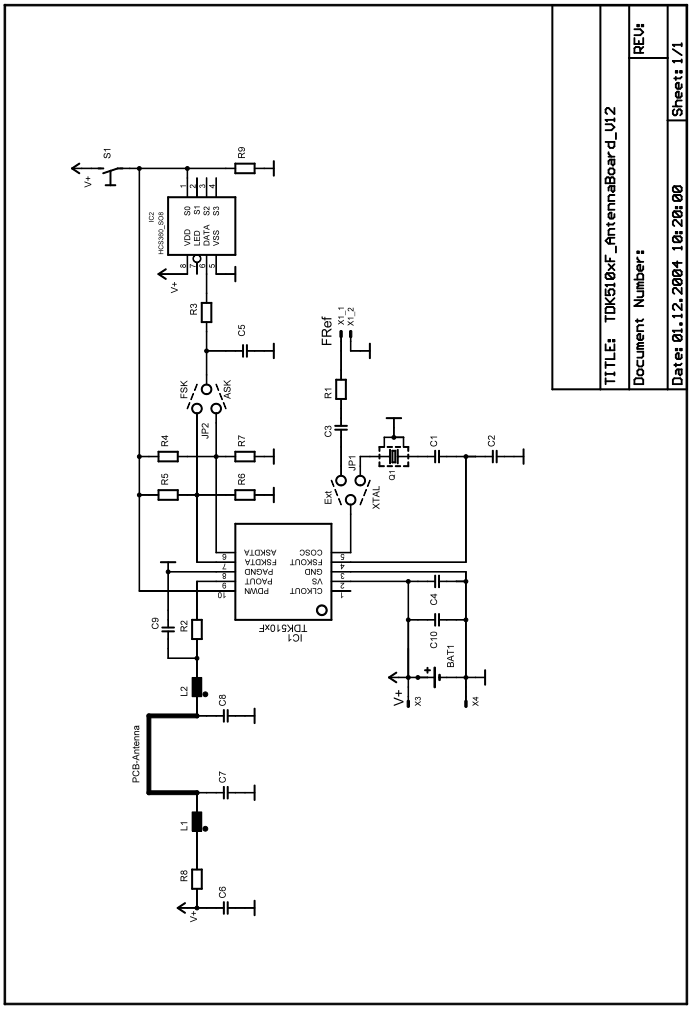


Figure 11 Stripline-antenna testboard schematic

3.5 Stripline-Antenna Testboard Layout

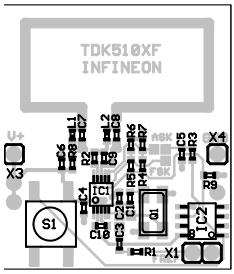


Figure 12 Top Side of TDK5101 F-Testboard with Stripline-Antenna

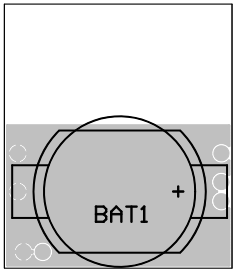


Figure 13 Bottom Side of TDK5101 F-Testboard with Stripline-Antenna

Please note that this board layout may be used for both high- and low-power applications, see also the bill of materials on the subsequent pages.
In case of ASK operation the solder bridge JP2 has to be shortened in the “ASK”-position, in case of FSK modulation in the“FSK” position.
Solder bridge JP1between C1, C2 and C3) gives a choice of operating the board with the on-board crystal as reference (“XTAL” shortened, i.e. close to C1 and C2) or with an external clock generator (solder bridge shorts pads between C3 and C2).

3.6 Bill of Material (Stripline-Antenna Testboard) high power mode, FSK modulation

Reference	Value	Specification
R1	open	
R2	0R	0603, SMD-Jumper
R3	0R	0603, SMD-Jumper
R4	82k	0603, +/-5%
R5	open	
R6	open	
R7	100n	0603, X7R, +/-10%
R8	18R	0603, +/-1%
R9	15k	0603, +/-5%
C1	15p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0,1p
C3	open	
C4	open	
C5	open	
C6	10n	0603, X7R, +/-10%
C7	12p	0603, C0G, +/-1%
C8	open	
C9	10p	0603, C0G, +/-1%
C10	47n	0603, X7R, +/-10%
L1	82n	0603, EPCOS SIMID, +/-2%, B82496C3820G
L2	0R	0603, SMD-Jumper
X1	n.e.	
X3	n.e.	
X4	n.e.	
S1	push-button	STTSKHMPW, ALPS
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	9843.75 kHz, CL=12pF	Tokyo Denpa TSS-3B 9843.75 kHz Spec.No.1053-921
IC1	TDK5101F	P-TSSOP-10
IC2	HCS360	SO8
BAT1	battery holder	HU2031-1, Renata
	battery	CR2032, Renata

3.7 Bill of Material (Stripline-Antenna Testboard) low power mode (for Japanese market), FSK modulation

Reference	Value	Specification
R1	open	
R2	0R	0603, SMD-Jumper
R3	0R	0603, SMD-Jumper
R4	82k	0603, +/-5%
R5	open	
R6	open	
R7	100n	0603, X7R, +/-10%
R8	4k7	0603, +/-1%
R9	15k	0603, +/-5%
C1	15p	0603, C0G, +/-1%
C2	6p8	0603, C0G, +/-0,1p
C3	open	
C4	open	
C5	open	
C6	10n	0603, X7R, +/-10%
C7	330p	0603, C0G, +/-10%
C8	18p	0603, C0G, +/-1%
C9	10p	0603, C0G, +/-1%
C10	47n	0603, X7R, +/-10%
L1	0R	0603, SMD-Jumper
L2	39n	0603, EPCOS SIMID, +/-2%, B82496C3390G
X1	n.e.	
X3	n.e.	
X4	n.e.	
S1	push-button	STTSKHMPW, ALPS
JP1	solder bridge	in position "XTAL"
JP2	solder bridge	in position "FSK"
Q1	9843.75 kHz, CL=12pF	Tokyo Denpa TSS-3B 9843.75 kHz Spec.No. 1053-921
IC1	TDK5101F	P-TSSOP-10
IC2	HCS360	SO8
BAT1	battery holder	HU2031-1, Renata
	battery	CR2032, Renata